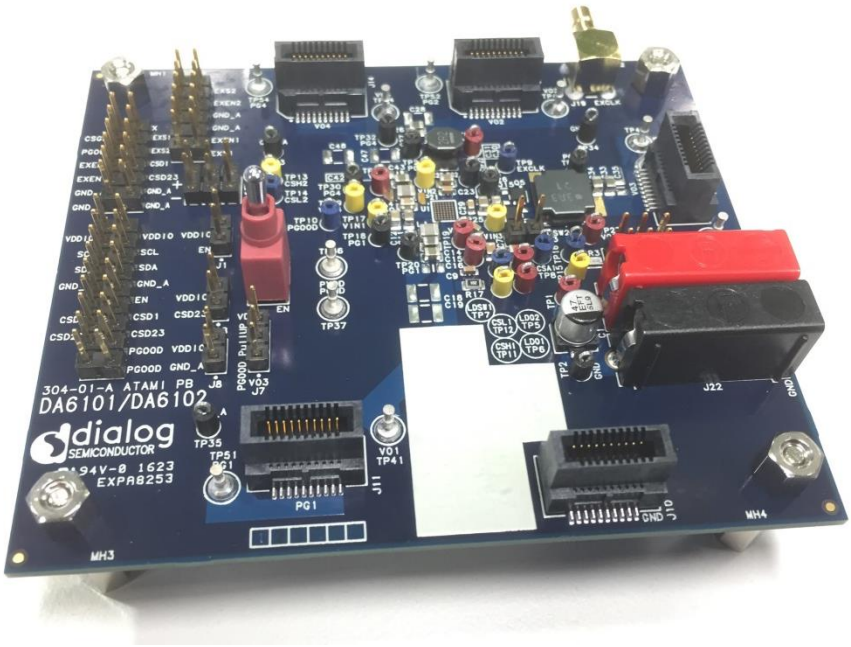
DA6102

Performance Board User Guide

UM-PM-028

Abstract

This guide explains the basic setup and operation of the DA6102 Performance Board. The Performance Board is a complete power solution which can be configured through I2C interface. I2C programming is simplified via GUI software and USB hardware interface which are also described in this document. The DA6102 is a high efficiency PMIC designed for 2-cell powered systems with 3 bucks, 1 buck-boost, 2 LDOs, and programmable control for external load switches and regulators.



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[1] DA6102_datasheet

[2] 304-01-C_PCB, DA6102 PCB Layout

[3] 304-01-C1_SCH, DA6102 PCB Schematic

[4] 304-01-C1_BOM_UG, DA6102 Bill of Materials

2 Introduction

The DA6102 is a highly integrated multi-channel PMIC designed for 2-cell lithium-ion battery powered systems. The wide input voltage range allows direct battery connection for each channel to maximize battery life. The PMIC also includes a highly accurate input current sense with circuit breaker control for battery current sensing and over-current shut down. The DA6102 integrates two buck regulators, a buck-boost regulator, a high current buck controller, and two always-on LDOs. This high level of integration combined with high frequency operation (up to 3MHz) minimizes both PCB size and external component count for the smallest possible solution size.

The DA6102 is a very flexible solution; multiple features can be configured through I2C interface, including output voltage levels, switching frequency, output sequencing, and fault protection. Most features are also configurable by OTP, allowing simplified setting of output voltages and start-up sequence.

The Performance Board itself includes the minimum external components to operate as a stand-alone power system. The Performance Board is designed to operate over the full range of the DA6102: 4.5V-11.5V input supply, and between -40C to 85C ambient temperature. Each channel has additional output capacitor pads to optimize performance according to the application. Test points are provided for easy probing of both input and output nodes.

I2C communication is accessible via the J2 header. Complete I2C programming and monitoring is available with the DA6102 SmartCanvas GUI in combination with Dialog's USB to I2C conversion module.

3 Setting up the Board

Before powering up and enabling the DA6102 Performance Board, ensure that all required connections are in place. Connect the main input supply to the VBATT and GND banana sockets. The input voltage range for normal operation is 4.5V to 11.5V. The input current sense (CS1) limit is set by default to 1.3A and can be increased by register setting to 3.2A. Therefore, the input supply current limit should be set higher than 1.5A and increased as needed if the CS1 limit is changed. Input supply lead lengths should be reasonably short, less than 50cm is recommended.

Loads for each channel should be connected at the turret test points listed in Table 4; do not apply the load until the channel is enabled. Input and output voltages can be measured and monitored at the smaller ring test points also listed in Table 4.

Figure 1 shows the locations of the main power connections, with monitoring points marked in dashed lines. Also shown are three AGND test points. These are quieter ground points for signal measurement and should not be used for high currents.

Input voltage can be monitored via test points at each channel's input capacitors. Those points for Channel 1 are highlighted by square boxes in Figure 1.

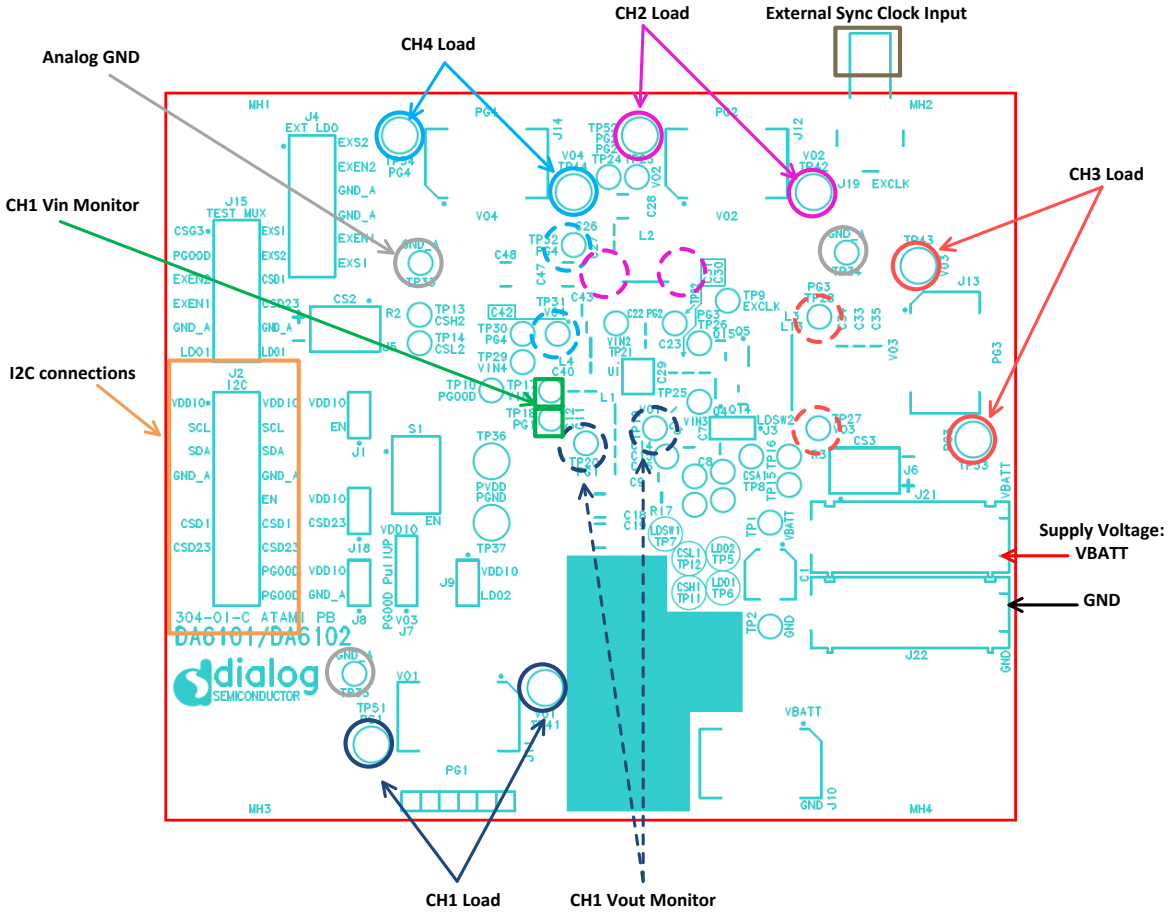

Figure 1: Basic Power Connections

3.1 Jumper Settings

All Performance Board pin headers are listed in Table 3 along with a description of their functions. As shown in Figure 2, the following jumpers are typically installed, but not necessary:

- J3 to connect the LDSW2 input to Channel 3 output
- J7 to pullup PGOOD to VDDIO
- J18 to pullup CSD23 to VDDIO
- J1 connects the EN switch to VDDIO pullup

In the default configuration, J3 and J18 should be installed and J7 should be set to the VDDIO position.

J1 is typically installed, but not necessary if EN is controlled by an external signal.

J9 connects the LDO2 output to supply VDDIO. Do not install J9 when using the USB conversion module.

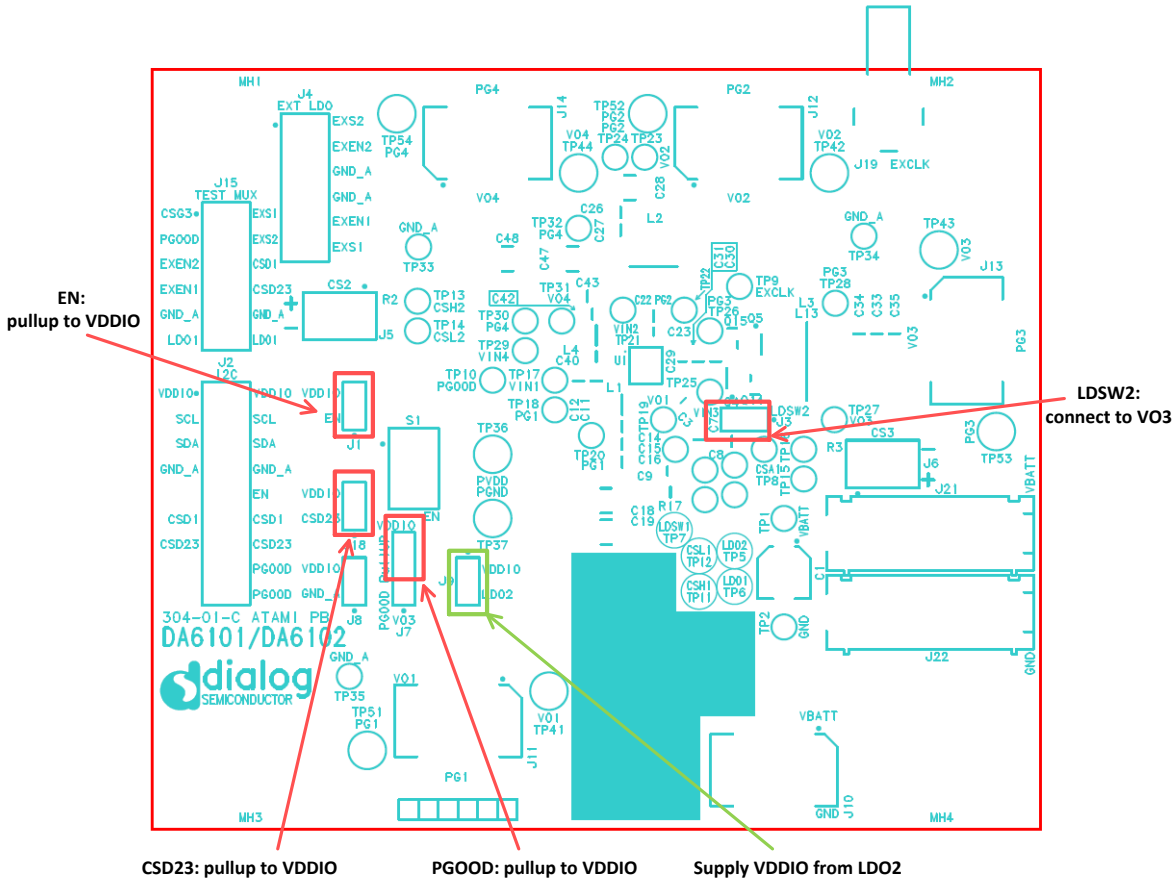

Figure 2: Typical Jumper Settings

3.2 USB-I2C Conversion Module

A separate USB to I2C conversion module is provided with the DA6102 Performance Board. The conversion module allows seamless interfacing from the GUI to the Performance Board with a few simple connections, providing access to all the DA6102 registers.

3.3 I2C Connections and VDDIO

The four required connections for I2C communication are made from the J2 header to the USB conversion module, as shown in Table 1.

Table 1: J2 Pin Connections to USB Conversion Module

SIGNAL	VDDIO	SCL	SDA	GND
J2-Pin	1, 2	3, 4	5, 6	7, 8
USB Module wire	Red	Yellow	Blue	Black

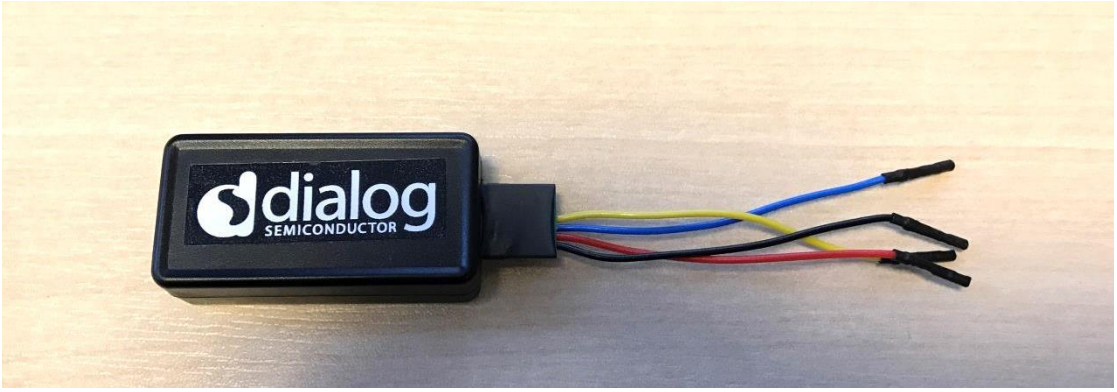

Figure 3: USB Conversion Module

The USB conversion module has on-board 2.2kΩ pullup resistors for SDA and SCL. For this reason the pullup resistors on the Performance Board, R9 and R10, are not installed by default.

The USB conversion module provides the 3.3V VDDIO supply from USB power. When the USB-I2C conversion module is used, the on-board VDDIO must be connected (red jumper wire to J2 Pin-1 or Pin-2).

If the USB conversion module is not used, there are two options for supplying VDDIO power.

- An external supply (1.5V to 5.0V) connected to J2 or J8
- LDO2 (3.12V default) connected to VDDIO via J9 jumper

R9 and R10 are unpopulated pullup resistors for I2C communication. Install these resistors if they are not present on the I2C host controller (10kΩ is recommended).

Even if I2C is not used, VDDIO must be powered and R9 and R10 installed.

3.4 Power-Up and Enable

Once the required supply, load, vddio, and I2C connections are made, apply power to VBATT and connect the USB cable (in either order). LDO1 and LDO2 will ramp up and the DA6102 will be ready to operate.

Start the GUI.

IMPORTANT NOTE: The Current Sense 1 channel (CS1) supplies the input voltage to the switching channels via Q1 and R1. Therefore, CS1 must be enabled by I2C before the start-up sequence begins. If CS1 is not used, it can be externally bypassed with a jumper from TP1 to TP36.

Enable (EN) can be controlled by the switch, S1, or by external signal. In either case, the center switch position disables the DA6102.

For switch control, install J1 and set the switch down, towards the Dialog logo, to enable.

For external signal control, set the switch in the opposite direction and apply a logic level signal at J2, pin 9. Pin 9 is the unlabelled pin directly across from the pin 10, labelled ‘EN’. Pin 10 connects directly to the EN pin of the IC.

When EN is switched high, each channel enabled in the “Buck Enable” register will ramp up according to the programmed start-up sequence.

PGOOD becomes active after all channels have completed start-up.

4 Switching Channel Options

Refer to the DA6102 datasheet for details of each channel's specifications and functionality.

Each switching channel has additional output capacitor pads on both the top and bottom of the PCB. Output capacitors can be added within the recommended datasheet range without any setting changes, except for Channel 3 which may require a change to register 0x21.

The electrolytic input capacitor, C1, is used to dampen possible oscillations that may occur due to long input leads in the lab environment. This capacitor is not necessary in an actual application.

Channel 3 has two overlapping footprints for Q4 and Q5 to fit 2x2mm uDFN and SOT-23 size FETs. In addition, the FET gate drives have 10Ω resistors in series with the gates at R12 and R13. These can be adjusted to speed up or slow down the LX3 rise and fall time.

Channel 3 also has an extended solder pad area at L3 to allow placement of various size inductors.

Changing the inductor on any channel will usually require a change to the compensation settings; refer to the datasheet, registers 0x20 and 0x21.

Each channel has a resistor in series with the FB pin: R4, R5, R6, and R7. R4 is installed with 0 ohm, while the others are shorted and not installed. These resistor pads are used for loop gain and phase measurements and should not be modified in normal operation and evaluation.

5 Current Sense and External Regulators

To use the current sense load switches CS2 and CS3, external supplies can be connected to the J5 and J6 input headers. The three pins in each header column are connected: pins1, 3, and 5 are the input side, marked '+'. Note that the test points labelled CSLx and CSHx are connected across the current sense resistors, not the input jumpers.

The current sense channels CS1, CS2, and CS3 can be enabled and disabled via I2C even while the EN pin is low.

For external LDO control via the EXS and EXEN pins, use the 12 pin header, J4. The two pins in each header row are connected (1-2, 3-4, etc.). While one pin is used for external connection the other can be used for voltage monitoring.

6 Load Capability

Table 2 below describes the maximum recommended load for each channel. Above this level, a current limit, thermal shutdown, or other fault event may occur.

Constant resistance loads should always be used, as constant current loads may pull a disabled output below the negative absolute maximum rating and cause damage.

Table 2: Maximum Load Current

Channel	Max DC Load	Comment
LDO1	300 mA	CH1 enabled (LDSW1 = 0A)
LDO1 (low)	70 mA	Applies with CH1 disabled
LDSW1	200 mA	LDO1=0A, CH1 enabled
LDO2	200 mA	
CH1	700 mA	
CH2	2.2A	
CH3	4A	With default external FETs
CH4	600 mA	
CS1 (PVDD)	1.3A default limit	Total input current through R1 Limit can be modified by register setting
CS2	3A default limit	Limit can be modified by register setting
CS3	1.7A default limit	Limit can be modified by register setting

7 Measuring and Monitoring

The four switching channels each have two pairs of Vout and PG test points. The larger turret type should be use for load connections. The smaller ring type test points are closer to both the output caps and FB point, making them better suited for measuring ripple, regulation, efficiency, and transient response. The exception is the VO3 test point. It is too close to L3 to get a clean scope measurement. Either the VO3 turret or spare output capacitor pads should be used for scope measurement of Channel 3 output voltage.

When measuring efficiency, be sure to measure input and output voltage close to the input and output caps, not at the supply and load source.

When measuring ripple or transient response, good probing technique is critical. PCB trace and scope probe parasitics can add false artifacts to sensitive measurements. Disconnecting any LX node probe is also good practice when measuring ripple and noise.

Each switching channel has semi-isolated copper areas for PG and VIN. Although all grounds connections are the same node, one channel's power ground should not be used as the load connection or measurement point for another channel's ground.

Each channel has a small solder mask opening at the inductor pads. This can be used to monitor the LX nodes.

A simple method for good probing is shown in Figure 4. The inductance of the probe ground lead adds high frequency impedance and can also pick up noise from nearby switching nodes. A much better practice is to use a short wire ground looped around the probe, and mounted directly to the GND side of the output capacitor.

When non-switching signals are being measured, such as LDO1 or PGOOD, the ground lead is not critical. For these signals it is recommended to use the quite AGND test pins.

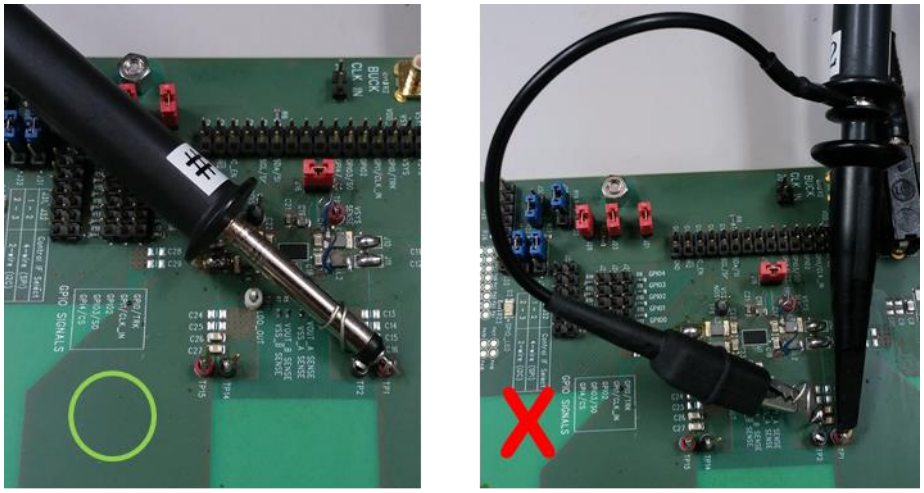

Figure 4: Good and bad probing technique

8 Other Features

The DA6102 can be synchronized to an external clock using the J19 SMB connector. The applied signal must be between 1.5MHz and 3MHz with a maximum level of 5V.

Test point TP9 can also be used in place of J19.

The external clock input is terminated with R14, a 51Ohm resistor to ground.

J3 connects the LDSW2 input to the Channel 3 output. If another voltage is used or LDSW2 is not used, the jumper can be removed. The LDSW2 input voltage must be applied or high impedance before LDSW2 is enabled. The optional capacitor C10 is provided as an additional bypass capacitor for LDSW2 in case of a noisy source.

The DA6102 has two open drain status pins: PGOOD and CSD23. Headers J7 and J18 connect these pins to VDDIO as a default pullup voltage. J7 can be used to select the PGOOD pullup voltage as VDDIO or VO3.

The status of both pins can be monitored at J2.

Alternately, PGOOD can be set to CMOS mode by register setting 0x22. In CMOS mode, leave the J7 jumper open.

CSD1 is a logic level status output and can also be monitored at J2.

CSA, the analog output of CS1, can be monitored at TP8.

9 GUI Operation

The DA6102 SmartCanvas GUI provides simple access to the control registers. All features such as output voltage setting, fault behaviour, start-up sequence, and switching frequency are programmable through several methods within the GUI.

To install the SmartCanvas GUI, open the setup file: ***setup_DA6102_GUI***

Follow the installer instructions to install the GUI in the desired destination folder. Once installed, connect the USB conversion module and start the GUI.

9.1 Main Screen

Figure 5 below shows an overview of the main screen. The GUI is divided into 4 sections: the main register R/W, Control, Command Log, and Register Info. A separate window can be opened for Register Search.

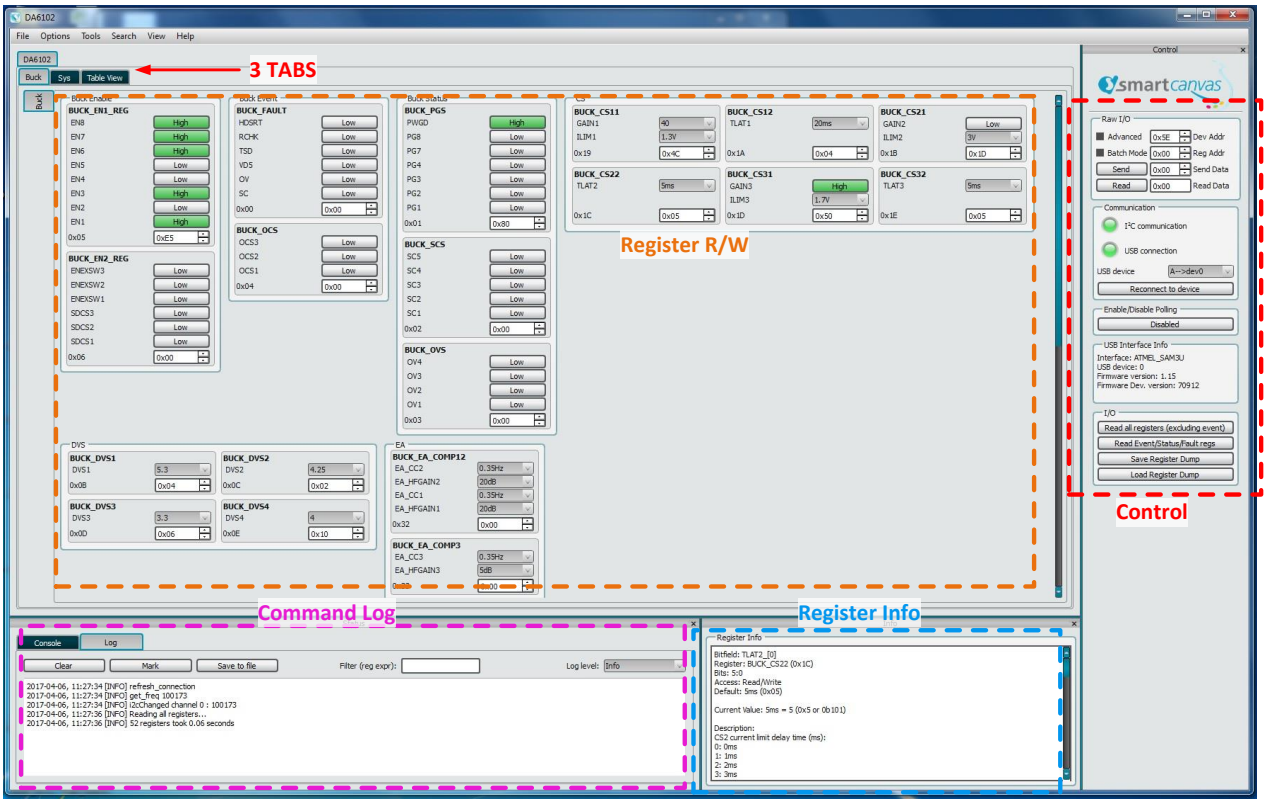

Figure 5: SmartCanvas GUI Main Screen

Each 8-bit register is shown in a box, with register name, address, and bit descriptions. Hovering over any register box will show the details of that register in the Register Info box.

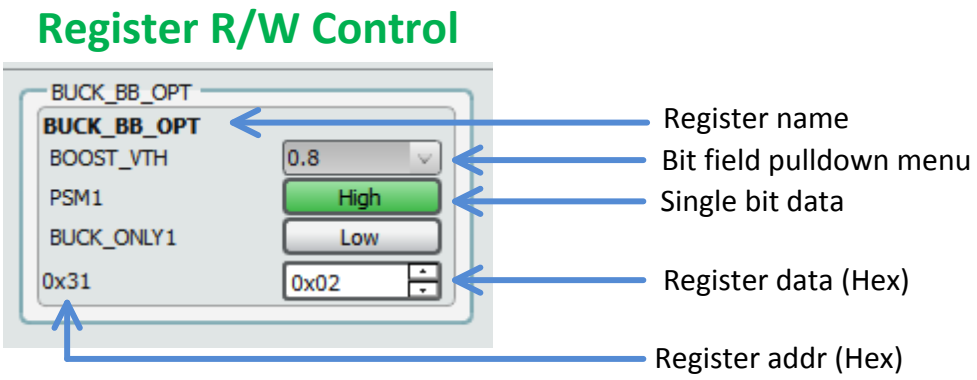

Figure 6: Register R/W box detail

Setting a new value at any bit or bit-field in the Register R/W section will immediately write the new data to the DA6102.

9.2 Register Search

To easily find any register, open the ‘Search’ window located in the search menu. Simply enter the register name or address and click Find. The register box will be highlighted in green as shown in Figure 7.

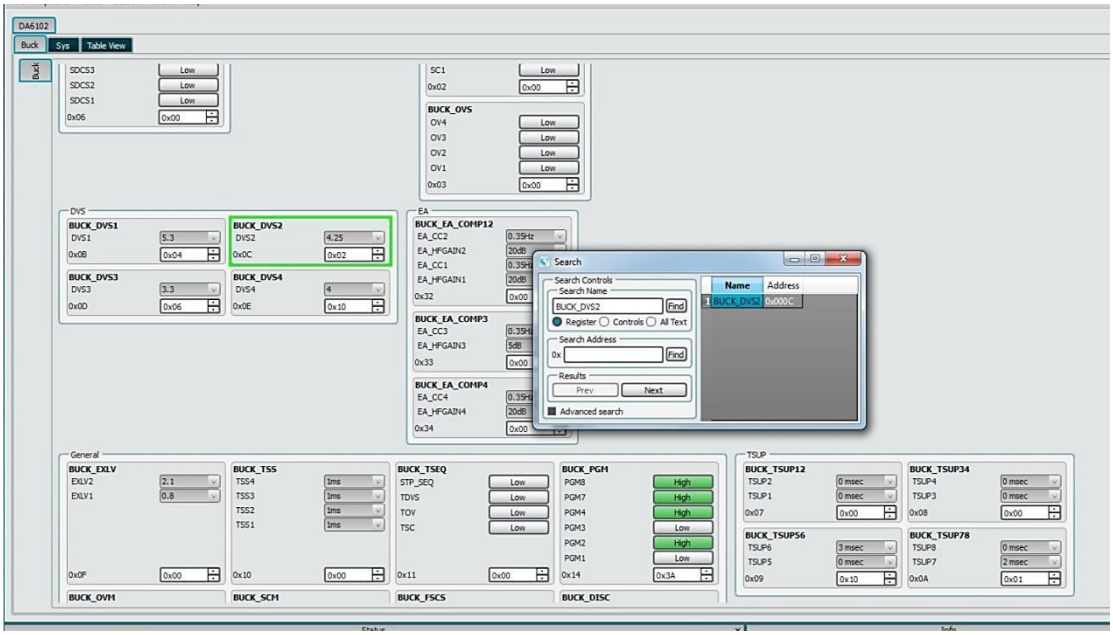

Figure 7: Register Search Window

9.3 READ Data

There are three methods available to read back register data:

- In the ‘Control’ section, set polling to ‘Enabled’. This continuously reads all registers and updates the display. This method is convenient, but not recommended as continuous polling may create additional noise or be disturbed by switching noise.
- In the I/O box at the bottom of the ‘Control’ section, click ‘Read all registers’, which will perform a one-time read.
- In the ‘Raw I/O’ box at the top of the ‘Control’ section, enter the address you want to read and click the ‘Read’ button. The data will appear in the ‘Read Data’ box.

The ‘Raw I/O’ box can also be used to directly write to any register by setting the address, data, and clicking ‘Send Data’.

9.4 Sys and Table View Tabs

There are two tabs in addition to the main Register R/W section: Sys, and Table View.

While most of the registers can be found in the main Buck tab, a few such as frequency are listed in the Sys tab. There is no functional difference between these two tabs.

The Table View tab shows the full register map in the same format as the datasheet. Double clicking any register box will allow that register to be written, shown in Figure 8. Alternately the left column can be used to write to the register directly.

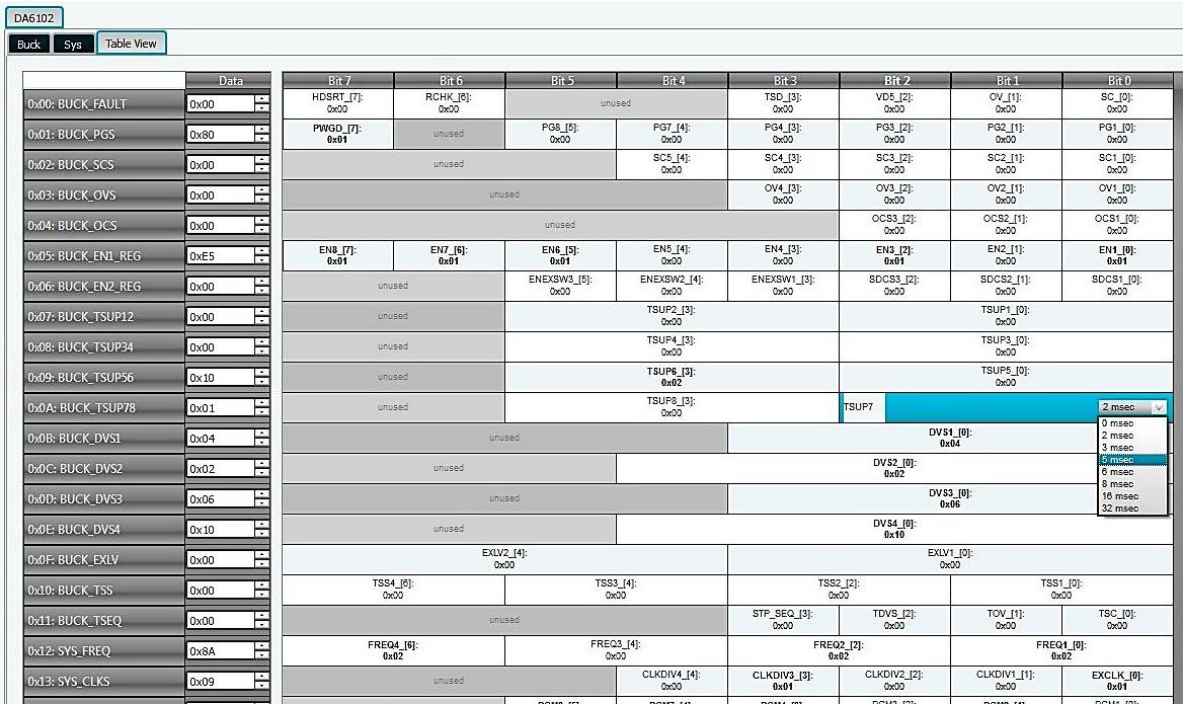

Figure 8: GUI Table View Tab

9.5 Communication

Within the control section is the Communication box. The indicators here will appear red or green to indicate the status of the USB connection to the conversion module, and I2C connection to the DA6102.

10 PCB Information

The DA6102 Performance Board is a 6 layer PCB, manufactured on RoHS compliant FR4 material.

All layers are 1oz (35um) copper weight, with the following layer assignments:

- Top Layer: power routing for VIN, PG, LX, and Vo
- Layer 2: PG (power ground) plane
- Layers 3 and 4: signal routing and flooded PG layer
- Layer 5: VDD plane
- Bottom Layer: quiet AGND plane and FB routing

Other than the top layer, each layer is flooded with copper to optimize thermal performance. The thermal resistance (θ_{JA}) of the DA6102 mounted on the Performance board is approximately 34C/W. This allows for normal operation with up to 1.1W of IC power dissipation at 85C ambient temperature.

Table 3: Jumper Functions

Ref. Des.	Pins	Function
J1 (EN pullup)	1	EN switch pullup voltage
	2	VDDIO, install jumper to use VDDIO as EN pullup voltage
J2 (I2C)	1, 2	VDDIO
	3, 4	SCL
	5, 6	SDA
	7, 8	GND
	9	EN switch external signal input
	10	EN pin
	11, 12	CSD1
	13, 14	CSD23
	15, 17	Open
	16, 18	PGOOD pin
J3 (LDSW2)	1	VO3
	2	LDSW2 input, install jumper for VO3 to source LDSW2
J4 (EXT LDO)	1, 2	EXS2, external regulator 2 output sense
	3, 4	EXEN2, external regulator 2 enable
	5, 6, 7, 8	Ground
	9, 10	EXEN1, external regulator 1 enable
	11, 12	EXS1, external regulator 1 output sense
J5 (CS2)	1, 3, 5	CSH2, current sense 2 input supply high
	2, 4, 6	Current sense 2 input supply low
J6 (CS3)	1, 3, 5	CSH3, current sense 3 input supply high
	2, 4, 6	Current sense 3 input supply low
J7 (PGOOD pullup)	1	VO3, jumper here to use VO3 as pullup voltage
	2	PGOOD pullup voltage for open drain mode
	3	VDDIO, jumper here to use VDDIO as pullup voltage
J8 (VDDIO)	1	Ground
	2	VDDIO input connection for external supply
J9 (VDDIO from LDO2)	1	VDDIO input connection for supplying from LDO2 Do not use if using the USB conversion module
	2	LDO2 output voltage
J18 (CSD23 pullup)	1	CSD23 pin, current sense 2 and 3 open drain flag
	2	VDDIO, CSD23 pullup voltage
J19 (EXCLK)	SMB	EXCLK, external clock input
J21 (VBATT)	Banana socket	VBATT, main supply
J22 (GND)	Banana socket	GND, main supply
J11 – J14 *	-	VO1 – VO4 test connectors, * Dialog internal use
J10 *	-	VBATT test connector, * Dialog internal use
J15 *	1-12	Test connector, * Dialog internal use

Table 4: Test Point Listing

Part Number	Pairs with	Type	Function
TP1	TP2 (GND)	Ring	Battery voltage
TP5	TP33, 34, 35 (AGND)	Ring	LDO2
TP6	TP33, 34, 35 (AGND)	Ring	LDO1
TP7	TP33, 34, 35 (AGND)	Ring	LDSW1, load switch 1 output
TP8	TP33, 34, 35 (AGND)	Ring	CSA1, current sense 1 analog output
TP9	TP33, 34, 35 (AGND)	Ring	EXCLK, external clock input
TP10	TP33, 34, 35 (AGND)	Ring	PGOOD, power good flag
TP11	TP12 (low)	Ring	CS1 current sense voltage
TP13	TP14 (low)	Ring	CS2 current sense voltage
TP15	TP16 (low)	Ring	CS3 current sense voltage
TP17	TP18 (GND)	Ring	VIN1
TP19	TP20 (GND)	Ring	VO1
TP21	TP22 (GND)	Ring	VIN2
TP23	TP24 (GND)	Ring	VO2
TP25	TP26 (GND)	Ring	VIN3
TP27	TP28 (GND)	Ring	VO3
TP29	TP30 (GND)	Ring	VIN4
TP31	TP32 (GND)	Ring	VO4
TP36	TP37 (GND)	Turret	PVDD, input voltage for switching channels
TP41	TP51 (GND)	Turret	VO1 load connection
TP42	TP52 (GND)	Turret	VO2 load connection
TP43	TP53 (GND)	Turret	VO3 load connection
TP44	TP54 (GND)	Turret	VO4 load connection
TP33, 34, 35		Ring	AGND, quiet ground

Note 1 Ground test points are listed as pairs with signal test points

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