User's Manual

VERSALDEMO1Z

User's Manual: Demonstration Board

Core Power Solutions

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VERSALDEMO1Z

Demonstration Board

VERSALDEMO1Z is a power reference board designed in collaboration with Xilinx to provide full power rails for Xilinx Versal ACAP, including adaptable engines, AI engines and scalar engines, as well as external DDR memory.

Renesas power solutions for Xilinx Versal ACAP feature the ISL68225 digital multiphase controller and ISL99360 smart power stage for core power, as well as the ISL91211A multiphase PMIC and ISL85009 and ISL8026 DC/DC regulators for remaining power rails.

This orderable reference board serves both as a proven turnkey reference design for customers to jump start their design, as well as an evaluation platform for quick and easy power testing.

Key Features

- The ISL68225 digital multiphase controller and ISL99360 smart power stage provide a high efficiency Vcore solution over a wide load range.
- The ISL91211A power management IC (PMIC) solution provides a highly-integrated compact design for multiple Versal lower current rails.
- The DC/DC regulators provide complete solutions for the rest of the power needs by Versal.

Ordering Information

Part Number	Description
VERSALDEMO1Z	Renesas Xilinx Versal power reference demonstration board

Related Literature

For a full list of related documents, visit our website:

- Xilinx Versal ACAP device page

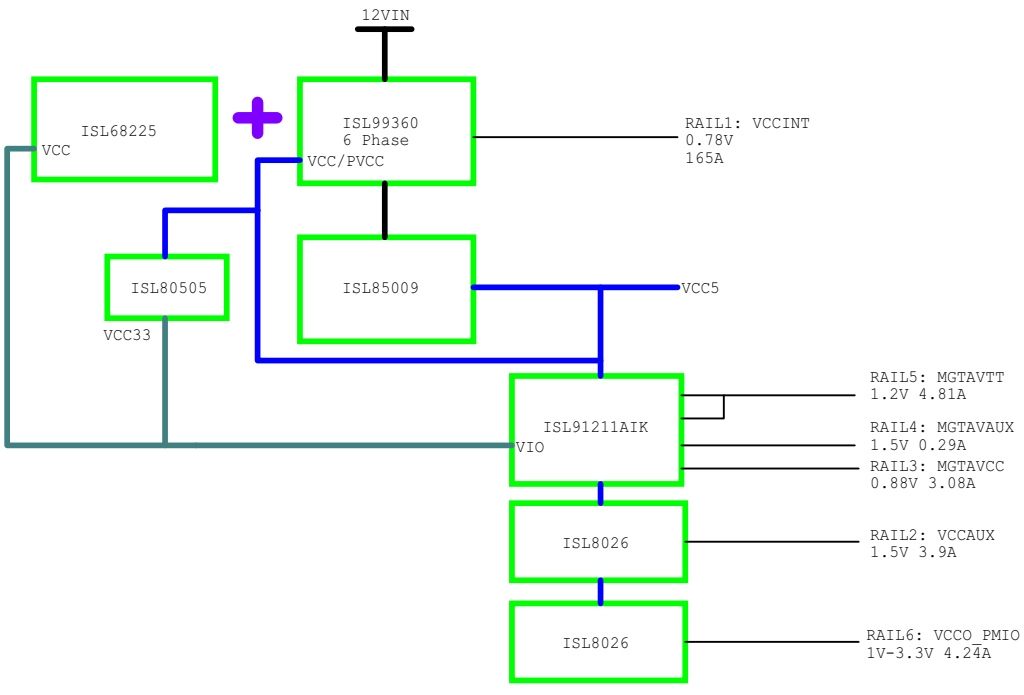


Figure 1. Block Diagram of Power Management Solution for the Renesas Reference Board

1. Functional Description

Figure 1 presents the architecture of the Renesas power management solution employed in this reference board. This power solution is used to support user case 1 and user case 3 of the Xilinx Versal ACAP. As shown in Figure 1, this solution is based on a 12V input, which is a common input for main boards. There are six independent outputs provided by this solution, which is going to function as the Versal core power and bias supplies of other rails. Six output rails for Versal include VCCINT,VCCAUX, MGTAVCC, MGTAVAUX, MGTAVTT, and VCCO_PMIO. This Renesas power management solution is composed by using all Renesas competitive parts, including digital multiphase controller, Smart Power Stage (SPS), Power Management IC (PMIC), and switching regulator.

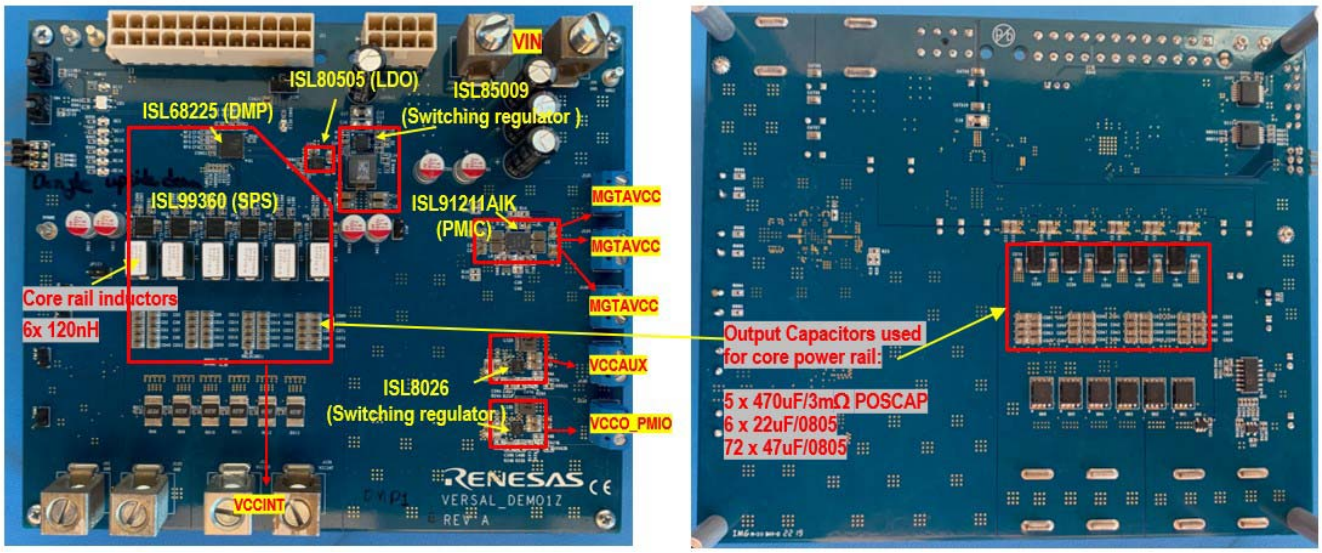


Figure 2. Top and Bottom View of Reference Board

1.1 Digital Multiphase Controller

The ISL68225 is a digital dual output multiphase (X+Y ≤ 9) PWM controller supporting the PMBus V1.3 interfaces. Either of the outputs can be configured to support any desired phase assignments up to a maximum of nine phases across the two outputs (X+Y). For example, 8+1, 7+2, 6+3, 5+4, or a single output operation such as a 9+0 configuration are supported. This allows flexible scalability to support a wide range of load current. The ISL68225 use the Renesas proprietary digital synthetic current modulation scheme to achieve the industry-best combination of transient response, ease of tuning, and efficiency across the full load range. You can use the intuitive Renesas Power Navigator™ software to configure and monitor the device.

With minimal external components, easy configuration, robust fault management, and highly accurate regulation capability, implementing a high performance, multiphase regulator has never been easier.

In this reference board, the digital multiphase controller together with Smart Power Stage (SPS) from Renesas was used to create the VCCINT rail, which has a current rating of 165A. The 6+0 configuration is set as default, and it can be modified by dropping or adding phases per current adjustment or efficiency optimization purpose. The default output voltage of 0.78V can be reconfigured using PowerNavigator.

1.2 Smart Power Stage (SPS)

The ISL99360 is compatible with the ISL68xxx/69xxx Digital Multiphase (DMP) controllers. The ISL99360 has integrated high accuracy current and temperature monitors that can be fed back to the controller to complete a multiphase DC/DC system. They simplify design and increase performance by eliminating the DCR sensing network and associated thermal compensation. Light-load efficiency is supported through a dedicated LFET control pin. An open-drain fault reporting pin simplifies the handshake between the SPS and controllers and can disable the controller during start-up and fault conditions. Six ISL99360 are employed in this reference board and they are controlled and driven by ISL68225 to create the VCCINT rail.

1.3 Power Management IC (PMIC)

The ISL91211AIK is a 4-phase, three output programmable Power Management IC (PMIC) and has independently OTP programmable voltage settings for each output. This flexibility allows to support an expandable and optimized power supply from a Xilinx high-end product to a low-end product. It is optimized with highly efficient synchronous buck converters capable of multiphase and single-phase operations that can deliver up to 5A per phase continuous output current. The ISL91211AIK delivers a highly robust power solution by featuring a controller based on the Renesas proprietary R5 technology, which provides tight output accuracy and load regulation, ultra-fast transient response, seamless DCM/CCM transitions, and requires no external compensation. In this reference board design, ISL91211AIK is used to output three power rails, including the MGTAVCC rail by two phases in parallel, and the MGTAVAUX rail through one phase, and the MGTAVTT rail through another phase. The default output voltage of each rail can be reconfigured using PowerNavigator.

1.4 Switching Regulator

The ISL8026 is highly efficient, monolithic, synchronous step-down DC/DC converters that can deliver 6A of continuous output current from a 2.5V to 5.5V input supply. The devices use current mode control architecture to deliver a very low duty cycle operation at high frequency with fast transient response and excellent loop stability. The ISL8026 can be configured for discontinuous or forced continuous operation at light load. Forced continuous operation reduces noise and RF interference, while discontinuous mode provides higher efficiency by reducing switching losses at light loads. Two ISL8026 were employed to provide the VCCAUX rail and VCCO_PMIO rail separately.

1.5 Quick Start Guide

The Renesas USB to PMBus Adapter is used to connect the PMBus interface on reference board with a USB interface to a PC to reconfigure settings.

1.5.1 Default settings

This reference board can be powered up directly without using PMBus interface. In this case, there is no need on power navigator for just general powerup to reach default settings, as listed in Table I. The power solution can be reconfigured by using PMBus option as guided in next section.

Table 1. Default Setting for Rails

Rails	Default Output voltage	Current Rating	Switching Frequency
VCCINT	0.78V	165A	600kHz
VCCAUX	1.5V	6A	1MHz
MGTAVCC	0.88V	5A	2MHz
MGTAVAUX	1.5V	5A	2MHz
MGTAVTT	1.2V	5A	2MHz
VCCO-PMIO	1.5V	6A	1MHz

1.5.2 Startup Procedures

1. Connect DC power supply to input terminal (nominated at 12V). Please take care of the current rating of supply, and a DC supply able to output 15A at 12V would be needed if running test under continuous full load conditions of rails.
2. Ensure the enabling switches (S3 and S4) are in the correct position.
3. Check the output rails.
4. Optional: Operation to follow when using the PMBus enable option

- Connect the USB Mini provided between the host computer and the USB to PMBus adapter.
- Connect USB to PMBus adapter to demonstration board to test or evaluate.

- Apply input power (labeled VIN) to the demonstration board.
- Download PowerNavigator from the Renesas website.
- Follow the instructions on the website.
- When PowerNavigator is installed, double-click on the PowerNavigator icon and follow the software's instructions. The Power Navigator User Manual can give you some details to start with, and you can find more than this on Renesas website. Please feel free to contact our engineer for support whenever needed.

5. Load transient test empowered by the reference board.

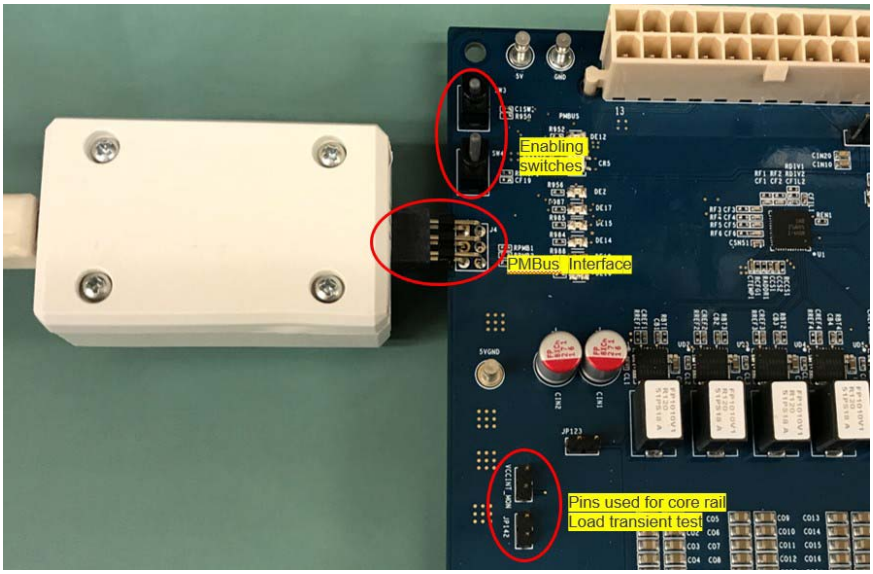


Figure 3. PMBbus Dongle (Enabling Switches and the Header for Load Transient Test)

Note: The PMBus dongle is connected downside up.

This reference board has embedded circuits to allow load transient test on core power rail. An active load circuit with parallel connected MOSFETs can sustain a pulsed load current as high as 130A. In order to reduce the thermal rise while achieving enough duration of full load during load transient test for the loop getting optimized, a load step waveform with long period but small duty cycle is highly recommended. To run the active load circuit, make sure the two pins of header JP142 are shorted to each other. (This shorted connection should be removed for any efficiency measurements.) In general, a pulsed signal from signal generator can be given through JP143, and the regulated load current can be monitored through IMON. For every 1V applied to JP143, the on-board active load will draw about 100A. The load slew rate can be controlled by adjusting the applied signal edge rate. See the VERSALDEMO1Z Circuit Schematics for more details.

2. Layout Guidelines

2.1 VERSALDEMO1Z Circuit Schematics

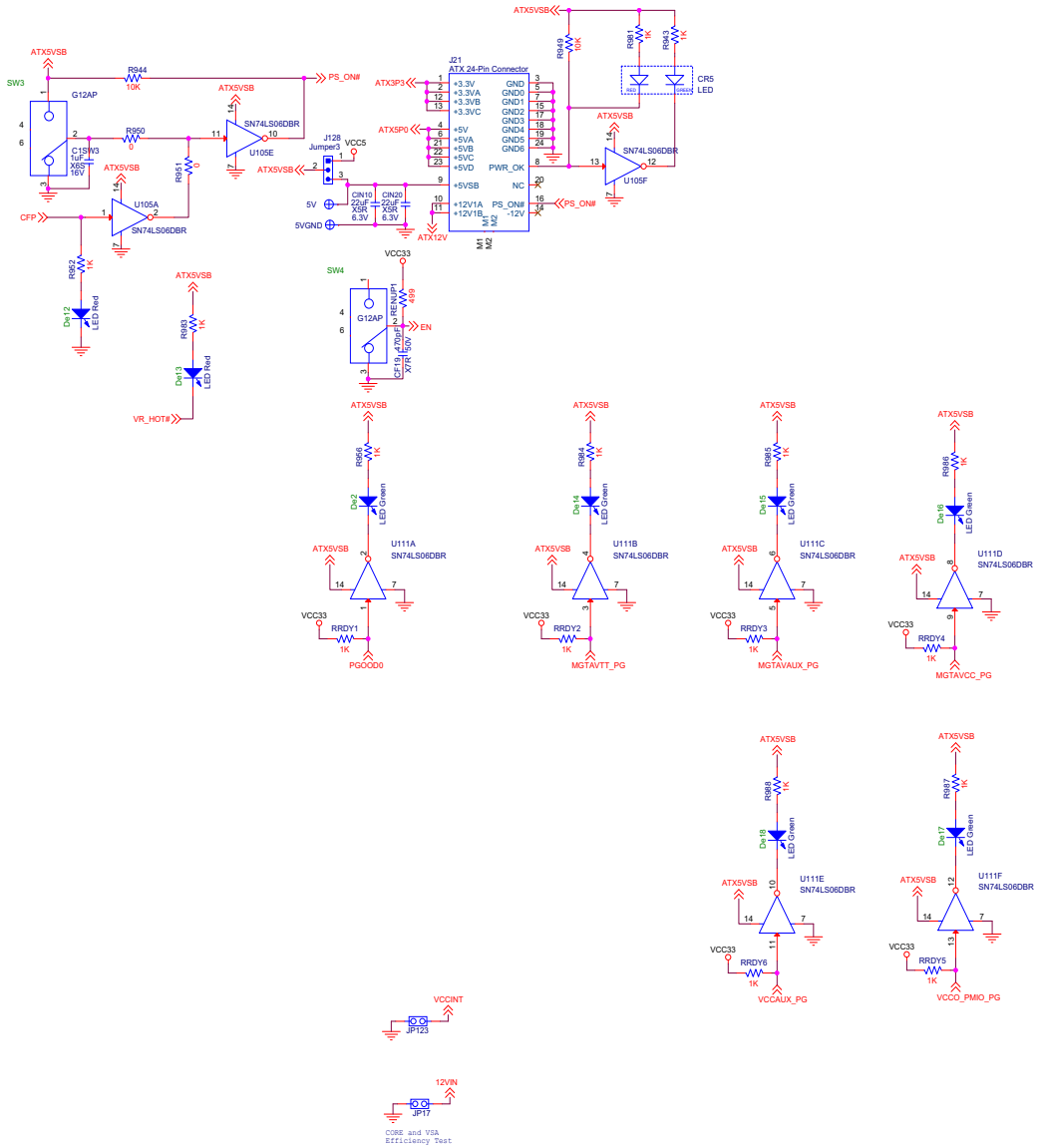
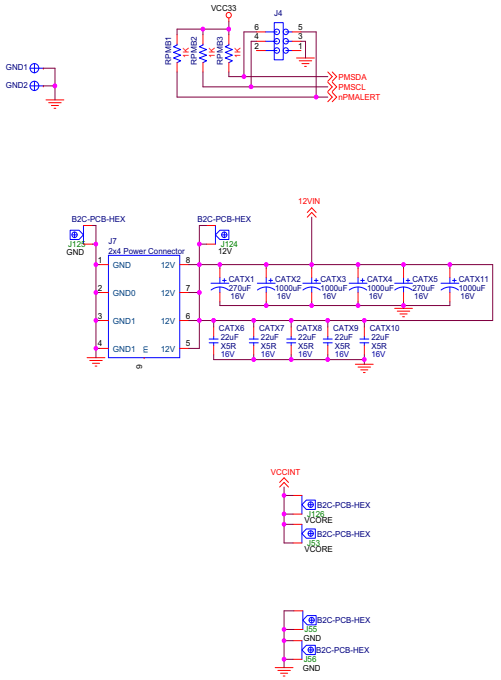


Figure 4. Schematic



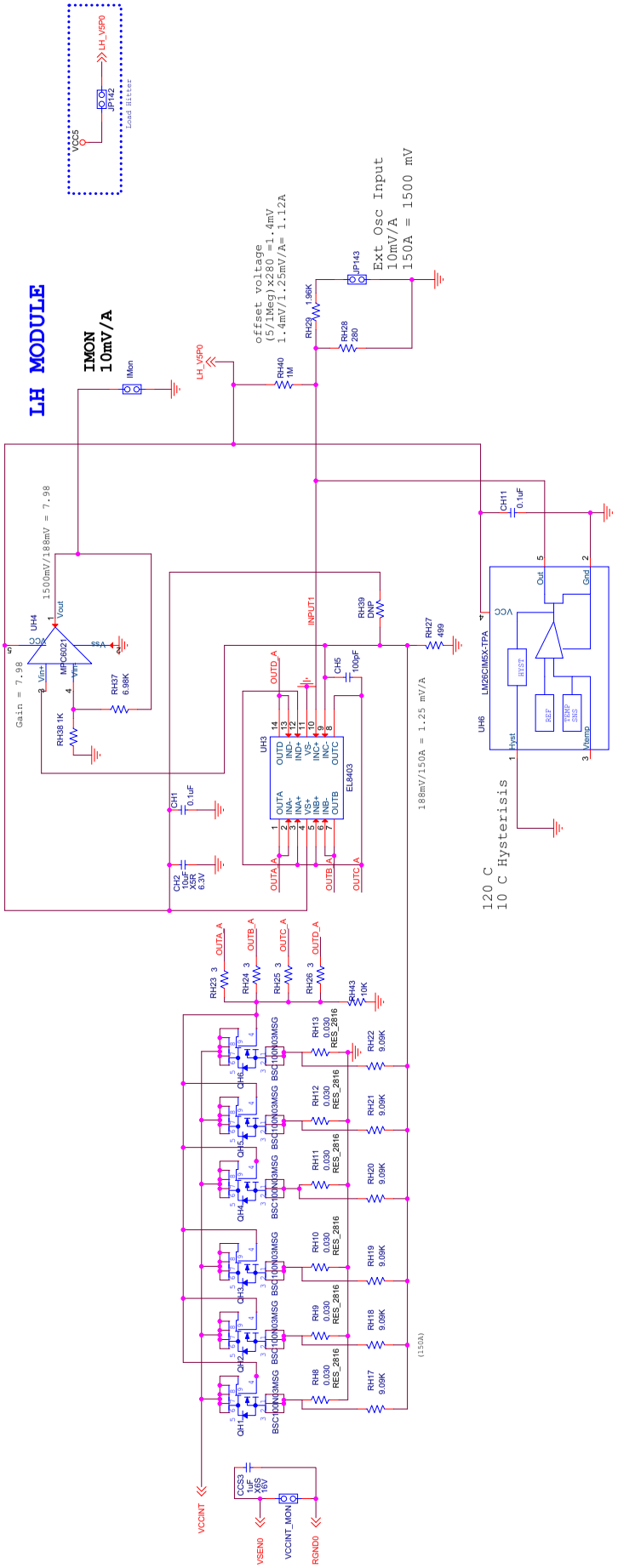


Figure 5. Schematic

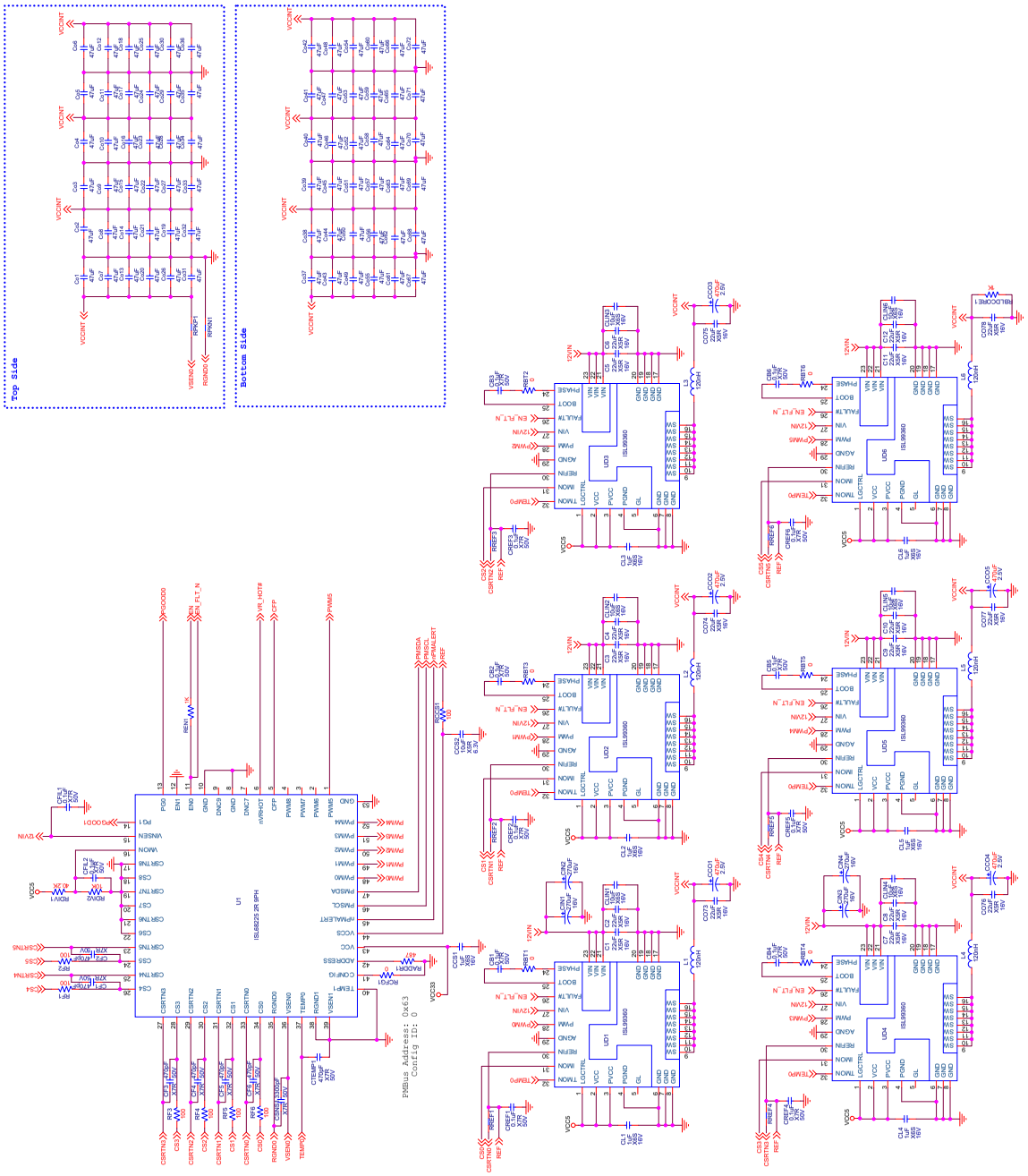


Figure 6. Schematic

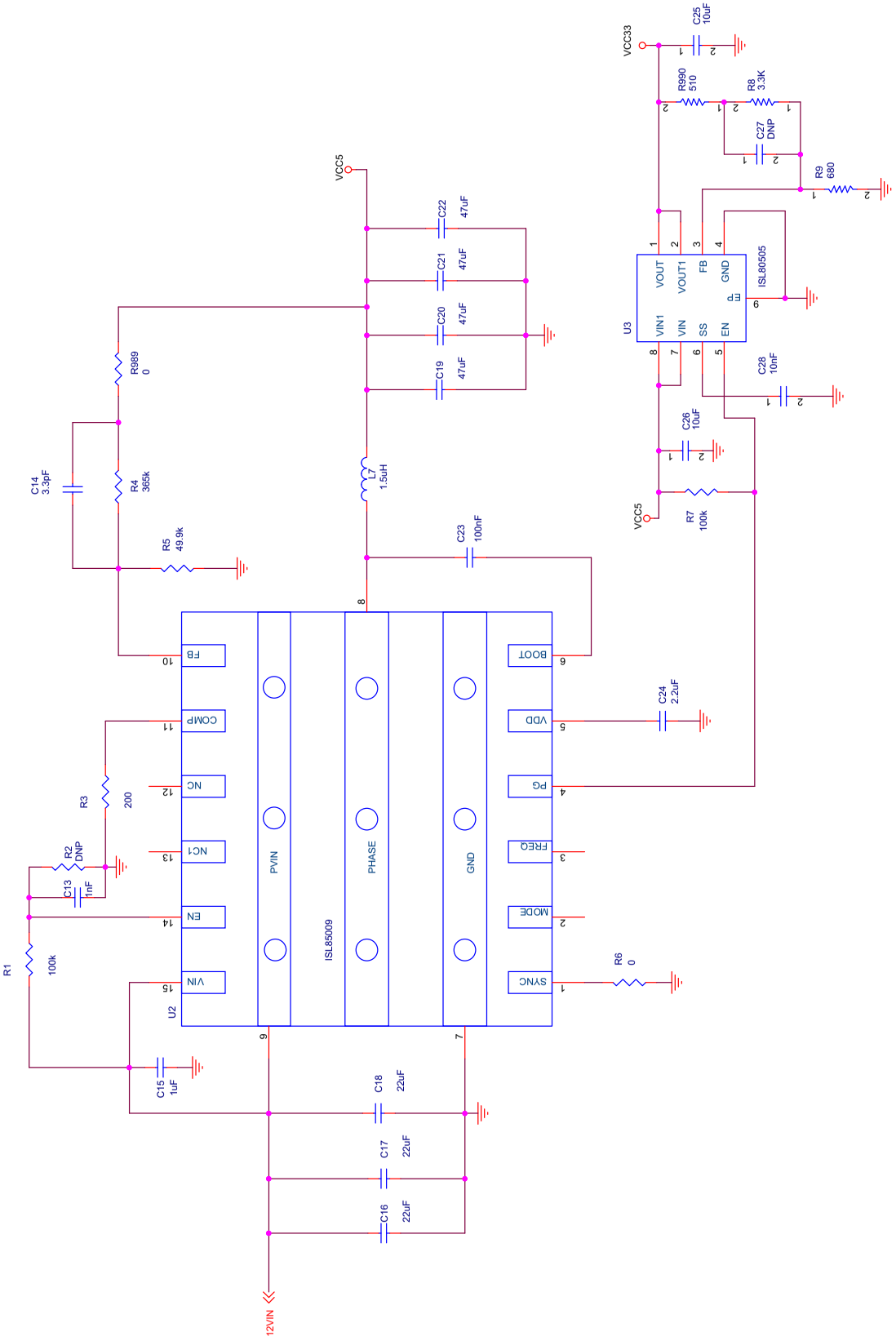


Figure 7. Schematic

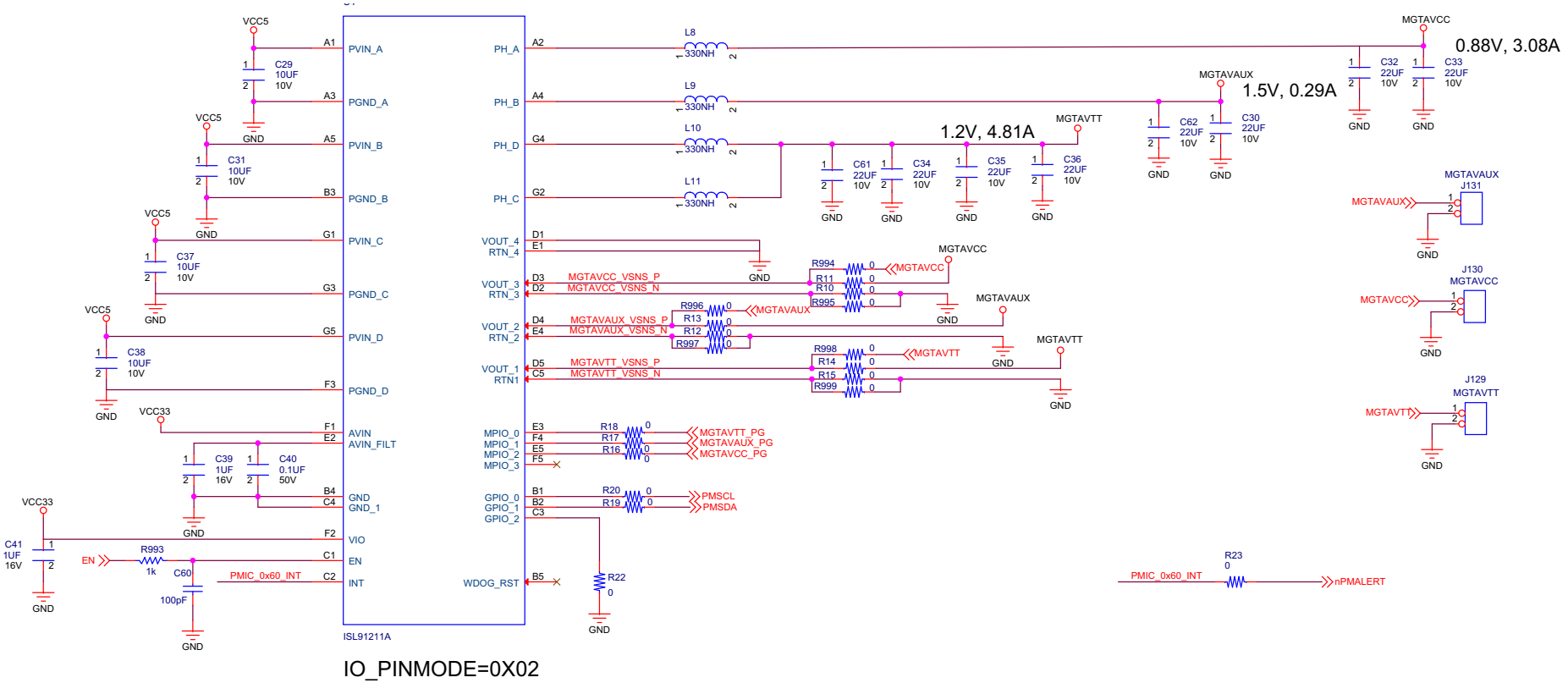


Figure 8. Schematic

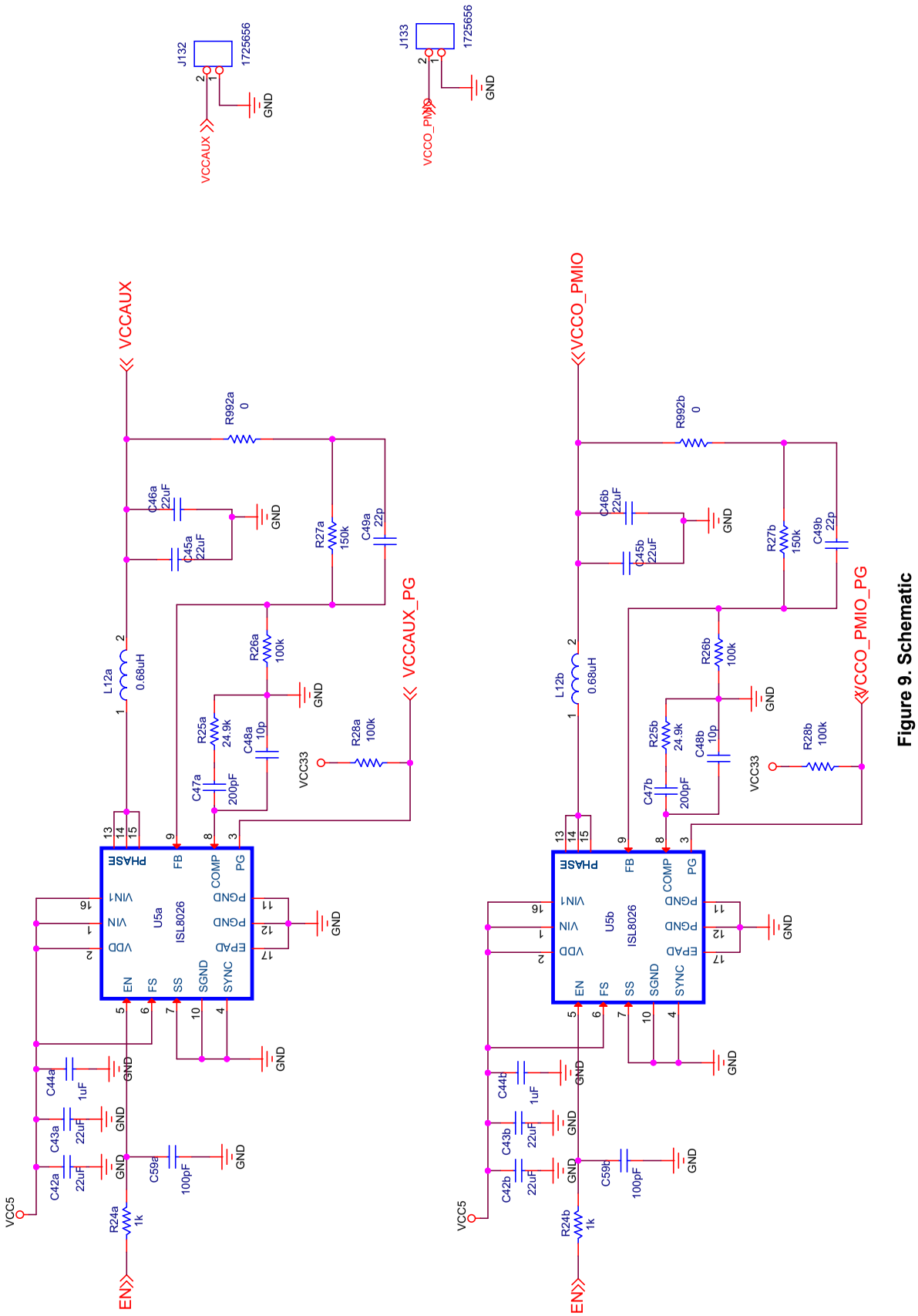


Figure 9. Schematic

3. Test Results

The performance test results includes the Versal demonstration board power map, digital multiphase features, VCCINT results, and all other rails test results. See Figure 2 for images of the reference board.

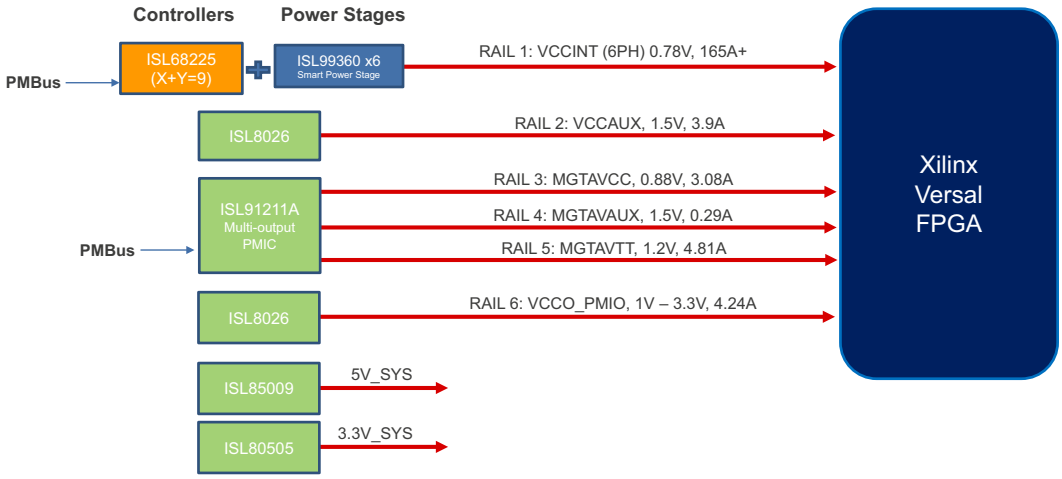


Figure 10. Power Map

3.1 Renesas Digital Multiphase Solutions

3.1.1 Digital multiphase controllers

- 50+ advanced digital multiphase controllers
  - Single, Dual, and Triple outputs
  - 2 to 20 phase support without phase doubler
- Support ANY CPU interface protocol
- Packages sizes from 4x4 to 8x8 QFN
  - 2-phase/ dual output in 32L 4x4mm QFN
  - 20-phase/dual output in 68L 8x8mm QFN

3.1.2 Industry leading performance

- Best-in-class transient response
- Excellent phase peak current management
  - Protects against inductor saturation without over design
- Industry first design support and debug tools
  - Serial interface packet logging: 1024 SVID command depth
  - Digital Test Bus: allows viewing of signals internal to the controller
  - Black Box: single point interface for fault diagnosis
- 48V conversion support
  - Common device characteristics and GUI

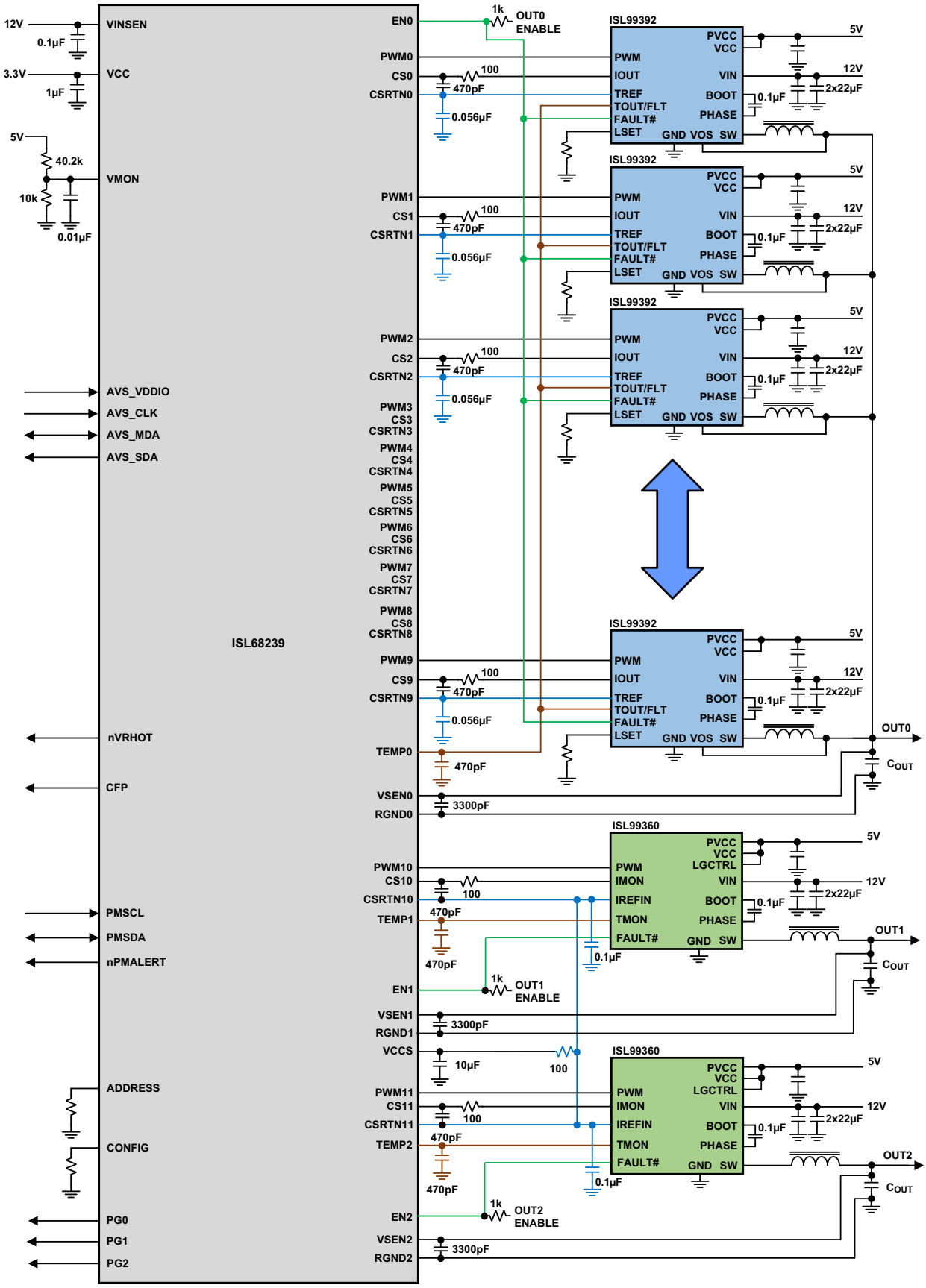


Figure 11. ISL68239 Application Diagram, 10+1+1 Solution Using Smart Power Stage

3.2 VCCINT Test Results

3.2.1 Startup and Shutdown Waveforms

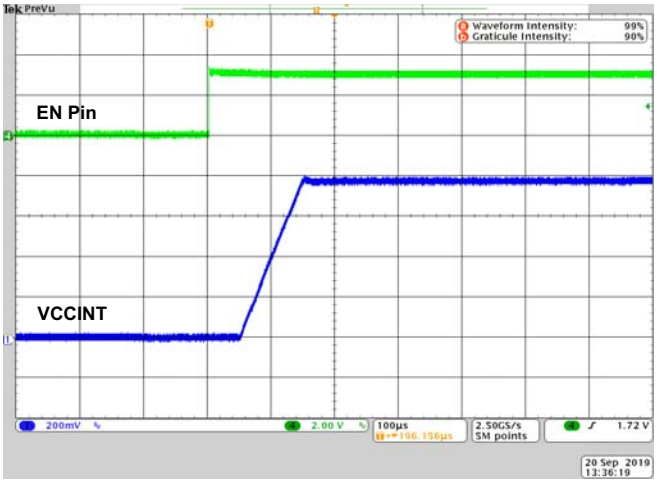


Figure 12. VCCINT Startup Waveform

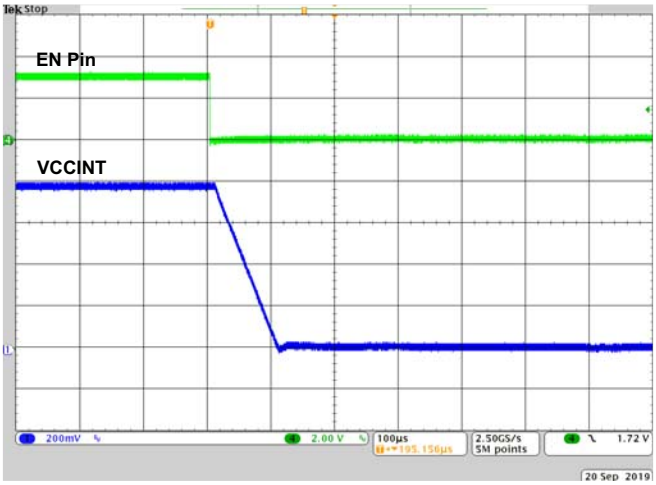


Figure 13. VCCINT Shutdown Waveform

3.3 VCCINT Efficiency

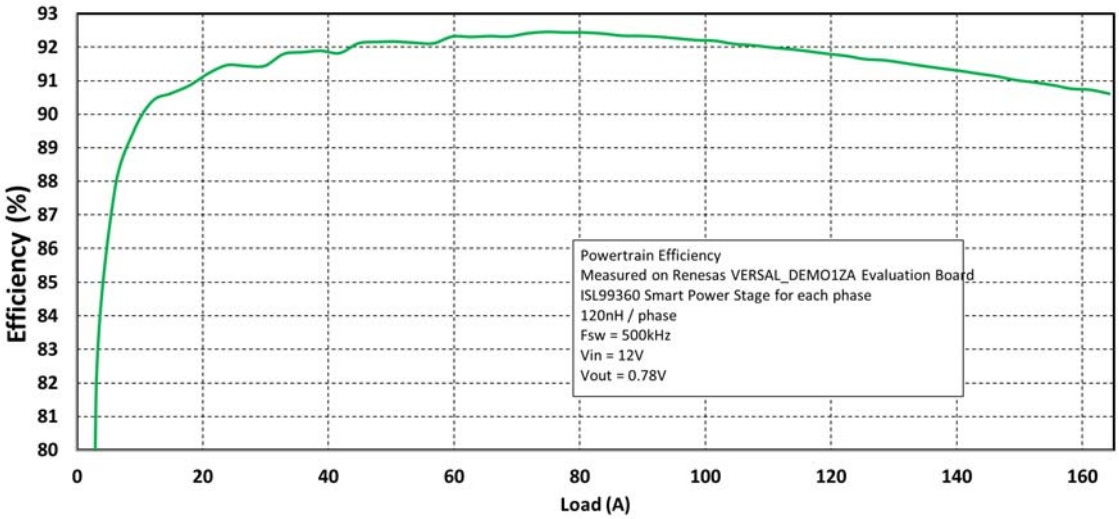


Figure 14. VCCINT Efficiency, 6-Phases

3.4 VCCINT I_{OUT} Telemetry Reporting

The board features excellent I_{OUT} reporting accuracy, with less than 2% error across full load range.

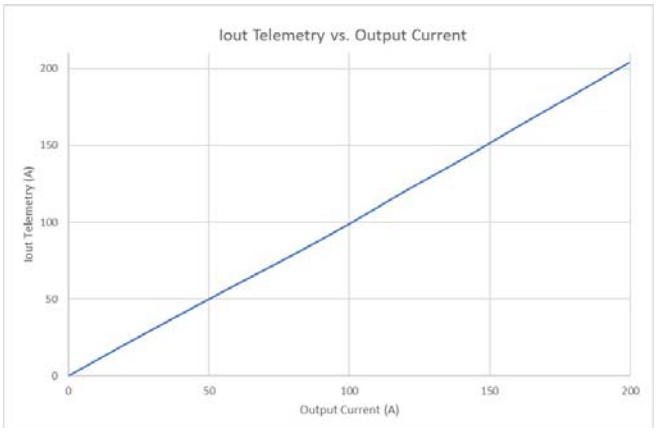


Figure 15. I_{OUT} Telemetry vs. Output Current

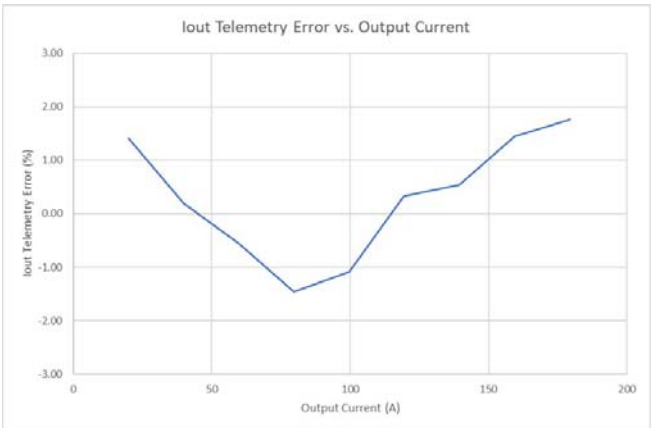


Figure 16. I_{OUT} Telemetry Error vs. Output Current

3.5 VCCINT OUTPUT Ripple

V_{OUT} ripple < ±5% at no load and 165A load. At no load, controller enters pulse skipping and diode emulation for improved efficiency.

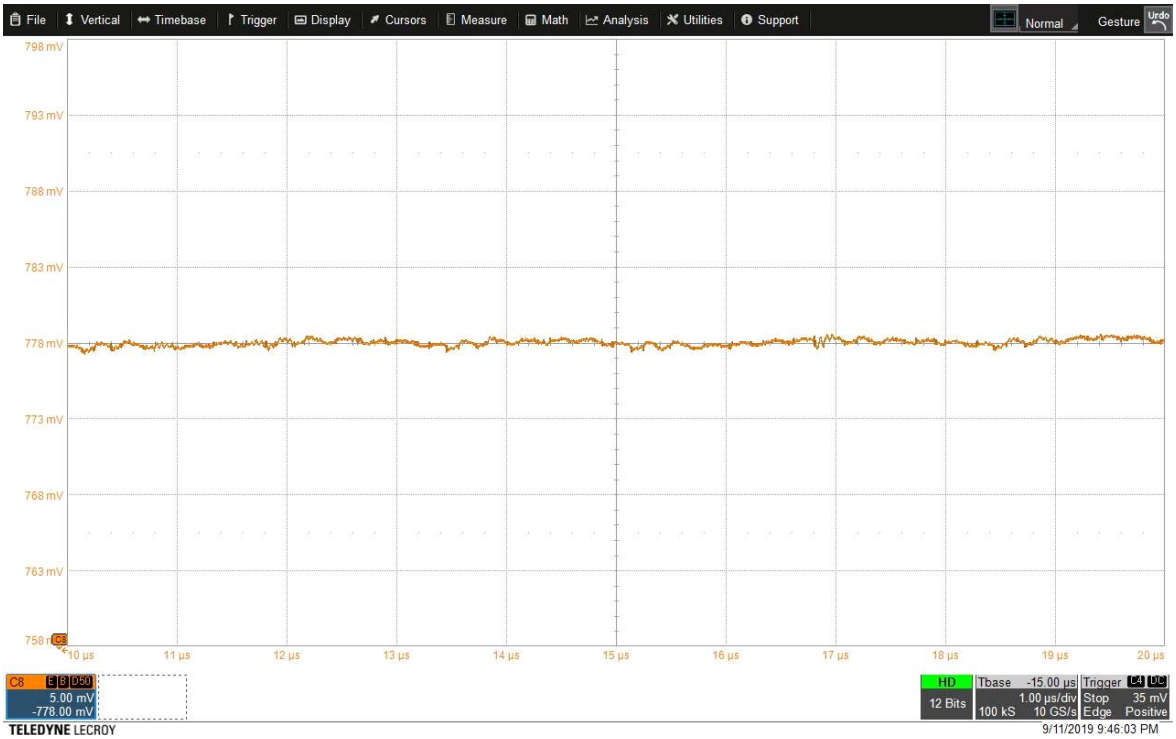


Figure 17. VCCINT OUTPUT Ripple, $12V_{IN}/0.78V_{OUT}$, No Load (PWF, DEM)

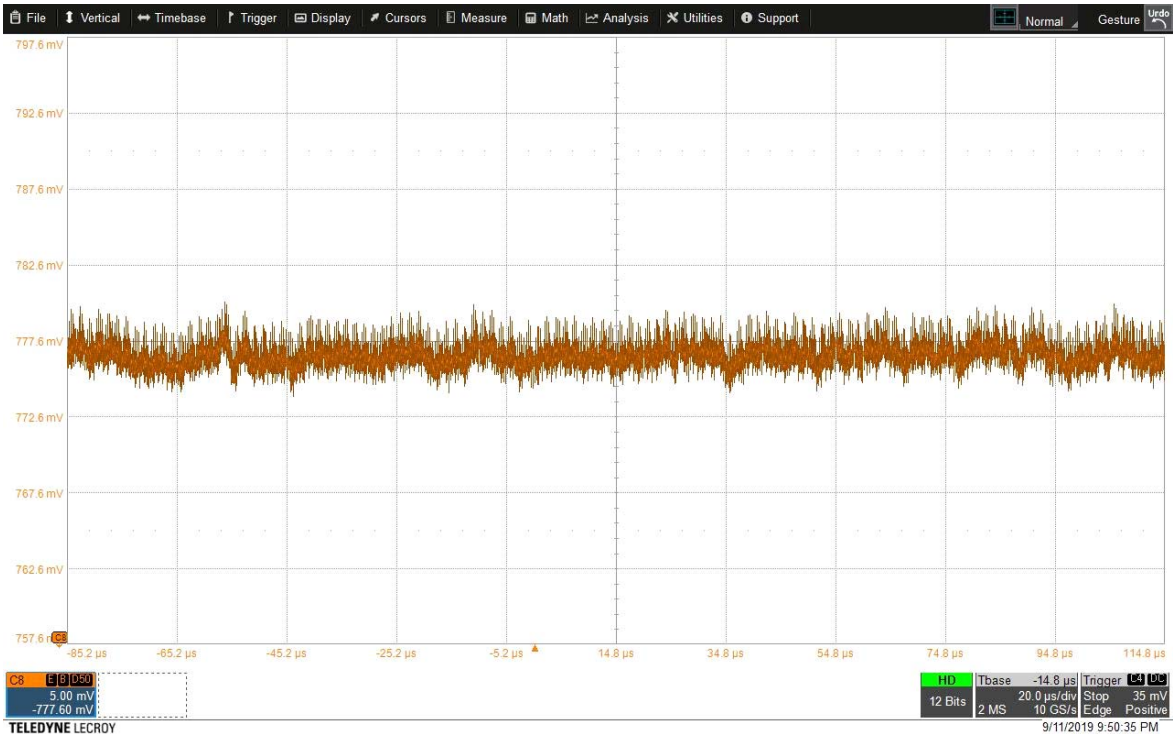
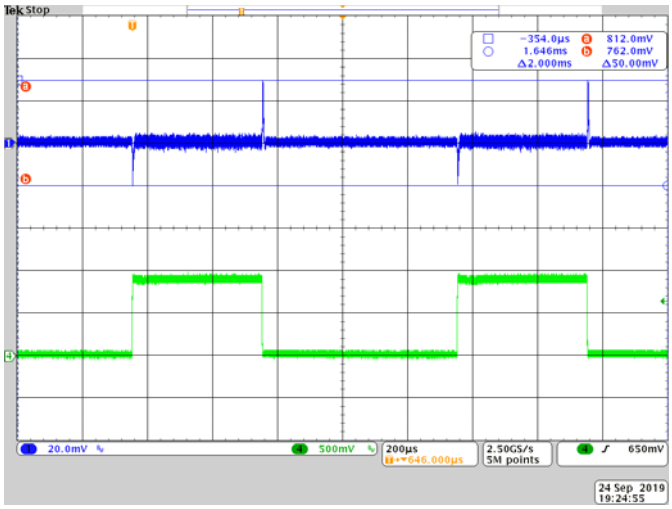


Figure 18. VCCINT OUTPUT Ripple, $12V_{IN}/0.78V_{OUT}$, Full Load 165A, V_{OUT} Ripple < ±5mV

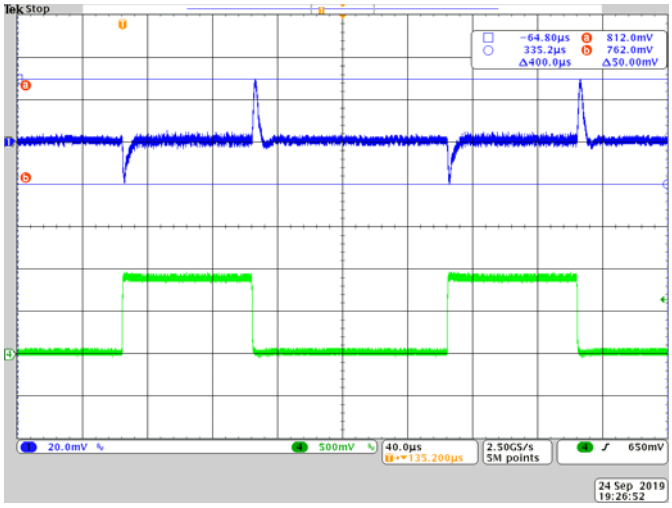
3.6 VCCINT Load Transient Waveforms



VCCINT Decoupling:

5 x 470µF/3mΩ POSCAP
6 x 22µF/0805
72 x 47µF/0805

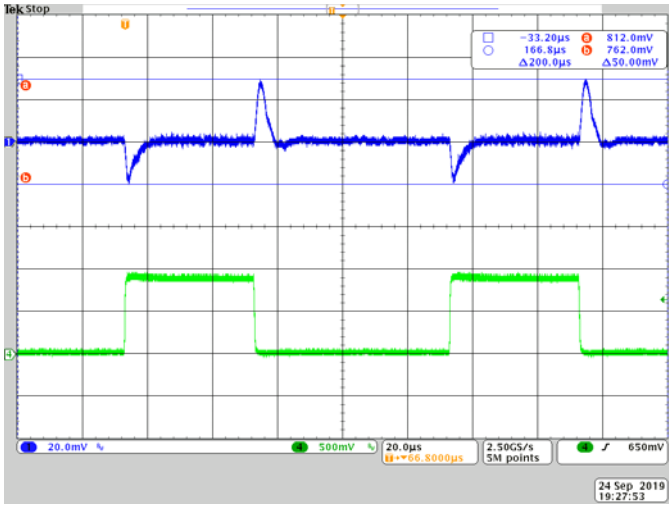
Figure 19. VCCINT Load Transient, $12V_{IN}/0.78V_{OUT}$/60A↔150A, 200A/µs, 1kHz Rep Rate, Measured at VCCINT_MON Test Point Bottom Side, Ch4: 50A/Div



VCCINT Decoupling:

5 x 470µF/3mΩ POSCAP
6 x 22µF/0805
72 x 47µF/0805

Figure 20. VCCINT Load Transient, 12V_{IN}/0.78V_{OUT}/60A↔150A, 200A/µs, 5kHz Rep Rate, Measured at VCCINT_MON Test Point Bottom Side, Ch4: 50A/Div



VCCINT Decoupling:

5 x 470µF/3mΩ POSCAP
6 x 22µF/0805
72 x 47µF/0805

Figure 21. VCCINT Load Transient, 12V_{IN}/0.78V_{OUT}/60A↔150A, 200A/µs, 10kHz Rep Rate, Measured at VCCINT_MON Test Point Bottom Side , Ch4: 50A/div

3.7 All Other Rails Test Results

3.7.1 VCCO_PMIO

Nominated Voltage: 1.5V, Max Load: 4.24A

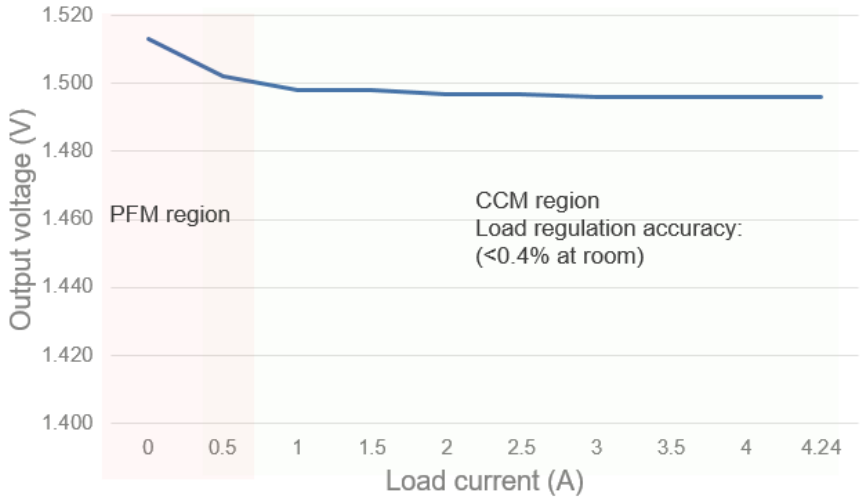


Figure 22. Load Regulation

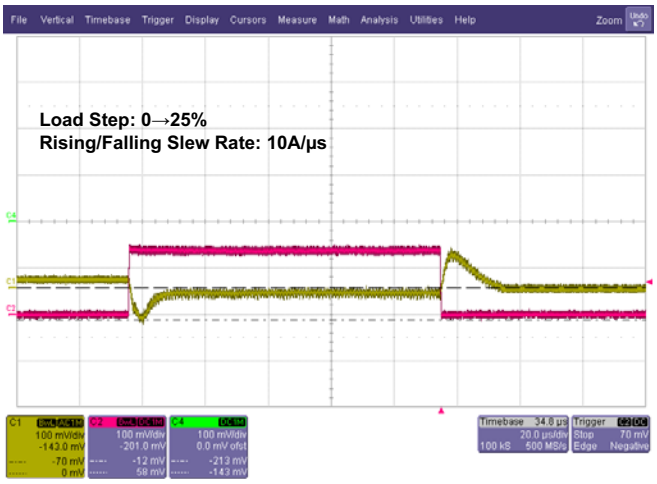


Figure 23. Load Transient Waveform

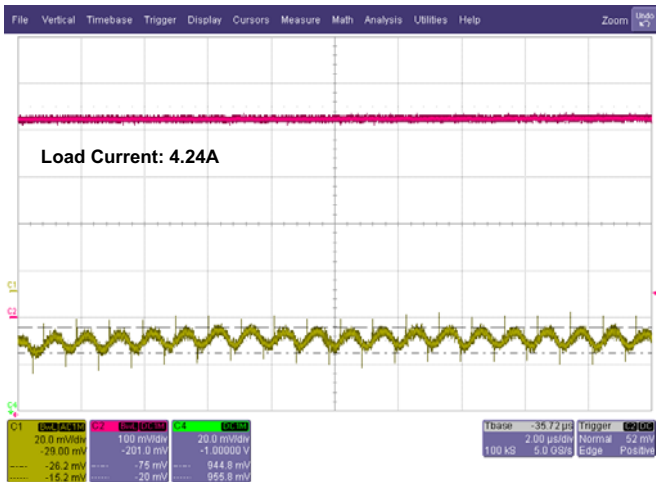


Figure 24. V_{OUT} Steady State Ripple

3.7.2 VCCAUX

Nominated Voltage: 1.5V, Max Load: 3.9A

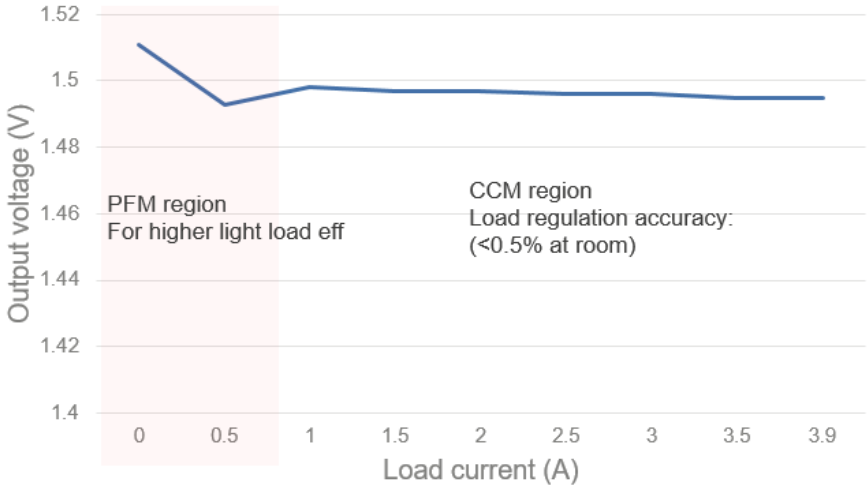


Figure 25. Load Regulation

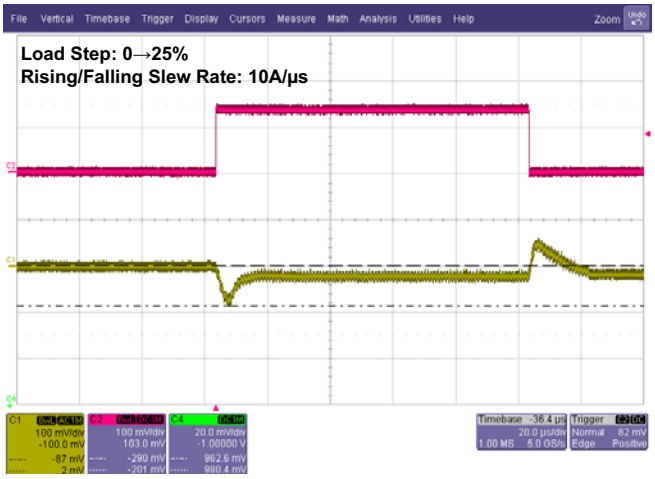


Figure 26. Load Transient Waveform

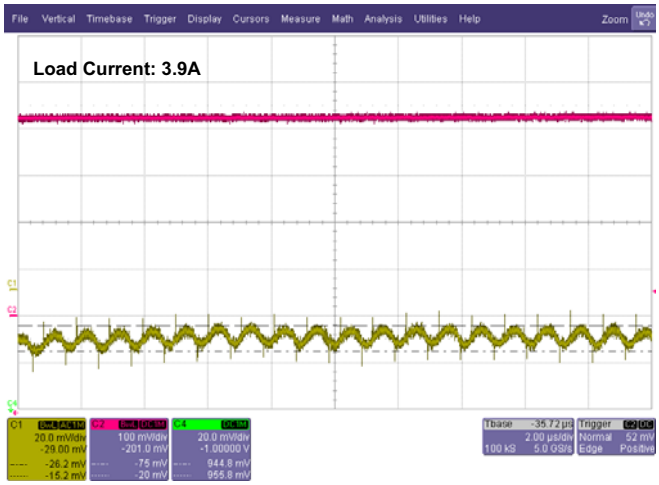


Figure 27. V_{OUT} Steady State Ripple

3.7.3 MGTAVTT

Nominated Voltage: 1.2V, Max Load: 4.81A

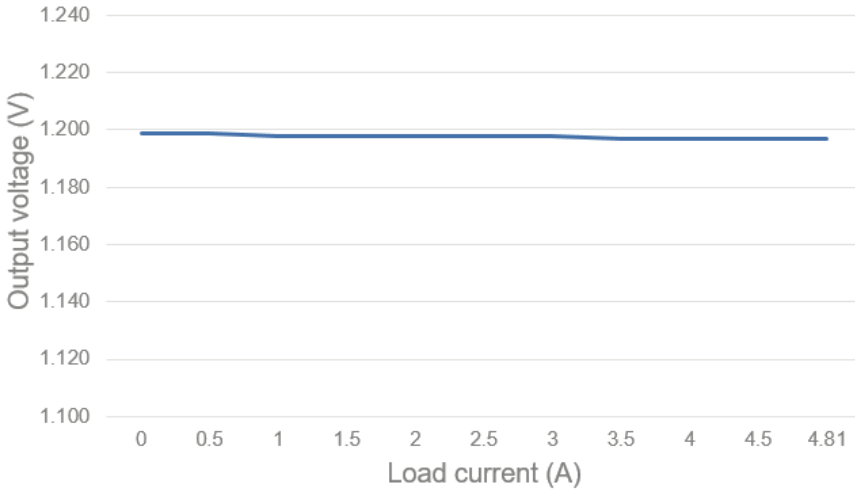


Figure 28. Load Regulation

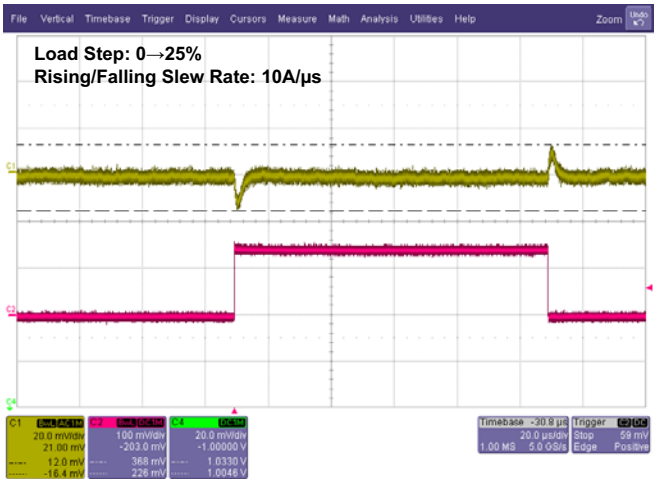


Figure 29. Load Transient Waveform

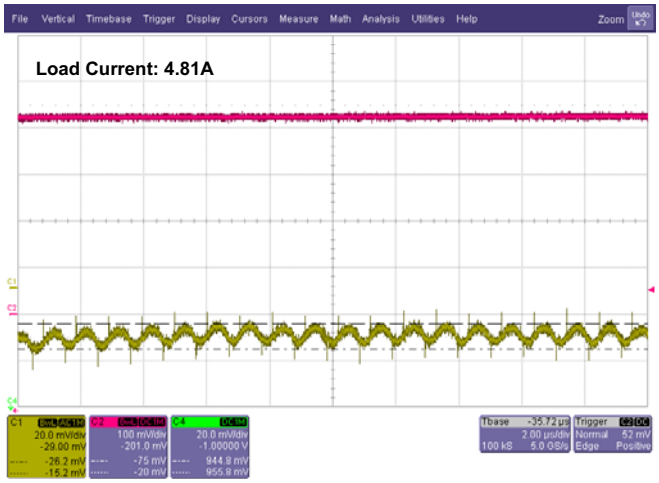


Figure 30. V_{OUT} Steady State Ripple

3.7.4 MGTAVAUX

Nominated Voltage: 1.5V, Max Load: 0.29A

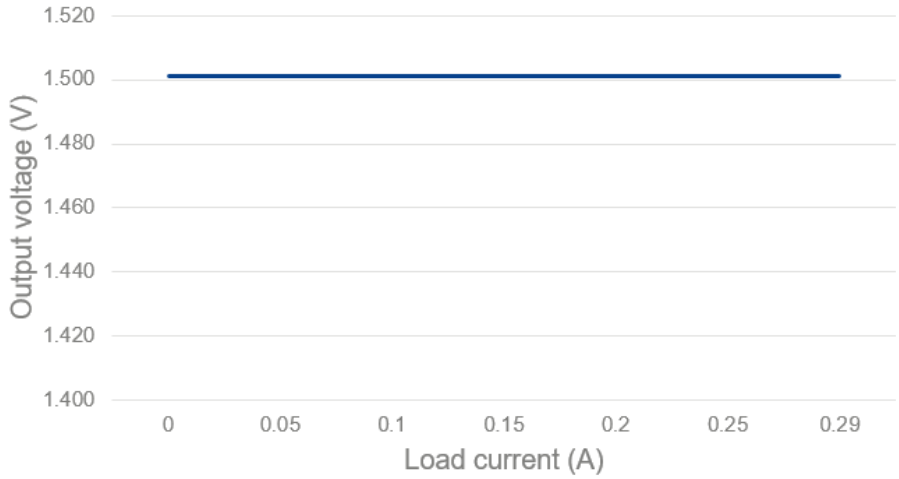


Figure 31. Load Regulation

Figure 32. Load Transient Waveform

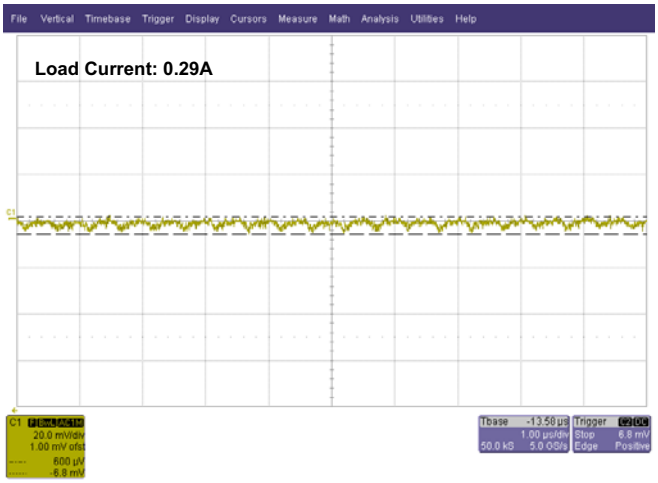


Figure 33. V_{OUT} Steady State Ripple

3.7.5 MGTAVCC

Nominated Voltage: 0.88V, Max Load: 3.08A

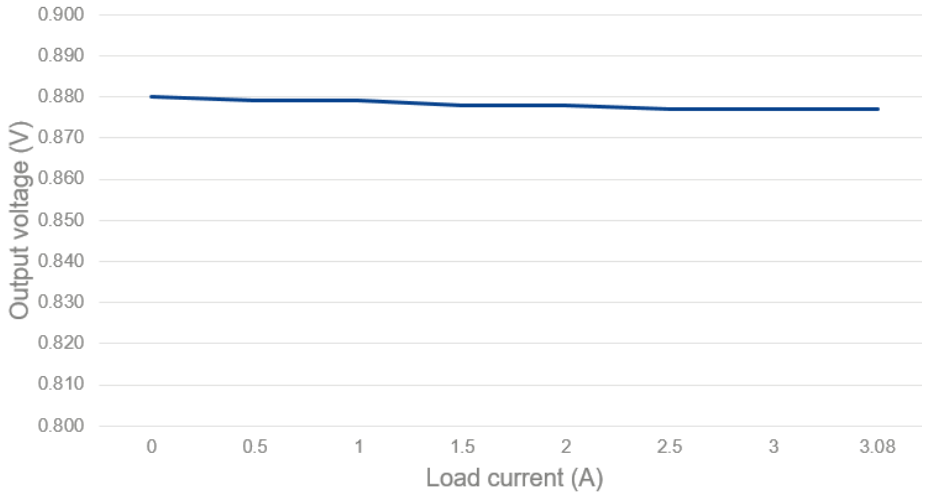


Figure 34. Load Regulation

Figure 35. Load Transient Waveform

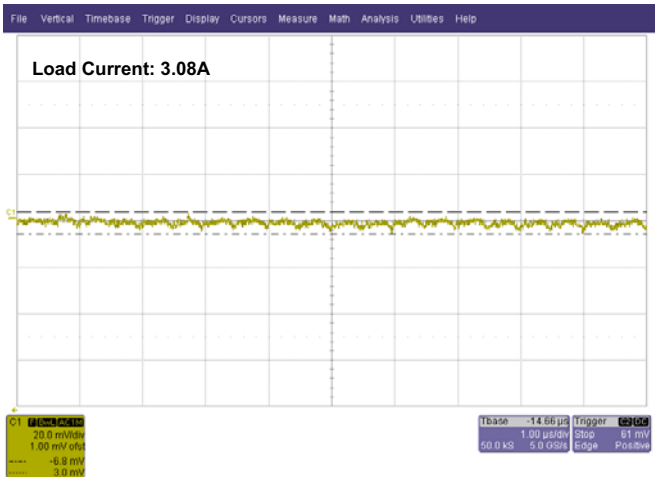


Figure 36. V_{OUT} Steady State Ripple

3.7.6 Startup and Shutdown

Startup and shutdown with no load condition

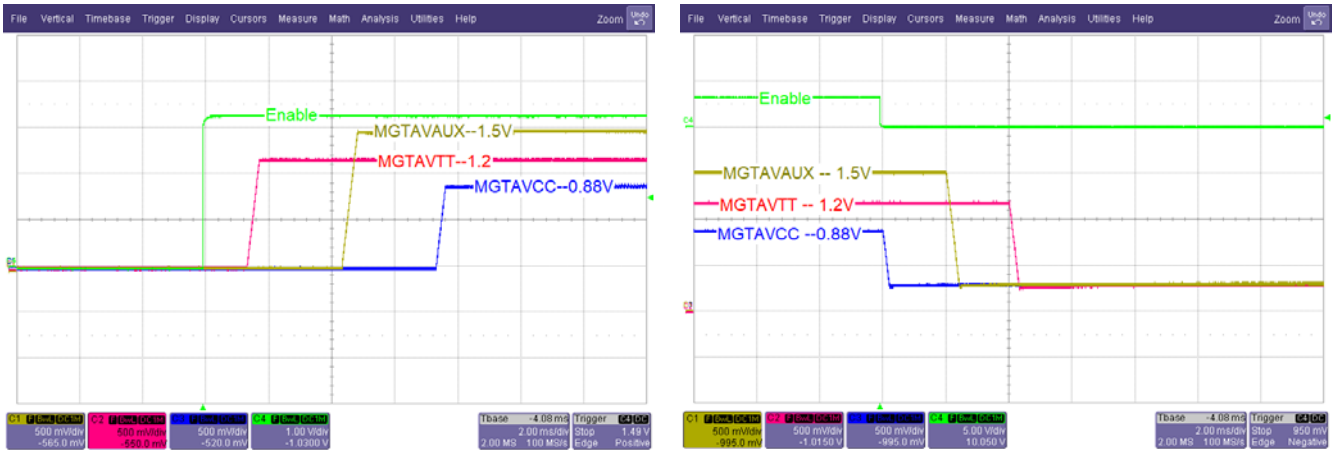


Figure 37. Power Rails from ISL91211 (PMIC)

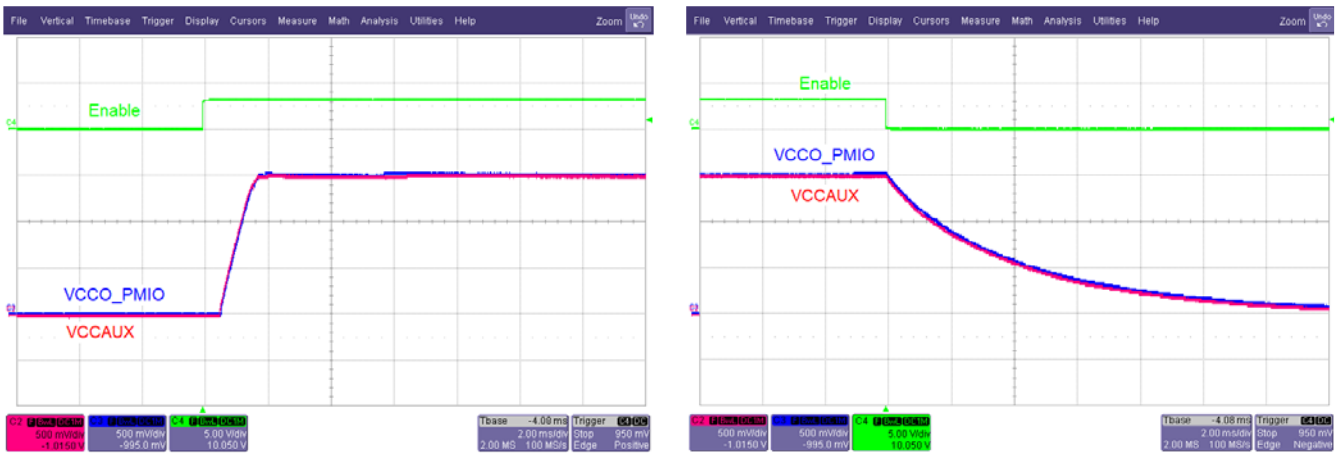


Figure 38. Power Rails of Two ISL8026 (Switching Regulator)

3.7.7 Thermal Performance of ISL91211(PMIC) and ISL8026 (Switching Regulator)

Thermal test was conducted after running each part under full load condition for 15mins, at room condition.

Figure 39. PMIC (ISL91211), All Three Rails Under Full Load Conditions

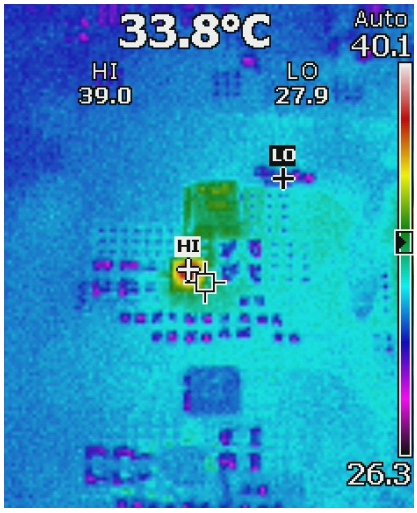


Figure 40. VCCO_PMIO (ISL8026) with Max Load = 4.24A

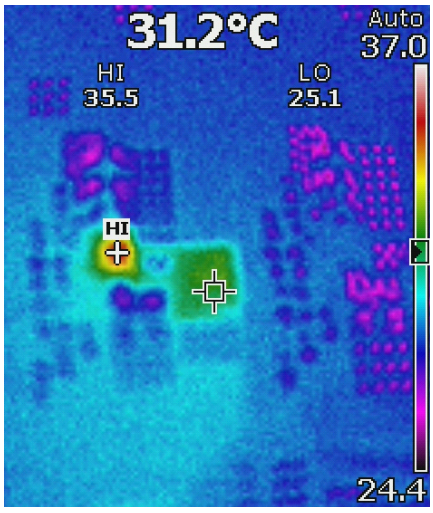


Figure 41. VCCAUX (ISL8026) with Max Load = 3.9A

4. Revision History

Rev.	Date	Description
1.00	Dec.13.19	Initial release

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