VIRTEX5MEZPWREV1Z

Radiation Hardened FPGA Power Solutions

AN1707
Rev.0.00
October 21, 2011

Intersil's Radiation Hardened FPGA Power Solutions

Introduction

The evolution of rad hard power solutions are being driven by changes implemented in the commercial market which have proven to provide higher efficiency and better performance. Space power is gradually adapting the distributed power architecture which dominates commercial power systems. Benefits of this architecture include reduction of distribution losses, improvement in regulation performance and a solution that can be modular. Another contribution that aids in the definition of radiation hardened power IC's is the rapid qualification and/or development of high performance digital components for space applications such as FPGA's and microprocessors. These digital IC's rival commercial counterparts in computing performance, low supply voltage and increased power consumption. Couple-in the need for a smaller, light-weight power solution and you will find Intersil at the forefront developing leading edge point-of-load (POL) regulators that meet the demands of today's space applications.

This application note discusses the VIRTEX5MEZPWREV1Z board, Intersil's reference design to power FPGA's in a radiation hardened environment. This particular board is optimized to power a Xilinx's Virtex-5 FPGA and features the ISL70001SRH and ISL70002SRH, rad hard POL buck regulators along with the ISL75051RH rad hard LDO.

FPGA Power Solution

The Virtex-5 requires a core voltage of 1.0V, which is supplied by the ISL70002SRH, an auxiliary voltage of 2.5V, which is supplied by the ISL70001SRH, and an I/O voltage of 3.3V which is supplied by the ISL75051RH (see Figure 1).

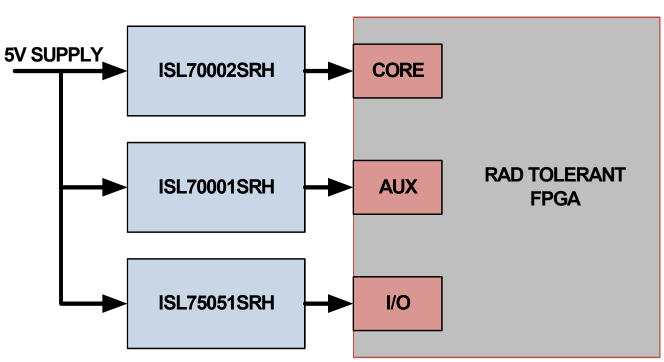


FIGURE 1. VIRTEX5MEZPWREV1Z BLOCK DIAGRAM

The ISL70001SRH and ISL70002SRH are both radiation hardened and SEE hardened high efficiency, monolithic synchronous buck regulators with integrated MOSFETs. These single chip power solutions operate over an input voltage range of 3V to 5.5V and provide a tightly regulated output voltage that is externally adjustable from 0.8V to ~85% of the input voltage. The ISL70001SRH can provide up to 6A ($T_J \leq +145°C$) of output current while the ISL70002SRH can provide up to 12A ($T_J \leq +150°C$) of output current.

The ISL75051SRH is a radiation hardened, low voltage, high current, single output LDO specified for up to 3.0A of continuous output current. It can operate over an input voltage range of 2.2V to 6.0V and is capable of providing output voltages of 0.8V to 5V with an external resistor divider. Dropout voltages as low as 65mV can be realized with this device.

Circuits Description

The 5V AC-DC adapter provides the input source through the 2.1mm barrel-jack connector. Proper sequence during power-up is maintained by connecting the PGOOD line of the ISL70002SRH to the ISL70001SRH's EN pin, which in turn has its PGOOD line tied to the EN pin of the ISL75051RH. This ensures that the core voltage is up first, followed by the auxiliary and then the I/O voltage (see Figure 3).

The output capacitors for each device have been chosen to minimize ESR in an effort to maintain output ripple <1% of the regulated voltage (for ISL70001SRH and ISL70002SRH) and to optimize the stability of the systems. KEMET's T530 series of tantalum capacitors offer ultra low ESR <15mΩ and are DLA certified.

Provisions for stability measurements are included. By replacing R23, R35 and R36 with 10Ω to 100Ω resistors and injecting the AC signal across TP1/TP2 for the ISL70001SRH, TP3/TP4 for the ISL70002SRH and TP5/TP6 for the ISL75051RH, AC measurements of the loop may be taken.

Radiation Tolerance

Total Iodizing Dose

These circuits are fabricated on a 0.6µm BiCMOS junction isolated process optimized for power management applications. They were hardened by design to achieve a Total Ionizing Dose (TID) rating of at least 100krads(Si) at the standard 50 to 300rad(Si)/s high dose rate as well as the standard <10mrad(Si)/s low dose rate. Well known TID hardening methods were employed such as closed geometry NMOS devices to reduce leakage and optimized bias levels for bipolar devices to compensate for gain reduction. For further information on radiation performance please navigate to www.intersil.com/space.

Single Event Effects

All three IC's were also hardened by design to a Linear Energy Transfer (LET) of 86.4MeV/mg/cm^2 by employing various SEE hardening techniques such as proper device sizing, filtering and special layout constraints. All three devices exhibit no latch-up or burnout up to their respective input voltage at an LET of 86.4 MeV/mg/cm^2.

Intersil is also the leader in Single Event Transient (SET) performance. The ISL70001SRH and the ISL70002SRH offer a <1% output voltage deviation due to SETs at an LET of 86.4MeV/mg/cm^2 (see Figure 2). Modern processors and FPGA offer a 5% tolerance window for the supply voltage. In some cases, the 5% tolerance includes DC voltage tolerance and transients due to load step or release and transients due to SETs.

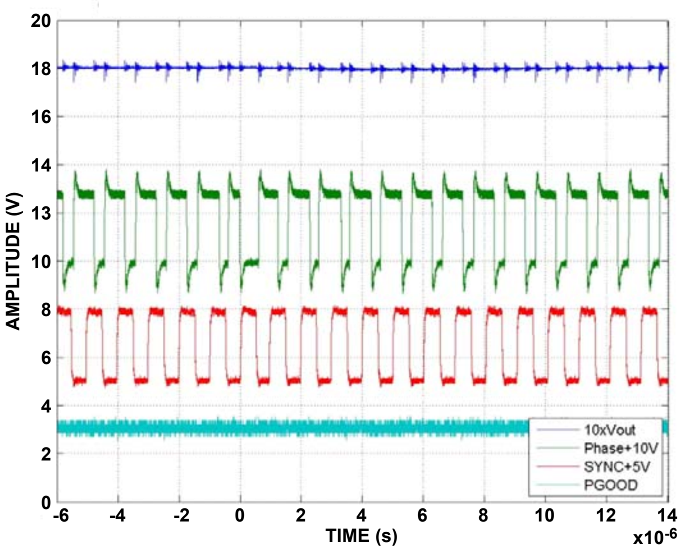


FIGURE 2. ISL70001SRH SET RESPONSE

Take for example, the ISL70001SRH. The output voltage tolerance is specified at 2%, this includes line and load regulation, and reference voltage tolerance over-temperature and radiation. An additional 1% may be attributed to end of life for the external resistors needed to set the output voltage. Load transients and SETs, it can safely be said, would not occur at the same time. Therefore, 2% can be allotted to a load transient which can be met with proper output filter selection. A total output voltage tolerance of 4% can be achieved - this includes DC shifts due to line, load and reference and SETs transients. A 5% output voltage tolerance will be achieved when there is a load transient. Intersil's rad hard POLs could easily meet the stringent requirements of modern space applications.

The ISL75051SRH also has class leading SET performance without the need of additional external filters as seen in other rad hard linear regulators. Figure 3 shows superimposed plots of LDO response during SETs. The upper and lower limits correlate to a 4% voltage perturbation. It can be seen that a -50mV deviation was the worst deviation seen in this run.

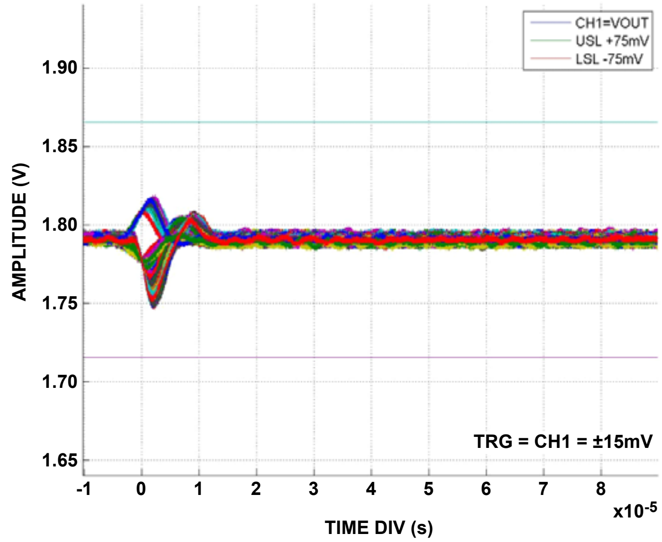


FIGURE 3. ISL75051SRH SET RESPONSE

Additional Design Features

This section discusses two additional features that may be added to further improve reliability and enhance the power capability of the reference design.

Current Sharing for the ISL70002SRH

Modern digital components are requiring greater supply currents to meet the demands for the ever increasing need of processing power in space systems. For applications where the core voltage requires more than 12A of continuous current, the ISL70002SRH may be used in a multiphase solution. Two ISL70002SRH's can current share and provide up to 19A of continuous current to the processor, FPGA, or any other load. The current share architecture features triple redundancy for single event transient mitigation. For a detailed description on current sharing refer to the ISL70002SRH datasheet.

Power-on Reset

The addition of a rad tolerant POR chip such as the ISL705ARH could further improve reliability by allowing proper sequence to initiate only after the 5V intermediate voltage has reached its optimal steady-state condition. With the added feature of a watchdog timer, the ISL705ARH will also monitor the FPGA or processor for proper execution and send a reset signal if not toggled within 1.0s. Intersil also offers the ISL706XRH series of voltage supervisors dedicated to 3.3V rails. For more information on the ISL705XRH and ISL706XRH see datasheet FN7662.

Related Literature

- ISL70001SRH Datasheet FN6947
- ISL70002SRH Datasheet
- ISL75051SRH Datasheet

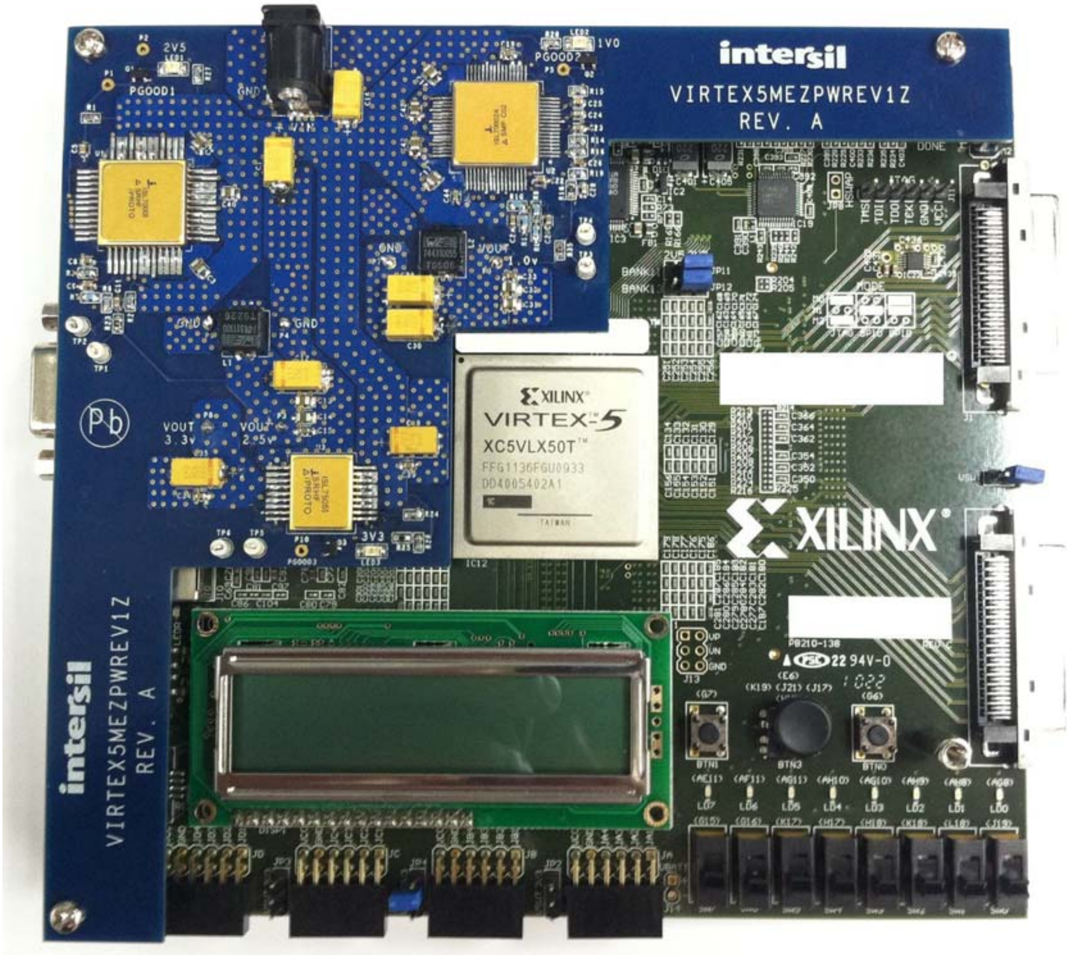


FIGURE 4. RADIATION HARDENED FPGA POWER SOLUTIONS REFERENCE DESIGN

Typical Performance Curves

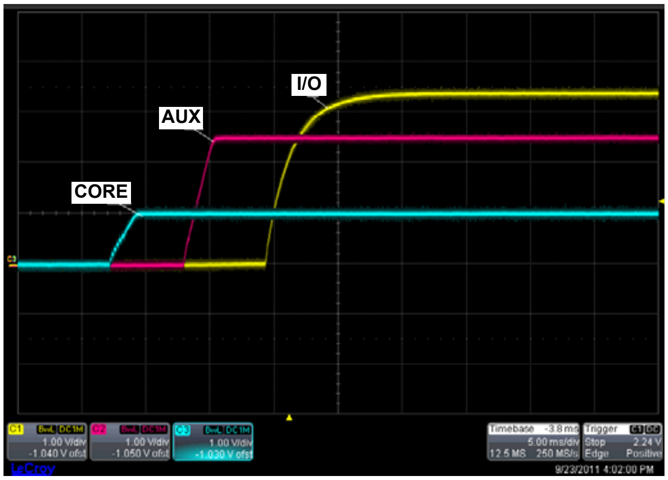


FIGURE 5. START-UP SEQUENCE

FIGURE 6. ISL70002SRH CORE OUTPUT VOLTAGE RIPPLE

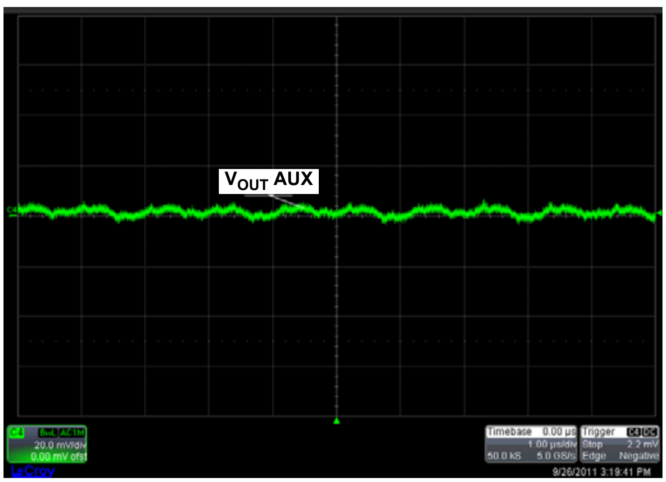


FIGURE 7. ISL70001SRH AUXILIARY VOLTAGE RIPPLE

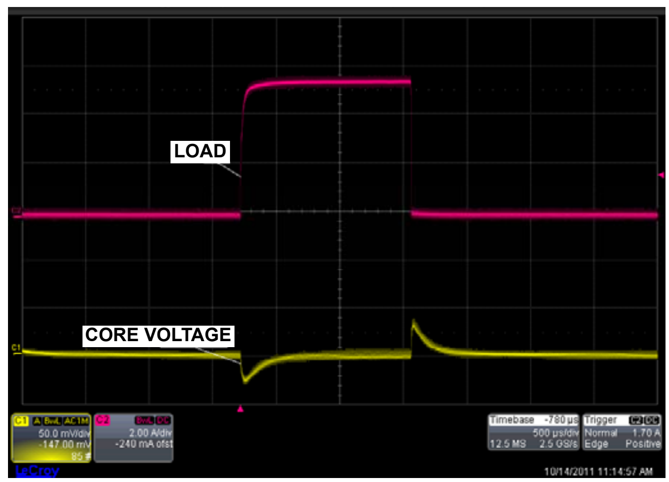


FIGURE 8. CORE VOLTAGE 3A LOAD TRANSIENT RESPONSE

FIGURE 9. AUXILIARY VOLTAGE 3A LOAD TRANSIENT RESPONSE

FIGURE 10. I/O VOLTAGE 1.5A LOAD TRANSIENT RESPONSE

Typical Performance Curves (Continued)

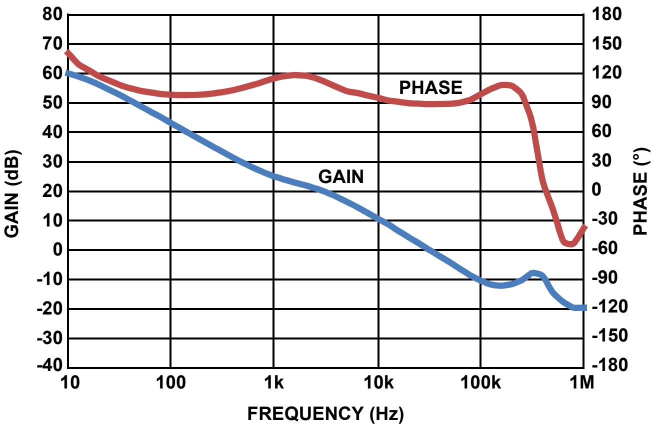


FIGURE 11. ISL70002SRH AC RESPONSE AT 12A LOAD

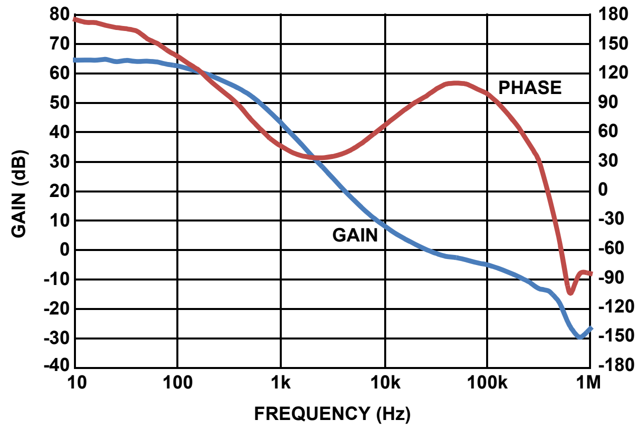


FIGURE 12. ISL70001SRH AC RESPONSE AT 6A LOAD

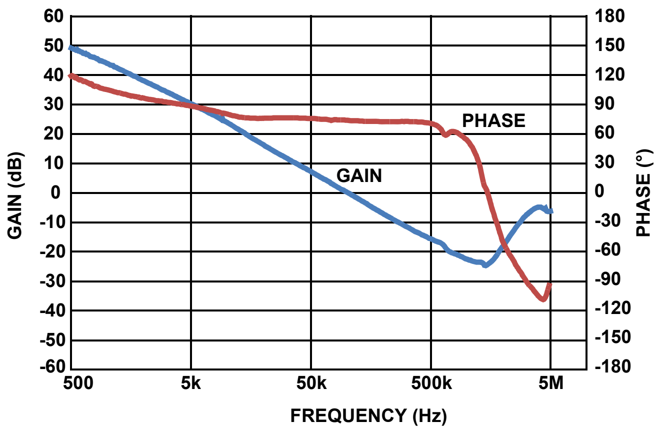
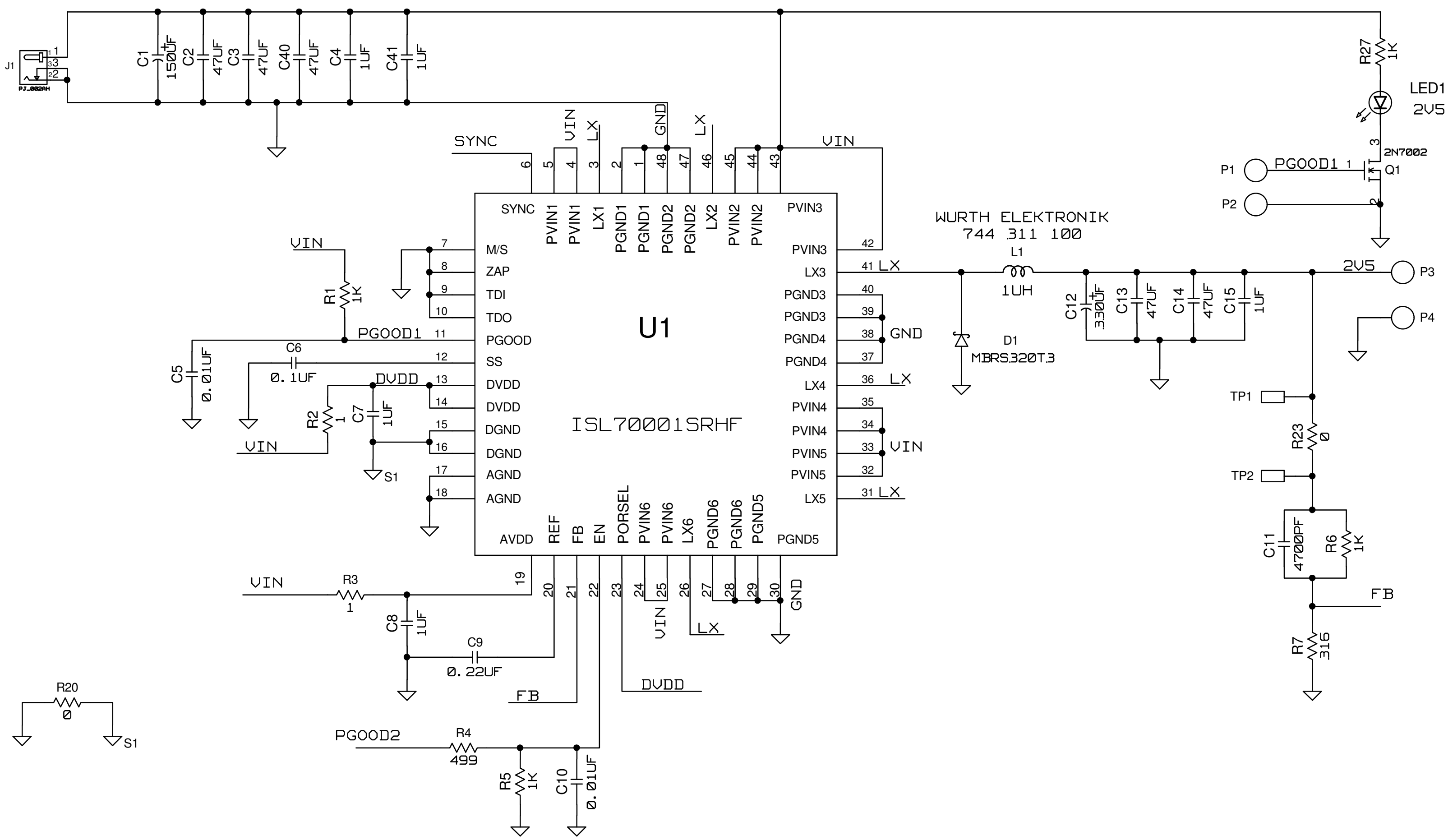
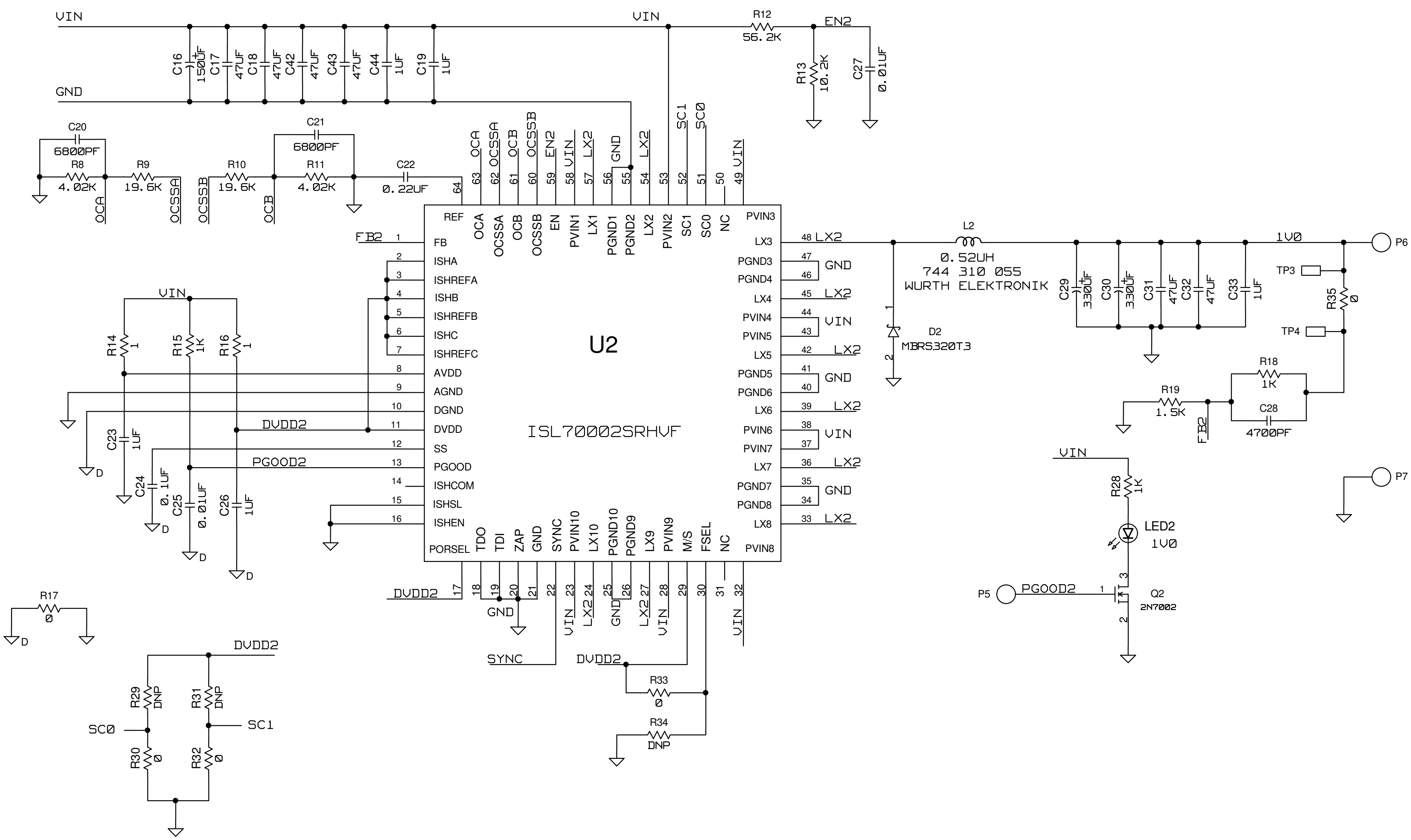


FIGURE 13. ISL75051SRH AC RESPONSE AT 3A LOAD

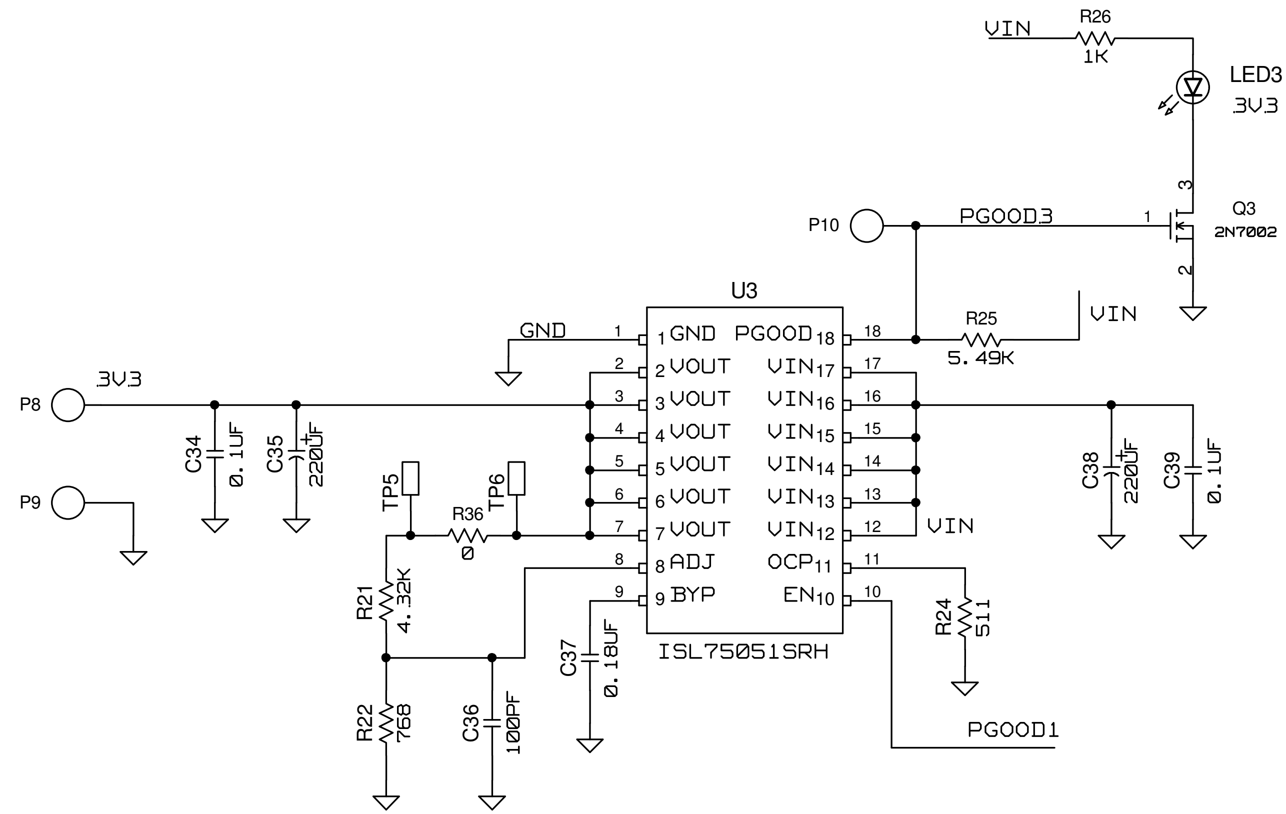
ISL70001SRH Schematic



ISL70002SRH Schematic



ISL75051RH Schematic



VIRTEX5MEZPWREV1Z Bill of Materials

REF DES.	PART NUMBER	QTY	MANUFACTURER	DESCRIPTION
Q1	2N7002-7-F	1	FAIRCHILD	N-Channel EMF Effect Transistor (Pb-Free)
Q2, Q3	2N7002L	2	ON Semi	N-Channel 60V 115mA MOSFET
TP1-TP6	5002	6	KEYSTONE	Miniature White Test Point 0.100 Pad 0.040 Thole
LED1-LED3	597-3311-407	3	Dialight	Surface Mount Green LED
R17, R20, R23, R30, R32, R33, R35, R36	ERJ3GEY0R00V	8	PANASONIC	Thick Film Chip Resistor
C37	GRM188R71E184KA88	1	GENERIC	Multilayer Cap
C36	H1045-00101-50V5	1	GENERIC	Multilayer Cap
C5, C10	H1045-00103-16V10	2	GENERIC	Multilayer Cap
C25, C27	H1045-00103-25V10	2	GENERIC	Multilayer Cap
C6	H1045-00104-16V10	1	GENERIC	Multilayer Cap
C24, C34, C39	H1045-00104-25V10	3	GENERIC	Multilayer Cap
C7, C8	H1045-00105-16V20	2	GENERIC	Ceramic Cap
C9, C22	H1045-00224-16V10	2	GENERIC	Multilayer Cap
C11, C28	H1045-00472-50V10	2	GENERIC	Multilayer Cap
C20, C21	H1045-00682-50V10	2	GENERIC	Multilayer Cap
C2, C3, C13, C14, C17, C18, C31, C32, C40, C42, C43	H1046-00476-16V20	11	GENERIC	Multilayer Cap
R29, R31, R34	H2505-DNP-DNP-1	3	GENERIC	Metal Film Chip Resistor (Do Not Populate)
R2, R3, R14, R16	H2511-00010-1/10W1	4	GENERIC	Thick Film Chip Resistor
R1, R5, R6, R27	H2511-01001-1/16W1	4	GENERIC	Thick Film Chip Resistor
R21	H2511-04321-1/16W1	1	GENERIC	Thick Film Chip Resistor
R24	H2511-05110-1/16W1	1	GENERIC	Thick Film Chip Resistor
R25	H2511-05491-1/16W1	1	GENERIC	Thick Film Chip Resistor
R12	H2511-05622-1/16W1	1	GENERIC	Thick Film Chip Resistor
R22	H2511-07680-1/16W1	1	GENERIC	Thick Film Chip Resistor
U1	ISL70001SRHF	1	INTERSIL	4.2A/6A Synchronous Buck Regulator
U2	ISL70002SRHVF	1	INTERSIL	12A Synchronous Buck Regulator w/MOSFET
D1, D2	MBRS320T3	2	ON-SEMI	3A 20V Schottky Power Rectifier
R26	MCR03EZPFX1001	1	ROHM	Metal Film Chip Resistor
J1	PJ-002AH	1	CUI-INC	DC Power Jack
R13	RG1608P-1022-B-T5	1	SUSUMU	Thick Film Chip Resistor
R18	S0603CA1001BEB	1	State of the Art	Thick Film Chip Resistor

VIRTEX5MEZPWREV1Z Bill of Materials (Continued)

REF DES.	PART NUMBER	QTY	MANUFACTURER	DESCRIPTION
R19	S0603CA1501BEZ	1	State of the Art	25ppm Thin Film Chip Resistor
R9, R10	S0603CA1962BEZ	2	State of the Art	25ppm Thin Film Chip Resistor
R7	S0603CA3160BEB	1	State of the Art	Thick Film Chip Resistor
R8, R11	S0603CA4021BEZ	2	State of the Art	25ppm Thin Film Chip Resistor
R15, R28	S0603CPX1001F10	2	State of the Art	Thick Film Chip Resistor
R4	S0603CPX4990F10	1	State of the Art	Thick Film Chip Resistor
C35, C38	T525D227M010ATE025	2	KEMET	Ripple 3000mA ESR 25mΩ Polymer Tantalum Capacitor
C1, C16	T530X157M016ATE015	2	KEMET	High Capacitance Ultra-Low ESR Tantalum SMD Cap
C12, C29, C30	T530X337M010ATE005	3	KEMET	High Capacitance Ultra-Low ESR Tantalum SMD Cap
C4, C15, C19, C23, C26, C33, C41, C44	TMK107BJ105KA-T	8	Taiyo Yuden	Ceramic Cap
U3	ISL75051SRH	1	INTERSIL	18 Pin Flat-Pack Package K18.A
P1-P10	PAD_80	10	GENERIC	0.080 Pad with .037 Plated Thru Hole
L1	744311100	1	Wurth Elektronik	SMT Power Inductor
L2	744310055	1	Wurth Elektronik	SMT Power Inductor

VIRTEX5MEZPWREV1Z Board Layout

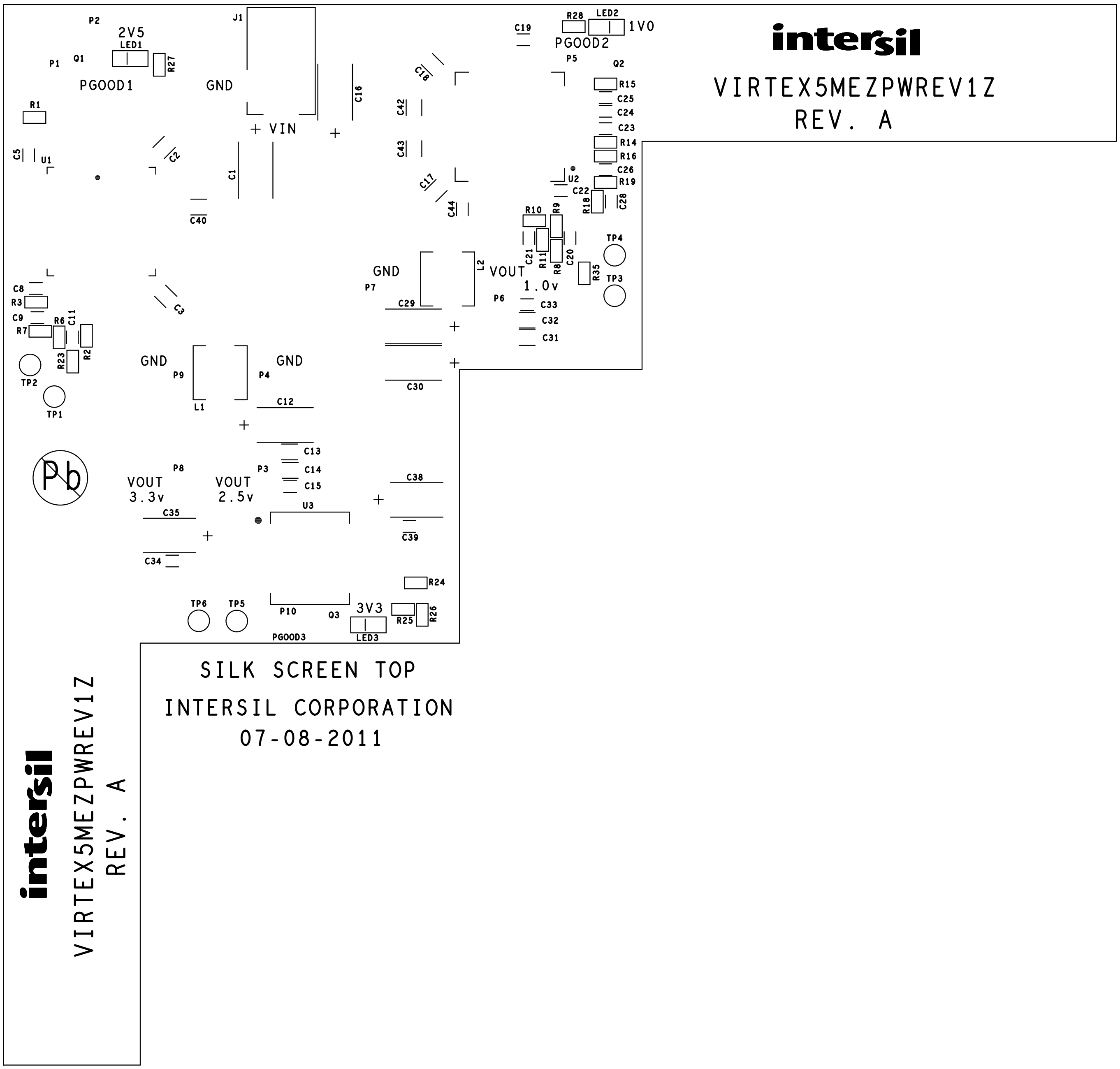


FIGURE 14. TOP COMPONENTS

VIRTEX5MEZPWREV1Z Board Layout (Continued)

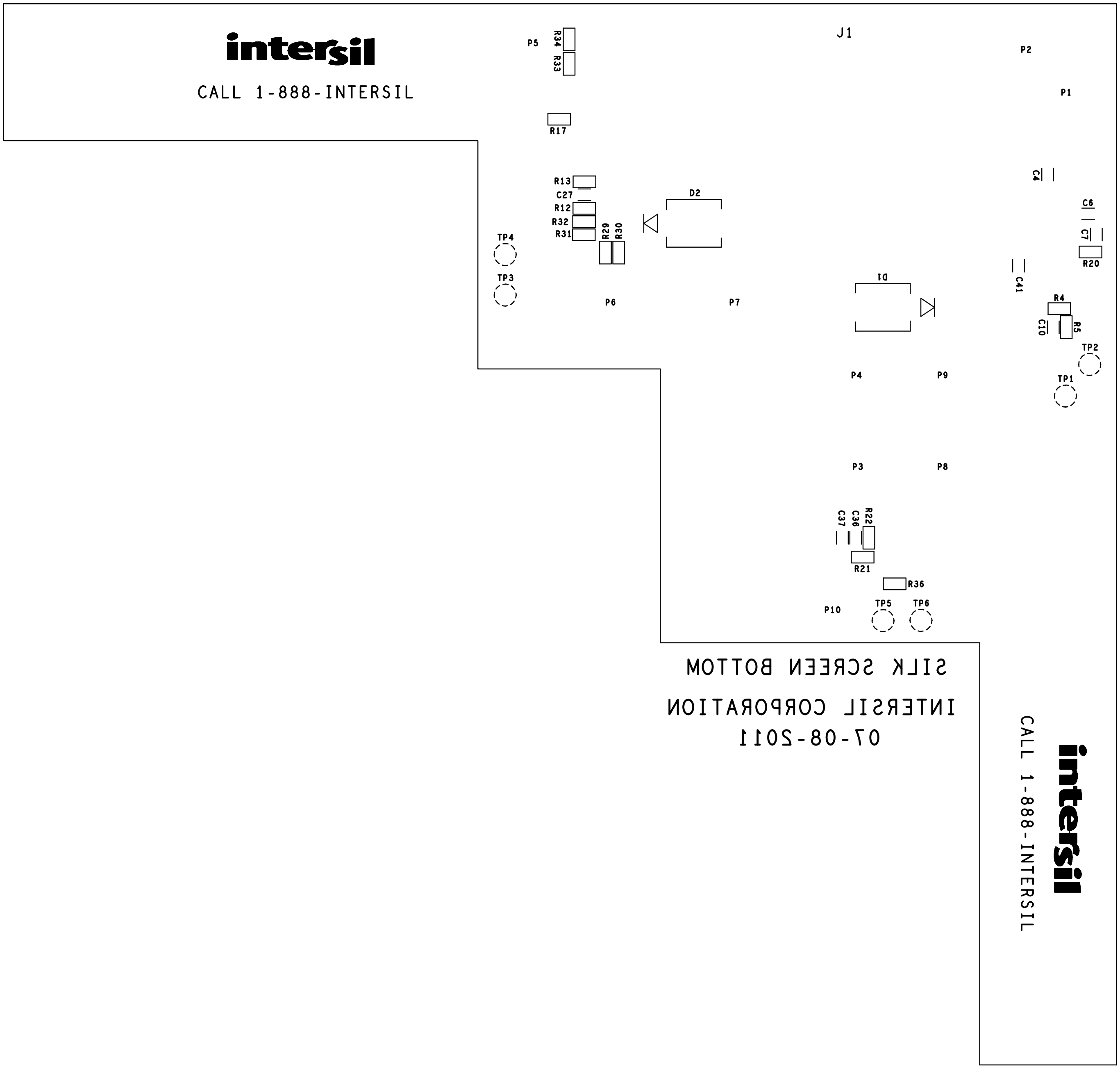


FIGURE 15. BOTTOM LAYER (MIRRORED)

VIRTEX5MEZPWREV1Z Board Layout (Continued)

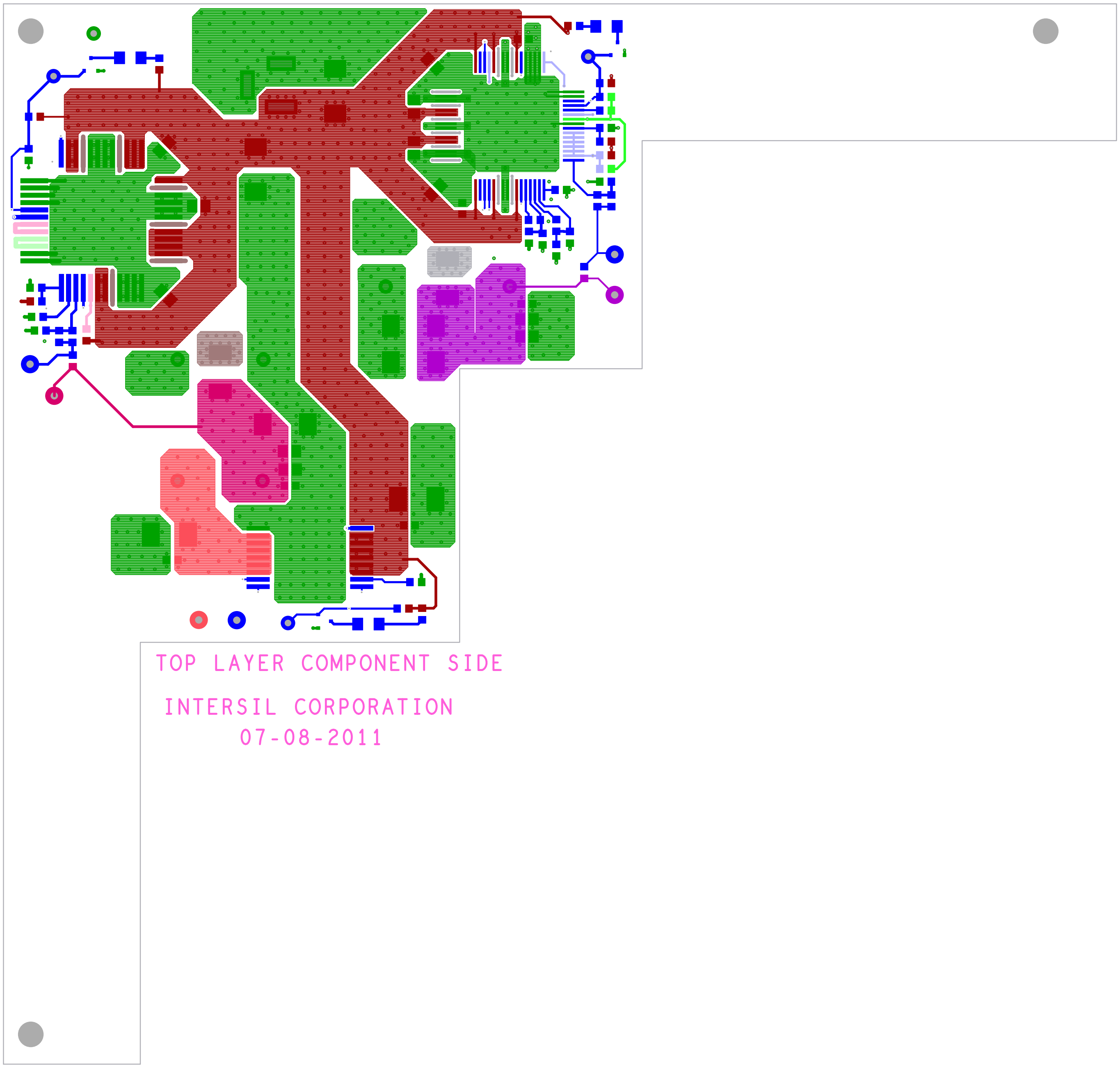


FIGURE 16. 1ST LAYER

VIRTEX5MEZPWREV1Z Board Layout (Continued)

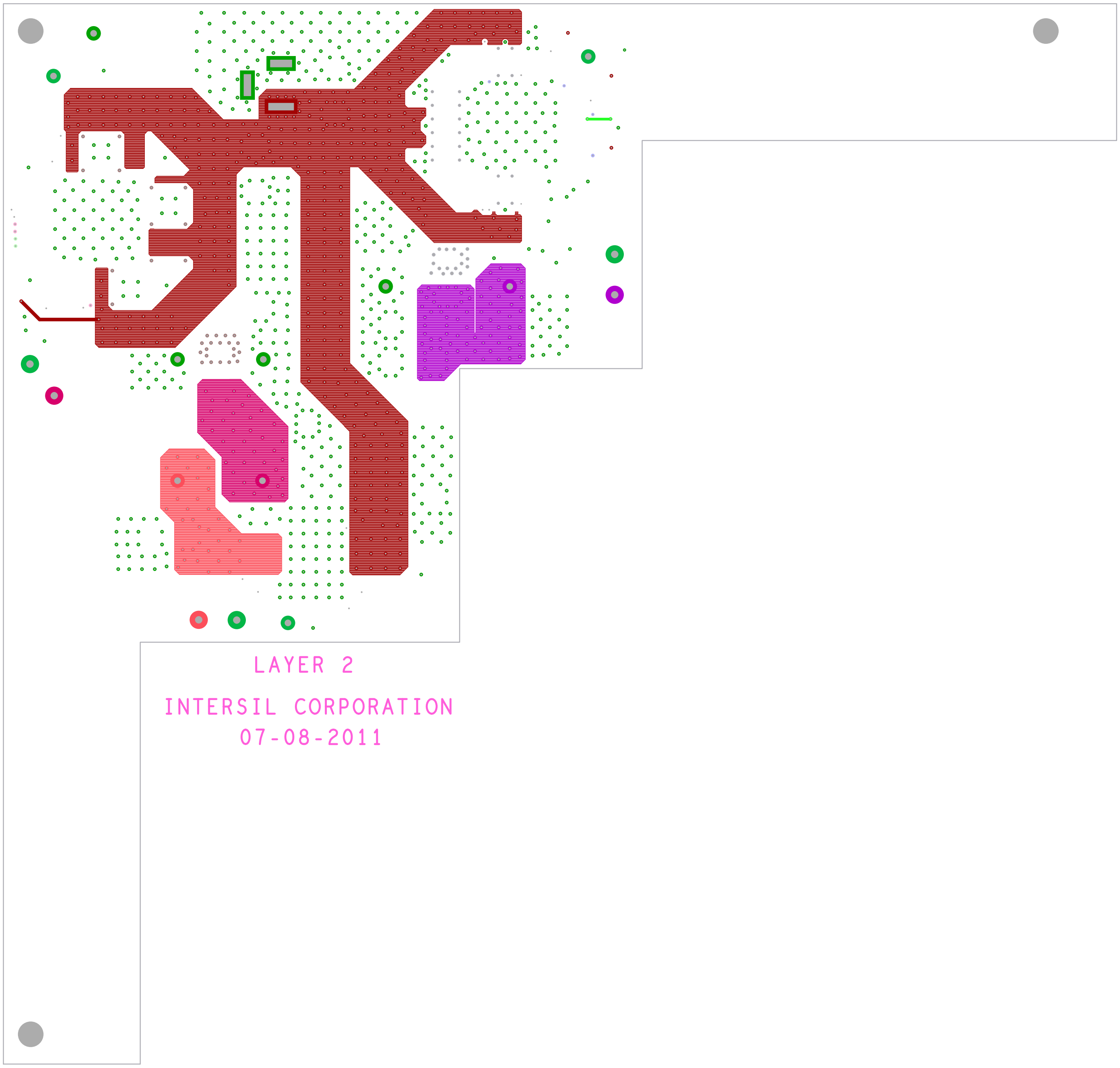


FIGURE 17. 2ND LAYER

VIRTEX5MEZPWREV1Z Board Layout (Continued)

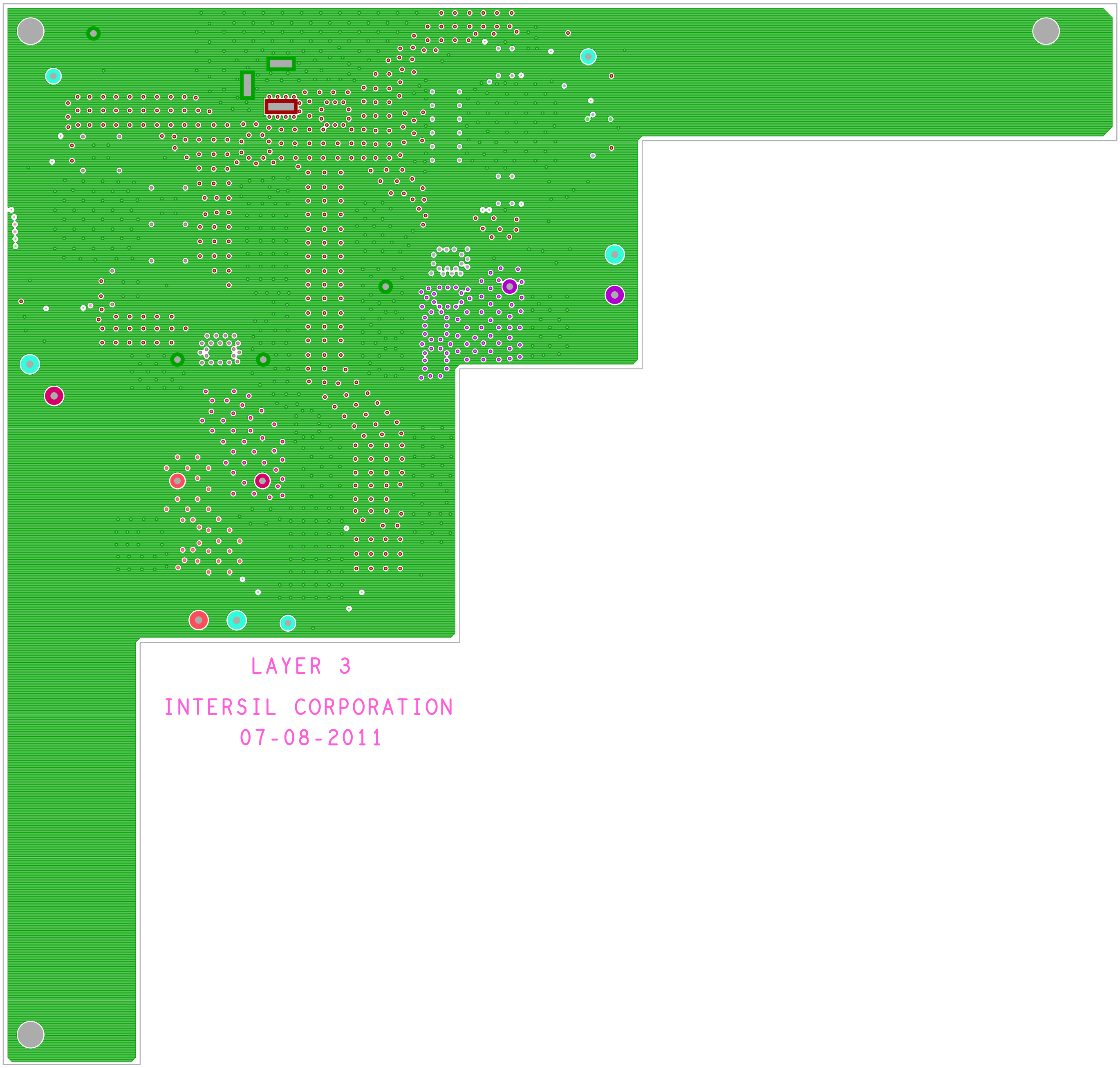


FIGURE 18. 3RD LAYER

VIRTEX5MEZPWREV1Z Board Layout (Continued)

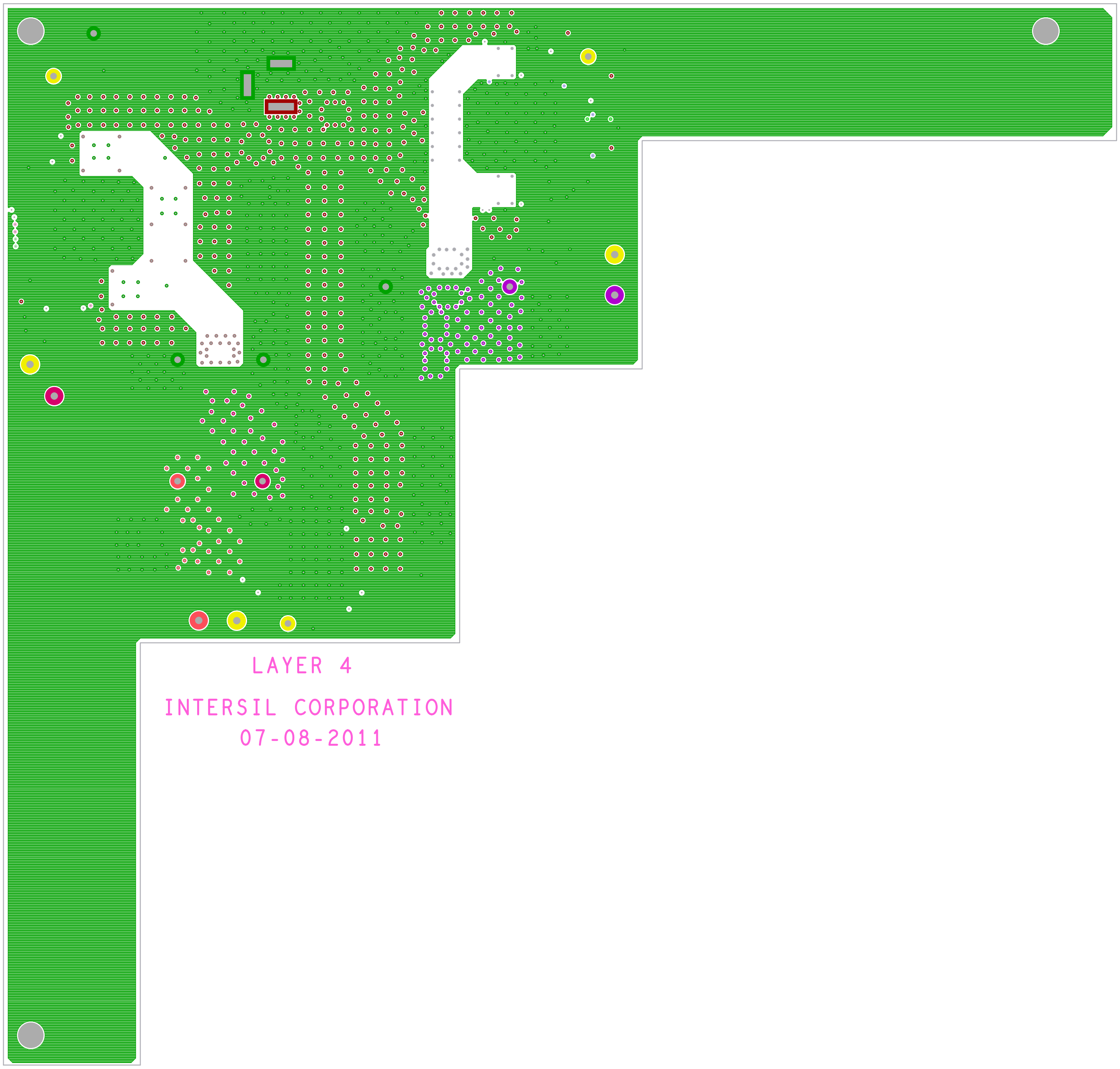


FIGURE 19. 4TH LAYER

VIRTEX5MEZPWREV1Z Board Layout (Continued)

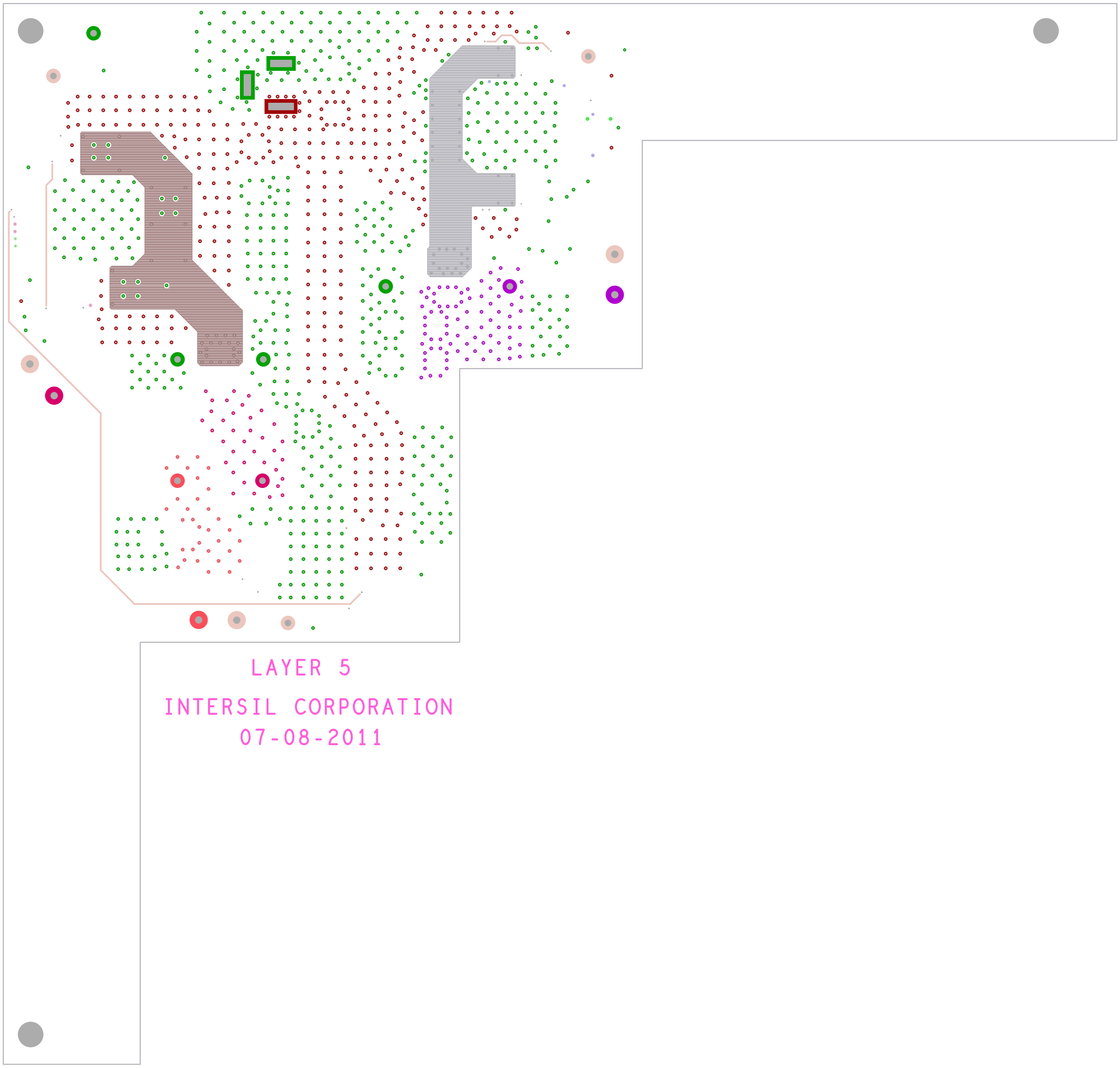


FIGURE 20. 5TH LAYER

VIRTEX5MEZPWREV1Z Board Layout (Continued)

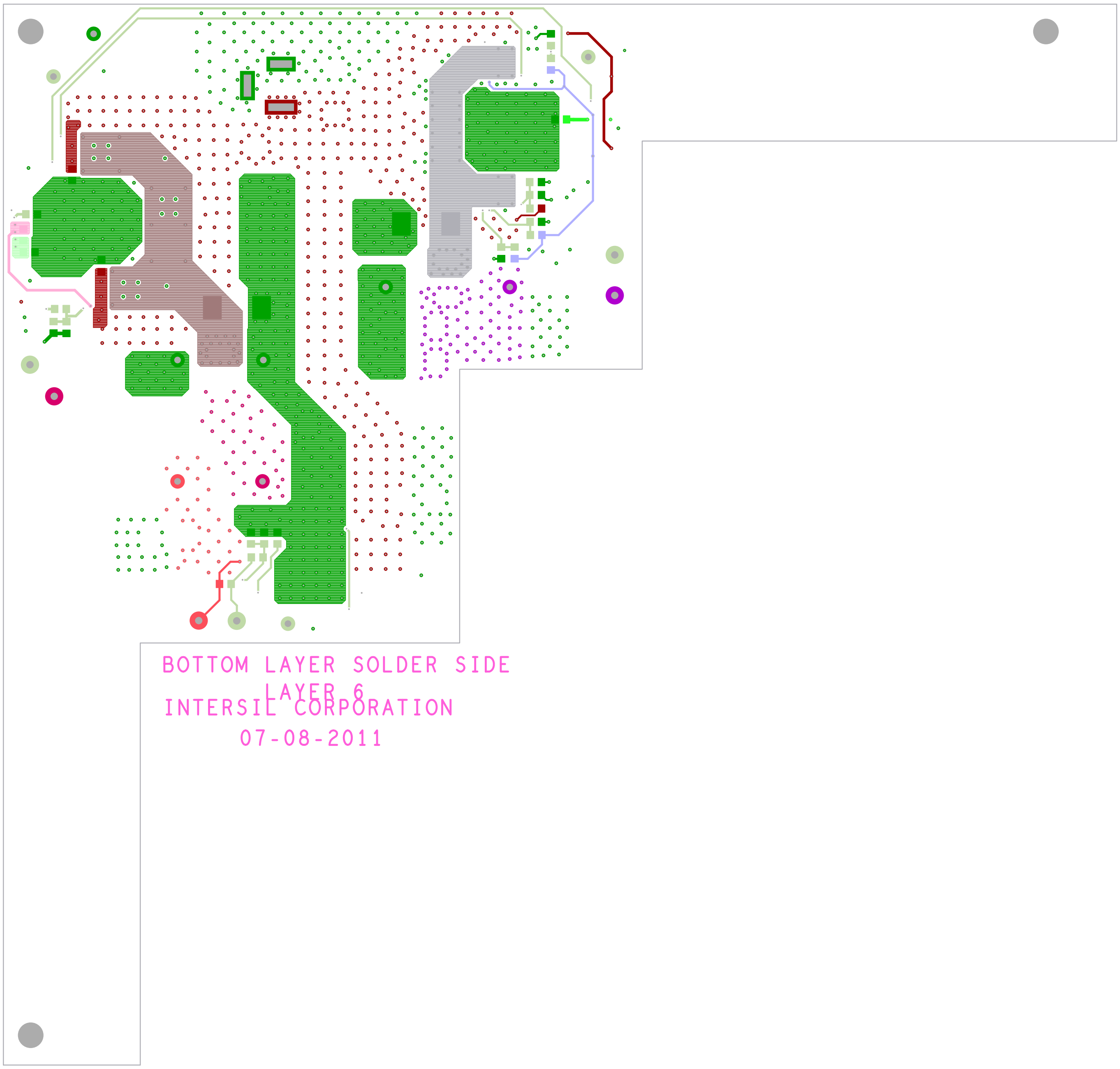


FIGURE 21. 6TH LAYER

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