Using the HSP45116 / HSP45116A as a Complex Multiplier Accumulator

TB327
Rev.1.00
July 1998

Introduction

The Intersil HSP45116/HSP45116A Numerically Controlled Oscillator/Modulator can be also used as a high speed 16-Bit Multiplier/Accumulator (CMAC). This technical briefing details the part configuration to perform such functions; it provides a functional block diagram of the interface circuit that is required, and it shows the timing diagrams of the data and control signals involved.

The features of the HSP45116/HSP45116A configured as a CMAC include:

- 25 or 33MHz Output Rate of the Complex Vector (HSP45116)
- 52MHz Output Rate of the Complex Vector (HSP45116A)
- 16-Bit Complex Inputs
- 20-Bit Complex Output
- 32-Bit Internal Accumulator
- Two's Complement or Offset Binary (Unsigned) Outputs Available
- Peak Bit Growth in the Accumulator Available through Status Pins
- The HSP45116A additionally provides higher speed operation at 52MHz, and is available in a 160 Ld MQFP.

The HSP45116/HSP45116A combines a high performance quadrature numerically controlled oscillator and a high speed 16-bit complex multiplier/accumulator.

To utilize the HSP45116/HSP45116A as a CMAC only, a number of input pins have to be set at the logic levels as specified on the attached Pin Settings for Complex Multiplier Operation Table. These pin assignments are necessary in order to bypass the operations of the Numerically Controlled Oscillator (NCO) and advance the data directly to the CMAC portion of the device. In order to accomplish proper data alignment within the part, some external interface circuitry is required as illustrated on the functional block diagram of Figure 1.

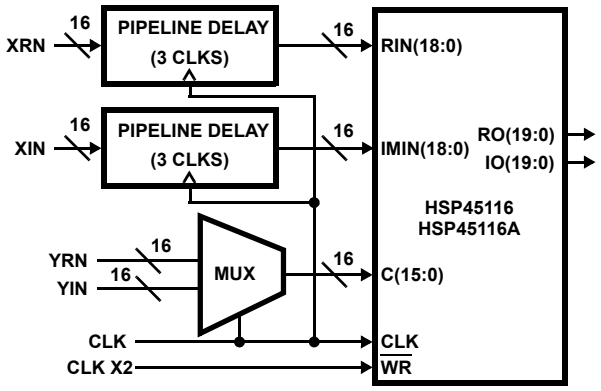
Each complex input includes a real and an imaginary component. Notice that while the first complex input vector is being clocked in the HSP45116/HSP45116A through the parallel input ports RIN(18:0) and IMIN(18:0), the second complex input vector is being clocked from a single 16-bit input port (C(15:0)), by clocking one complex component at the time. This implies that the clock of the second complex vector ($\overline{WR}$) must be twice the frequency of the clock for the first complex vector (CLK).

The exact timing relationships between inputs, outputs, control signals, and clocks are shown on Figure 2. Given the timing diagram of Figure 2 and the external interface circuit as shown on Figure 1, then full data alignment can be accomplished.

Figure 3 shows an internal block diagram of the device. The block diagram illustrates the additional data path of the second complex vector being input through the C(15:0) port follows before it lines up with the first complex vector internal to the device. In addition, this second input vector C(15:0) must be transferred to the CMAC without being altered by any of the NCO HSP45116/HSP45116A functions.

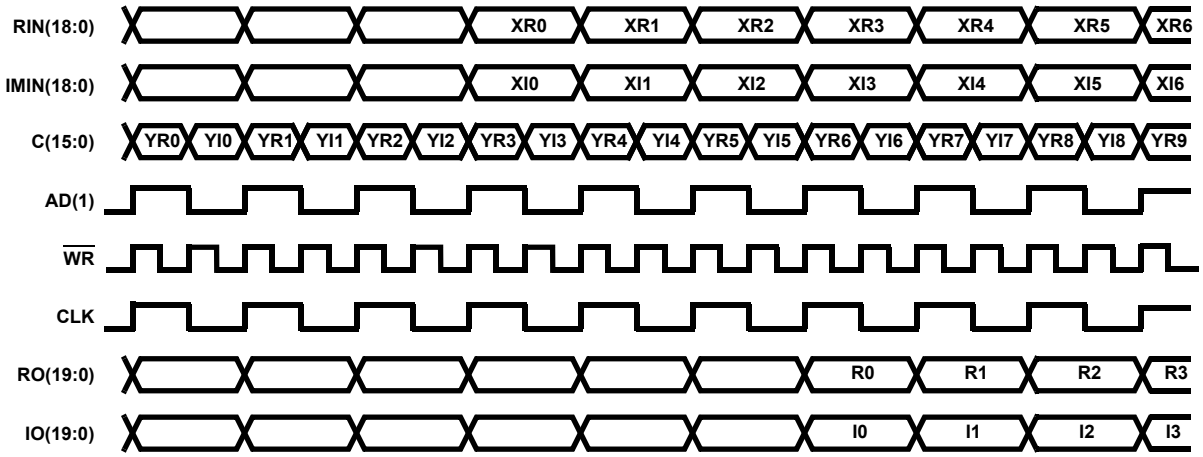
The highlighted signal path of the second complex vector C(15:0), shows the three additional registers that the data is being clocked through compared with the direct path (to the CMAC) of the first complex vector of the RIN(18:0) and IMIN(18:0) inputs. This three register delay derives the requirement for the external pipeline delays as shown on Figure 1 for the data alignment of the two complex vectors. In addition, the suggested pin configuration, on the attached pin configuration table, allows the C(15:0) data to flow unaltered by any NCO operation to the inputs of the CMAC. By following this internal data path, one can verify that the suggested logic levels assure the transparent transfer of data to the CMAC portion of the HSP45116/HSP45116A.

Note that the maximum data size of the second complex input vector is 16 bits, for each of the real and imaginary components, while the data size of the first complex input through RIN(18:0) and IMIN(18:0) can accommodate a longer length.



NOTE: Refer to Figure 2 for timing relationship between input signals, control signals and clocks.

FIGURE 1. INTERFACE BLOCK DIAGRAM UTILIZING THE HSP45116/HSP45116A AS A CMAC



NOTES:

1. Timing assumes no accumulations of the complex product. Accumulations can be accomplished by controlling the ACC input (refer to DSP Data Book).
2. XR(n)=This represents the real data of the first input vector.
3. XI(n)=This represents the imaginary data of the first input vector.
4. YR(n)=This represents the real data of the second input vector.
5. YI(n)=This represents the imaginary data of the second input vector.

FIGURE 2. TIMING DIAGRAM OF THE HSP45116/HSP45116A USED AS A CMAC

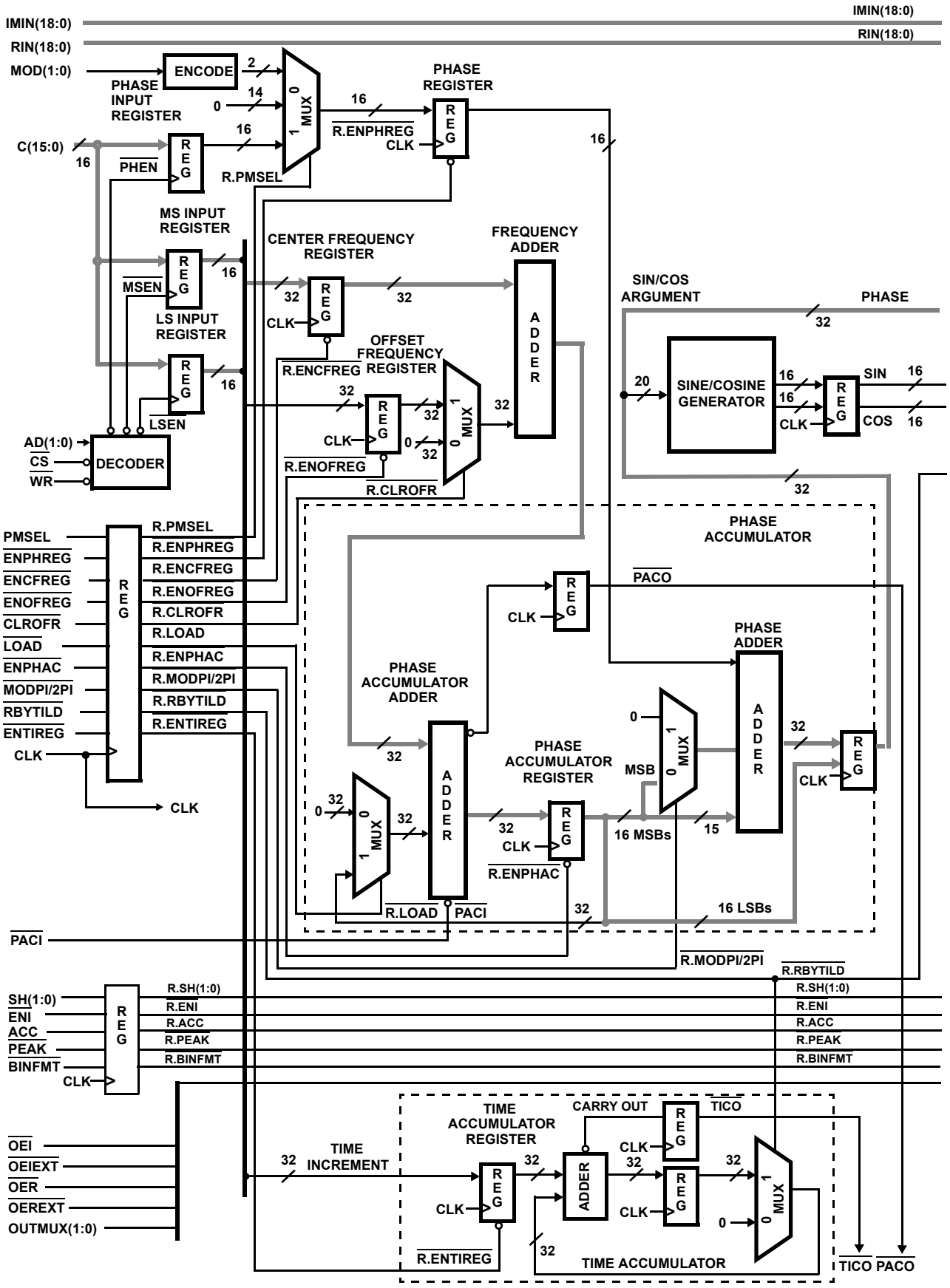


FIGURE 3. BLOCK DIAGRAM OF THE HSP45116/HSP4511A SHOWING SIGNAL PATHS WHEN USED AS A CMAC

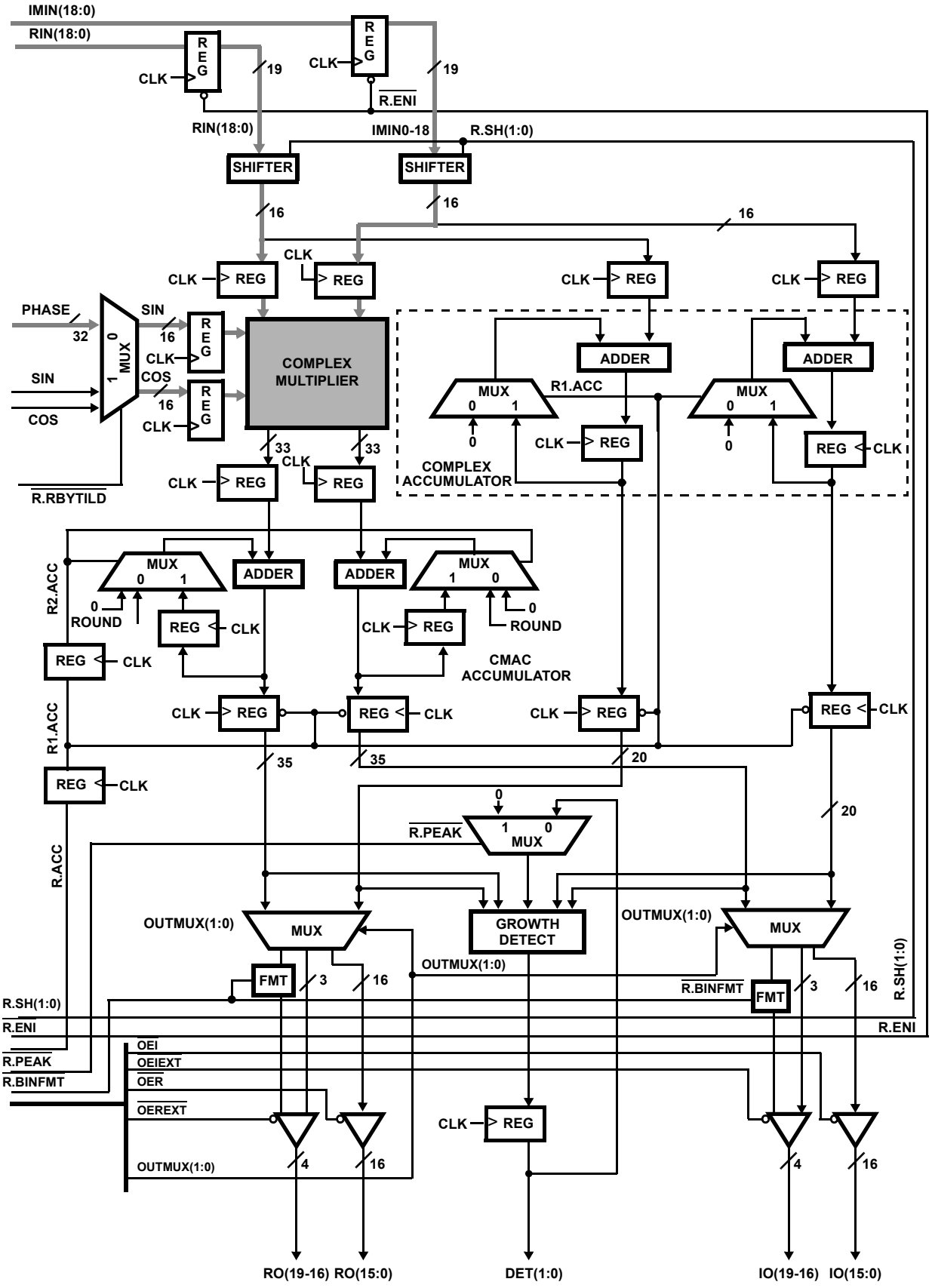


FIGURE 3. BLOCK DIAGRAM OF THE HSP45116/HSP4511A SHOWING SIGNAL PATHS WHEN USED AS A CMAC (Continued)

Pin Settings for Complex Multiplier Operation

NAME	PIN NUMBER (HSP45116)	PIN NUMBER (HSP45116A)	TYPE	DESCRIPTION
V_{CC}	A1, A9, A15, G1, J15, Q1, Q7, Q15	22, 34, 50, 87, 95, 102, 111, 124, 132, 145, 159	I	V_{CC}
GND	A8, A14, B1, H1, H15, P15, Q2, Q8	7, 20, 32, 48, 62, 73, 83, 92, 98, 108, 114, 119, 125, 131, 143, 157	I	GND
C(15:0)	N8-11, P8-13, Q9-14	54-61, 63-70	I	Input for real and imaginary for one of the complex vectors.
AD(1:0)	N7, P7	51, 52	I	Selects to write alternatively (R) or (I) data from C(15:0).
$\overline{CS}$	P6	47	I	Chip Select.
$\overline{WR}$	Q6	53	I	Writes C(15:0) data, must be twice the clock frequency.
CLK	Q5	49	I	Clock.
$\overline{ENPHREG}$	M1	27	I	Logic “0”.
$\overline{ENOFREG}$	N1	28	I	Logic “1”.
$\overline{ENCRFEG}$	N5	42	I	Logic “0”.
$\overline{ENPHAC}$	Q3	43	I	Logic “0”.
$\overline{ENTIREG}$	P5	44	I	Logic “0”.
$\overline{ENI}$	Q4	45	I	Logic “0”.
$\overline{MODPI}/\overline{2PI}$	N6	46	I	Logic “0”.
$\overline{CLROFR}$	P4	41	I	Logic “0”.
$\overline{LOAD}$	N4	38	I	Logic “0”.
MOD(1:0)	M3, N3	35, 36	I	Both pins at Logic “0”.
PMSEL	P3	39	I	Logic “0”.
$\overline{RBYTILD}$	L3	30	I	Logic “0”.
$\overline{PACI}$	P2	37	I	Logic “1”.
PACO3	L13	79	O	
TICO3	P1	33	O	
RIN(18:0)	C1, C2, D1, D2, E1-3, F1-3, G2, G3, H2, H3, J1-3, K1, K2	2-19, 21, 23	I	Input for real data for one of the input vectors with the imaginary data at IMIN(18:0).
IMIN(18:0)	A2-7, B2-7, C3-8, D3	1, 138-142, 144, 146-156, 158	I	Input for imaginary data for one of the input vectors with the real data at RIN(18.0)
SH(1:0)	K3, L1	24, 25	I	Shift Control Inputs. These lines control the input shifters of the RIN and IIN inputs of the complex multiplier. The shift controls are common to the shifters on both of the busses.
ACC	L2	26	I	Accumulate/Dump Control. This input controls the complex accumulators and their holding registers. When high, the accumulators accumulate and the holding registers are disabled. When low, the feedback in the accumulators is zeroed to cause the accumulators to load. The holding registers are enabled to clock in the results of the accumulation. This input is registered by CLK.
$\overline{BINFMT}$	N2	31	I	This input is used to convert the two’s complement output to offset binary (unsigned) for applications using D/A converters. When low, bits RO19 and IO19 are inverted from the internal two’s complement representation. This input is registered by CLK.

Pin Settings for Complex Multiplier Operation (Continued)

NAME	PIN NUMBER (HSP45116)	PIN NUMBER (HSP45116A)	TYPE	DESCRIPTION
$\overline{\text{PEAK}}$	M2	29	I	This input enables the peak detect feature of the block floating point detector. When high, the maximum bit growth in the output holding registers is encoded and output on the DET(1:0) pins. When the $\overline{\text{PEAK}}$ input is asserted, the block floating point detector output will track the maximum growth in the holding registers, including the data in the holding registers at the time that $\overline{\text{PEAK}}$ is activated.
OUTMUX(1:0)	N12, N13	71, 72	I	Logic “0”.
RO(19:0)	C15, D14, D15, E14, E15, F13-15, G13-15, H13, H14, J13, J14, K13-15, L15, M15	84-86, 88-91, 93-94, 96-97, 99-101, 103-107, 109	O	These three state outputs are controlled by $\overline{\text{OER}}$ and $\overline{\text{OEREXT}}$. OUTMUX(1:0) select the data output on the bus.
IO(19:0)	A10-13, B8-15, C9-14, D13, E13	110, 112-113, 115-118, 121-123, 126-130, 133-137	O	Imaginary output data bus. These three-state outputs are controlled by $\overline{\text{OEI}}$ and $\overline{\text{OEIEXT}}$. OUTMUX(1:0) select the data output on the bus.
DET(1:0)	N15, L14	81, 82	O	These output pins indicate the number of bits of growth in the accumulators. While $\overline{\text{PEAK}}$ is low, these pins indicate the peak growth. The detector examines bits 15-18, real and imaginary accumulator holding registers and bits 30-33 of the real and imaginary CMAC holding registers. The bits indicate the largest growth of the four registers.
$\overline{\text{OER}}$	P14	74	I	Three-state control for bits RO(15:0). Outputs are enabled when the line is low.
$\overline{\text{OEREXT}}$	M13	76	I	Three-state control for bits RO(19:16). Outputs are enabled when the line is low.
$\overline{\text{OEI}}$	M14	79	I	Three-state control for bits IO(15:0). Outputs are enabled when the line is low.
$\overline{\text{OEIEXT}}$	N14	77	I	Three-State control for bits IO(19:16). Outputs are enabled when the line is low.
$\overline{\text{RND}}$	N/A	75	I	Round enable (available on HSP45116A only). This input enables rounding of the output data precision from 9 to 20 bits (see HSP45116A Description and Operation). This input is active “low”. This input must be tied either high or low.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

RENESAS

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 7.0