Converting a Fixed PWM to an Adjustable PWM

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Description

This application note goes through the thought processes of how to convert a fixed PWM single output into a 0.7V to 1.3V adjustable output regulator. Even though the EL7554 is used as an example, this application note is applicable to any PWM using a similar voltage feedback control.

Key feature of the PWM that allows us to design such a circuit is the feed-back loop technique. The results of the voltage feed-back will cause the PWM to drive the output voltage in an attempt to maintain 0.8V at its feedback pin (FB). The typical feedback network is a simple resistive voltage divider to ground. Thus, the feedback voltage has a linear relationship to the output voltage. That is, the voltage at the FB pin will be 0.8V when the output voltage is at the desired voltage level and the PWM will adjust the output up or down linearly, to maintain 0.8V on the FB pin.

I have selected the EL7554 integrated FET PWM as a good example to use in designing such a circuit.

Data sheet can be downloaded at:
http://www.intersil.com/data/fn/fn7360.pdf

Main Concept

You can adjust the divider to supply 0.8V at the feed-back pin for a different V_{OUT}. To convert the output to an adjustable PWM would be a simple implementation of a trim pot. This technique works well as long as the V_{OUT} is above 0.8V. Thus, for the upper limit of this design, 1.3V for V_{OUT} is simple; just divide 1.3V down to 0.8V for the FB pin.

Yet, how can we use a simple divider to ground for the lower output limit of 0.7V? Obviously you cannot, as the output is already below the desired 0.8V feedback level. Thus, we have two cases to address. Let's start with the more difficult case of programming the EL7554 for a 0.7V V_{OUT}. Then, we will address the simpler implementation of the 1.3V upper limit.

Overcoming a Limitation with V_{OUT} = 0.7V

Since you cannot divide down 0.7V output to reach the 0.8V FB pin requirement, then you must consider dividing up the 0.7V to reach the 0.8V. You will need to find a voltage greater than 0.8V to use in the divider network. V_{CC} input of the EL7554 is 3.3V. Thus, connecting the end of the resistor divider string to V_{CC}, you can reach 0.8V when the output is at 0.7V. See Figure 1. For a concept of the circuitry see Figure 1.

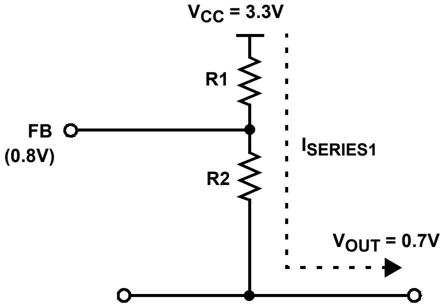

FIGURE 1.

You need to consider the noise and variations with V_{CC} to reduce this impact on the feedback sense circuit. A simple solution to reduce variations in V_{CC} is having a local large bypass cap at the V_{CC} pin. Using a 0.1µF or 0.01µF cap in parallel with the large V_{CC} decoupling capacitor (4.7µF) will help to reduce any high frequency noise and buffer V_{CC} variations. Ceramic capacitors are preferred for their low ESR and thus, higher current supply.

Designing the Circuit for Just V_{OUT} = 0.7V

How much current is too much or too little for a stable divider voltage at the FB pin? Reducing the current requirement on the local bypass cap will improve the local V_{CC} stability. The trade off is between divider current, $I_{SERIES1}$, vs the FB pin input current, I_{FB} vs noise induced by large resistor values.

Determining the Initial V_{FB} Series Divider Values

A simple rule of thumb will help determine a reasonable voltage divider current for the feedback voltage. You will need to reduce the effects of the FB pin current variations from impacting the $I_{SERIES1}$ and thus, helping to stabilize the voltage at the FB pin. The rule of thumb is to have the $I_{SERIES1}$ 10 to 100 times that of I_{FB} current. I_{FB} is spec'd at 100nA typical and 200nA max. So, using the rule of thumb 2µA might be a good selection for $I_{SERIES1}$. Yet, dropping 3.3V to 0.8V with a 2µA series current would result in a resistor value of 1.24MΩ resistor. Any small variations in the $I_{SERIES1}$ or environmental noise could induce variations in the FB voltage. Sharp edge digital signals or switching transients can induce a reasonably large voltage across this high impedance. A 1MΩ resistor could also induce noise in the feedback loop so values in this range should be avoided.

Thus, you need to have the $I_{SERIES1}$ large enough to keep the values of R1 and R2 (see Figure 1) small enough to limit the induce noise and improve stability of V_{FB}. You do not want the series current so great that it will load down V_{CC}. Remember, using a large by pass cap connected to the top of R1 will act as a supply stabilizer and you do not want too much current to be drawn by the divider from the by pass cap to induce large variations on the V_{FB} pin.

After all is said and done, looking at the current specification for the V_{FB} pin, I selected $I_{SERIES1}$ = 100µA for the divider series current as a good trade off. Thus, R2 is the 0.8V minus the output voltage, divided by the $I_{SERIES1}$ and for an output of 0.7V, R2 will be:

R2 = $(V_{FB}-V_{OUT})/I_{SERIES1}$ or (0.8V-0.7V)/100µA = 0.1V/100µA = 1kΩ

R1 is simpler:

R1 = $(V_{CC}-V_{FB})$/100µA or (3.3V-0.8V)/100µA = 2.5V/100µA = 25kΩ

Designing the Circuit for Just V_{OUT} = 1.3V

Since V_{OUT} is greater than V_{FB}, this is simply a voltage divider at the output to ground. Again keeping the current, $I_{SERIES2}$ (see Figure 2), in the voltage divider such that it does not load the output. The max output current is 4A and using the 10:1 rule of thumb, you can use anything under 400mA. An additional constraint is to keep the heat dissipation of the resistors low and thus, the size and cost of the resistors small.

The calculations for the series resistors would be the same as before but at what series current? Keeping in mind the final solution will need to support the full range down to 0.7. Again, back to the rule of thumb, you should keep the current 10x that of the 0.7V $I_{SERIES2}$ or 1mA. This will reduce the influence of the 0.7V $I_{SERIES1}$ on the final bias point of the series resistors. There will be more on this later when discussing the complete solution for the adjustable EL7554 V_{OUT} 0.7V to 1.3V.

Applying the rule of thumb, $I_{SERIES1}$ = 100µA in the 0.7V bias network, thus $I_{SERIES2}$ would be 1mA in the 1.3V bias network. The computation would be:

R3 = (1.3V-0.8V)/1mA or 0.5/1mA or 500Ω

R4 = (0.8V)/1mA or 800Ω

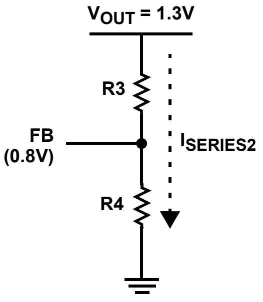

FIGURE 2.

Computing the Final Design

Up to now we have not considered the total solution, just the 1.3V and 0.7V limits separately. Using this approach, we have two basic circuits but now we need to refine the solution to encompass the total system requirements.

Lets discuss the basic architecture, then we can refine the above two designs into one single design that would meet the full span, V_{OUT} = 0.7V to 1.3V.

Key Point

The output range is a voltage above and below V_{FB} of 0.8V. Yet, the EL7554 will control the internal FETs to maintain the 0.8V on FB pin. So, our final design must support V_{OUT} above and below 0.8V on the FB pin.

Let's Start with the Main Problem, V_{OUT} = 0.7V

What if you tied the bottom of R2, not to V_{OUT}, but to some lesser voltage than V_{OUT}, such that when V_{OUT} desired is 1.3V, you have V_{FB} = 0.8V. You will might a solution that would cover the range of 0.7V to 1.3V.

The simple way of insuring the feedback voltage is in relationship to V_{OUT} and in the range of V_{FB} = 0.8V, is to use a simple divider to ground on the output. The junction point of the two series resistors is the reference point for the feedback circuit and still reflects the output voltage. You can adjust the ratio of this divider to control the sensitivity of the overall feedback circuit to changes in V_{OUT}. For the sake of simplicity, I will keep it a simple divide by 2 and worry about the sensitivity issue later. The resulting conceptual circuit would be (see Figure 3).

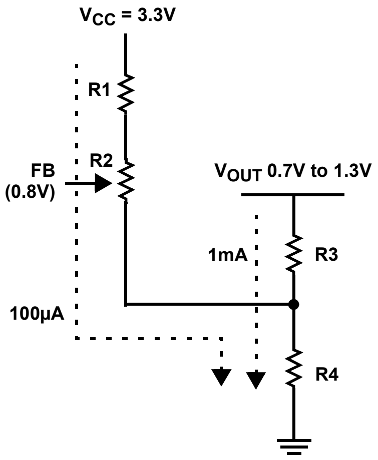

FIGURE 3.

A First Approximation

We just need to get into the ballpark for the resistor values at this point in the design. The approach is to select the mid operating range and then evaluate the calculations of the resistors for the full range. Then, we will consider the minimum and maximum range to select the proper potentiometer to insure the adjustable range meets the requirements.

If you consider the V_{OUT} range, 0.7V to 1.3V, the mid range would be 1V. Thus we start with as a first approximation:

V_{OUT} = 1V

Determining the Value for R3 and R4

Back to set the series current for this divider. Remember the 0.7V feedback circuit current was set at 100µA. Well, here again we invoke the rule of thumb. You need to isolate the feedback current from influencing the divider node voltage.

Thus, using the 10:1 rule, the divider series current would be 1mA. Since the output nominal voltage is 1V and the series current is 1mA, then the resistor array would be:

$R3 + R4 = V_{OUT}$ norm/I series or 1V/1mA or 1kΩ.

To keep it simple we selected to have the divider a simple 2:1 thus, the node would be 500mV, then R3 = R4 = 500Ω. Thus, the feedback reference node is set to:

$V_{NODE} = 0.5V$

Final Computations

We need to compute R1 and R2 and then use the upper and lower V_{OUT} limits to determine the range of the potentiometer we need to use in-place of R2.

Keeping with the output node of 1V, the R3-R4 node voltage would be 0.5V and the feedback current of 100µA. You can now compute R1+R2.

$R1+R2=(V_{CC}- V_{NODE})/100µA$, (3.3V-0.5V)/100µA=2.8V/100µA=28kΩ

We need to consider one operational restriction, the V_{NODE} must be lower than 0.8V when the output is at 1.3V. If we use a simple approach, divide by 2 series resistor array, V_{NODE} will be at 0.65V when the output is 1.3V and V_{NODE} would be 0.35V when the output is 0.7V. Thus from R3+R4 = 1kΩ:

R3 = R4 = 500Ω

At this point we have selected the two branch currents such that the selections result in reasonable resistor values such that the three currents, I_{FB}, $I_{SERIES1}$ and $I_{SERIES2}$, do not influence the key nodes. We have computed values for R1 through R4. The next step is to compute the value of the potentiometer needed to meet the range of V_{OUT}.

Assume the V_{OUT} to ground divider design is fixed, let's calculate the range of R2 so we can select the potentiometer to meet the design programmable range of 0.7V to 1.3V. Start at the bottom of the R1, R2 series resistors. This node will be ½ the V_{OUT} or:

$V_{OUT} = 0.7V$ then $V_{NODE} = 0.35V$

$V_{OUT} = 1.3V$ then $V_{NODE} = 0.65V$

Next is to calculate the voltage drops across R2 for each case:

With $V_{OUT} = 0.7V$ then: VR2 = 0.8 - 0.35V = 0.45V

With $V_{OUT} = 1.3V$ then: VR2 = 0.8 - 0.65V = 0.15V

Using the series current $I_{SERIES1}$ = 100µA, the range for R2 will be:

$V_{OUT} = 0.7V$ then R2 = 0.45V/100µA = 4.5kΩ

$V_{OUT} = 1.3V$ then R2 = 0.15V/100µA = 1.5kΩ

Thus, a 5kΩ potentiometer would work well in this design. Yet, to remove the need for manual adjustments, I would recommend you consider using a Digitally Controlled Potentiometer (DCP). So, we need to find a DCP with 5kΩ wiper to end resistances (a two terminal DCP). Using DCP selection guide:
http://www.intersil.com/design/psg/Data_Conversion.pdf

You will find we offer 10k DCPs but no 5k DCPs. Yet, if you use a 10k DCP with enough resolution (number of taps), you can use 5k of the 10k range. Remember, the total series resistance for $I_{SERIES1}$, is 28.5k to ground. Also, don't forget the DCP has a series wiper resistance. Wiper resistance is a fixed resistance and may impact the voltage feed back at the V_{FB} pin. Yet, if we configure the DCP properly, the Wiper resistance will have minimal impact on the voltage setting at the V_{FB} pin.

Back to the search for a DCP: We need a 10k DCP that will operate at 3.3V and offer a good resolution. The resolution is a function of the end-end resistance and the number of taps (taps). The more taps the better the resolution for each tap and thus, the output voltage programming resolution. One last requirement is for a Non-Volatile DCP which will store the wiper position when power is removed and restore pre-shutdown wiper position at power-up.

Search Criteria

Supply - the same as the PWM or 3.3% ±10%.

Resolution - maximum number of tap for best resolution.

Wiper Resistance - small value, in the range of the tap resolution.

Non-Volatile - to retain programmed position during power-up.

The key search criteria's are V_{CC} and resolution/number of taps. Using the URL listed before, we come up with the ISL95810 which seems to be a good fit.

ISL95810: (URL for the data sheet:
http://www.intersil.com/data/fn/fn8090.pdf)

V_{CC} range - 2.7V-5.5V

End to End resistance - 10kΩ

Number of taps - 256 taps

Wiper resistance - 70Ω (200Ω max)

Non-volatile - Yes

The ISL95810 tap-to-tap resistance resolution is 10kΩ/256 taps or about 40Ω/tap. Since we only need 5k, the resolution of the DCP setting is 40/5,000 or less than 1%. The DCP end to end resistance is ±20%. We will need to look more closely at the overall DCP resolution in mV/tap later on. For now, the DCP has enough resolution to compensate for other inaccuracies in the circuit.

Here I would like to address the wiper resistance. The typical wiper resistance of ISL95810 is 70Ω with maximum of 200Ω. If we design the circuit such that the wiper resistance only carries the V_{FB} current (200nA max) then the worst case voltage drop would be:

V_{WIPER} = 200Ω * 200nA or 40µV

Thus, the wiper resistance will have little, if any, impact on the V_{FB} pin voltage setting (40µV on 800mV is only 0.005%). To remove R_{WIPER} from impacting V_{FB}, the Wiper cannot carry any of the I_{SENSE1} current. So, just treat the DCP as a three terminal POT as shown in Figure 4.

Since the total resistance in this leg is 28kΩ, we would only have to change R1 to 18kΩ and the DCP would make up the other 10kΩ. (See Figure 4 for the complete circuit).

The total resistance seen by $I_{SERIES1}$ does not change due to the wiper setting. Thus V_{FB} is totally dependent on V_{OUT}.

The Final Circuit

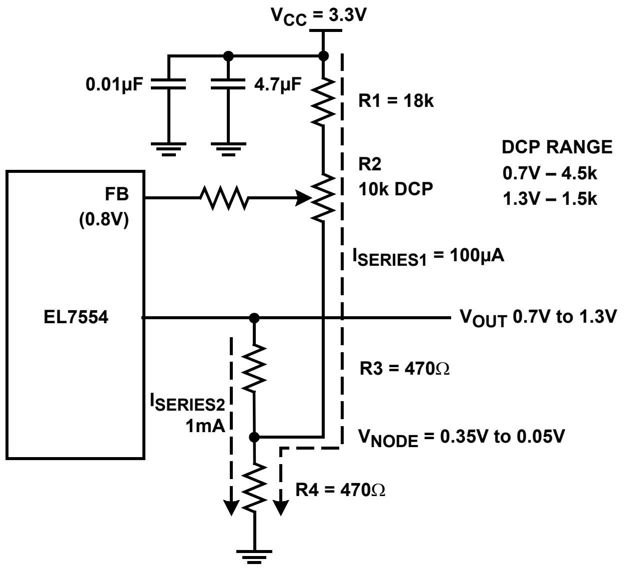

FIGURE 4.

DCP mV/Tap Resolution

We could look at resolution and accuracy as a percentage but it is more meaningful to look at the DCP in terms of mV/tap then look at the overall accuracy in percent. For sake of discussion, I will first assume all external fixed resistors are 0.1%. Therefore, the overwhelming inaccuracy is due to the DCP end to end resistance. The resolution of the DCP in voltage divider mode is $I_{SERIES1}$*R2/256:

$I_{SERIES1} = V_{CC}/(R1 + R2_{NOM} + R4)$

So, the Resolution is:

$3.3V*(R2_{NOM}/(R1+R2_{NOM}+R4)*256))$ or
3.3V*(10k/(18k+10k+500)*256)) = 4.5mV per tap

The ±20% of total resistance error of the DCP only represents a ±0.6mV error of wiper voltage setting. To calculate this just substitute for R2 the upper and lower limits based on the ±20% error:

$R2 = R2_{NOM}$ +20% = 12k and $R2 = R2_{NOM}$ -20% = 8k

1) 3.3V*12k/(18k+12k+0.47k)*256 = 5.08mV ~ 5.1mV

2) 3.3V*8k/(18k+8k+0.47k)*256 = 3.89mV ~ 3.9mV

The delta is 5.1mV-3.9mV = 1.2mV thus the error is ±0.6mV.

Initial DCP Tap Setting

Computing the initial tap setting for the different output voltages is simple. First, determine the voltage drop across the DCP from the desired wiper position to the bottom of the DCP. Then divide that delta voltage by the mV/Tap.

Voltage drop: We need V_{FB} = 0.8V, and is the wiper voltage. The bottom of the DCP, as noted before, would be either:

0.35V for V_{OUT} = 0.7V

0.65V for V_{OUT} = 1.3V

Thus, the correct wiper position for 0.7V V_{OUT} should be 100 decimal:

(0.8V-0.35V)/4.5mV = 100 taps.

For 1.3V of output voltage, the correct wiper position should be 33 decimal:

(0.8V-0.65V)/4.5mV = 33 taps.

Calibration - You might consider monitoring the output and adjusting the DCP wiper position to improve the accuracy to within 4.5mV. A small look-up table can be created for easy adjustment of V_{OUT} with accuracy less than 1%.

If you cannot calibrate but do need a few discrete accurate output voltage settings, you can use a series of precision resistors and a quad CMOS switch in place of the DCP. The cost would be greater than using a DCP with calibration. Yet, you can achieve the tight accuracy without calibration use of the resistors and switch.

Summary

You can modify the standard PWM with voltage feedback to convert it to a programmable PWM using a DCP using a few external resistors. You can also design the feedback in such a way as to expand the output range below the V_{FB} program level by shifting the divider reference point above ground. Yet, you do need to consider series current variation impact on your component selections.

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