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REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPR.

F

F

HSP50415EVAL1 SCHEMATICS

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E

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C


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B

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A

A

DRAWN BY: STEVE HARRELL	DATE: 11/22/99	ENGINEER:	DATE:
RELEASED BY:	DATE:	TITLE: HSP50415EVAL1	
UPDATED BY:	DATE:		
	TESTER:	MASK#	HRDWR ID
	FILENAME:	REV. B2	
	SHEET 1 OF 4		

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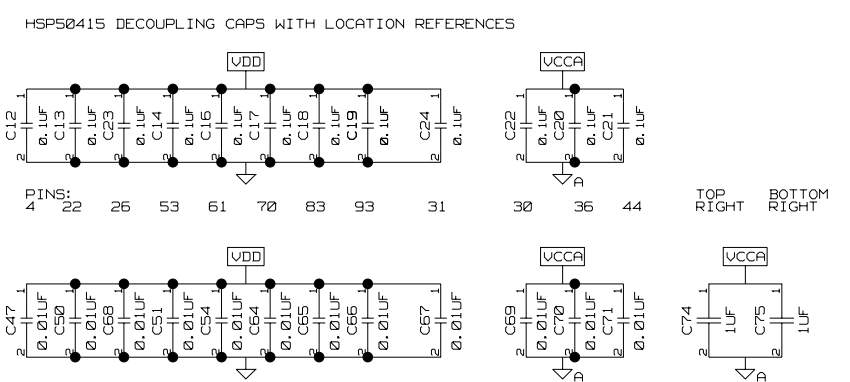
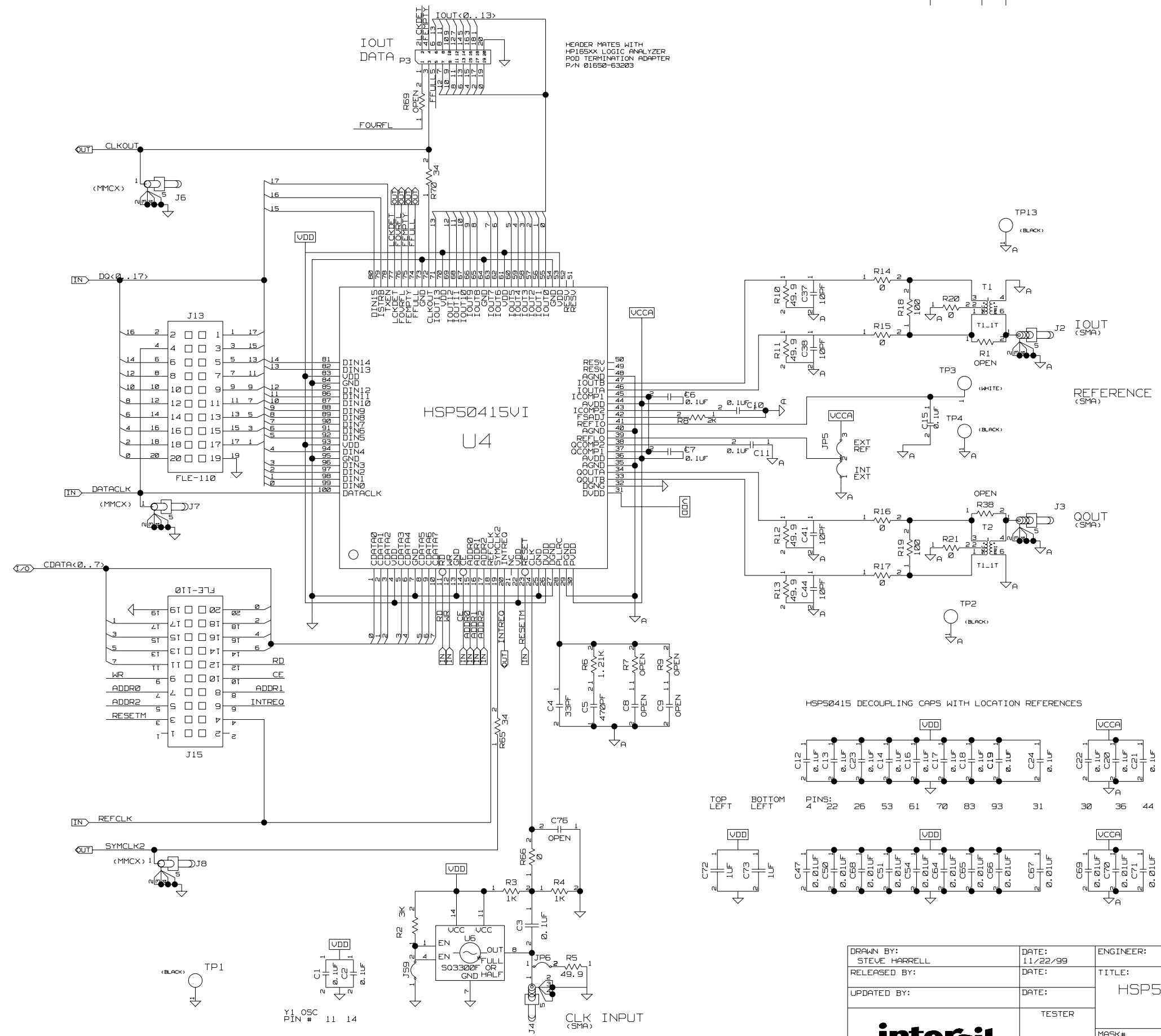
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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.



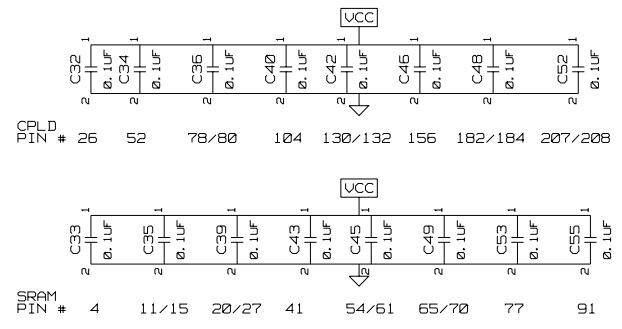
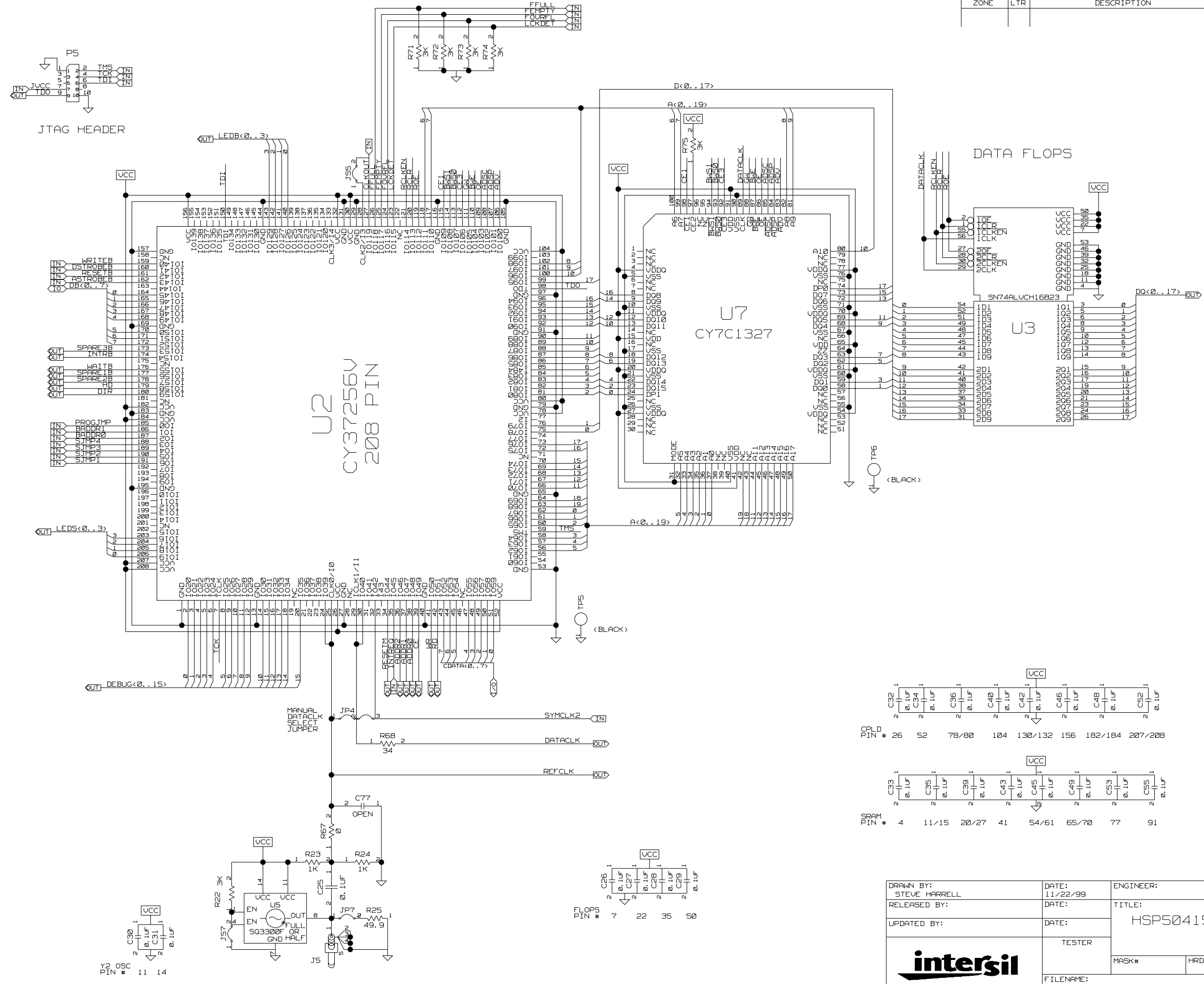
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RELEASED BY:	DATE:	TITLE: HSP50415EVAL1	
UPDATED BY:	DATE:	TESTER:	MASK#
		FILENAME:	REV. B2
		SHEET 2 OF 4	

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F E D C B A

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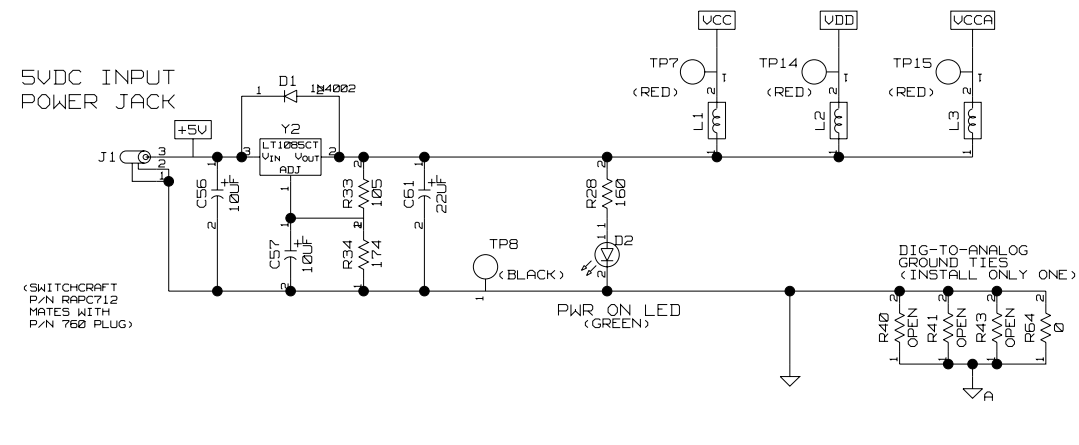
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ZONE	LTR	DESCRIPTION	DATE	APPR.



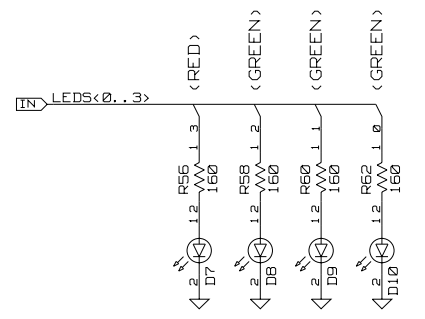
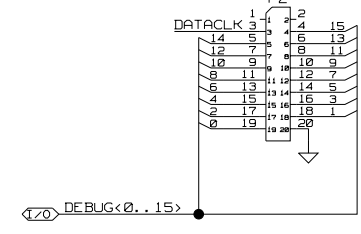
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			3 OF 4

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPR.

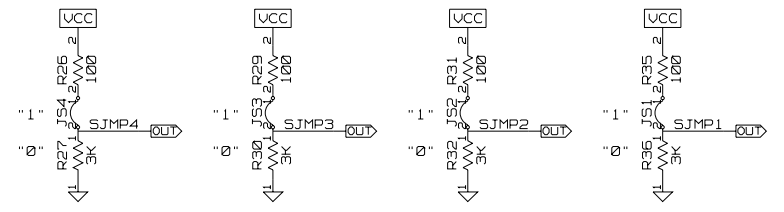
3.3VDC POWER DISTRIBUTION



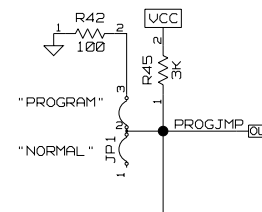
CPLD DEBUG



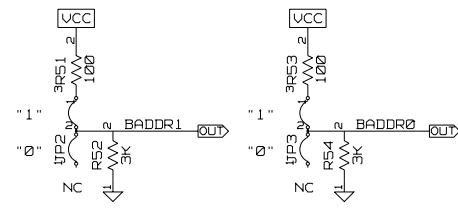
BOARD REVISION SOLDER JUMPERS



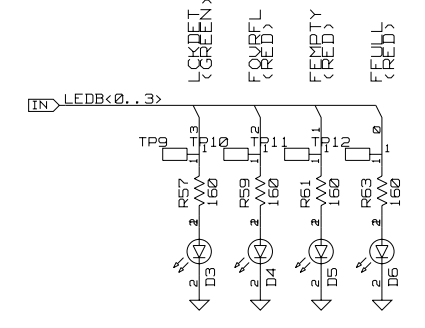
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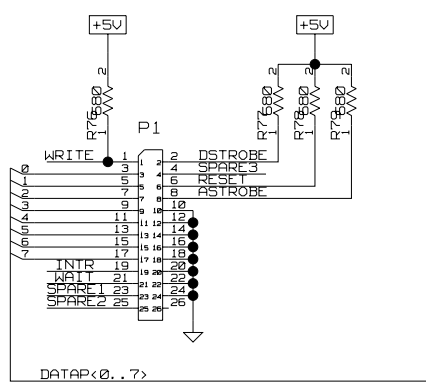
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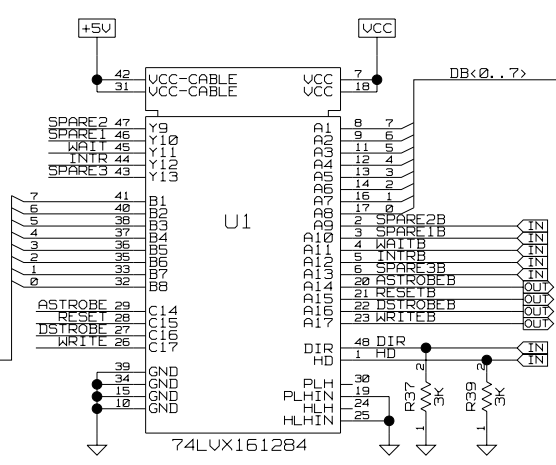
'415 STATUS LEDs



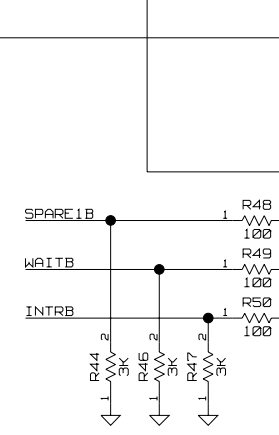
IDC26 PIN HEADER (HOST PRN INTERFACE)



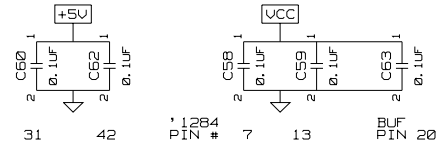
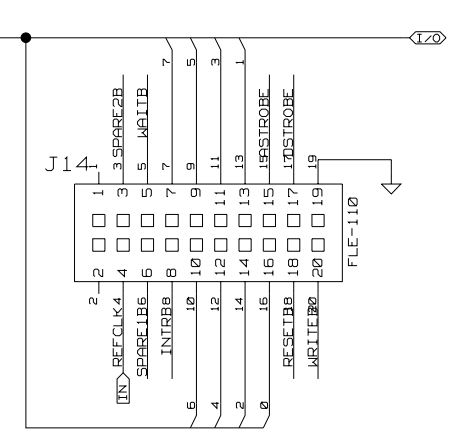
IEEE1284 TRANSCEIVER



JTAG BUFFER



HOST DEBUG



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RELEASED BY:	DATE:	TITLE: HSP5041SEVAL 1	
UPDATED BY:	DATE:	TESTER:	
		MASK#	HRDWR ID
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