Product Advisory (PA)

Subject: Changes to the Power-up / Power-down Sequencing and Recovery from Brown-out Condition
Publication Date: 2/24/2023
Effective Date: 2/24/2023

Revision Description:
Initial Release

Description of Change:
This notice is to inform you that the High-Performance Serial MRAM Memory datasheet has been updated as follows:

- Wording changes in Chapter 3 - Table 2 (Signal Description)
- Chapter 7 (Device Initialization) has been revised. The proper (and required) device initialization is now described in more detail.
- Some parameters in Chapter 7 - Table 6 and Table 7 (Power Up/Down Timing) have been updated, to reflect the new requirements for proper power-up/down sequencing.

Changes are as reflected in Appendix A of the notice.

The test program was revised to the new specification on 11/15/22. All the material shipped after 01/01/23 has been screened to the revised test program.

Affected Product List:
Please refer to Appendix B

Reason for Change:
Update power supply sequencing and DC tables to provide proper power up and power down guidelines for the MRAM family of devices. These updates address gaps in the datasheet and provide additional guidance to the customer.

Impact on Fit, Form, Function, Quality & Reliability:
There is no change to form, fit, function, quality and reliability of the device.

Product Identification: Parts shipped after 01/01/23 are screened to the new specification. For more information please contact Renesas.

Qualification Status: Not Applicable
Sample Availability Date: Not Applicable
Device Material Declaration: Available upon request

Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Renesas within 30 days of the publication date.

Appendix A - Description of Change

The highlighted texts and graphs below show the datasheet updates.

1. Chapter 3 - Signal Description and Assignment
Table 2: Signal Description

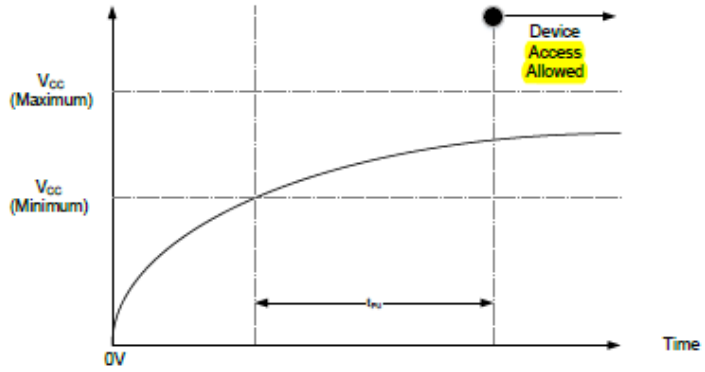
Signal	Type	Description
CS#	Input	**Chip Select:** When CS# is driven High, the device will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS# Low enables the device, placing it in the active mode. After power-up, a falling edge on CS# is required prior to the start of any instructions.
WP# / IO[2]	Input / Bidirectional	**Write Protect (SPI):** Write protects the status register in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven. WP# is valid only in Single SPI mode. This pin can be tied to Vcc if not used. **Bidirectional Data 2 (DPI/QPI):** The bidirectional I/O transfers data into and out of the device in Dual and Quad SPI modes.
CLK	Input	**Clock:** Provides the timing for the serial interface. Depending on the mode selected, either single (rising or falling) edge or both edges of the clock are utilized for information transfer. In Single Data Rate mode (SDR) command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. In Double Data Rate mode (DDR) command is latched on the rising edge of the clock. Address and Data inputs are latched on both edges of the clock. Similarly, Data is output on both edges of the clock. The following two SPI clock modes are supported. • *SPI Mode 0 (CPOL = 0, CPHA = 0) – SDR and DDR* • *SPI Mode 3 (CPOL = 1, CPHA = 1) – SDR only*
IO[3]	Bidirectional	**Bidirectional Data 3 (DPI/QPI):** The bidirectional I/O transfers data into and out of the device in Dual and Quad SPI modes. This pin can be tied to Vcc if not used.
SI / IO[0]	Input / Bidirectional	**Serial Data Input (SPI):** The unidirectional I/O transfers data into the device on the rising edge of the clock in Single SPI mode. **Bidirectional Data 0 (DPI/QPI):** The bidirectional I/O transfers data into and out of the device in Dual and Quad SPI modes.

2. Chapter 7 - Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- Ramp up V_{CC} (t_{RVR})
- CS# must follow V_{CC} during power-up (a 10KΩ pull-up Resistor to V_{CC} is recommended)
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum)
- During initial Power-up, recovering from power loss or brownout, a delay of t_{PU} is required before normal operation commences
- Upon Power-up, the device is in Standby mode

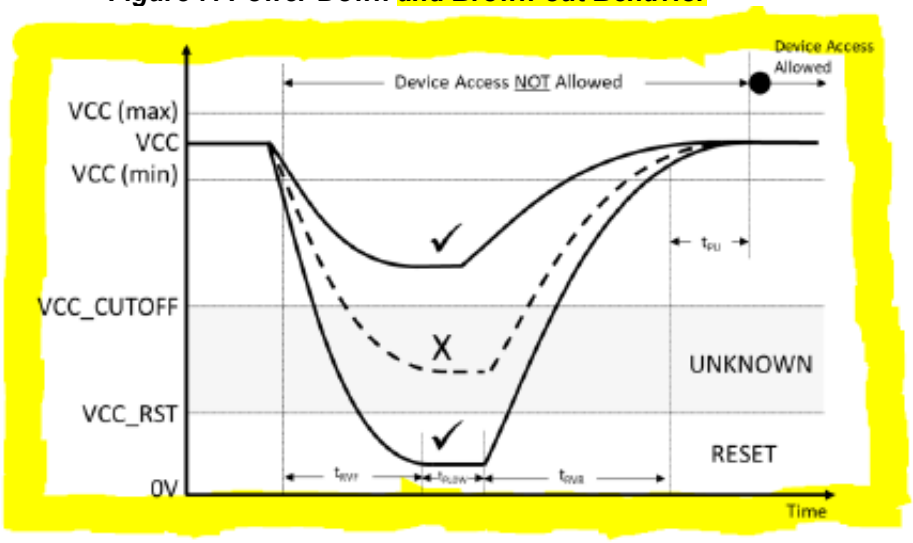
Figure 1: Power-Up Behavior



When powering down or in case of brown-out, the following procedure is required to turn off the device correctly:

- Ramp down V_{CC} below V_{CC_RST} level
- CS# must follow V_{CC} during power-down (a 10KΩ pull-up Resistor to V_{CC} is recommended)
- The device must not be selected and that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum)
- The Power-up timing and device initialization needs to be observed after V_{CC} ramps up above V_{CC} (minimum)
- To stabilize the V_{CC} level, suitable decoupling capacitors close to package V_{CC} pin is recommended
- Chip functionality not guaranteed if V_{CC} ramps down between V_{CC_CUTOFF} and V_{CC_RST} and then ramps up to V_{CC}

Figure 7: Power-Down and Brown-out Behavior



3. Chapter 7
Table 6: Power Up/Down Timing - 3.0V

Parameter	Symbol	Test Conditions	3.0V			
			Minimum	Typical	Maximum	Units
V_{CC} Range	V_{CC}	All operating voltages and temperatures	2.7	-	3.6	V
V_{CC} Ramp Up Time to V_{CC} (min)	t_{RVR}		30	-	1500	µs
V_{CC} Ramp Down Time to V_{CC_RST}	t_{RVF}		20	-	-	µs
V_{CC} Power Up to First Instruction	t_{PU}		250	-	-	µs
V_{CC} Cutoff – Must Initialize Device	V_{CC_CUTOFF}		1.6	-	-	V
V_{CC} Reset	V_{CC_RST}		0	-	0.3	V
V_{CC} Power Down Low Time	t_{PLOW}		1000	-	-	µs
Time to Enter Deep Power Down	t_{EDPD}		-	-	3	µs
Time to Exit Deep Power Down	t_{EXDPD}		-	-	400	µs
Time to Enter Hibernate	t_{ENTHIB}		-	-	3	µs
Time to Exit Hibernate	t_{EXHIB}		-	-	450	µs
CS# Pulse Width	t_{CSDPD}		50	-	-	ns

4. Chapter 7
Table 7: Power Up/Down Timing - 1.8V

Parameter	Symbol	Test Conditions	1.8V			
			Minimum	Typical	Maximum	Units
V_{CC} Range	V_{CC}	All operating voltages and temperatures	1.71	-	2.0	V
V_{CC} Ramp Up Time to V_{CC} (min)	t_{RVR}		30	-	1000	µs
V_{CC} Ramp Down Time to V_{CC_RST}	t_{RVF}		20	-	-	µs
V_{CC} Power Up to First Instruction	t_{PU}		250	-	-	µs
V_{CC} Cutoff – Must Initialize Device	V_{CC_CUTOFF}		1.6	-	-	V
V_{CC} Reset	V_{CC_RST}		0	-	0.2	V
V_{CC} Power Down Low Time	t_{PLOW}		1000	-	-	µs
Time to Enter Deep Power Down	t_{EDPD}		-	-	3	µs
Time to Exit Deep Power Down	t_{EXDPD}		-	-	400	µs
Time to Enter Hibernate	t_{ENTHIB}		-	-	3	µs
Time to Exit Hibernate	t_{EXHIB}		-	-	450	µs
CS# Pulse Width	t_{CSDPD}		50	-	-	ns

Appendix B – Affected Product List

Part Numbers		
M10042040108X0IWAR	M10162040108X0IWAR	M10082040054X0IWAR
M10042040108X0IWAY	M10162040108X0IWAY	M10082040054X0IWAY
M10042040108X0ISAR	M10162040108X0ISAR	M10082040054X0ISAR
M10042040108X0ISAY	M10162040108X0ISAY	M10082040054X0ISAY
M10042040108X0PWAR	M10162040108X0PWAR	M10082040054X0PWAR
M10042040108X0PWAY	M10162040108X0PWAY	M10082040054X0PWAY
M10042040108X0PSAR	M10162040108X0PSAR	M10082040054X0PSAR
M10042040108X0PSAY	M10162040108X0PSAY	M10082040054X0PSAY
M30042040108X0IWAR	M30162040108X0IWAR	M30082040054X0IWAR
M30042040108X0IWAY	M30162040108X0IWAY	M30082040054X0IWAY
M30042040108X0ISAR	M30162040108X0ISAR	M30082040054X0ISAR
M30042040108X0ISAY	M30162040108X0ISAY	M30082040054X0ISAY
M30042040108X0PWAR	M30162040108X0PWAR	M30082040054X0PWAR
M30042040108X0PWAY	M30162040108X0PWAY	M30082040054X0PWAY
M30042040108X0PSAR	M30162040108X0PSAR	M30082040054X0PSAR
M30042040108X0PSAY	M30162040108X0PSAY	M30082040054X0PSAY
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M10082040108X0IWAY	M10042040054X0IWAY	M10162040054X0IWAY
M10082040108X0ISAR	M10042040054X0ISAR	M10162040054X0ISAR
M10082040108X0ISAY	M10042040054X0ISAY	M10162040054X0ISAY
M10082040108X0PWAR	M10042040054X0PWAR	M10162040054X0PWAR
M10082040108X0PWAY	M10042040054X0PWAY	M10162040054X0PWAY
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M10082040108X0PSAY	M10042040054X0PSAY	M10162040054X0PSAY
M30082040108X0IWAR	M30042040054X0IWAR	M30162040054X0IWAR
M30082040108X0IWAY	M30042040054X0IWAY	M30162040054X0IWAY
M30082040108X0ISAR	M30042040054X0ISAR	M30162040054X0ISAR
M30082040108X0ISAY	M30042040054X0ISAY	M30162040054X0ISAY
M30082040108X0PWAR	M30042040054X0PWAR	M30162040054X0PWAR
M30082040108X0PWAY	M30042040054X0PWAY	M30162040054X0PWAY
M30082040108X0PSAR	M30042040054X0PSAR	M30162040054X0PSAR
M30082040108X0PSAY	M30042040054X0PSAY	M30162040054X0PSAY