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Product Specifications of the SH726A and SH726B MCUs

Function			78K0R/LG3-M μPD78F8070
Internal memory		Flash memory (Self-programmable)	128 KB
		RAM	7 KB
Memory space			1 MB
Clock	Main	High-speed system	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 2 to 20 MHz: VDD = 2.7 to 3.6 V / 2 to 5 MHz: VDD = 1.8 to 2.7 V
		Internal high-speed oscillation	Internal oscillation 1 MHz (TYP.) or 8 MHz (TYP.) or 20 MHz (with PLL) selected by an option byte
	Subsystem		XT1 (crystaloscillation, external subsystem clock input (EXCLKS1) 32.768 kHz (TYP.)
	Internal low-speed oscillation (for WDT)		Internal oscillation 30 kHz (TYP.)
General-purpose registers			8-bit × 32 registers (8-bit × 8 registers × 4 banks)
Minimum instruction execution time			0.05 μs (high-speed system clock: fMX = 20 MHz operation)
			0.125 μs (high-speed internal oscillation clock: fIH = 8 MHz (TYP.) operation)
			30.5 μs (subsystem clock: fSUB = 32.768 kHz operation)
Instruction set			• 8-bit operation, 16-bit operation • Multiplication (16-bit × 16-bit)

			• Bit manipulation (set, reset, test and Boolean operation), etc.
I/O ports	Total		45
	I/O	CMOS	39
		N-ch O.D.	2
	Output	CMOS	1
	Input	CMOS	3
Timer			• 16-bit timer: 12 channels • Watchdog timer: 1 channel • Real-time counter: 1 channel • Real-time counter 2: 1 channel
	Timer outputs		3 (PWM output: 3 (Timer array unit 0))
	RTC outputs		1 • 1 Hz (Subsystem clock: fSUB = 32.768 kHz) • 32.768 kHz (Subsystem clock: fSUB = 32.768 kHz)
10-bit successive approximation type A/D			2 channels
24-bit ΔΣ-type A/D			4 channels
Serial interface	UART supporting LIN-bus		1 channel
	CSI / UART / simplified I2C		1 channel
	UART		1 channel
	Multimaster I2C		1 channel
LCD controller / driver			Internal voltage boosting method, capacitor split method, and external resistance division method are switchable
	Segment signal output		40
	Common signal output		4
Multiplier / divider			16-bit × 16-bit = 32-bit (multiplication), 32-bit / 32-bits = 32-bit, 32-bit remainder

		(division)
DMA controller		2 channels
Vectored interrupt sources	Internal	32
	External	4
Power calculation circuit		Provided
Power quality measurement circuit		Provided
Digital frequency conversion circuit		Provided
Reset		• Reset by RESET pin • Internal reset by watchdog timer • Internal reset by power-on-clear • Internal reset by low-voltage detector • Internal reset by illegal instruction execution Note
Power-on-clear circuit		• Power-on-reset: 1.61±0.09 V • Power-down-reset: 1.59±0.09 V
Low-voltage detector	VDD voltage detector	1.91 V to 3.45 V (11 stages)
	EXLVI voltage detector	1.21 V
On-chip debug function		Provided
BCD adjustment		
Power supply voltage		VDD = 1.8 to 3.6 V
Operating ambient temperature		TA = −40 to +85 deg C
Package		100-pin plastic LQFP (Fine pitch, 14 × 14-mm)

Note) When instruction code FFH is executed. Reset by illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.