

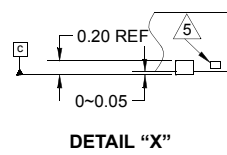
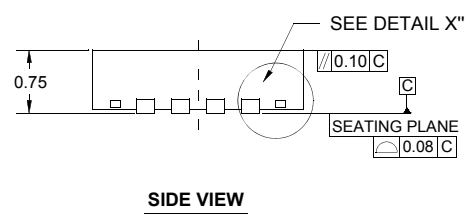
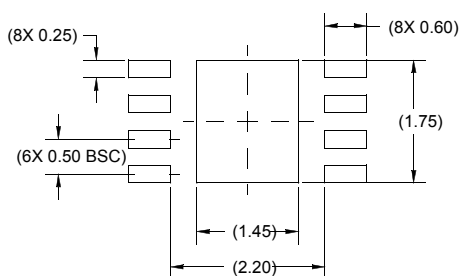
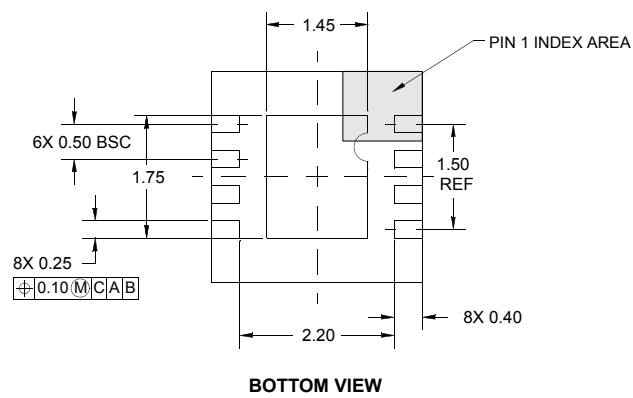
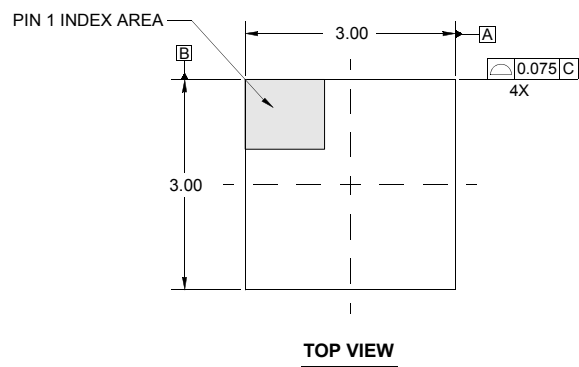
Plastic Packages for Integrated Circuits

Package Outline Drawing

L8.3x3G

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE (TDFN)

Rev 1, 5/15



NOTES:

- Controlling dimensions are in mm.
Dimensions in () for reference only.
- Unless otherwise specified, tolerance: Decimal ± 0.05
Angular $\pm 2^\circ$
- Dimensioning and tolerancing conform to JEDEC STD MO220-D.
- The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
- Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).