

## RZ/N1D, RZ/N1S, RZ/N1L Group

### CONNECT IT! ETHERNET RZ/N1x GettingStarted

#### Introduction

RZ/N1 is a family of scalable ARM® based industrial Ethernet switches. Due to the integrated performant ARM® Cortex®-A7 CPU, they are ideal choice for building products such as Programmable Logic Controllers (PLC), complex remote-IO slaves, industrial switches, gateways or operator terminals.

This guide provides an overview of the Solution Kit package and provides reference to the important documentation for assisting you in a quick evaluation of the RZ/N1x device. It represents a short reference for the RZ/N1x Solution Kits and provides an overview of the kit packages and a description of their structure.

This guide is an addition to the extensive RZ/N1 device documentation. RZ/N1 board and RZ/N1 software documentation you may find in the SW packages and/or in the document specific area of the RZ/N1 Solution Kit release. The Solution Kit boards can solely be used for evaluation purposes. It is not allowed to use those boards for commercial purposes.

- **Chapter 0** gives an insight into the RZ/N1 Solution Kit content and provides a reference to important documentation.
- **Chapter 2** describes how to use the Solution Kit Installer to install (copy) the dedicated documents and SW structures on your PC.
- **Chapter 3** gives a short overview about tools you might need for your HW and SW development.

For jumping directly to the quick start guide for bringing up your board for the first time, please open the respective quick start guide document from the solution kit's root directory:

CONNECT IT! ETHERNET RZ/N1D : [r01qs0022edxxxx-rzn1d-connectit.pdf](#)

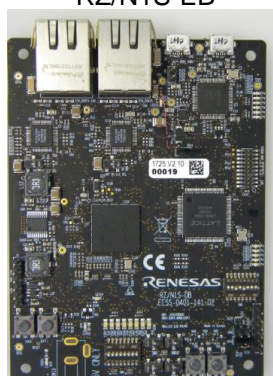
CONNECT IT! ETHERNET RZ/N1S : [r01qs0021edxxxx-rzn1s-connectit.pdf](#)

CONNECT IT! ETHERNET RZ/N1L : [r01qs0020edxxxx-rzn1l-connectit.pdf](#)

RZ/N1D-EB



RZ/N1S-EB



RZ/N1L-EB



## List of Abbreviations and Acronyms

| Abbreviation      | Full Form   |
|-------------------|---|
| A7                | Short name for Arm Cortex-A7 CPU  |
| M3                | Short name for Arm Cortex-M3 CPU  |
| CTC / MCTC        | Core-to-Core / Micro- Core-to-Core communication scheme between A7 and M3         |
| API               | Application Programming Interface   |
| Baremetal         | Programming strategy not using an operation system (OS) – OS-less                 |
| BSDL              | Boundary Scan Description Language  |
| BSP               | Board Support Package   |
| CANopen / CO      | CANopen Bus Protocol (CAN: Controller Area Network)                               |
| CPLD              | Complex Programmable Logic Device; kind of FPGA                                   |
| DFU               | Device Firmware Update Tool   |
| DLR               | Device Level Ring Protocol  |
| EtherCAT / ECAT   | EtherCAT Network Protocol   |
| EtherNet/IP / EIP | EtherNet/IP Network Protocol  |
| EULA              | End User Licensing Agreement / License document                                   |
| GPIO              | General Purpose Input/Output Device Pins  |
| EPL               | Ethernet POWERLINK Network Protocol   |
| IDE               | Integrated Development Environment (e.g. IAR EWARM)                               |
| Schematic         | Electronic circuit diagram(s)   |
| BOM               | Bill of Materials; list of all components used in the circuit                     |
| PCB               | Printed Circuit Board / board with electronic components                          |
| Solution Kit      | Electronic board with debugger, cables and a SW/document package                  |
| PLC               | Programmable Logic Controller (e.g. master which is controlling different slaves) |
| PMU               | Power Management Unit; takes care for all power aspects incl. power-on and -off   |
| PNIO              | PROFINET IO Protocol  |
| PROFINET          | Process Field Network Protocol  |
| lwIP              | Lightweight IP Protocol   |
| GOAL              | Generic OS Abstraction Layer, Communication Framework on RZ/N1x                   |
| CLI               | Command Line Interface; included in GOAL  |
| LLDP              | Link Layer Discovery Protocol   |
| NVM               | Non-volatile memory, e.g. flash, EEPROM   |
| OS                | Operating System (e.g. Linux, ThreadX)  |
| RT                | Real-Time   |
| USBH / USBF       | Universal Serial Bus – Host / Function  |
| MSEBI             | Medium Speed External Bus Interface   |
| HW                | Hardware  |
| HW-RTOS           | HW based accelerator in the R-IN Engine for real-time OS (ultron) acceleration    |
| R-IN Engine       | Cortex-M3 CPU based HW module including embedded switch and accelerators          |
| SW                | Software  |
| ultron            | Micro-Itron; real-time operation system used on the RZ/N Cortex-M3 CPU            |
| HSR               | High-Availability Seamless Redundancy Protocol for substation automation          |
| PRP               | Parallel Redundancy Protocol for substation automation                            |
| IBIS              | I/O Buffer Information Specification for pin signal simulation                    |
| PinMux            | Pin and GPIO multiplexing to map interface features to different pins             |

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Sercos is a registered trademark of Sercos International e.V.

Ethernet POWERLINK is the registered trademark of Ethernet POWERLINK Standardization Group (EPSC).

CAN (Controller Area Network) : An automotive network specification developed by Robert Bosch GmbH of Germany

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## 1. RZ/N1 Solution Kits

RZ/N1x is a new Renesas SoC family mainly targeting powerful industrial automation and communication applications. With the RZ/N1x Solution Kits and the accompanying document and evaluation software package, Renesas enables a quick and easy evaluation of the RZ/N1x hardware and its software and the development of RZ/N1x based products. The software and tool ecosystem was built with several partners well known in the embedded and the industrial automation arena and together with Renesas they provide a comprehensive hardware and software expertise for complex industrial automation and communication systems. Please note that the provided SW is a limited for evaluation purposes only! The software cannot and must not be used in development project or in an actual product.

### 1.1 CONNECT IT! ETHERNET RZ/N1D

The **CONNECT IT! ETHERNET RZ/N1D** Solution Kit is based on the RZ/N1D, a 5-port, industrial Ethernet communication SoC in a 400BGA package. The device features two independent blocks integrated in a single package – a communication block based on the proven multi-protocol R-IN Engine, as well as an application block with a dual ARM® Cortex®-A7 and a variety of peripherals, including a DDR memory interface required for rich operating systems like Linux. Along this external memory The RZ/N1D additionally includes 2 MB internal SRAM. The RZ/N1D Solution Kit contains everything you need for fast evaluation and rapid prototyping of multiple industrial Ethernet protocols.

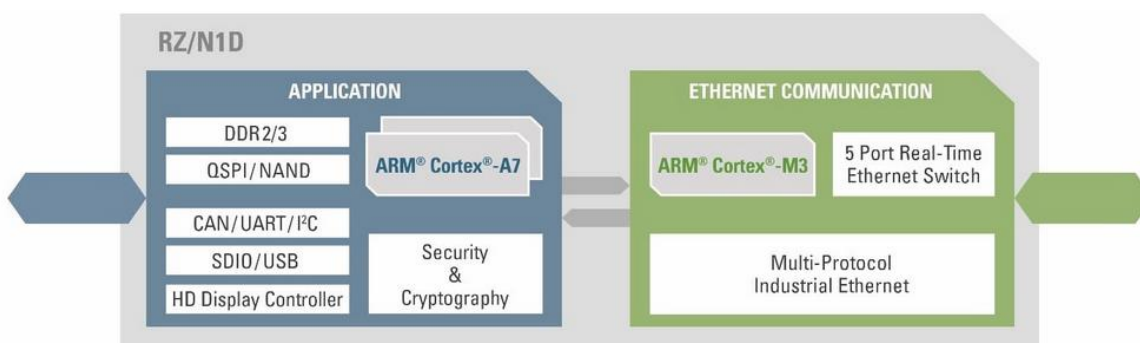


Figure 1-1: RZ/N1D Functional Overview

For jumping directly to the quick start guide for the RZ/N1D Solution Kit please refer to the document [YCONNECT-IT-RZN\\_V1.xlr01qs0022edxxx-rzn1d-connectit.pdf](#)

### 1.2 CONNECT IT! ETHERNET RZ/N1S

The **CONNECT IT! ETHERNET RZ/N1S** Solution Kit is based on the RZ/N1S, a 5-port, industrial Ethernet communication SoC in a 324BGA package. As the RZ/N1D the device features two independent blocks integrated in a single package – a communication block based on the proven multi-protocol R-IN Engine, as well as an application block and a variety of peripherals. In contrast to the RZ/N1D, RZ/N1S includes only a single ARM® Cortex®-A7 CPU without an external DDR interface, but with 6MB internal SRAM. Please refer to the RZ/N1S device documentation for further differences. Also the RZ/N1S Solution Kit contains everything you need for fast evaluation and rapid prototyping of multiple industrial Ethernet protocols.

For jumping directly to the quick start guide for the RZ/N1S Solution Kit please refer to the document **YCONNECT-IT-RZN\_V1.xr01qs0021edxxx-rzn1s-connectit.pdf**

### 1.3 CONNECT IT! ETHERNET RZ/N1L

The **CONNECT IT! ETHERNET RZ/N1L** Solution Kit is based on the RZ/N1L, a 3-port, industrial Ethernet communication SoC in a 196BGA package. In contrast to the RZ/N1D and RZ/N1S the device has just the communication block based on the proven multi-protocol R-IN Engine with 6MB internal SRAM (no ARM® Cortex®-A7 CPU and no external DDR interface). Please refer to the RZ/N1L device documentation for further differences. Also the RZ/N1L Solution Kit contains everything you need for fast evaluation and rapid prototyping of multiple industrial Ethernet protocols.

For jumping directly to the quick start guide for the RZ/N1L Solution Kit please refer to the document **YCONNECT-IT-RZN\_V1.xr01qs0020edxxx-rzn1l-connectit.pdf**

### 1.4 RZ/N1 Device Comparison

The following image gives a rough overview about the features of the different RZ/N1 devices and their main differences. For more details refer to the respective RZ/N1x User Manuals.

|                     | RZ/N1D  | RZ/N1S  | RZ/N1L  |
|---------------------|---|---|---|
| CPU                 | Dual Cortex A7 + Cortex M3 (R-IN Engine)                                | Single Cortex A7 + Cortex M3 (R-IN Engine)                              | Cortex M3 (R-IN Engine)   |
| Supported Protocols | PROFINET, EtherCAT, EtherNet/IP, SERCOS, POWERLINK, Modbus TCP, CANopen | PROFINET, EtherCAT, EtherNet/IP, SERCOS, POWERLINK, Modbus TCP, CANopen | PROFINET, EtherCAT, EtherNet/IP, SERCOS, POWERLINK, Modbus TCP, CANopen |
| Target Application  | PLC, HMI, Switch  | PLC, HMI, Switch  | Remote IO   |
| Internal Memory     | 2MB   | 6MB   | 6MB   |
| Integrated PHY      | ×   | ×   | ×   |
| DDR Interface       | ⊕   | ×   | ×   |
| Crypto              | ⊕   | ⊕   | ×   |
| LCD Controller      | ⊕   | ⊕   | ×   |
| Switch              | 5 / 3 Port  | 5 / 3 Ports   | 3 Ports   |
| Redundancy          | HSR, PRP, DLR, MRP  | PRP, DLR, MRP   | DLR   |
| Package             | 400BGA / 324BGA   | 324BGA / 196BGA   | 196BGA  |

Figure 1-2: RZ/N1x Device Feature Overview

### 1.5 RZ/N1D / RZ/N1S / RZ/N1L CPU Board Hardware

The CONNECT IT! RZ/N1x Solution Kits are including the RZ/N1x CPU Boards (RZ/N1D-DB, RZ/N1S-DB or RZ/N1L-DB) and are providing you with the most important RZ/N1x device interfaces:

- Fast Ethernet (MII/RMII) (2 x)
- NOR flash
- DDR3 (RZ/N1D-DB only)
- USB Device/Host

- Serial USB debug port including 5V power
- GPIOs
- User LEDs and user switches
- I-Jet Lite debugger interface

Additionally you get an I-Jet Lite debugger for your first SW development steps with the RZ/N1 Solution Kit. You find the RZ/N1D, RZ/N1S and RZ/N1L CPU Board documentation including setup notes and schematics under **YCONNECT-IT-RZN\_V1.x\Documents\RZN.Boards\RZN1n-DB** (with n = D, S, L).

## 1.6 CONNECT IT! ETHERNET RZ/N1-EB

In case you want to use the RZ/N1x interfaces which are not provided by the RZ/N1D-DB and/or RZ/N1S-DB CPU boards you can use the optional expansion board **CONNECT IT! RZ/N1 Expansion Board (RZ/N1-EB)**. Together with one of the CPU boards above this gives access to the full set of RZ/N1D or RZ/N1S interfaces. The expansion board has no stand-alone capability and requires an RZ/N1D or RZ/N1S CPU board. On the other side the RZ/N1L-DB board cannot be used together with the RZ/N1-EB board, as all interfaces are already included on the CPU board.

The documentation for the expansion board including the setup notes and the schematics you may find under **YCONNECT-IT-RZN\_V1.x\Documents\RZN.Boards\RZN1-EB**.

## 1.7 Software

All RZ/N1x Solution Kits contain also a software release package that enables the user to evaluate various functionalities of an advanced communication and processing device in the industrial automation industry. The release package is also available for download on the Renesas RZ/N website. The software ecosystem of RZ/N1 is broad and complex, due to different SW partners, several supported operating systems (OS), many industrial real-time communication protocols, different development environments and a mixed feature support of the three RZ/N1x CPU boards with or without the RZ/N1-EB expansion board. The software packages are stored in the release directory **YCONNECT-IT-RZN\_V1.x\Software**.

Documents for the software packages are available under the path **YCONNECT-IT-RZN\_V1.x\Documents\RZN.Software\** and partially in the corresponding software directories.

Following is a short overview about the main software items of the RZ/N1x Solution Kits.

### 1.7.1 GOAL & Protocol Stacks

Coping with the real-time requirements and growing demands for Industrie 4.0 applications, Renesas provides a variety of industrial real-time communication protocols that are implemented on communication module of RZ/N1x – the Cortex M3 core in an effective combination with a 5-port switch and various accelerators. This communication module inside the RZ/N1x is called R-IN Engine (Renesas Industrial Network Engine). With this architecture the RZ/N1x devices are delivering a high performance, low power, enhanced and flexible communication features to the outside world, which is independent from the applications side (RZ/1D and RZ/N1S).

Based on these requirements the company port GmbH and Renesas have developed the **Generic Open Abstraction Layer (GOAL)** middleware for Renesas R-IN Engine based processor families. The GOAL consists

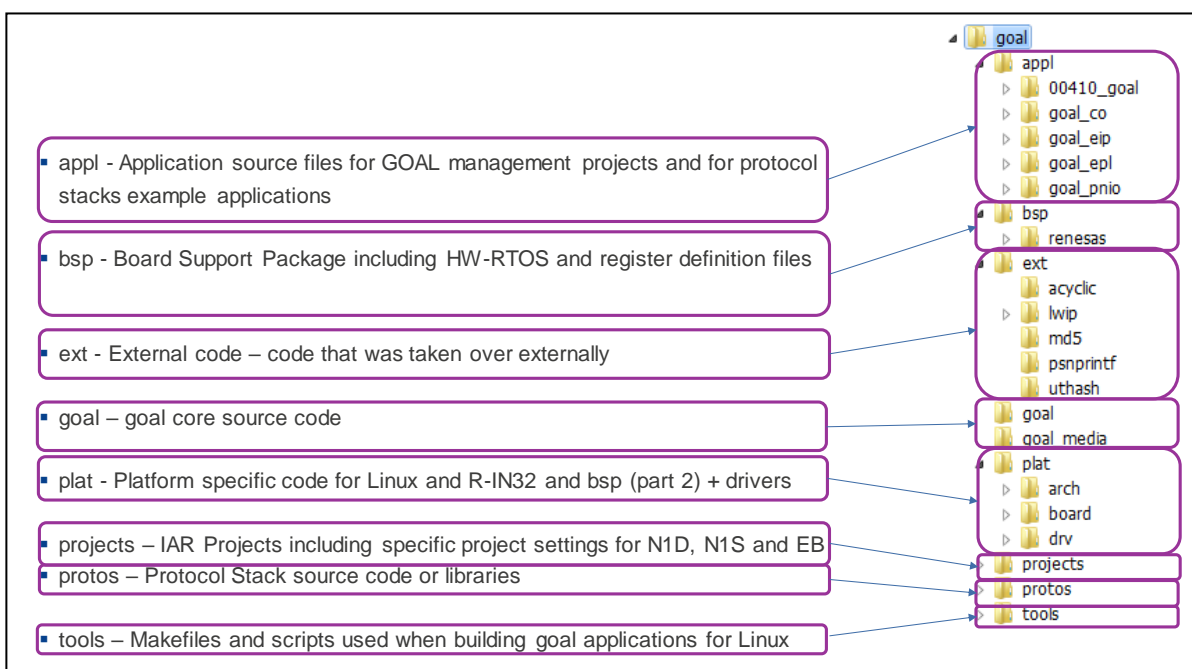
of several layers of software for accessing the underlying R-IN platform resources, but also to access the protocol stacks via dedicated APIs.

Out of the box the middleware provides support for:

- PROFINET, EtherCAT, EtherNet/IP, Modbus, POWERLINK and CANopen
- Supporting protocols such as TCP/IP (lwIP), SNMP, RSTP, etc.
- API for PHY and Switch Management
- Inter-processor communications (Core-to-Core, CTC) with shared memory, mailboxes, etc.

A variety of sample applications are delivered together with the GOAL software package explaining the basic functionalities of the run-time system and show how to configure the different components and how to write a GOAL based portable application. You may find the IAR GOAL sample projects in the directory **YCONNECT-IT-RZN\_V1.x\Software\GOAL\projects\**. As the R-IN Engine on the RZ/N1x boards are functionally identical this GOAL package is covering all three boards with different IAR projects.

Figure 1-3 shows the file structure of the GOAL package on the release available in the directory **YCONNECT-IT-RZN\_V1.x\Software\GOAL\**.



**Figure 1-3: GOAL File Structure** (previous version)

Furthermore, GOAL middleware was ported to Linux, allowing the user to develop user space applications using GOAL APIs. Additionally, with the Core2Core APIs the user could create communication channels for message transmission between Cortex A7 and Cortex M3 core.

The GOAL applications and projects overview document **YYMMDD\_RZN\_release\_overview\_vx\_y.xlsx** summarizes all implemented software examples of the current GOAL version. This EXCEL table shows and distinguishes between:

- Available protocol and application example
- Used RZ/N1x board including RZ/N1-EB Expansion Board

- Applied SW structure on the RZ/N1D and RZ/N1S devices covering A7 (AC, Application Core) and M3 (CC, Communication Core) with or without Core-to-Core (CTC) communication between the two cores
- Used protocol and tool versions

### 1.7.2 Linux (only for RZ/N1D) & U-Boot (RZ/N1D and RZ/N1S)

The RZ/N1 Linux Board Support Package comes distributed for RZ/N1D demo board and runs on the Cortex A7. U-Boot BSP is distributed for both RZ/N1S and RZ/N1D. It includes the drivers for all the required peripherals including clock controller, Pinmux, UART, DDR, QSPI, NAND, Ethernet MAC, 5port Switch, RGMII/GMII Converters, SDHC, I2C and USB Host/Function. Furthermore, for customers that are interested in Yocto based Linux development, Renesas provides the respective Yocto recipes to build the Linux, U-Boot and root file system. All of these are stored under **YCONNECT-IT-RZN\_V1.x\Software\U-Boot-and-Linux** in the Solution Kit installation folder.



The Operating System (OS) Linux has been implemented for the RZ/N1D and is running on the Dual-Core ARM® Cortex®-A7 CPUs. The Linux example is only running on the RZ/N1D-DB board and requires the available external DDR memory. As provided, the BSP includes also a root file system. The size of the flash memory storing the boot images and file system for the RZ/N1D is limited. Thus, the file system can be extended on an SD card on the RZ/N1-EB board.

You will need the dfu-util tool for either Linux or Windows to write the binaries to the flash memory of the board. Please refer to the directory **YCONNECT-IT-RZN\_V1.x\Documents\RZN.Software\U-Boot-and-Linux\Documentation** for more information about Linux and U-Boot BSP for RZ/N1. Quick start guide **YCONNECT-IT-RZN\_V1.x\r01qs0022edxxx-rzn1d-connectit.pdf** provides some guidelines to bring U-Boot and Linux on the RZ/N1D board.

Please also refer to the available Linux documentation on the web site from the Linux organization [www.linux.org](http://www.linux.org).

### 1.7.3 ThreadX Real-Time Operation System (RZ/N1D and RZ/N1S)

The Real-Time Operating System (RTOS) ThreadX is Express Logic's advanced Real-Time Operating System (RTOS) designed specifically for deeply embedded, real-time, and IoT applications. It has been implemented for the RZ/N1D and RZ/NS and is running on the ARM® Cortex®-A7 CPU.



This software is a limited version of ThreadX provided for RZ/N1x evaluation and cannot be used in development or in an actual product. For further details please read the provided ThreadX documents stored in the release document path **YCONNECT-IT-RZN\_V1.x\Documents\RZN.Software\ThreadX\**.

Please also refer to the available ThreadX documentation on the web site from Express Logic <http://rtos.com/products/threadx> and related licensing info on and <http://rtos.com>.

### 1.7.4 CODESYS PLC Example (only for RZ/N1D + RZ/N1-EB)



CODESYS is the product name of the complete software family of IEC 61131 programming tools development by the company 3S – Smart Software Solutions GmbH. The CODESYS PLC runtime example is running under a standard Linux environment including switch support on the ARM® Cortex®-A7 CPU and requires the RZ/N1-EB Expansion board to support the used interfaces. The ARM® Cortex®-M7 CPU is not used in this demo due to simplicity.

Please read the **YCONNECT-IT-RZN\_V1.x\Documents\RZN.Software\U-Boot-and-Linux\RZN1-Linux-QRZN1D-Quick-Start-Guide.pdf** and the **RZN1-CODESYS-Quick-StartGuide** software documents for further details. The document **CODESYSControl\_V3\_Manual.pdf** gives basic information to start working with CODESYS and to understand the internal mechanisms.

Please also refer to the available CODESYS documentation on the web site from 3S [www.codesys.com](http://www.codesys.com).

### 1.7.5 PRP – Parallel Redundancy Protocol (only for RZ/N1D)

PRP is an Ethernet based network protocol which can be implemented in SW. It is protecting a network against failure of any network component by transferring and receiving the frames into/from two independent Ethernet sub-networks.

**Important:** Please read the additional PRP information in the Solution Kit release notes

### 1.7.6 HSR- High-Availability Seamless Redundancy (only for RZ/N1D)

HSR is an Ethernet based network protocol used for electrical substation automation which requires dedicated HW support. It is protecting a network against failure of any network component by sending and receiving the frames inside an Ethernet ring structure to/from both directions. The HSR software is running on the Cortex-A7 CPUs under a Linux environment. The Cortex-M3 is not used in this evaluation example.

Please read the **YCONNECT-IT-RZN\_V1.x\Documents\RZN.Software\HSR\IEC\_62439-3\_HSR\_Demo\_Kit** documentation for further details about setting up the RZ/N1x HSR demo on the RZ/N1D and RZ/N1-EB Expansion board.

You find the corresponding HSR software example in **YCONNECT-IT-RZN\_V1.x\Software\HSR**.

**Important:** Please read the additional HSR information in the Solution Kit release notes

### 1.7.7 OS-Less / Baremetal Drivers

The baremetal driver for RZ/N1L are meant to demonstrate how to interface to the various interface IPs of the Renesas RZ/N1 devices in an OS-less environment. It consists of a sample OS-less application and a set of Firmware Integration Technology (FIT) modules for the following and other features:

- bsp – Board Support Package module - provides support for RZ/N1 devices and boards
- dma – Drivers for Direct Memory Access
- gmac – Gigabit MAC support
- a5psw -- Advanced 5-port Switch support



- gpio – Provides device specific support e.g. for multiplexed functionality of IPs
- i2c – I2C Controller
- iomux – RZ/N1x Pin Multiplexing
- msebi – Medium Speed External Bus Interface; prallel interface with many use case options
- qspi – Quad SPI Memory
- sdio – Secure Digital Input/Output; SD Card
- spi – Serial Peripheral Interface
- timer – General Timers
- uart – Standard UARTs
- usb – Universal Serial Bus – Function CDC, Host CDC & Hub
- wdt – Watch Dog Timer

Please refer to the Readme.Release document and the Baremetal Driver software folder **YCONNECT-IT-RZN\_V1.x\Documents\RZN.Software\BaremetalDrivers** for further release details.

## 1.8 RZ/N1 Tools

Inside of the Solution Kit software package, Renesas is providing some tools which are useful for typical programmers and designers to work with our platform. The directory in the release is **...YCONNECT-IT-RZN\_V1.x\Tools**. The tools currently include the HTML-based PinMux tool, PC drivers, IBIS models (I/O Buffer Information Specification) for RZ/N1x devices in different variants (BGA400, BGA324 and BGA196 packages) and an IAR Embedded Workbench which can be used under a 30-days trial condition for the RZ/N1x Solution Kit evaluation. Other tools, which are not included in this release, but might be of interest for the user, are described in chapter 3 Miscellaneous Tools for Hardware and Software Development.

### 1.8.1 PinMux Tool

The PinMux Tool is used to support the customer with the pin multiplexing configuration, providing a graphical user interface. The user specifies the peripheral signals and their respective external pinouts. This HTML based application also detects and resolves conflicts in the configurations and it generates code (C header file for U-Boot and GOAL, and device tree file for Linux) that is used to configure the device at initialization time. The tool can be found under **...YCONNECT-IT-RZN\_V1.x\Tools\PinMux**.

It includes a light documentation “Quick Start” in its first “Package” tab. Following steps need to be done to generate the pin multiplexing for a new RZ/N1 board. For the Solution Kit boards these steps has been done already and the generated PinMux code is integrated into the SOFTWARE evaluation packages:

- Step 1:** Select the RZ/N1x device and device package you want to use on your board
- Step 2:** Pick all the peripherals you want to use on your board
- Step 3:** Map the GPIO to an interface function, or the interface function to the GPIO pin
- Step 4:** Check the RZ/N1 package footprint
- Step 5:** Generate the code used for the pin multiplexing in the start-up phase of your application

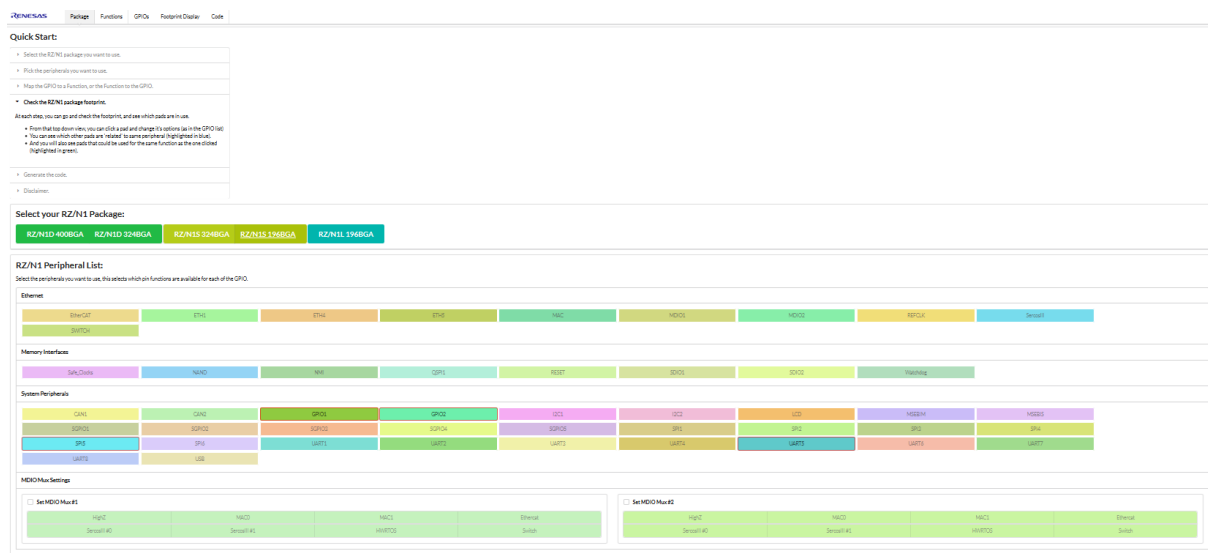


Figure 1-4: PinMux Tool

### 1.8.2 IAR Embedded Workbench for ARM (EWARM)

IAR EWARM is used in the development of the software running on Cortex-M3 core in the R-IN Engine and partially on the Cortex-A7 application side.

Renesas provides the exact version used to develop the software on the Cortex-M3 side assuring that it can be further flawlessly developed or adapted. The used IDE installation executable for IAR EWARM can be found in the RZ/N Solution Kit under **YCONNECT-IT-RZN\_V1.xTools\IAREWARM**. After installation you can use the IAR projects of the RZ/N1 GOAL software application examples. If using the 30 days trial version be aware that you cannot continue the evaluation under that condition.

Please visit the IAR website [www.iar.com](http://www.iar.com) for technical and licensing details.

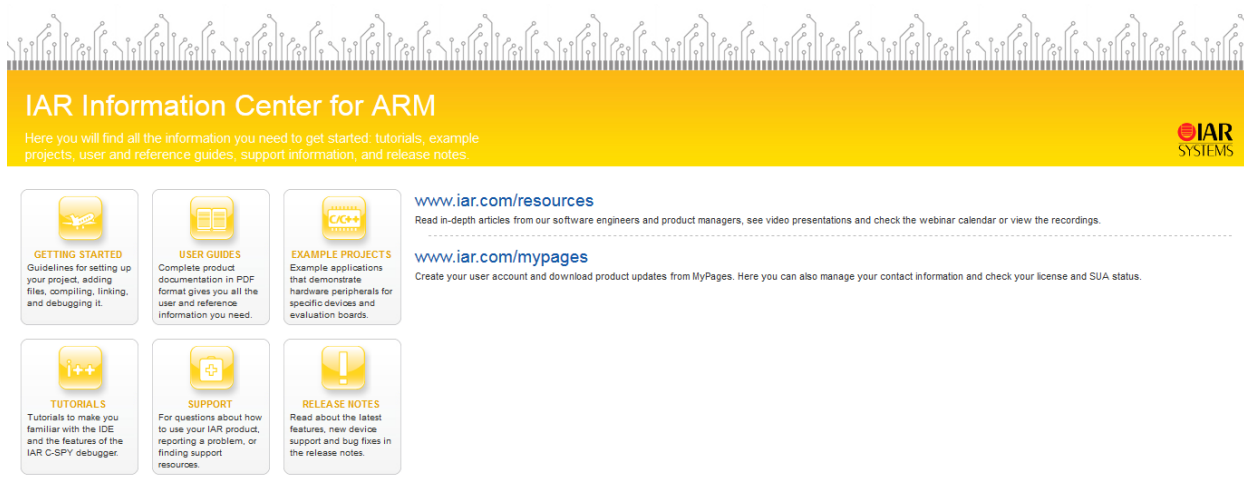


Figure 1-5: IAR Embedded Workbench for ARM Information Center

### 1.8.3 FTDI PC Serial USB Drivers

To use the serial USB interfaces of the RZ/N1x Solution Kits you might need to install the FTDI serial USB drivers on your Windows PC. Some Windows PCs are installing it automatically however. The drivers are located under ...**YCONNECT-IT-RZN\_V1.x\Tools\FTDI**.

## 1.9 Documentation

The documentation is available in the release directory ...**YCONNECT-IT-RZN\_V1.x\Documents**

- **YCONNECT-IT-RZN\_V1.x\Documents\RZN**  
RZ/N1 User Manuals and Datasheets covering all RZ/N1x devices in all packages. The User Manual is divided into 4 parts:
  - Introduction part (architecture, address spaces, clock generation, reset, IOs, ...)
  - System part (CPUs, NoC, internal/external memories, debugging, USB, DMA, ...)
  - Peripheral part (\*UART, SPI, GPIO, Timer, CAN, ADC, LCD controller, ...)
  - Ethernet part (R-IN Engine, HW-RTOS, GMAC, ESC, HSR, SERCOS III, MDIO, ...)Additionally the RZ/N1 Data Sheet gives an overview about the RZ/N1 features.
  
- **YCONNECT-IT-RZN\_V1.x\Documents\RZN.Boards** –  
All board specific documentation consisting of layout, schematics and setup notes for the RZ/N1x CPU Boards and the RZ/N1 Expansion Board. Further on it includes the environment and data of the programmable components of the CPU boards, like CPLD, PMU and FTDI serial-to-USB.
  
- **YCONNECT-IT-RZN\_V1.x\Documents\RZN.Software**  
All software related documentation (GOAL, Linux, Application Notes, CODESYS, ThreadX, etc.)
  
- **YCONNECT-IT-RZN\_V1.x\Documents\RZN.SolutionKit**  
RZ/N1x Solution Kit documentation including an introduction video. The video is not covered by the RZ/N1 Installer described in chapter 2.

## 2. Installation Setup

After you have setup the hardware, this chapter provides the references to two main guidelines to get your first software running on the board. The main software entities include U-Boot on the Cortex A7 core and GOAL with an example application on the Cortex M3. This chapter provides reference to the documents that will guide you through programming QSPI with the software and running it. U-Boot is available for RZ/N1D and RZ/N1S, Linux is available only for RZ/N1D and ThreadX is available for RZ/N1D and RZ/N1S.



### 2.1 RZ/N1x Document and Software Installation

The installer assists you in copying only the relevant items to your PC.

To copy the RZ/N1x documents, SW and tools from the release to your PC you can optionally use the available autorun installer which is available in the release. Basically, you must select between the board(s) you are using and the related data type you want to copy to your local PC drive.

The installation related script is in directory **YCONNECT-IT-RZN\_V1.x\Install** and runs the copy process according to your made selection. The SW package is a mixture between generic software items for several RZ/N1 boards and some very specific packages which run only on one board or on a specific combination with the RZ/N1-EB expansion board. You may ignore the Install directory.

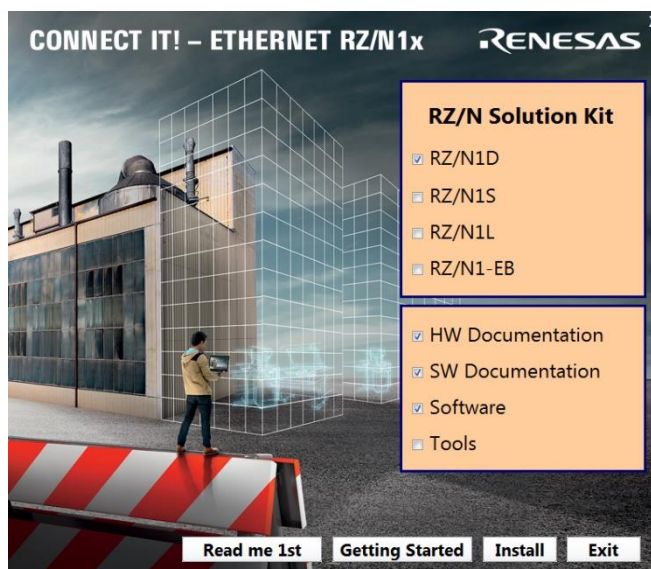


Figure 2-1: RZ/N1x Installer Window

The button **Read me 1<sup>st</sup>** will display a text document showing the details of the current RZ/N1 release version including details about its content. Please check this document carefully when you want to update an old version of the Solution Kit.

The button **Getting Started** will display this document.

For the installation with the button **Install** (a copy process) you can select certain sets of elements available in the release. For this you have to make the following steps:

**Step 1:** Make your **RZ/N1 board(s) selection**. Depending upon the boards the RZ/N1x Installer selects a different set of documents and software packages.

**Step 2:** Make your **selection of the data type** you want to install (copy) on your PC. The figure above is showing the default selection when starting the RZ/N1x Installer.

**Step 3:** Press the **Install** button to start the copy process.

**Step 4:** You are asked to accept the shown license agreement before you can proceed.

**Step 5:** You can change the **installation target directory** if required

**Step 6:** Press the **Install** button again. The default directory path is C:\data\Connect\_it\_RZN.

By pressing the **Exit** or **[X]** button in the top right window area you can stop the RZ/N1x installer.

**Important Note:**

Please be cautious when using this installer with a new release for the installation of new SW in order not to overwrite SW changes or additions you have made on a previous SW version of the RZ/N1 SW package.

### 3. Miscellaneous Tools for Hardware and Software Development

Several board and SW setup and develop steps might require certain tool depending on your PC. These tools are not included in this release. The following list gives an overview about these tools with a short description and related links to download the tool and for further information:

#### 3.1 dfu-util

dfu-util is a host side implementation of the DFU 1.0 and DFU 1.1 specifications of the USB forum. DFU is intended to download and upload firmware to/from devices connected over USB. Using dfu-util you can download firmware to your DFU-enabled device or upload firmware from it. Please refer to chapters 3.1 and 3.2 in ...\\YCONNECT-IT-RZN\_V1.x\\Documents\\RZN.Software\\U-Boot-and-Linux\\RZN1-U-Boot-User-Manual.pdf for a short summary on how to install the tool for Windows or Linux.

- Link <http://dfu-util.sourceforge.net>
- Manual <http://dfu-util.sourceforge.net/dfu-util.1.html>

#### 3.2 Zadig

**Zadig** is a Windows application that installs generic USB drivers, such as WinUSB, libusb-win32/libusb0.sys or libusbK, to help you access USB devices. Please check chapter 3.2.2 in ...\\YCONNECT-IT-RZN\_V1.x\\Documents\\RZN.Software\\U-Boot-and-Linux\\RZN1-U-Boot-User-Manual.pdf for an overview of installation steps to register the Board as USB Download Gadget in Windows.

- Link <http://zadig.akeo.ie/>
- FAQ <https://github.com/pbatard/libwidi/wiki/FAQ#Zadig>

#### 3.3 FT\_Prog (Mprog)

FT\_PROG (previously named mProg) is the current EEPROM programming utility from FTDI. MProg has the ability to erase, program, read and read and parse the EEPROM contents for the FT4232H serial-to-USB device on the RZ/N1 boards. MProg has a clear user interface for selecting settings and a facility to save EEPROM templates to file which can be loaded later for programming more devices. The used device configuration data is stored in the board document directories.

- Link [www.ftdichip.com/Support/Utilities.htm#FT\\_Prog](http://www.ftdichip.com/Support/Utilities.htm#FT_Prog)
- Manuals [www.ftdichip.com/Support/Documents/AppNotes/AN\\_124\\_User\\_Guide\\_For\\_FT\\_PROG.pdf](http://www.ftdichip.com/Support/Documents/AppNotes/AN_124_User_Guide_For_FT_PROG.pdf)

### 3.4 Lattice Diamond

The Diamond Toolchain from Lattice is used to design and download CPLD Data. The used MachXO2 device is supported from the free of charge version. The used device configuration data is stored in the board document directories.

- Link <http://www.latticesemi.com/en/Products/DesignSoftwareAndIP/FPGAandLDS/LatticeDiamond.aspx>
- Manual [www.latticesemi.com/view\\_document?document\\_id=52212](http://www.latticesemi.com/view_document?document_id=52212)

### 3.5 Lattice PacDesigner

The PacDesigner Toolchain from Lattice is used to design PMU devices from Lattice. On the RZ/N1-boards the ProcessorPM device (POWR605) is used. To program these devices the program utility from the Diamond Toolchain is used. The Tool can be used free of charge. The used device configuration data is stored in the board document directories.

- Link [www.latticesemi.com/en/Products/DesignSoftwareAndIP/MixedSignalDS/PacDesigner.aspx#\\_31E497BC0E744ACA8B3FC5B8892B2AAB](http://www.latticesemi.com/en/Products/DesignSoftwareAndIP/MixedSignalDS/PacDesigner.aspx#_31E497BC0E744ACA8B3FC5B8892B2AAB)
- Manual [www.latticesemi.com/view\\_document?document\\_id=51568](http://www.latticesemi.com/view_document?document_id=51568)

### 3.6 RZ/N1x Pin IBIS Modeling

With the provided RZ/N1x IBIS models for different device packages, PCB signals driven by the input/output buffers of RZ/N1x devices can be simulated in detail. The signal behavior can be modeled based upon voltage and current curve data, which are derived from measurement results or detailed circuit simulation. The IBIS models can be found in the **TOOLS/IBIS** directory of the RZ/N1x Solution Kit release.

### 3.7 RZ/N1x Pin Boundary Scan Models

With the provided RZ/N1x BSDL models (Boundary Scan Definition Language) the release includes all necessary data for all RZ/N1x devices to set up a Boundary Scan test for the production of the PCB. The BSDL models can be found in the **TOOLS/BSDL** directory of the RZ/N1x Solution Kit release.

### 3.8 RZ/N1x Power Estimation Tool (PET)

With the provided RZ/N1x Power Estimation Tool customer can estimate a rough power consumption under certain RZ/N1x use cases. The PET can be found in the **TOOLS/PowerEstimation** directory of the RZ/N1x Solution Kit release.

**Revision History**

| Rev.  | Date        | Description |  |
|-------|-------------|-------------|--|
|       |             | Page        | Summary  |
| 0.01  | 23.Jul.2017 | -           | Draft  |
| 0.02  | 24.Jul.2017 | -           | First revision   |
| 1.2   | 12.Oct.2017 | -           | Many text additions and improvements<br>Addition of new SW packages available for RZ/N: ThreadX, CODESYS, PRP, HSR, ...<br>Addition of RZ/N1S Solution Kit and adaptation to the Solution Kit version V1.2<br>Overview about used tools for HW and SW Development<br>Graphical additions |
| 1.2.1 | 17.Nov.2017 | -           | Several text improvements  |
| 1.2.2 | 20.Dec.2017 | -           | Different Updates<br>- Added GOAL Support for EtherCAT<br>- IBIS Models for RZ/N1D and RZ/N1S (new)  |
| 1.3   | 06.Feb.2018 | -           | Addition of the RZ/N1L Solution Kit related descriptions<br>Addition of Baremetal Drivers<br>Several updates improvements and corrections  |
| 1.4   | 01.Mar.2018 | -           | Update due to quick start guides creation for RZ/N1D/S/L   |
| 1.5   | 31.Jul.2018 | -           | Update to correspond to Solution Kit v1.3.1  |
| 1.6   | 12.Nov.2018 | -           | Update to correspond to Solution Kit v1.4<br>Added new BSDL features   |
| 1.7   | 15.Mar.2019 | -           | Update to correspond to Solution Kit V1.4.1 with some minor improvements and extensions<br>Added some information regarding ThreadX (limitations, licensing)   |
| 1.8   | 1.Oct.2019  | -           | Removed Solution Kit Version in document header<br>General document updates and Solution Kit adaptations<br>Modified notifications for PRP and HSR<br>Added the Power Estimation Tool in a new chapter<br>FTDI FT_Prog as the new tool version replacing Mprog                           |
| 1.9   | 31.Jan.2020 |             | Changed format   |



## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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