

AMD ZCU102 with Renesas ClockMatrix, ITU-T G.8273.2

Contents

1. Results Summary	2
1.1 Notes on Testing with a Physical Layer Clock	2
2. Test Configuration.....	3
3. G.8273.2: Noise Generation	4
3.1 ONEPPS Analysis	5
3.2 FILTEREDTIMEERROR Analysis	6
3.3 CTE Analysis	7
3.4 DTE Analysis	8
3.5 DTEHF Analysis	9
3.6 DTEMTIE Analysis	10
3.7 DTETDEV Analysis.....	11
4. G.8273.2: Holdover	12
4.1 ONEPPS Analysis	13
4.2 MTIE Analysis.....	14
5. G.8273.2: Noise Generation – No SyncE	15
5.1 ONEPPS Analysis	16
5.2 FILTEREDTIMEERROR Analysis	17
5.3 CTE Analysis	18
5.4 DTE Analysis	19
5.5 DTEHF Analysis	20
5.6 DTEMTIE Analysis	21
5.7 DTETDEV Analysis.....	22
6. G.8273.2: Holdover – No SyncE	23
6.1 TIE Analysis.....	24
7. G.8273.2: Noise Tolerance	25
7.1 ONEPPS Analysis	26
8. G.8273.2: SyncE Transient.....	27
8.1 ONEPPS Analysis	28
8.2 TransientResponse Analysis	29
9. G.8273.2: SyncE to 1PPS Noise Transfer	30
9.1 ONEPPS Analysis	31
9.2 SyncENoiseTransfer Analysis	32
10. G.8273.2: PTP to 1PPS Noise Transfer	33
10.1 ONEPPS Analysis	34
10.2 PTPNoiseTransfer Analysis.....	35
11. Revision History	36

1. Results Summary

Standard	Test Case	Results
G.8273.2	Noise Generation	Pass
G.8273.2	Holdover	Pass
G.8273.2	Noise Generation – No SyncE	N/A
G.8273.2	Holdover – No SyncE	Pass
G.8273.2	Noise Tolerance	Pass
G.8273.2	SyncE Transient	Pass
G.8273.2	SyncE to 1PPS Noise Transfer	Pass
G.8273.2	PTP to 1PPS Noise Transfer	Pass

1.1 Notes on Testing with a Physical Layer Clock

FTS uses a SyncE clock from the test equipment as an additional clock source. A DPLL (configured for ITU-T G.8262 EEC1) is locked to the SyncE source and is connected to the PTP DPLL via the combo bus. For FTS there is no filter on the combo bus connection.

Synced software is used to manage the SyncE clock based on the QL level from the test equipment for tests required a physical layer clock. A category 1 (QL-PRTC) SyncE source from the test equipment is connected to the SyncE input on Clock Matrix and is qualified before PTP (PCM4L/PTP4I) is started.

2. Test Configuration

Table 1. Test Configuration 1

Device Under Test	AMD + CM
Oscillator	Rakon E6241LF TCXO
1pps Source	Symmetricom TP5000
Instrument	Paragon Neo
Instrument Serial Number	00036081
Ethernet Interface	Optical

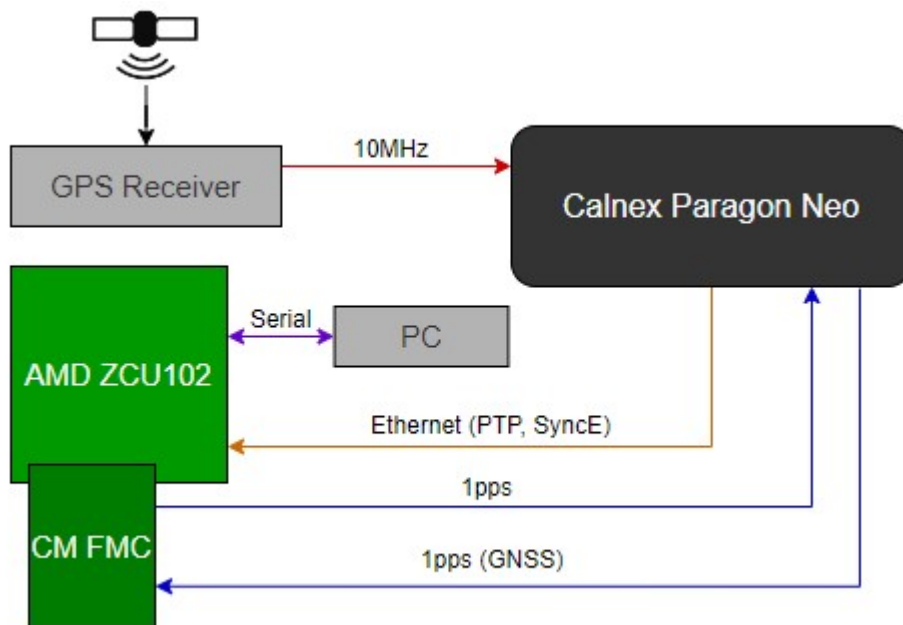


Figure 1. Equipment Configuration 1

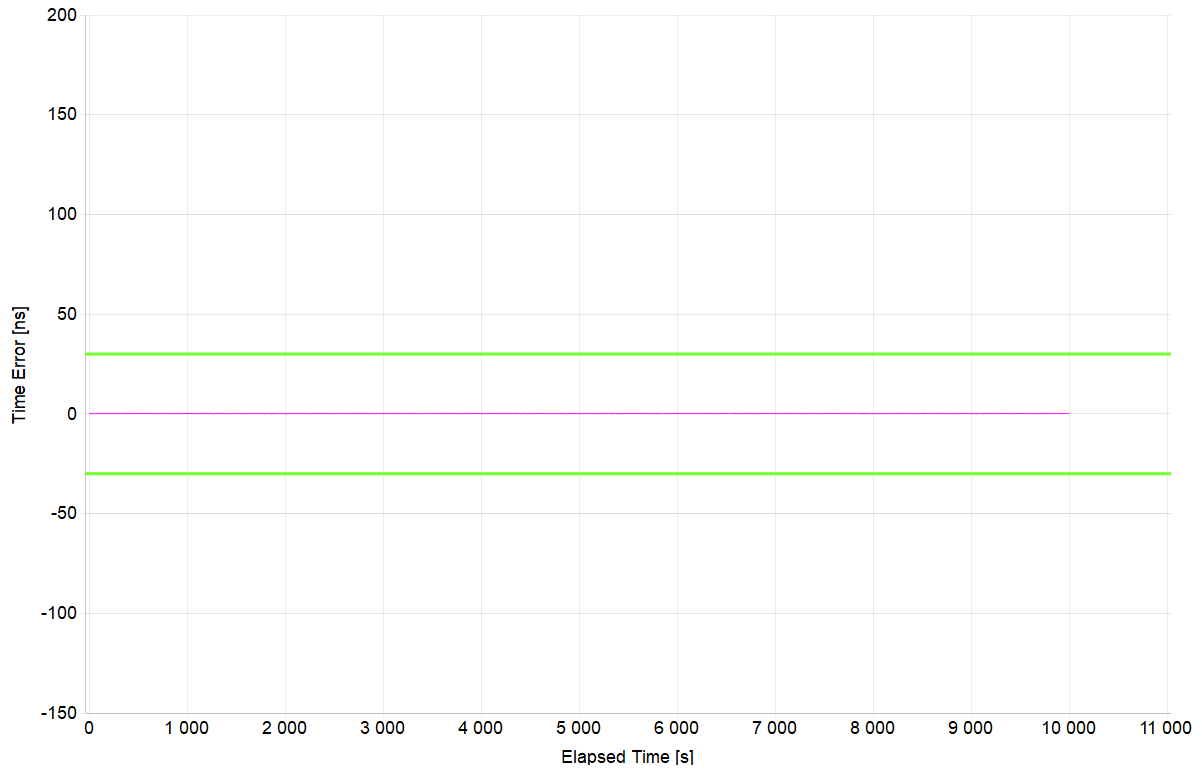
3. G.8273.2: Noise Generation

Test Description	Noise Generation
Report Date	22-10-18_08-30-41
Packet Rate (pkt/s)	16
Test Duration	02:46:40
Time to Phase Lock (s)	16

All Mask Results	Pass
Mask ONEPPS	0.03μs
Mask ONEPPS Result	Pass
Mask FILTEREDTIMEERROR	0.005μs
Mask FILTEREDTIMEERROR Result	Pass
Mask CTE	0.01μs
Mask CTE Result	Pass
Mask DTE	0.01μs
Mask DTE Result	Pass
Mask DTEHF	0.07μs
Mask DTEHF Result	Pass
Mask DTEMTIE	G.8273.2 T-BC Provisional Class D Dynamic TE LF Const. Temp.
Mask DTEMTIE Result	Pass
Mask DTETDEV	G.8273.2 T-BC Provisional Class D Dynamic TE LF Const. Temp.
Mask DTETDEV Result	Pass

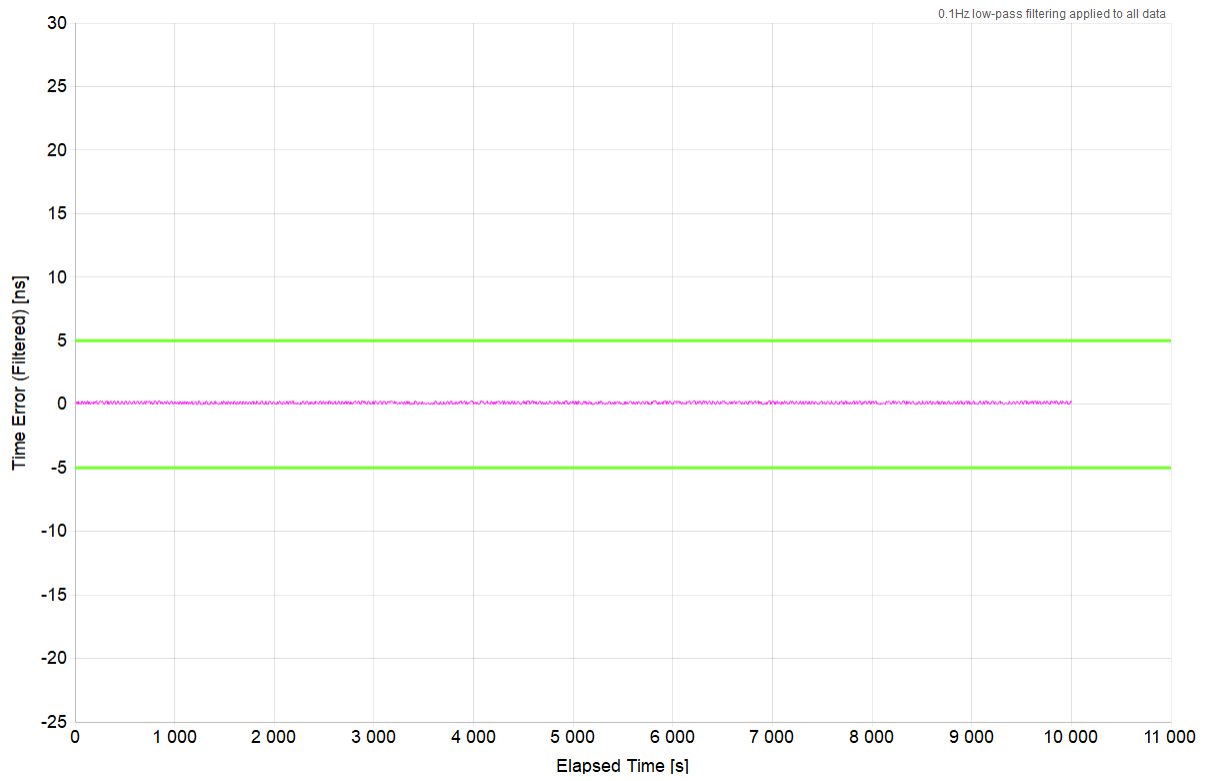
3.1 ONEPPS Analysis

Offset Removal Applied	On
Zero Offset	0ns



Mean [ns]	0.109
Min [ns]	-0.25
Max [ns]	0.25
Max-Min [ns]	0.5

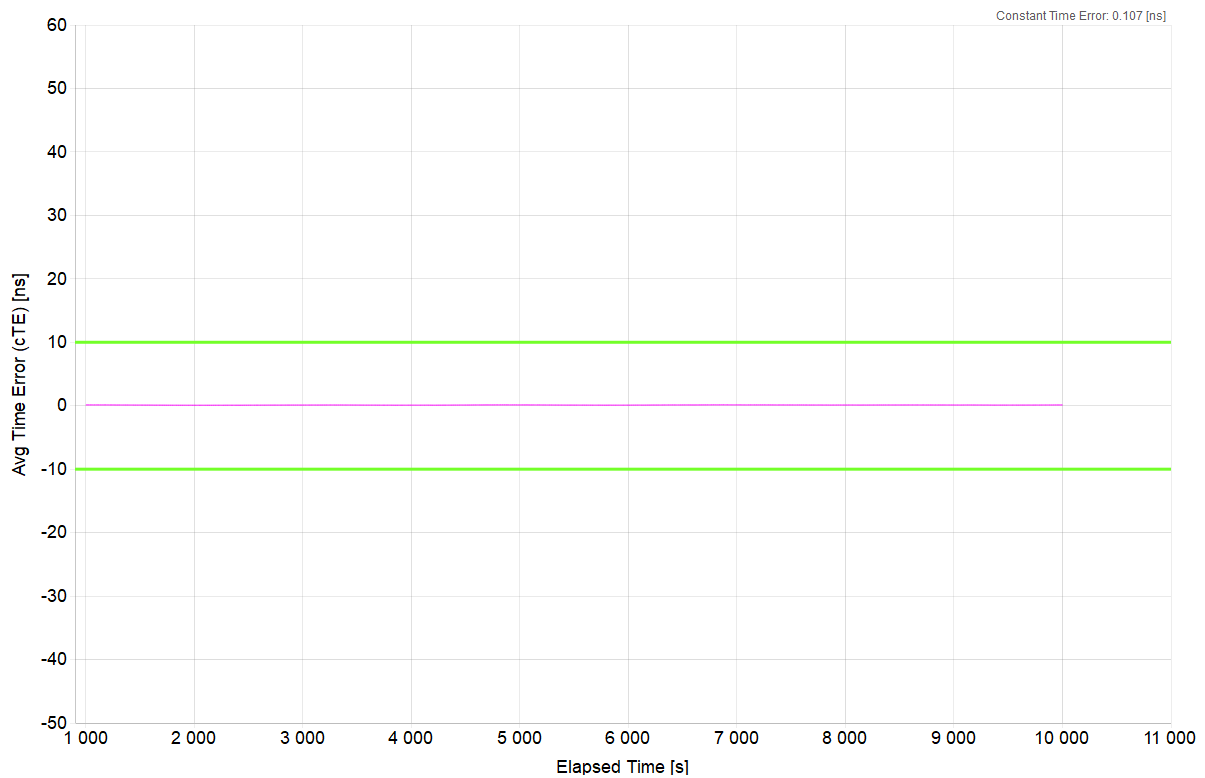
3.2 FILTEREDTIMEERROR Analysis



Mean [ns]	0.109
Min [ns]	-0.045
Max [ns]	0.25
Max-Min [ns]	0.295

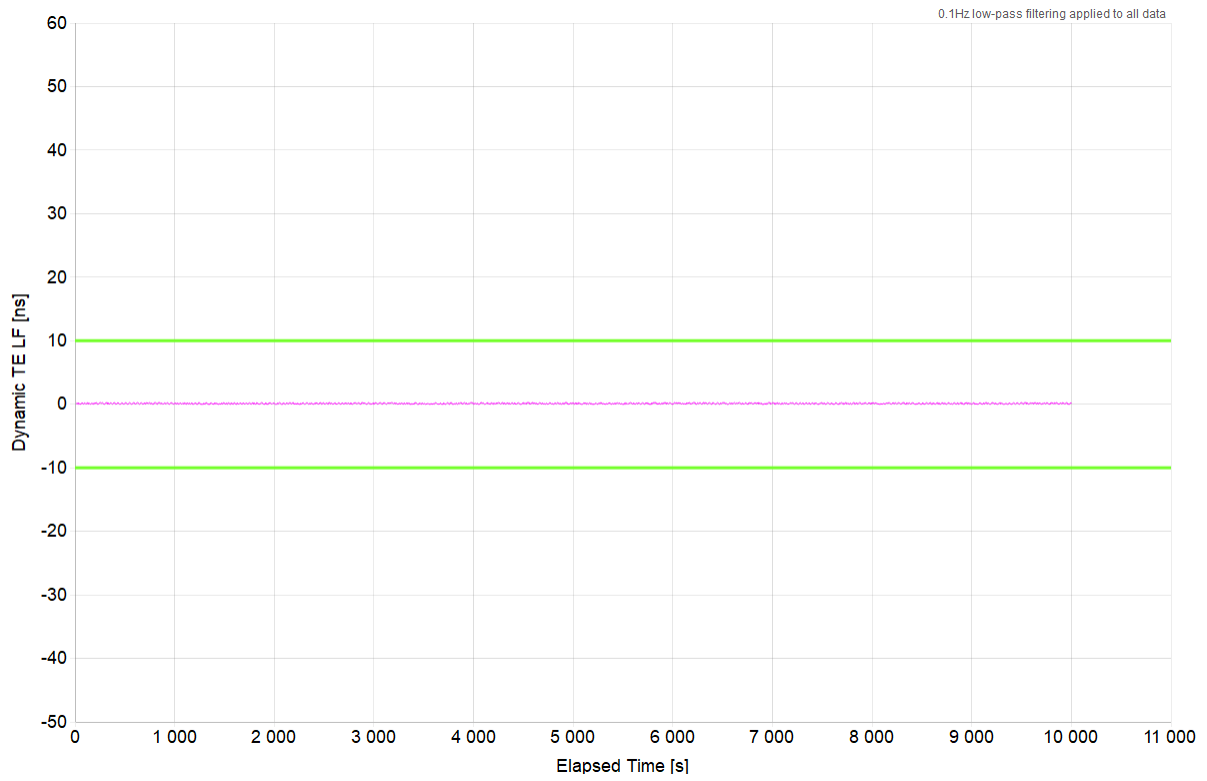
3.3 CTE Analysis

Averaging Time (s)	1000
---------------------------	------



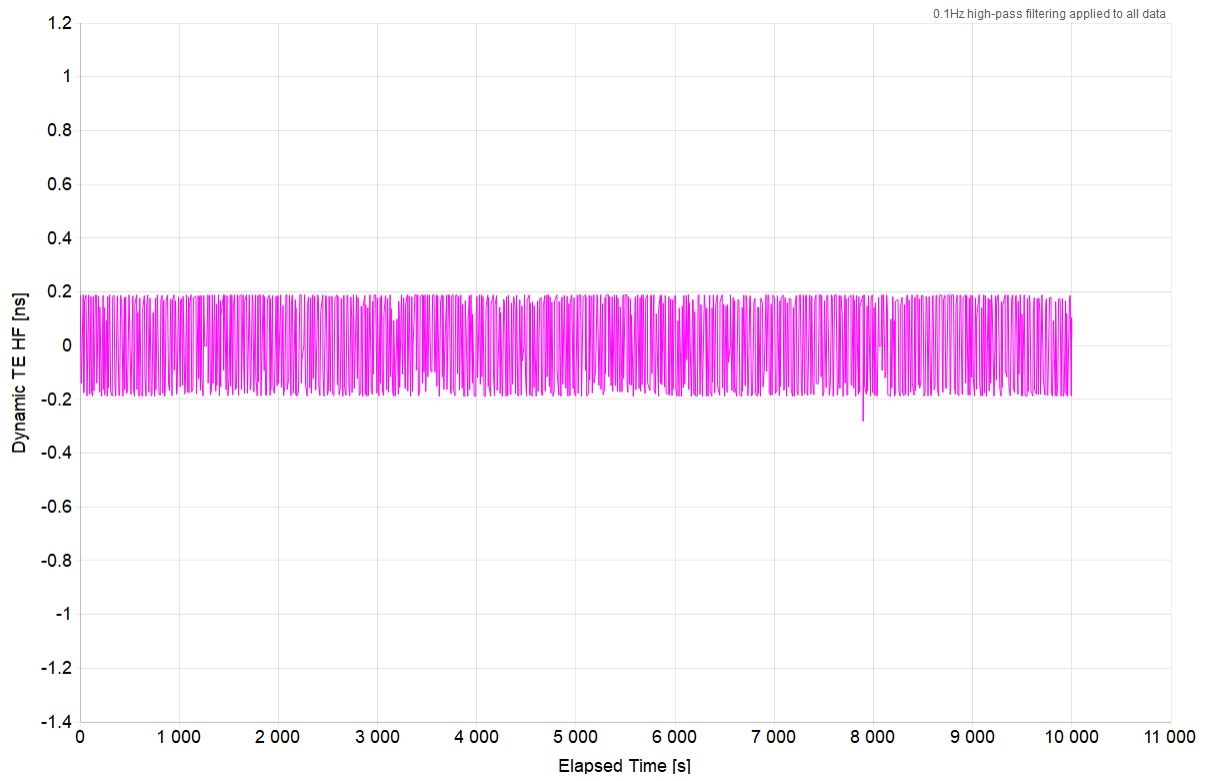
Constant Time Error [ns]	0.107
Min [ns]	0.08
Max [ns]	0.135
Max-Min [ns]	0.056

3.4 DTE Analysis



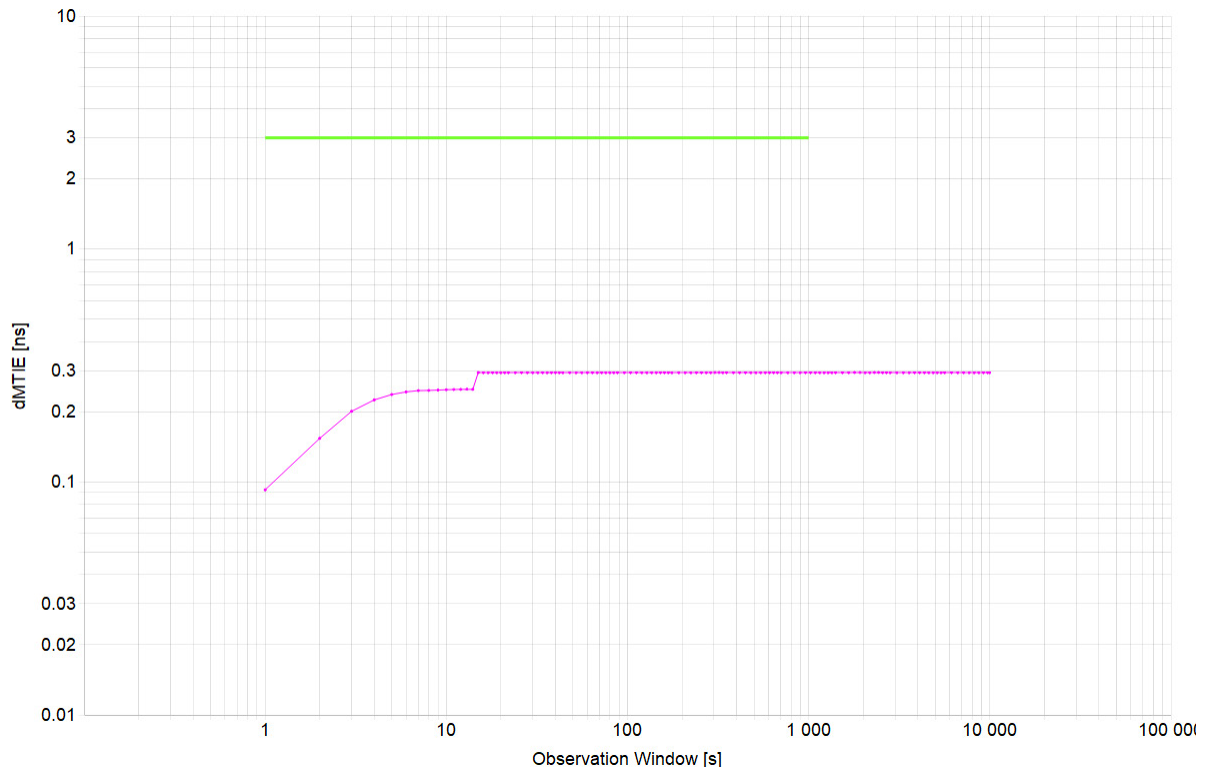
Mean [ns]	0.109
Min [ns]	-0.045
Max [ns]	0.25
Max-Min [ns]	0.295

3.5 DTEHF Analysis



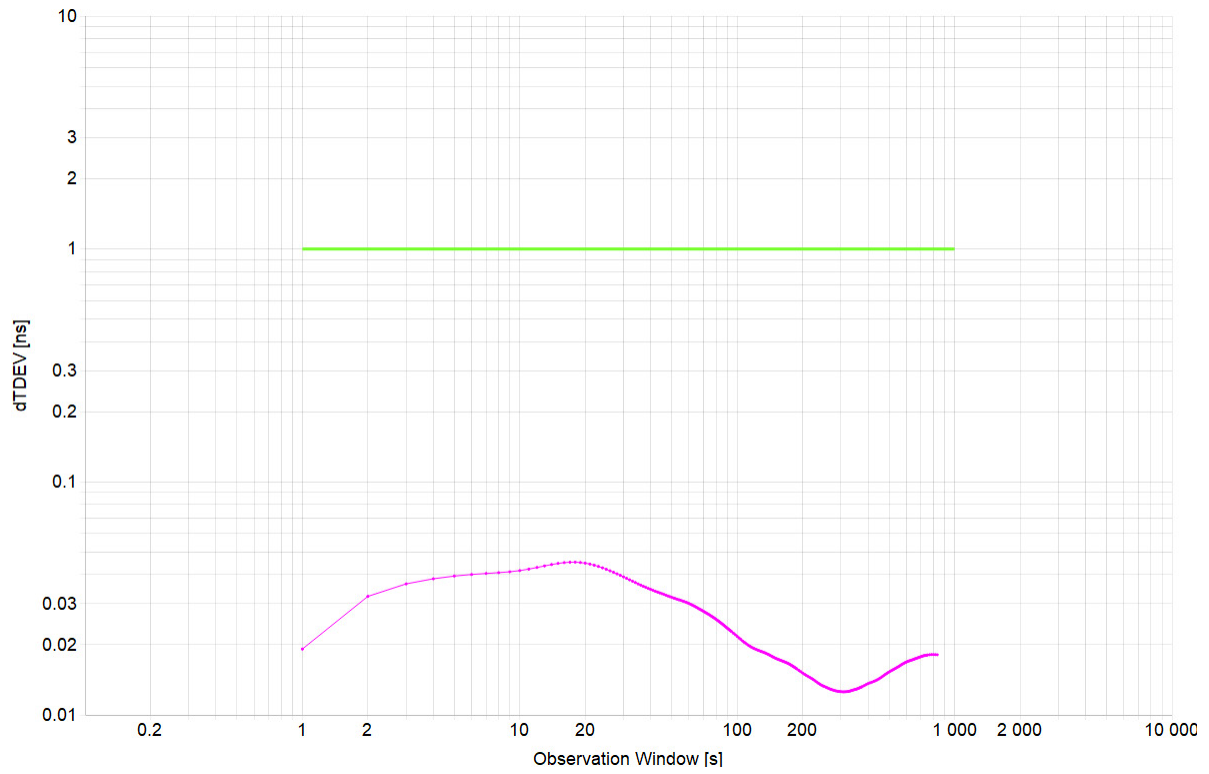
Mean [ns]	0
Min [ns]	-0.282
Max [ns]	0.189
Max-Min [ns]	0.471

3.6 DTEMTIE Analysis



Min [ns]	0.093
Max [ns]	0.295
Max-Min [ns]	0.202

3.7 DTETDEV Analysis



Min [ns]	0.013
Max [ns]	0.045
Max-Min [ns]	0.033

4. G.8273.2: Holdover

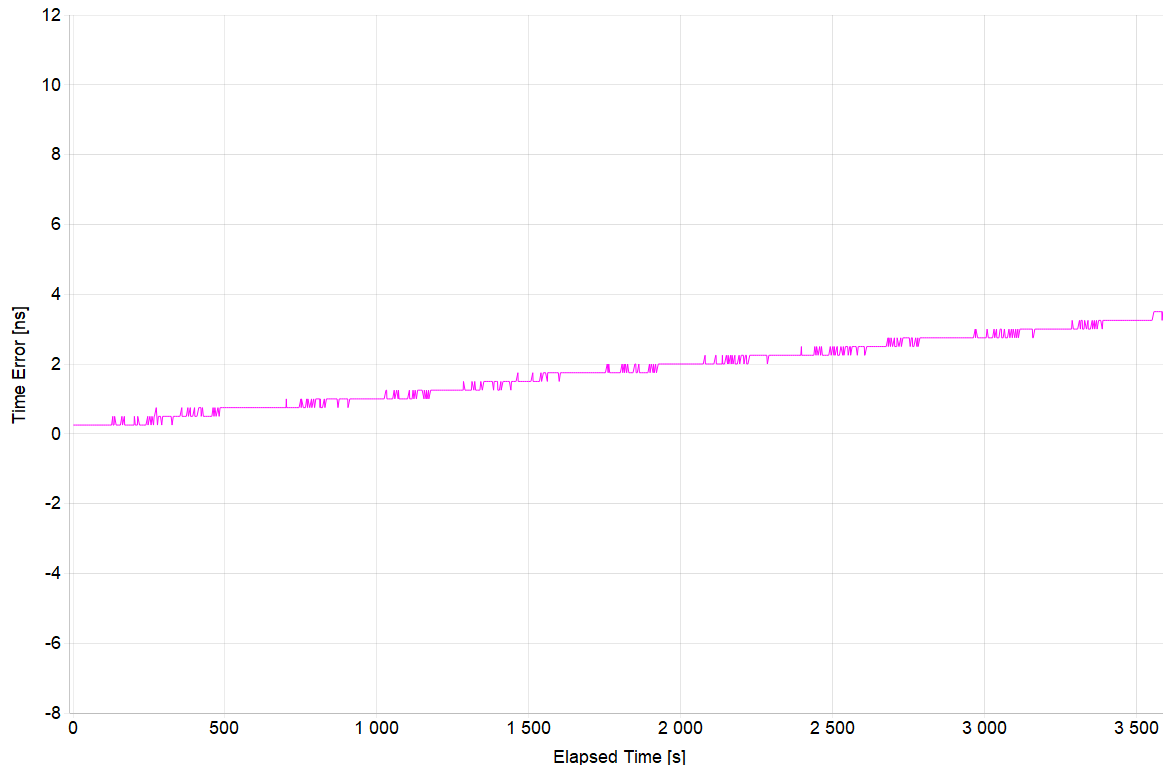
Test Description	Holdover
Report Date	22-10-18_08-30-41
Packet Rate (pkt/s)	16
Test Duration	00:59:57
Time to Phase Lock (s)	N/A

All Mask Results	Pass
Mask ONEPPS	-
Mask ONEPPS Result	No Mask
Mask MTIE	G.8273.2 T-BC Class B Time Holdover Const. Temp.
Mask MTIE Result	Pass

1. This test is a continuation of the previous Noise Generation test. This allows for an appropriate amount of settling time before collecting holdover data (10 000s). The results are split because holdover requires a different mask than noise generation.

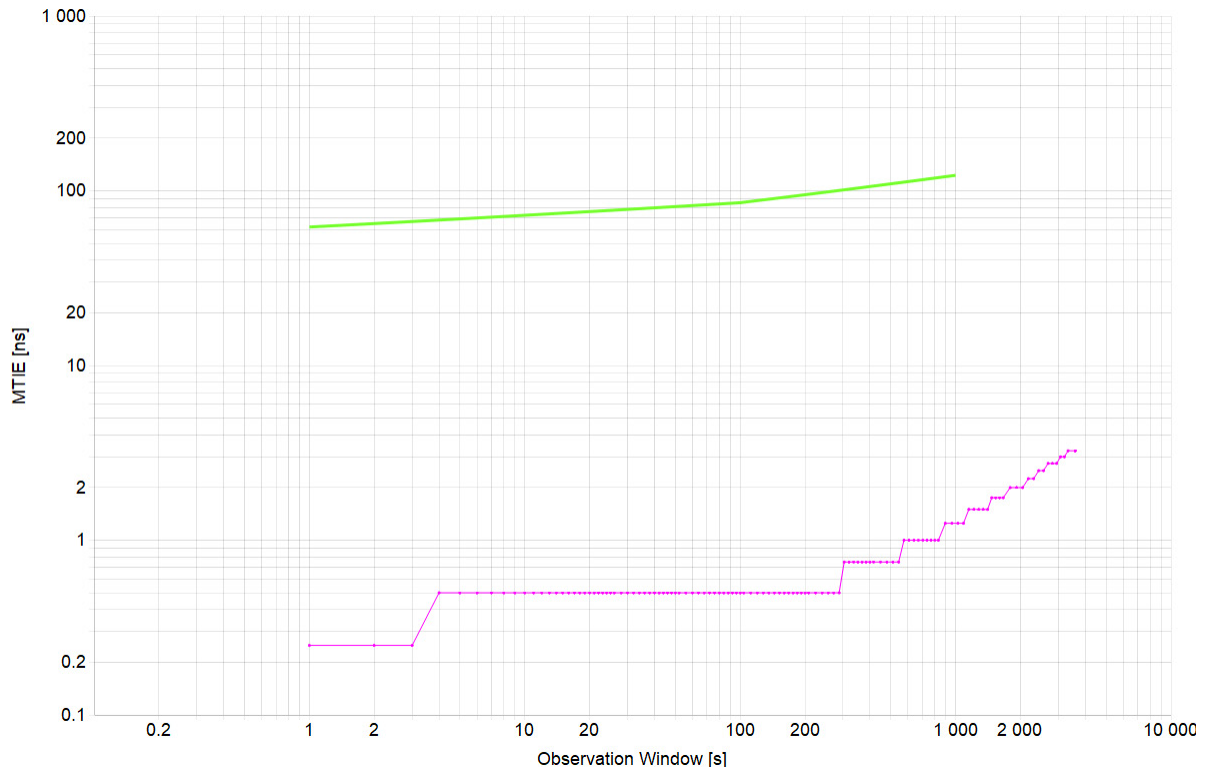
4.1 ONEPPS Analysis

Offset Removal Applied	Off
Zero Offset	0.25ns



Mean [ns]	1.777
Min [ns]	0.25
Max [ns]	3.5
Max-Min [ns]	3.25

4.2 MTIE Analysis



Min [ns]	0.25
Max [ns]	3.25
Max-Min [ns]	3

5. G.8273.2: Noise Generation – No SyncE

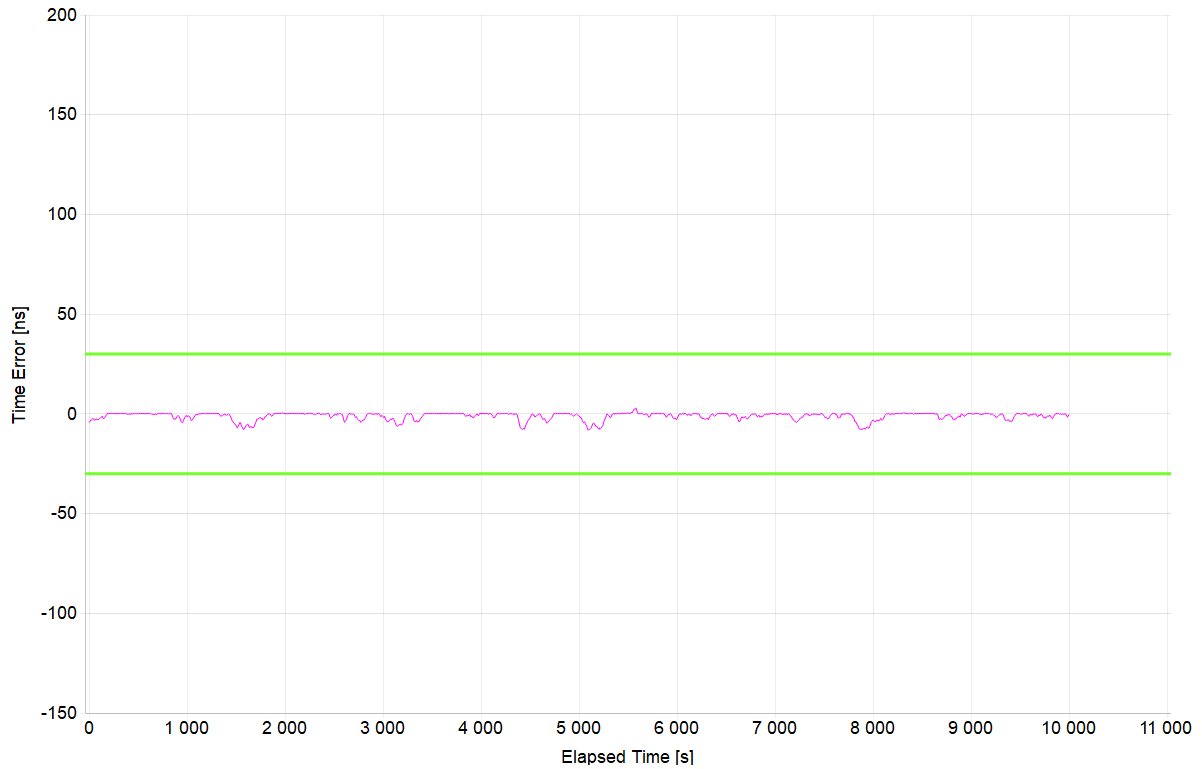
Test Description	Noise Generation – No SyncE
Report Date	22-10-18_08-30-41
Packet Rate (pkt/s)	16
Test Duration	02:46:40
Time to Phase Lock (s)	13

All Mask Results	N/A
Mask ONEPPS	0.03μs
Mask ONEPPS Result	Pass
Mask FILTEREDTIMEERROR	0.005μs
Mask FILTEREDTIMEERROR Result	Fail
Mask CTE	0.01μs
Mask CTE Result	Pass
Mask DTE	0.01μs
Mask DTE Result	Pass
Mask DTEHF	0.07μs
Mask DTEHF Result	Pass
Mask DTEMTIE	G.8273.2 T-BC Class C Dynamic TE LF Const. Temp.
Mask DTEMTIE Result	Fail
Mask DTETDEV	G.8273.2 T-BC Class C Dynamic TE LF Const. Temp.
Mask DTETDEV Result	Pass

1. Class C Masks are provided as a reference. This test is not covered by ITU-T G.8273.2 as it does not use a physical layer reference. Results are dependent on the oscillator performance.

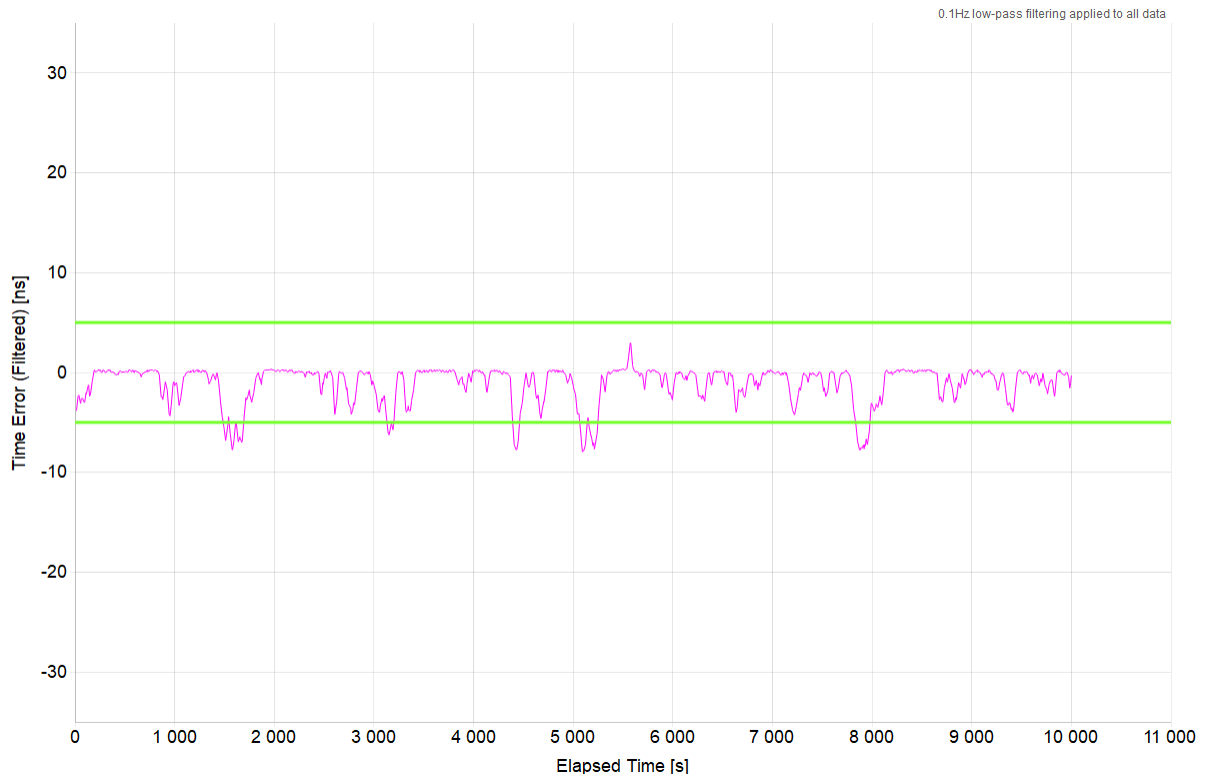
5.1 ONEPPS Analysis

Offset Removal Applied	Off
Zero Offset	-4ns



Mean [ns]	-1.145
Min [ns]	-8
Max [ns]	3
Max-Min [ns]	11

5.2 FILTEREDTIMEERROR Analysis



Mean [ns]	-1.141
Min [ns]	-7.939
Max [ns]	2.964
Max-Min [ns]	10.903

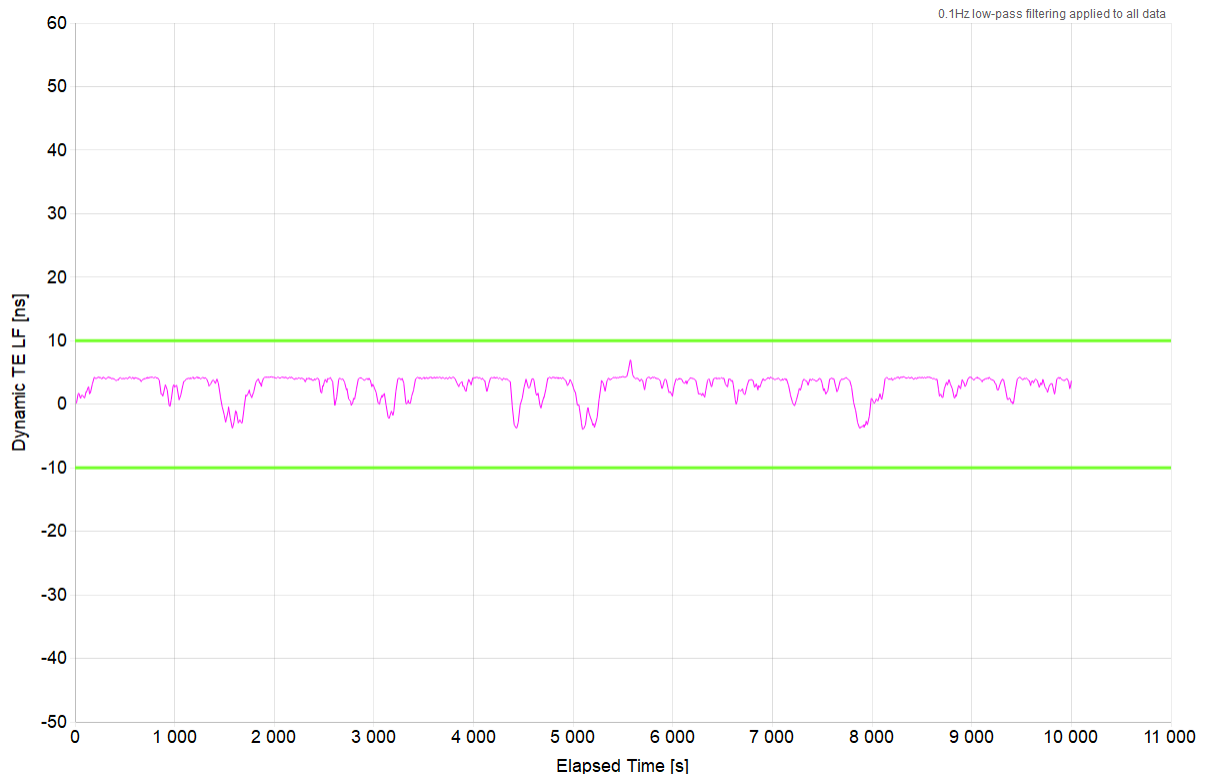
5.3 CTE Analysis

Averaging Time (s)	1000
---------------------------	------



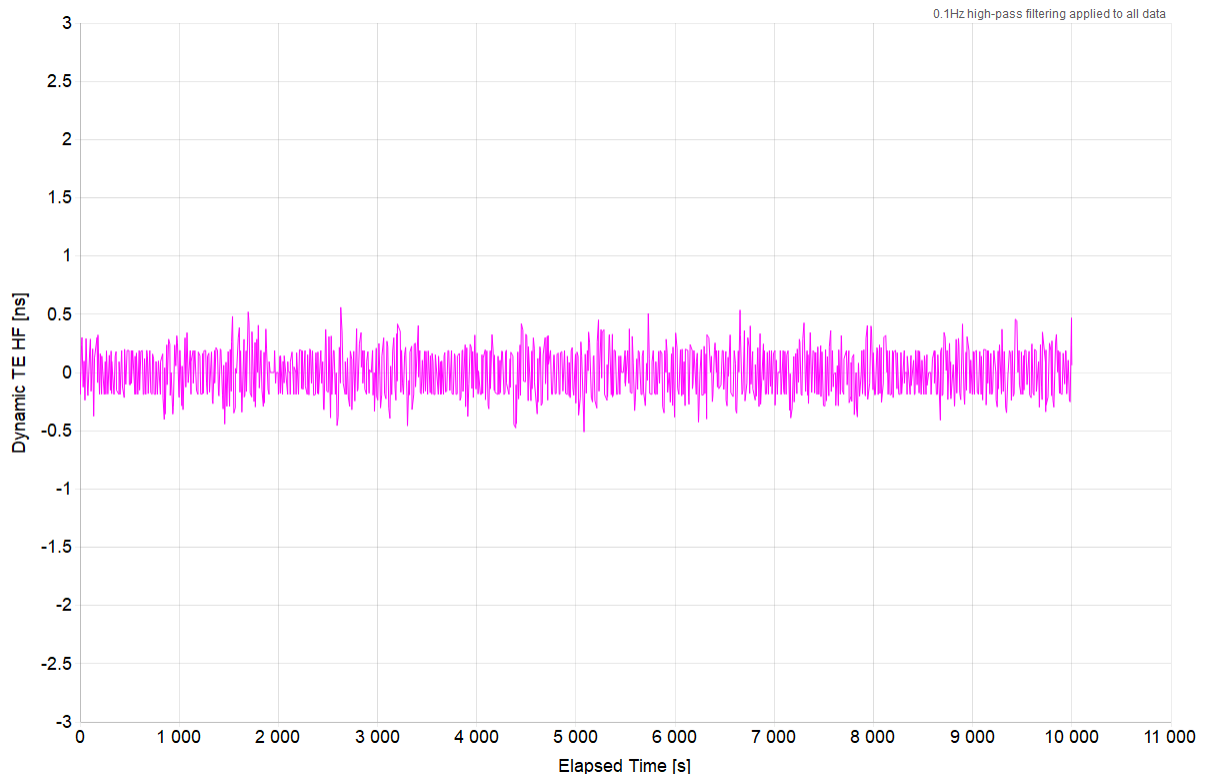
Constant Time Error [ns]	-1.185
Min [ns]	-2.681
Max [ns]	-0.199
Max-Min [ns]	2.482

5.4 DTE Analysis



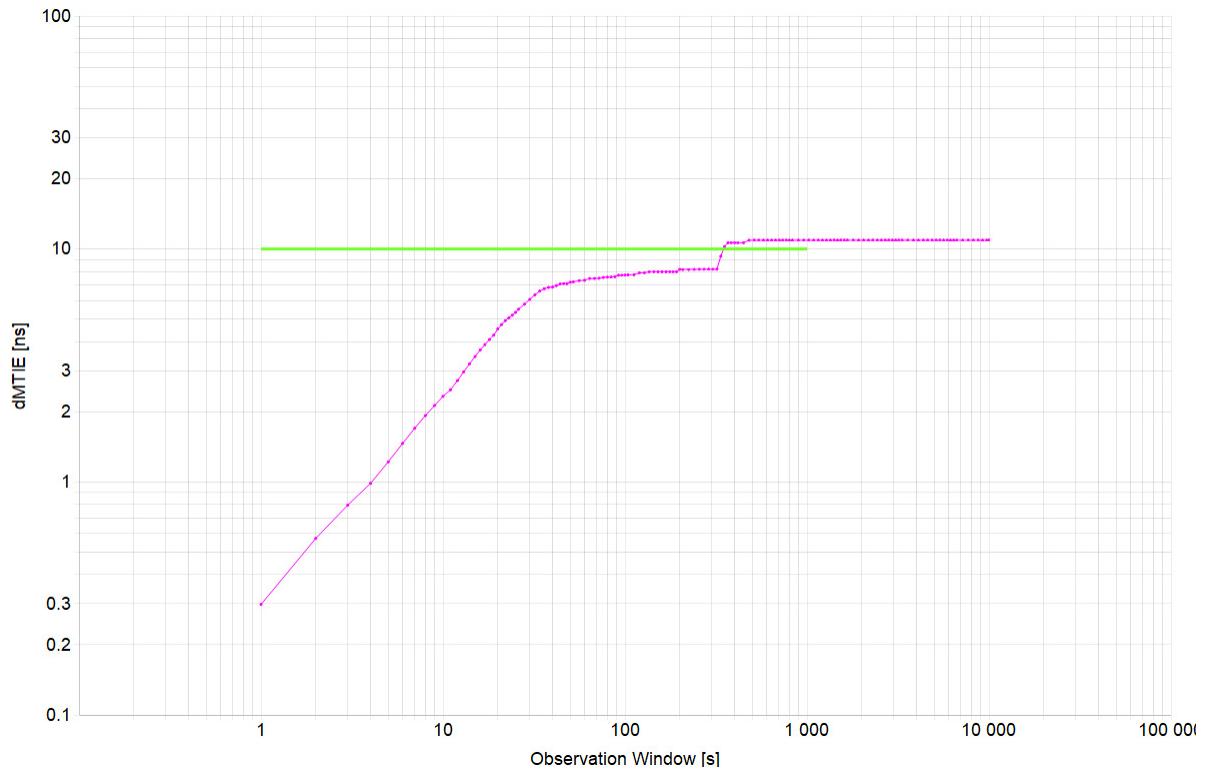
Mean [ns]	2.859
Min [ns]	-3.939
Max [ns]	6.964
Max-Min [ns]	10.903

5.5 DTEHF Analysis



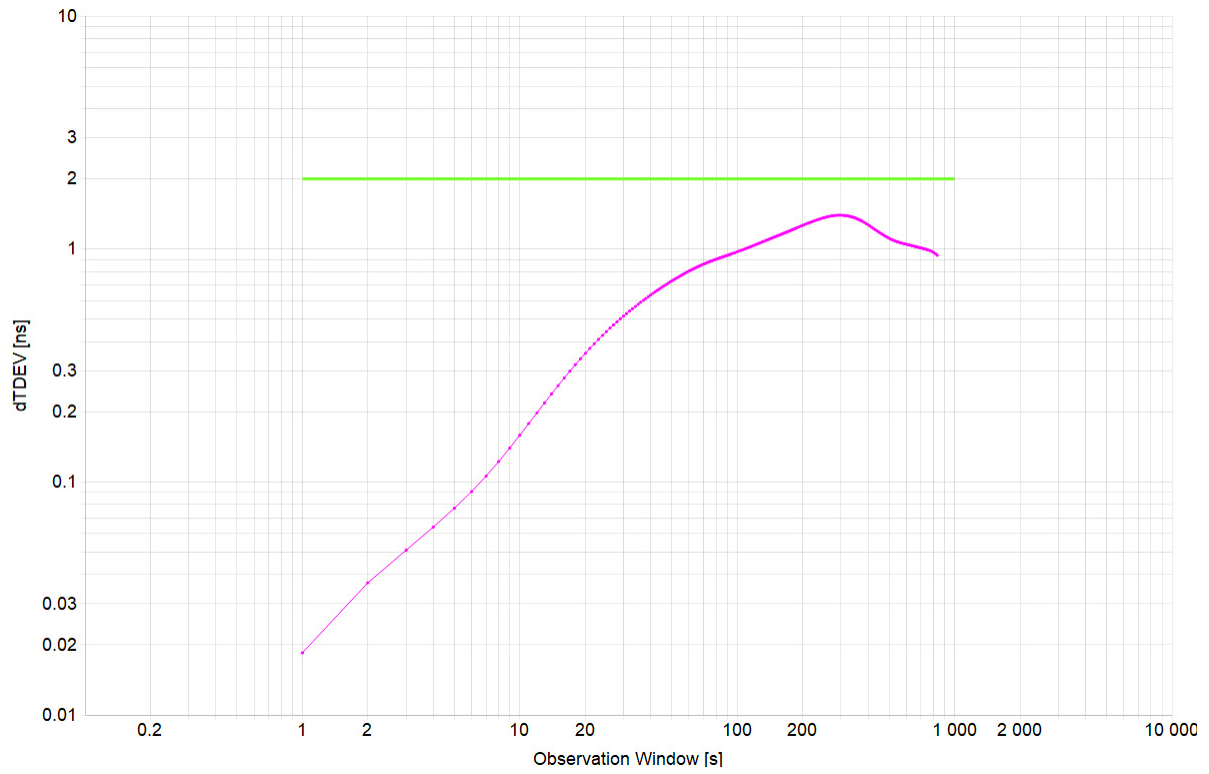
Mean [ns]	0.001
Min [ns]	-0.511
Max [ns]	0.56
Max-Min [ns]	1.07

5.6 DTEMTIE Analysis



Min [ns]	0.298
Max [ns]	10.903
Max-Min [ns]	10.605

5.7 DTETDEV Analysis



Min [ns]	0.018
Max [ns]	1.396
Max-Min [ns]	1.378

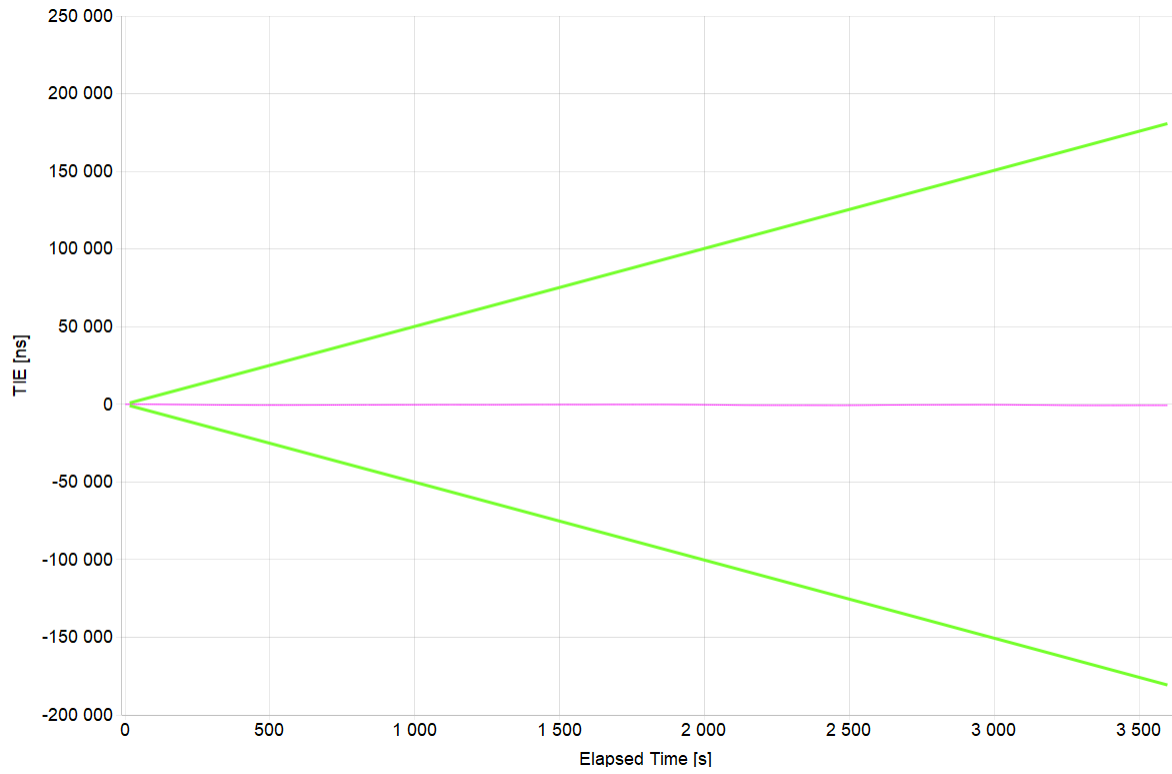
6. G.8273.2: Holdover – No SyncE

Test Description	Holdover – No SyncE
Report Date	22-10-18_08-30-41
Packet Rate (pkt/s)	16
Test Duration	00:59:57
Time to Phase Lock (s)	N/A

All Mask Results	Pass
Mask TIE	G.8262 EEC Opt. 1 Long-Term Holdover Const. Temp.
Mask TIE Result	Pass

1. This test is a continuation of the previous Noise Generation test. This allows for an appropriate amount of settling time before collecting holdover data (10 000s). The results are split because holdover requires a different mask than noise generation.

6.1 TIE Analysis



Mean [ns]	-408.212
Min [ns]	-744.25
Max [ns]	4.75
Max-Min [ns]	749

7. G.8273.2: Noise Tolerance

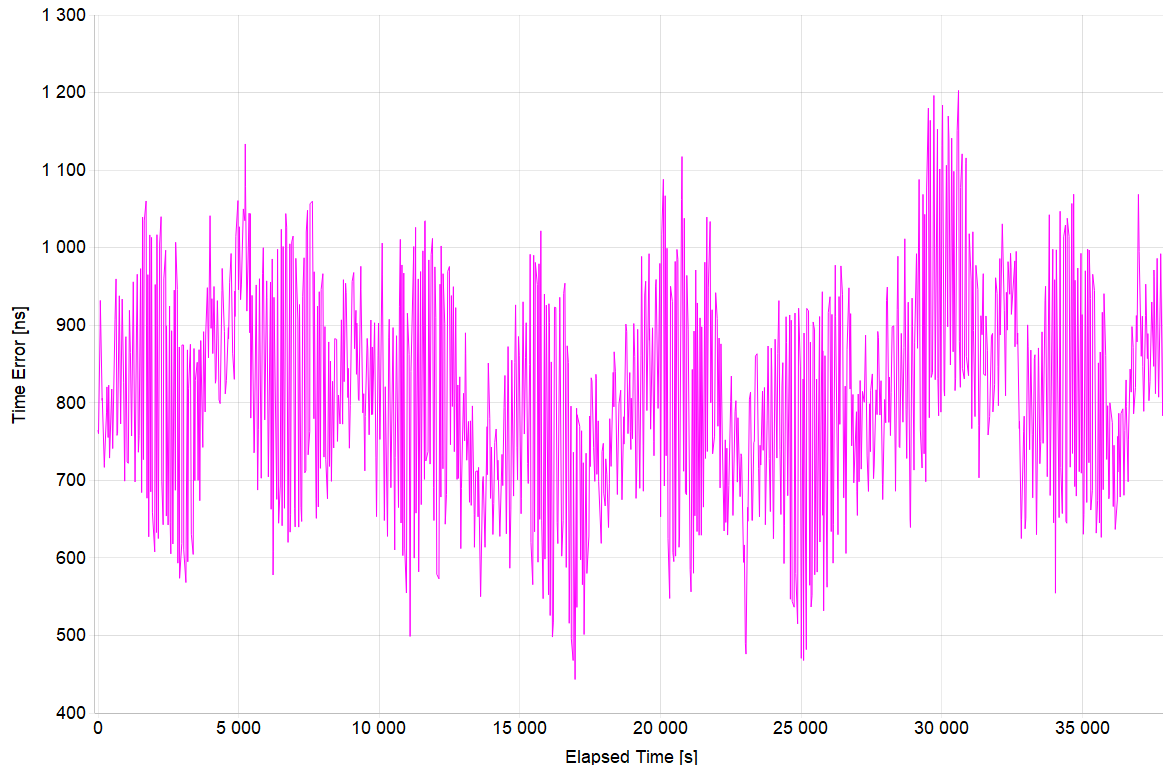
Test Description	Noise Tolerance
Report Date	23-03-07_08-22-53
Packet Rate (pkt/s)	16
Test Duration	10:33:17
Time to Phase Lock (s)	14

All Mask Results	Pass
Mask ONEPPS	-
Mask ONEPPS Result	No Mask

1. This test requires noise on both the PTP and SyncE sources. The PTP noise is the ITU-T G 8271.1 FTS pdv pattern provided by Calnex. The SyncE noise source is the noise tolerance wander table repeated throughout the length of the PTP pdv pattern. This is the same pattern used in Section 9 G.8273.2 SyncE to 1PPS Noise Transfer.

7.1 ONEPPS Analysis

Offset Removal Applied	Off
Zero Offset	764.697ns



Mean [ns]	811.069
Min [ns]	443.197
Max [ns]	1202.697
Max-Min [ns]	759.5

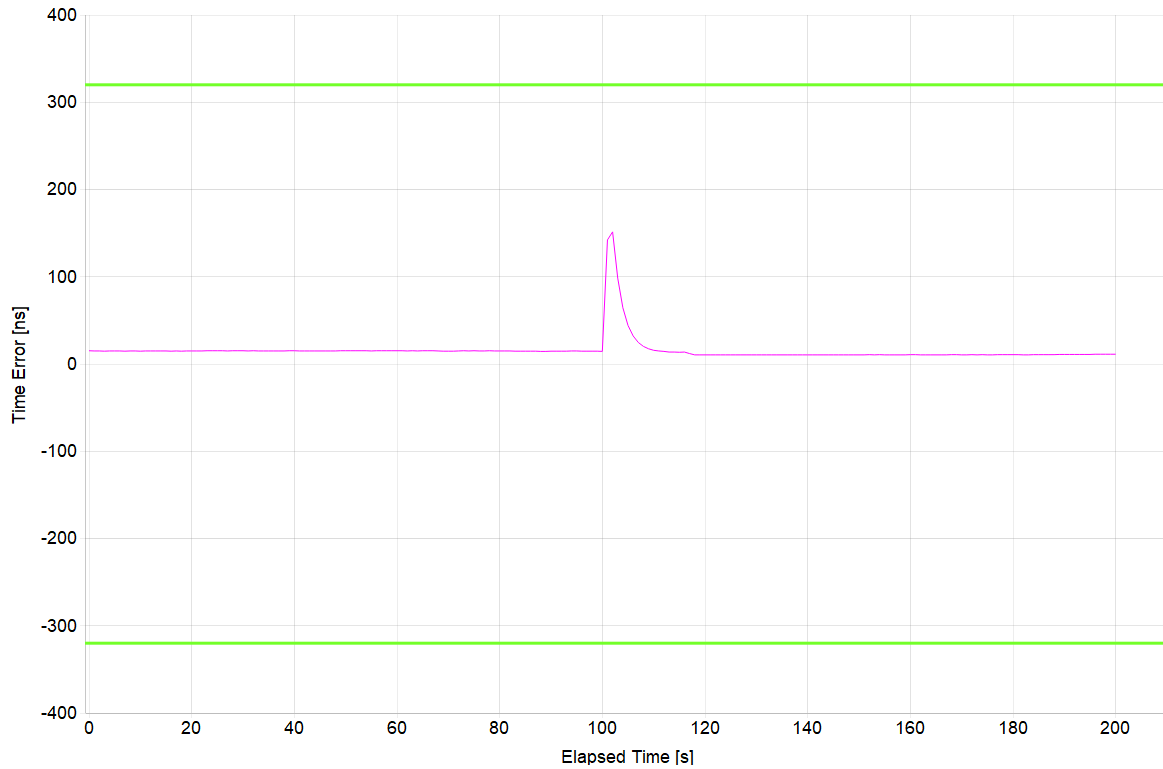
8. G.8273.2: SyncE Transient

Test Description	SyncE Transient
Report Date	22-10-18_08-30-41
Packet Rate (pkt/s)	16
Test Duration	00:03:20
Time to Phase Lock (s)	15

All Mask Results	Pass
Mask ONEPPS	0.32μs
Mask ONEPPS Result	Pass
Mask TransientResponse	G.8273.2 Phase Error
Mask TransientResponse Result	Pass

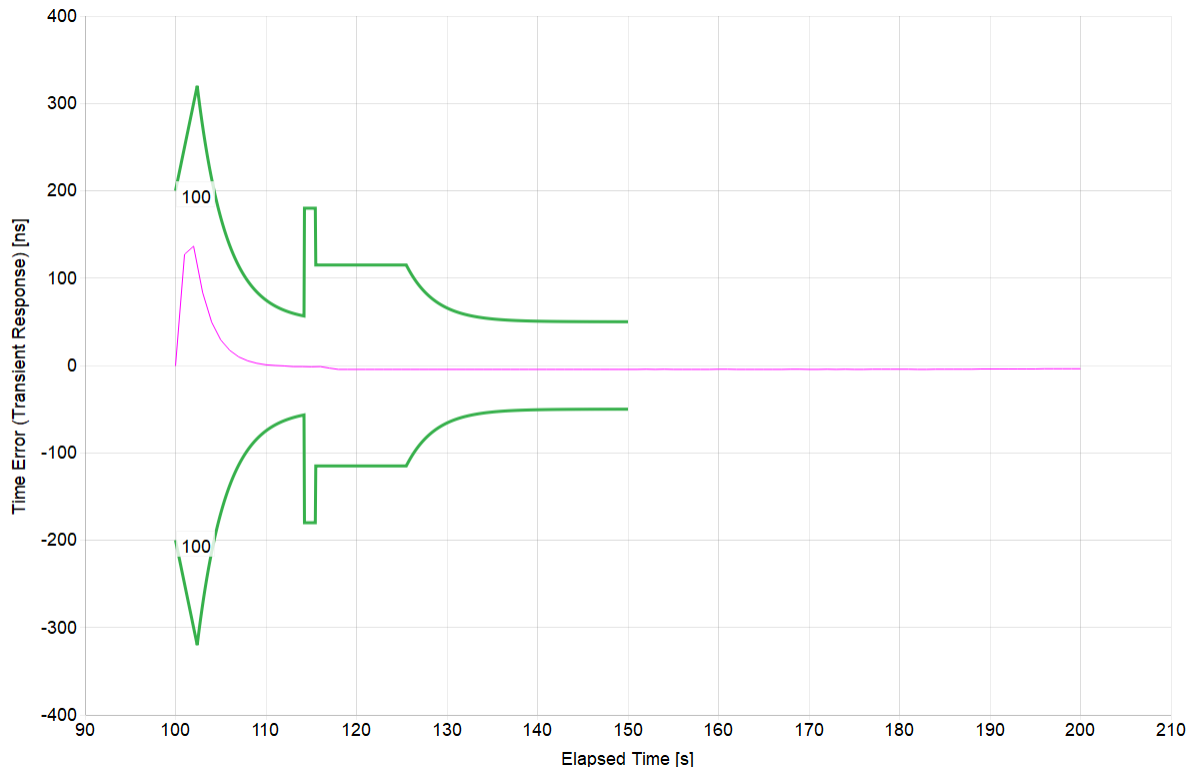
8.1 ONEPPS Analysis

Offset Removal Applied	Off
Zero Offset	15.197ns



Mean [ns]	15.403
Min [ns]	10.447
Max [ns]	151.447
Max-Min [ns]	141

8.2 TransientResponse Analysis



Mean [ns]	0.884
Min [ns]	-4.512
Max [ns]	136.488
Max-Min [ns]	141

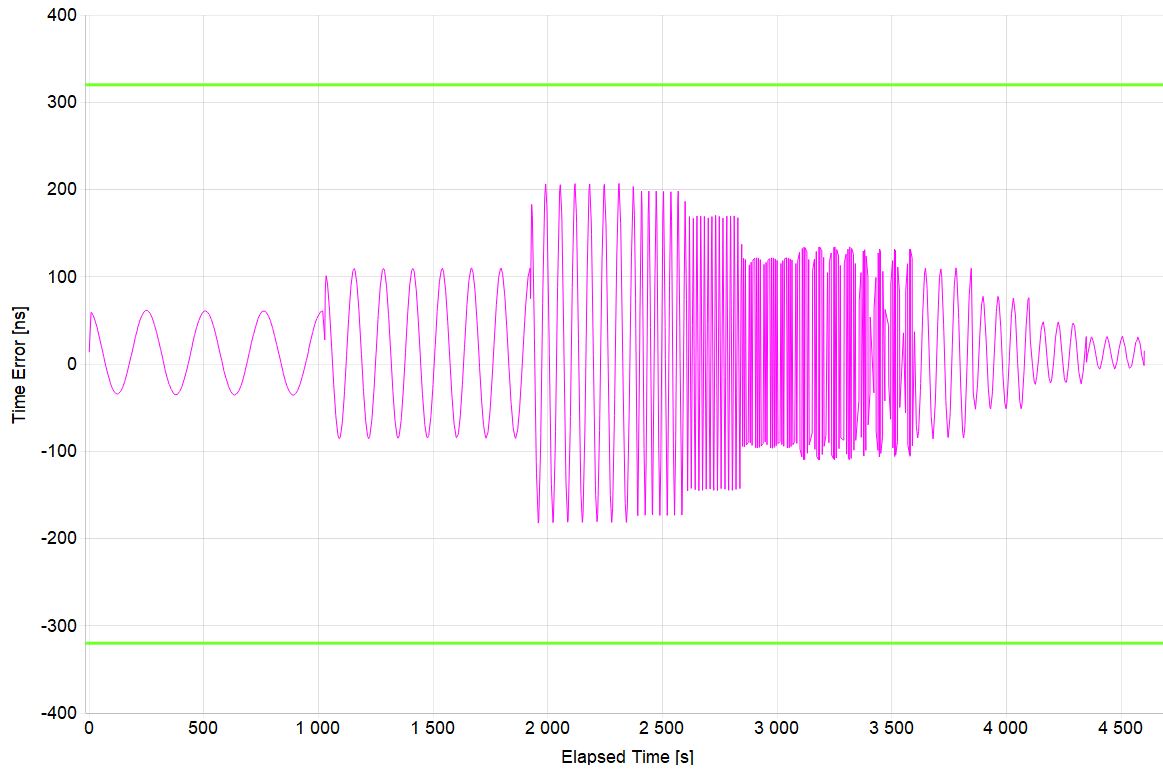
9. G.8273.2: SyncE to 1PPS Noise Transfer

Test Description	SyncE to 1PPS Noise Transfer
Report Date	22-10-18_08-30-41
Packet Rate (pkt/s)	16
Test Duration	01:16:41
Time to Phase Lock (s)	15

All Mask Results	Pass
Mask ONEPPS	0.32μs
Mask ONEPPS Result	Pass
Mask SyncENoiseTransfer	G.8273.2 Class A,B T-BCs Noise Transfer
Mask SyncENoiseTransfer Result	Pass

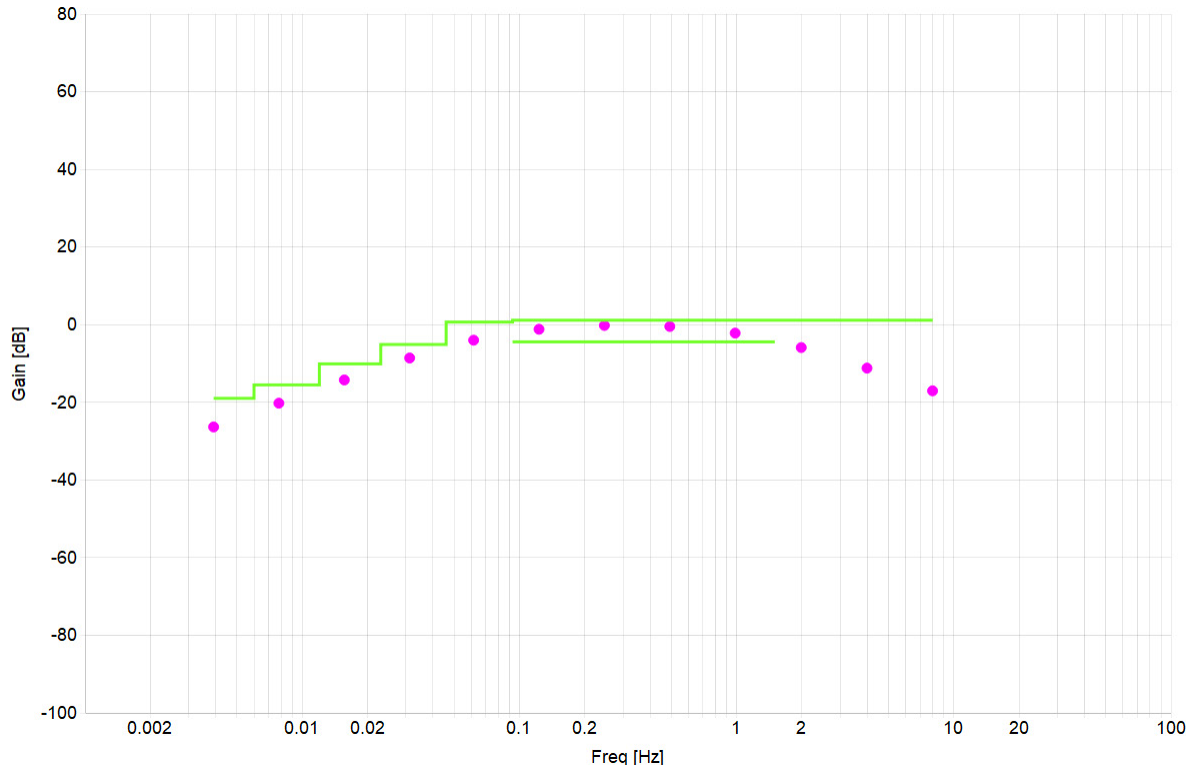
9.1 ONEPPS Analysis

Offset Removal Applied	Off
Zero Offset	13.947ns



Mean [ns]	12.232
Min [ns]	-182.303
Max [ns]	206.947
Max-Min [ns]	389.25

9.2 SyncNoiseTransfer Analysis



Point #	Freq (Hz)	Ampl (ns)	Duration (s)	Pk-Pk Output (ns)	Gain (dB)	Upper Pk-Pk Limit (ns)	Lower Pk-Pk Limit (ns)
1	0.00391	2000	1023.02	96.27	-26.35	225	-
2	0.00781	2000	896.29	194.88	-20.23	340	-
3	0.01563	2000	447.86	387.75	-14.25	630	-
4	0.03125	1000	224.00	371.75	-8.59	565	-
5	0.06156	500	243.66	315.10	-4.01	545	-
6	0.12313	250	251.77	218.05	-1.19	285	150
7	0.24625	250	251.78	243.98	-0.21	285	150
8	0.4925	250	249.75	236.89	-0.47	285	150
9	0.985	250	249.75	194.53	-2.18	285	150
10	1.985	250	249.87	126.74	-5.90	285	-
11	3.985	250	249.94	68.89	-11.20	285	-
12	7.985	250	249.97	35.15	-17.04	285	-

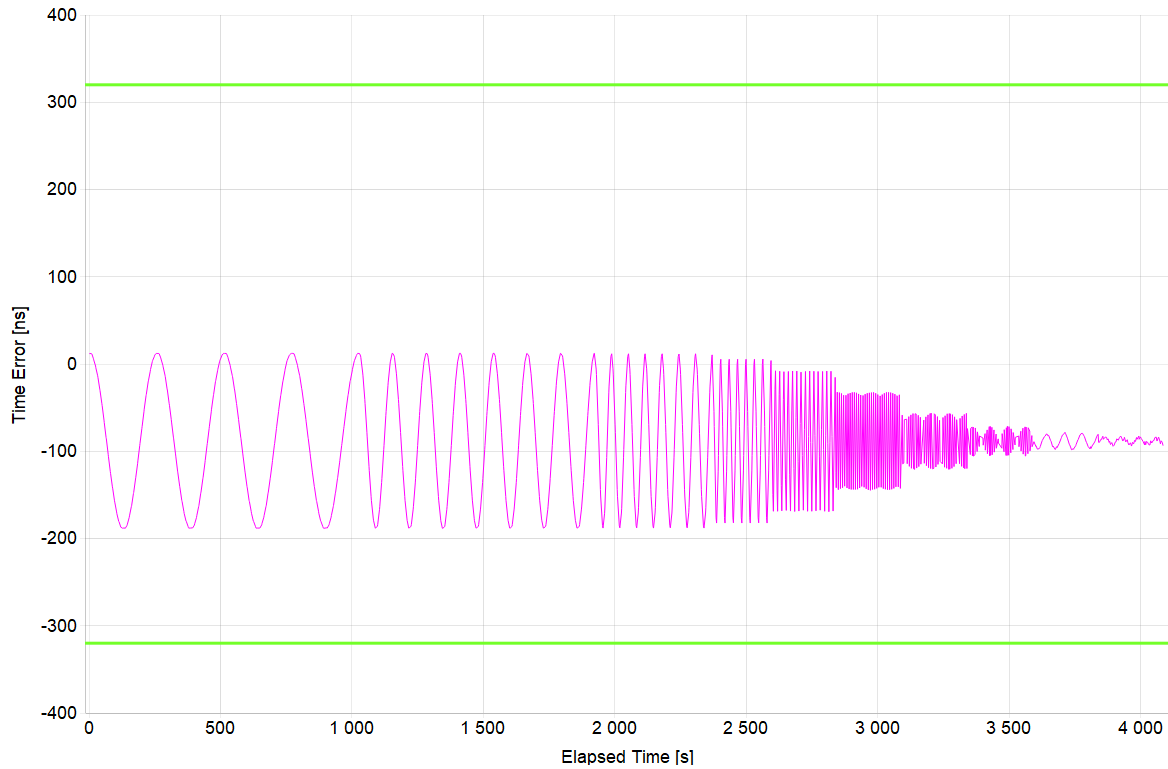
10. G.8273.2: PTP to 1PPS Noise Transfer

Test Description	PTP to 1PPS Noise Transfer
Report Date	22-10-18_08-30-41
Packet Rate (pkt/s)	16
Test Duration	01:08:04
Time to Phase Lock (s)	16

All Mask Results	Pass
Mask ONEPPS	0.32μs
Mask ONEPPS Result	Pass

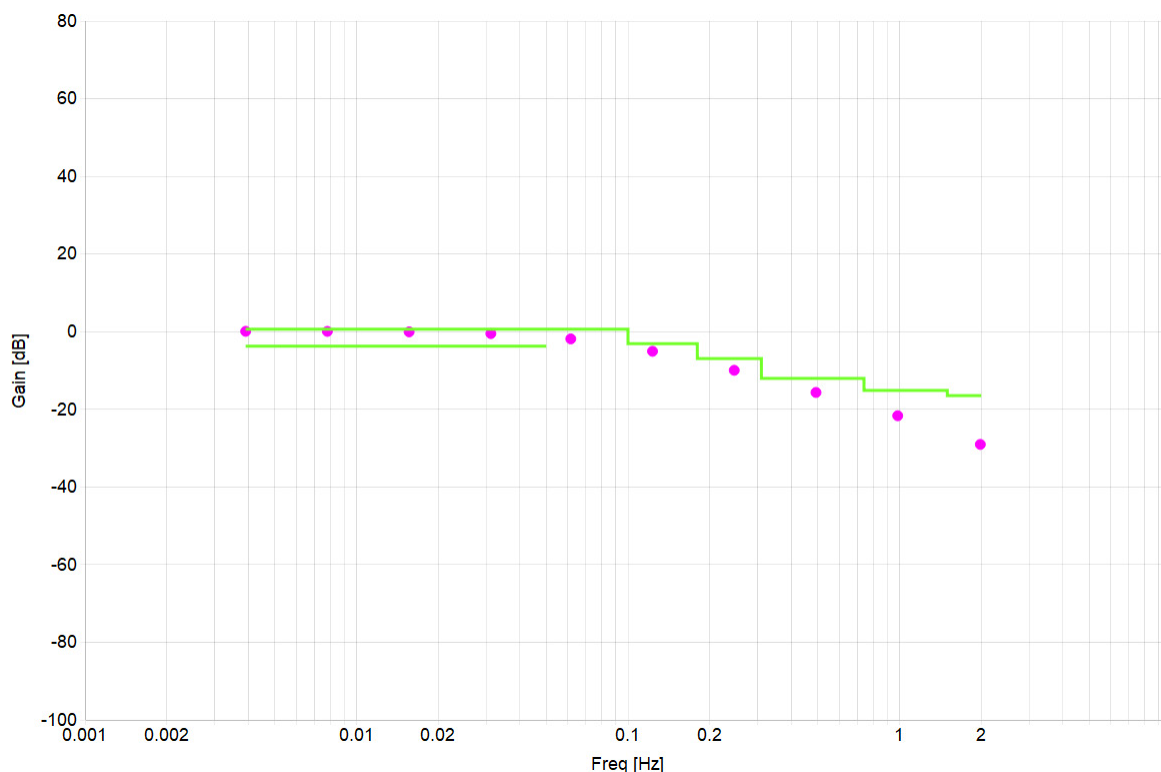
10.1 ONEPPS Analysis

Offset Removal Applied	Off
Zero Offset	11.947ns



Mean [ns]	-88.362
Min [ns]	-188.303
Max [ns]	12.197
Max-Min [ns]	200.5

10.2 PTPNoiseTransfer Analysis



Point #	Freq (Hz)	Ampl (ns)	Duration (s)	Pk-Pk Output (ns)	Gain (dB)	Upper Pk-Pk Limit (ns)	Lower Pk-Pk Limit (ns)
1	0.00390625	200	1024.00	201.97	0.09	215	130
2	0.0078125	200	896.00	201.41	0.06	215	130
3	0.015625	200	448.00	199.06	-0.04	215	130
4	0.03125	200	224.00	188.40	-0.52	215	130
5	0.0615625	200	243.65	161.23	-1.87	215	-
6	0.123125	200	251.78	111.72	-5.06	140	-
7	0.24625	200	251.78	63.61	-9.95	90	-
8	0.4925	200	249.75	32.92	-15.67	50	-
9	0.985	200	249.75	17.09	-21.36	35	-
10	1.985	200	249.87	6.93	-29.20	30	-

11. Revision History

Revision	Date	Description
1.01	Jul 16, 2024	Replaced Xilinx with AMD thought the document.
1.00	May 5, 2023	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.