ISL70001SRH

Single Event Effects (SEE) Testing of the ISL70001SRH Synchronous Buck Regulator

Introduction

The intense, heavy ion environment encountered in space applications can cause a variety of effects in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Latchup (SEL), Single Event Burnout (SEB), and Single Event Gate Rupture (SEGR). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. This report discusses the results of SEE testing performed on the ISL70001SRH synchronous buck regulator. This report is also applicable to the ISL71001SLHM and ISL70001ASEH devices as they use the same die.

Product Description

The ISL70001SRH is a monolithic synchronous buck regulator IC with integrated power MOSFETs. The device uses peak current-mode PWM control with integrated loop compensation and switches at a nominal frequency of 1MHz. It is fabricated on a 0.6µm BiCMOS junction isolated process optimized for power management applications. Available active devices include low voltage CMOS, high voltage DMOS, and complementary bipolars. With this chip and a handful of external components, a complete synchronous buck DC/DC converter can be readily implemented. The converter accepts an input voltage ranging from 3V to 5.5V and provides a tightly regulated output voltage ranging from 0.8V to ~85% of the input voltage at output currents ranging from 0A to 6A. Typical applications include Point Of Load (POL) regulation for FPGAs, CPLDs, DSPs, and microprocessors.

The ISL70001SRH was hardened by design to achieve a Total Ionizing Dose (TID) rating of at least 100krads(Si) at the standard 50-300rad(Si)/s High Dose Rate (HDR) in addition to the standard <10mrad(Si)/s Low Dose Rate (LDR). Well known TID hardening methods were employed such as use of closed geometry NMOS devices to reduce leakage and increased circuit bias to mitigate Enhanced Low Dose Rate Sensitivity (ELDRS) in bipolar devices. The ISL70001SRH was also hardened by design to a Linear Energy Transfer (LET) of 86.4MeV/mg/cm^2. Various SEE hardening techniques were used including proper device sizing, filtering, and special layout constraints. Triple Module Redundancy (TMR) plus a majority voter were used to harden the internal PWM control loop to SETs. Additional SET hardening was achieved by specifying or restricting the values of certain external components including bypass capacitors, feedback components, and a pull-up resistor.

Related Information

For a full list of related documents, visit our website:

- ISL70001SRH, ISL71001SLHM, ISL70001ASEH device pages

Contents

1. SEE Testing

1.1 Test Objectives

The ISL70001SRH was tested to determine its susceptibility to SEL, SEB, and SEGR and to characterize its SET behavior.

1.2 Test Facility

Testing was performed at the Texas A&M University (TAMU) Cyclotron Institute heavy ion facility. This facility is coupled to a K500 super-conducting cyclotron, which is capable of generating a wide range of test particles with the various energy, flux, and fluence levels needed for advanced radiation testing.

1.3 Test Set-Up

A schematic of the ISL70001SRH SEE test circuit is shown in Figure 1. The test circuit is a synchronous buck DC/DC converter configured to accept an input voltage from 3V to 5.5V and generate a nominal 1.8V output voltage. Output current was adjusted using a constant current electronic load.

Four ISL70001SRH test circuits were mounted to a test jig that can be rotated with respect to the ion beam. A 20 foot coaxial cable connected the test jig to a switch box in the control room that contained all of the monitoring equipment. The switch box allowed any one of the four test circuits to be controlled and monitored remotely.

Digital multimeters were used to monitor input voltage (VIN), output voltage (VOUT), and input current (IIN). Four LeCroy waveRunner 4-channel digital oscilloscopes were used to monitor, capture, and store key signal waveforms. Table 1 shows the scope configuration used during the testing. ΔPW refers to the change in pulse width and ΔT refer to the change period.

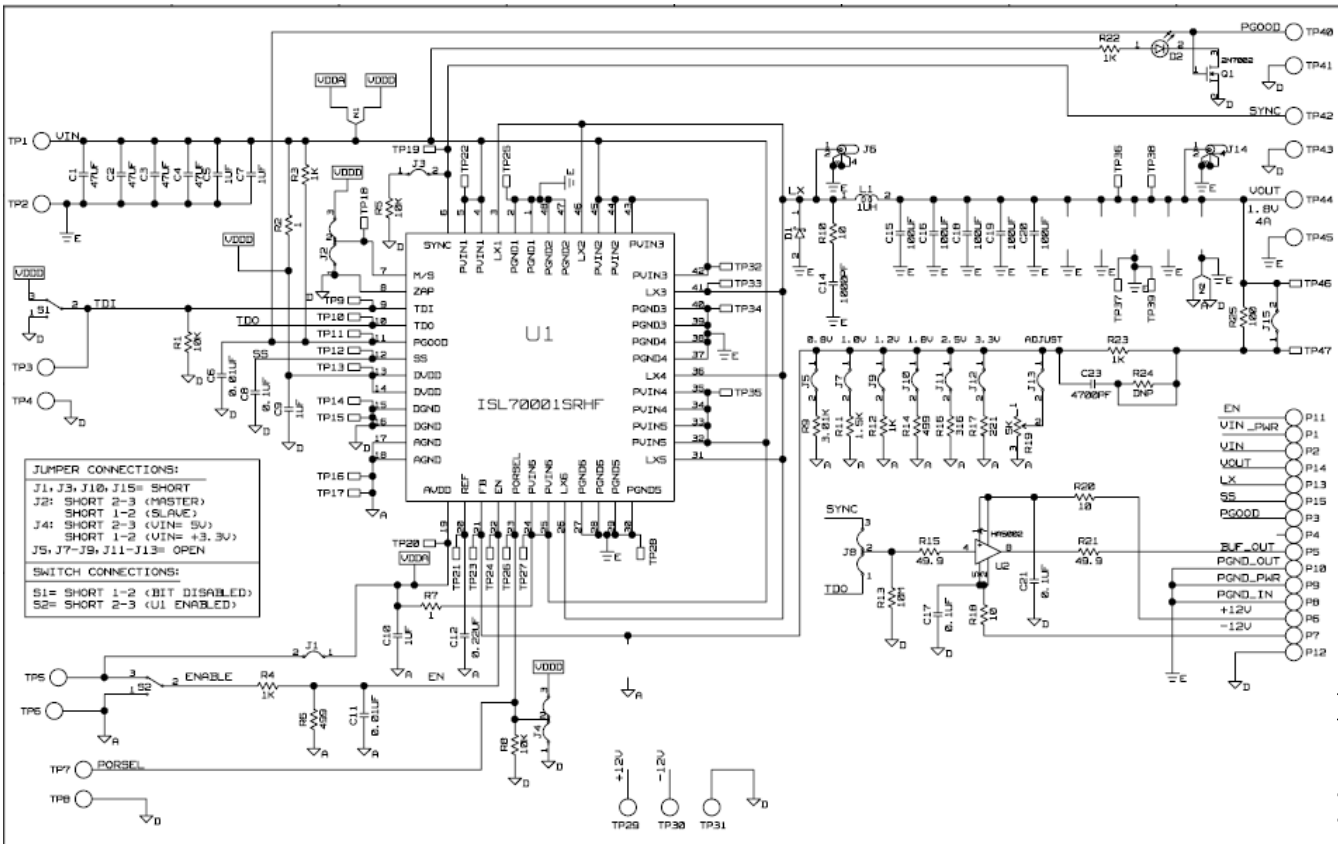


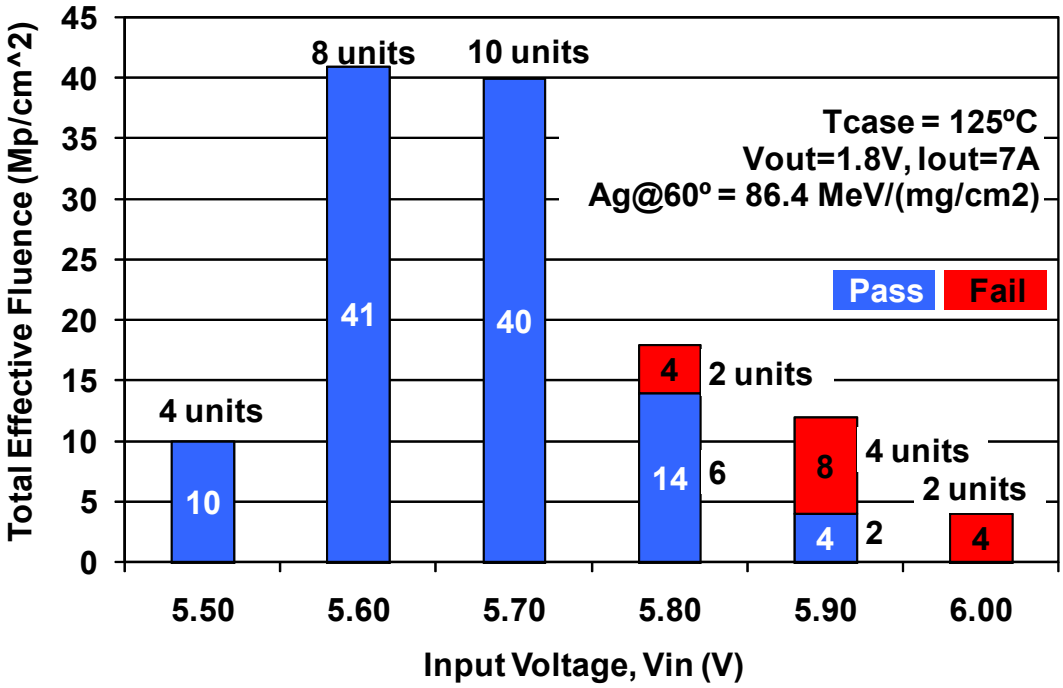
Figure 1. ISL70001SRH SEE Test Circuit Schematic

Table 1. Oscilloscope Configuration

Scope	Channel 1	Channel 2	Channel 3	Channel 4	Trigger
1	LX	VOUT	SS	PGOOD	LX (ΔPW = ±20%)
2	LX	VOUT	SS	PGOOD	LX (ΔT = +10%)
3	LX	VOUT	SS	PGOOD	LX (ΔT = -10%)
4	LX	VOUT	SS	PGOOD	PGOOD (<2.5V)

2. SEL/SEB/SEGR Testing

During SEL/SEB/SEGR testing, conditions were selected to maximize the electrical and thermal stresses on the Device Under Test (DUT), therefore, increasing the probability of failure. Input voltage (VIN) was initially set to 5.5V, which is the maximum recommended supply voltage rating for the device, and then increased in 0.1V increments. Output voltage (VOUT) was set to 1.8V. Output current (IOUT) was set to 7A, which is 1A above the 6A maximum recommended current rating for the device. Case temperature was maintained at 125°C by controlling current flowing into a resistive heat pad bonded to the underside of the DUT. This ensured that the junction temperature of the DUT exceeded 125°C, which is the maximum junction temperature anticipated for high reliability applications. DUTs from three fabrication lots were irradiated with Ag ions at a 60° incident angle, resulting in an effective LET of 86.4MeV/mg/cm^2. Figure 2 shows the results of SEL/SEB/SEGR testing.



Note: Units were tested with increasing input voltage (VIN) until failure.

Figure 2. SEL/SEB/SEGR Test Results

The criterion for failure was a greater that 5% increase in operating input current (I_{IN}) at I_{OUT} = 0A, post irradiation. I_{IN} is the total current consumed by the device and is comprised of currents flowing into the PVINx (power), DVDD (digital) and AVDD (analog) supply pins. Failed devices were not further irradiated. Failure analysis of three failed units revealed damage to the output NMOS power FET, but a root cause of failure determination proved elusive as the failure signatures of SEL, SEB, and SEGR can appear quite similar.

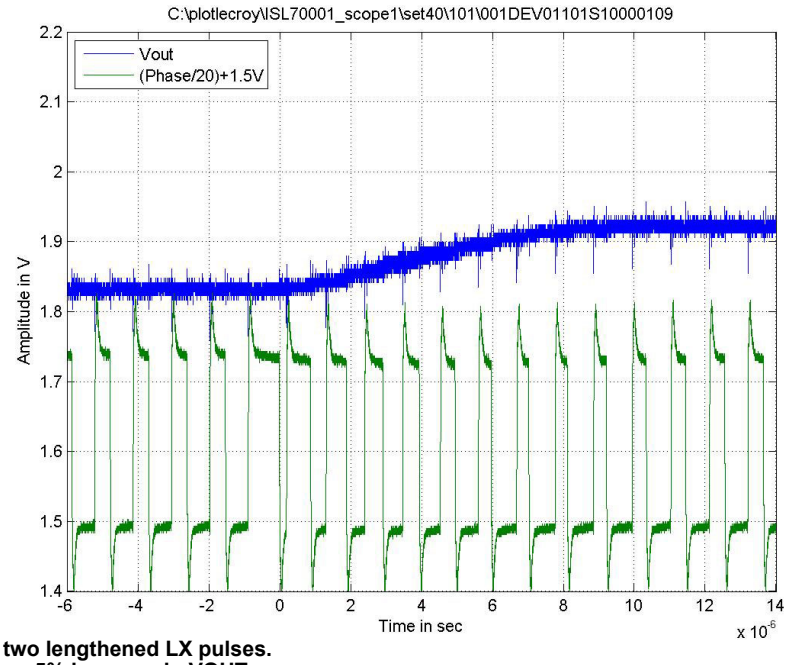
To assist with identification of root cause of failure, two additional experiments were performed. First, several ISL70001SRH devices were irradiated with neutrons to a fluence of $1x10^{12}$neutrons/cm^2 at White Sands Missile Range (WSMR). Neutron irradiation causes displacement damage that lowers the gain of parasitic bipolar devices involved in SEL/SEB, but has no effect on SEGR. Subsequent SEL/SEB/SEGR testing of these devices at TAMU did not show improvement in the maximum input voltage (VIN) that could be supported. Second, several ISL70001SRH devices were fabricated using a thicker gate oxide (170Å vs 140Å). Subsequent SEL/SEB/SEGR testing of these devices at TAMU showed an increase from 5.7V to 6.1V in the maximum input voltage (VIN) that could be supported. The results of both of these experiments implicate SEGR of the output NMOS power FET as the likely failure mechanism.

2.1 Baseline SET Testing (Unhardened Device)

To better assess the benefits of the SET hardening efforts, an ISL70001SRH chip was modified by Fixed Ion Beam (FIB) to disable two of the three redundant PWM control loops. This unhardened chip was then irradiated under the following test conditions:

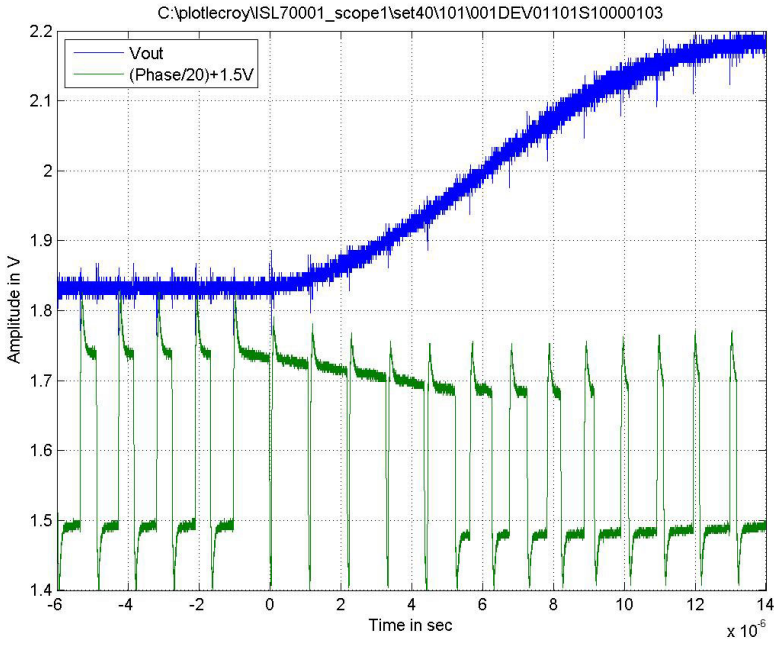
- V_{IN} = 5V
- V_{OUT} = 1.8V
- I_{OUT} = 4A
- T_C = 25°C
- Ag Ions at 0° incident angle
- LET = 43.2MeV/mg/cm^2
- Flux = $1.82x10^4$ to $3x10^6$ions/cm^2/s
- Fluence = $3x10^6$ions/cm^2

A total of 211 ΔPW SETs, 260 ΔT SETs, and 21 PGOOD SETs were captured with respective cross-sections of ~$7x10^{-5}$cm^2, ~$8.7x10^{-5}$cm^2, and ~$7x10^{-6}$cm^2. The best case ΔPW SET shown in Figure 3 resulted in two LX pulses with pulse widths approximately double that of a normal LX pulse and an output voltage perturbation of ~5%. The worst case ΔPW SET shown in Figure 4 resulted in five full-width LX pulses and an output voltage perturbation of ~20%.



Note: Green trace shows two lengthened LX pulses.
Blue trace shows an ~5% increase in VOUT.

Figure 3. Best Case ∆PW SET in an Unhardened Device



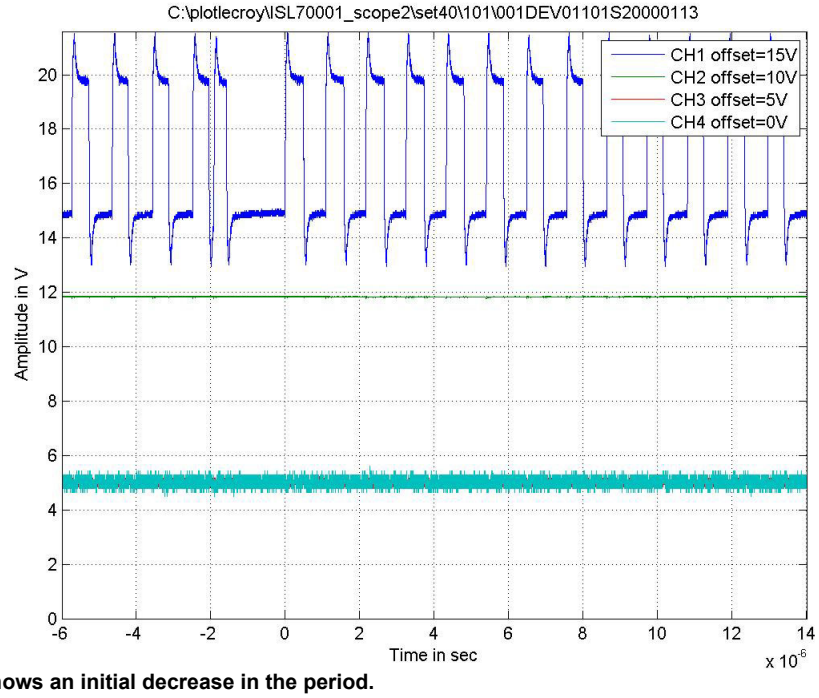
Note: Green trace shows five full-width LX pulses.
Blue trace shows an ~20% increase in VOUT.

Figure 4. Worst Case ∆PW SET in an Unhardened Device

Note: Many low voltage logic devices such as FPGAs have a recommended supply voltage tolerance of ±5% and an absolute maximum supply voltage tolerance of +10%. So best case, the output voltage transient resulting from an ion strike on an unhardened device almost exceeds the recommended supply voltage tolerance of a typical FPGA. And worst case, the output voltage transient resulting from an ion strike on an unhardened device greatly

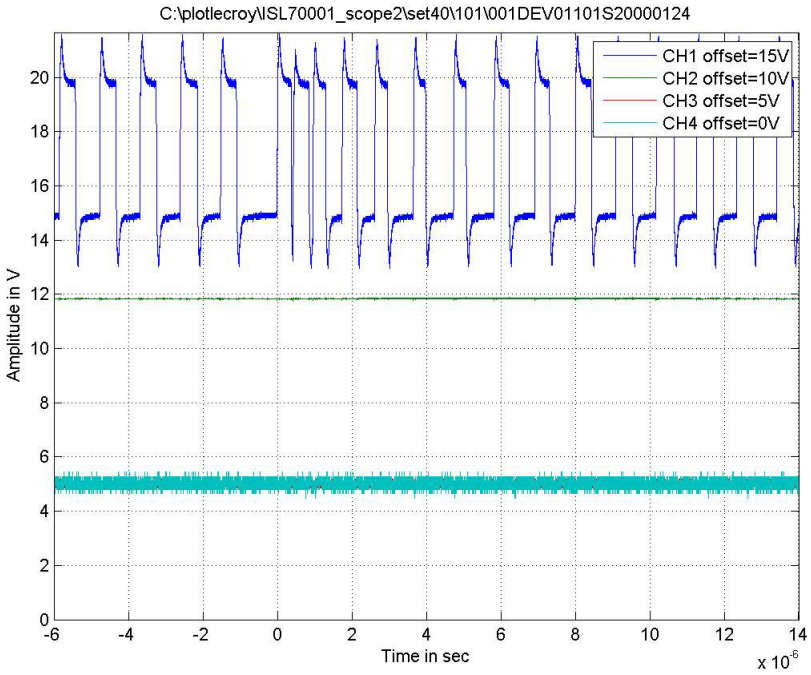
exceeds the absolute maximum supply voltage tolerance allowed for a typical FPGA. This makes a strong case for hardening the power IC by design to mitigate potentially destructive SETs.

Two representative examples of a ΔT SET in an unhardened device are shown in Figure 5 and Figure 6. Figure 5 shows a ΔT SET resulting in an initial decrease in the period while Figure 6 shows a ΔT SET resulting in an initial increase in the period.



Note: Blue trace shows an initial decrease in the period.

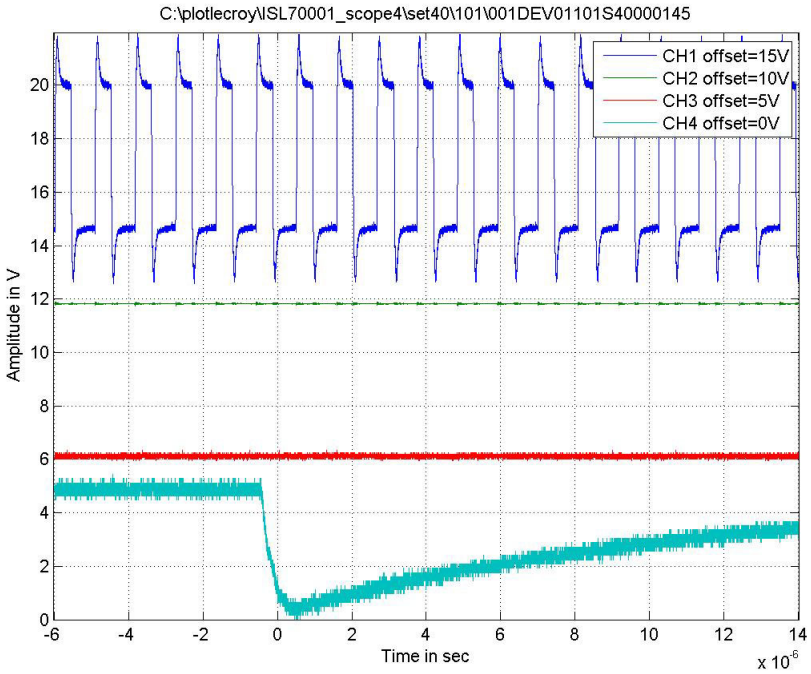
Figure 5. Example ΔT SET in an Unhardened Device



Note: Blue trace shows an initial increase in the period.

Figure 6. Example ΔT SET in an Unhardened Device

A representative example of a PGOOD SET in an unhardened device is shown in Figure 7.



Note: Aqua trace shows the PGOOD signal transitioning from high to low indicating a fault.

Figure 7. Example PGOOD SET in an unhardened device.

2.2 Baseline SET Testing (V_{IN} = 5V ±10%, Hardened Devices)

11 ISL70001SRH devices were irradiated under the following test conditions:

- V_{IN} = 5.5V
- V_{OUT} = 1.8V
- I_{OUT} = 4A
- T_C = 25°C
- Ag Ions at 0º incident angle
- LET = 43.2MeV/mg/cm^2
- Flux = 1.03x10^3 to 7.05x10^{4}ions/cm^2/s per run
- Fluence = 4.5x10^{6}ions/cm^2 per run
- Total Fluence = 15 runs x (4.5x10^{6}ions/cm^2 per run) = 6.75x10^{7}ions/cm^2

Four runs were with an external clock.

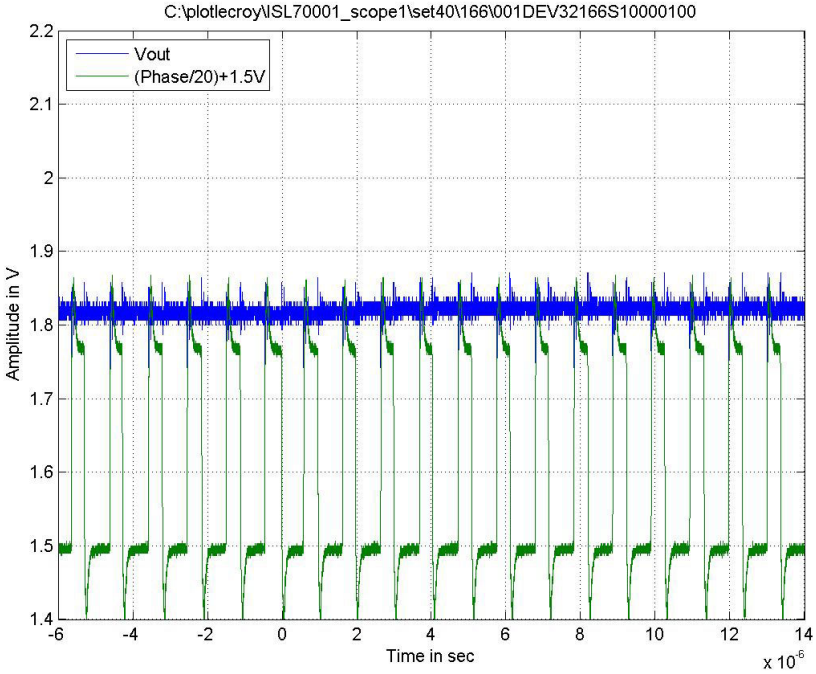
Five ISL70001SRH devices were irradiated under the following test conditions:

- V_{IN} = 4.5V
- V_{OUT} = 1.8V
- I_{OUT} = 4A
- T_C = 25°C
- Ag Ions at 0º incident angle
- LET = 43.2MeV/mg/cm^2
- Flux = 1.05x10^3 to 9.10x10^{3}ions/cm^2/s per run
- Fluence = 4.5x10^{6}ions/cm^2 per run
- Total Fluence = 5 runs x (4.5 x 106 ions/cm^2 per run) = 2.25 x 107 ions/cm^2

One ISL70001SRH device was irradiated under the following test conditions:

- V_{IN} = 4.5V
- V_{OUT} = 1.8V
- I_{OUT} = 4A
- T_C = 25ºC
- Ag Ions at 0º incident angle
- LET = 43.2MeV/mg/cm^2
- Flux = 5.17x10^{4}ions/cm^2/s
- Fluence = 4.1x10^{7}ions/cm^2

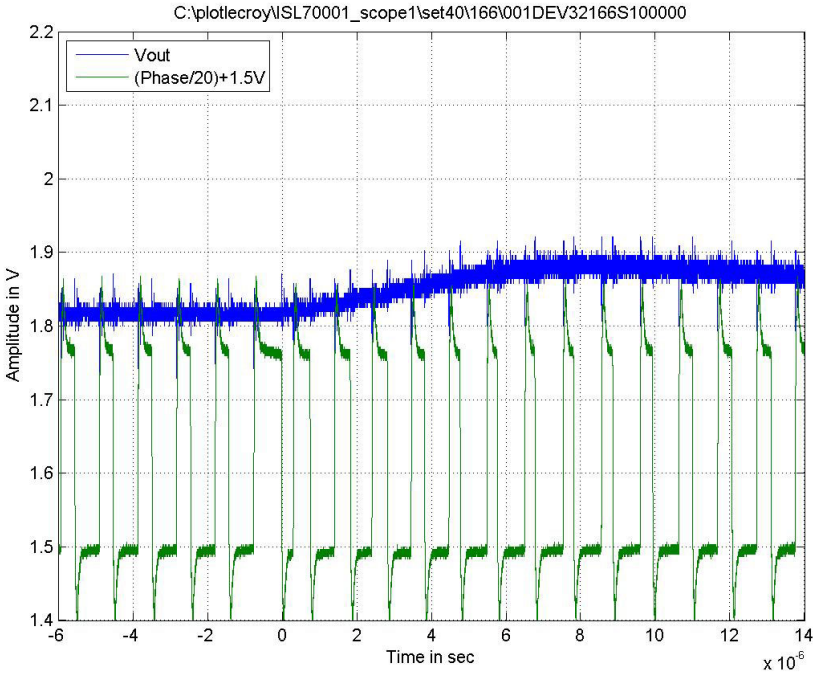
During the V_{IN} = 5.5V and 4.5V SET tests, a total of 11,530 events were captured with a combined 1.31x10^{8}ions/cm^2 fluence. Figure 8 shows a benign SET that was representative of all but 60 of the events.



Note: Green trace shows one slightly lengthened LX pulse just before t = 0. Blue trace shows VOUT is virtually undisturbed.

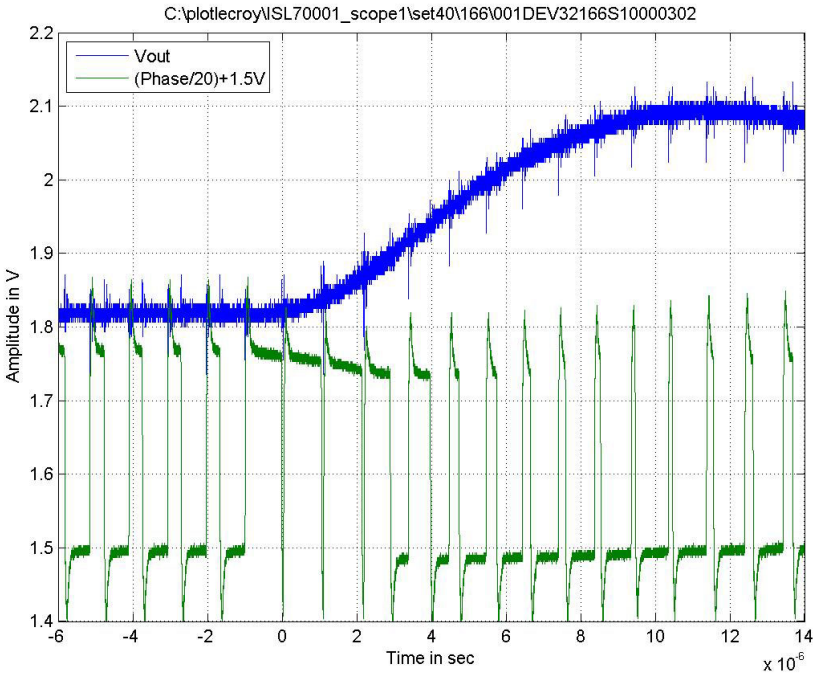
Figure 8. Typical benign SET at LET = 43.2MeV/mg/cm^2

The remaining 60 events were non-benign and took one of three forms as shown in Figure 9, Figure 10, and Figure 11. These non-benign events showed a strong flux dependence, which indicated they might result from double ions affecting the redundant PWM control loops.



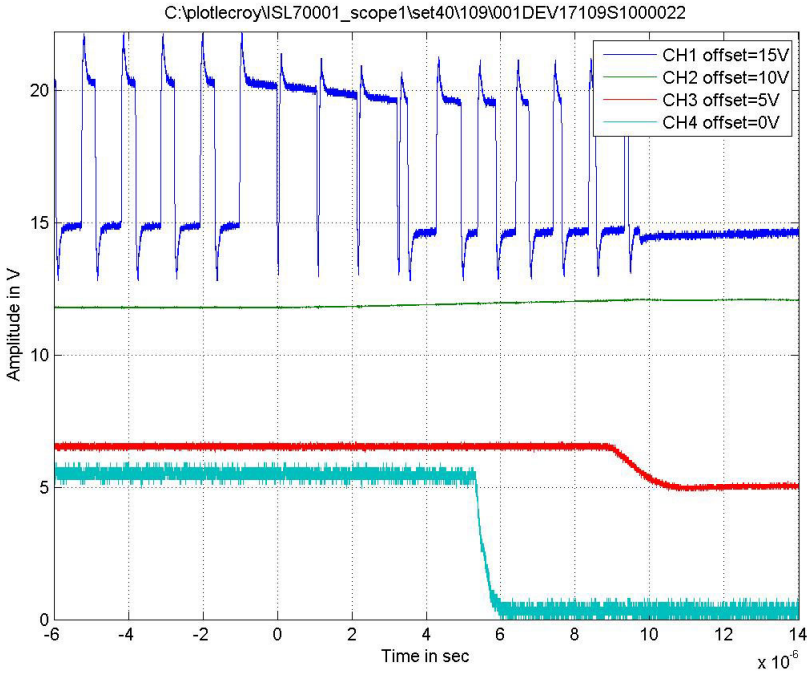
Note: Green trace shows one lengthened LX pulse followed by a 4-5 pulse recovery. Blue trace shows an ~4.5% increase in VOUT.

Figure 9. Non-benign SET at LET = 43.2MeV/mg/cm^2



Note: Green trace shows three full-width LX pulses followed by several lengthened LX pulses before recovery begins. Blue trace shows an ~16% increase in VOUT.

Figure 10. Non-benign SET at LET = 43.2MeV/mg/cm^2



Note: Blue trace shows four full-width LX pulses followed by current limited LX pulses and overcurrent protection shutdown. Red trace shows soft-start discharge. Aqua trace shows a PGOOD fault.

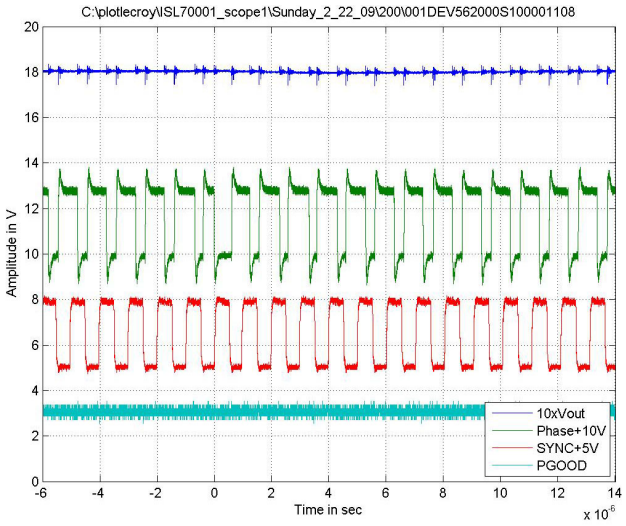
Figure 11. Non-Benign SET at LET = 43.2MeV/mg/cm^2

2.3 Baseline SET Testing (VIN = 3V, Hardened Devices)

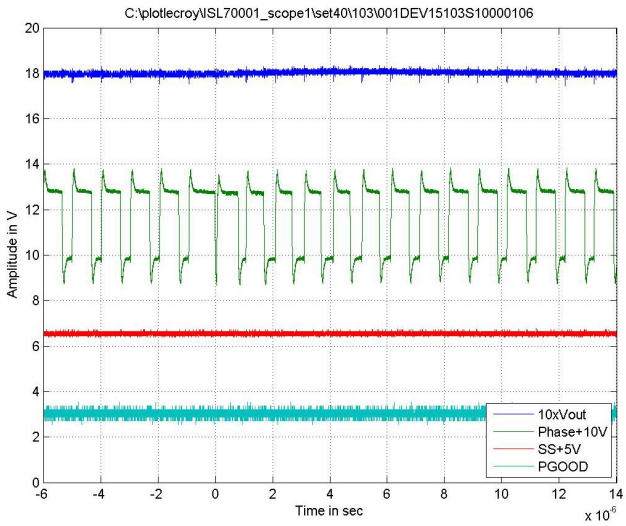
18 ISL70001SRH devices were irradiated under the following test conditions:

- V_{IN} = 3V
- V_{OUT} = 1.8V
- I_{OUT} = 4A
- T_C = 25°C
- Ag Ions at 0° incident angle
- LET = 43.2MeV/mg/cm^2
- Flux = 4.18x10^2 to 6.51x10^{4}ions/cm^2/s per run
- Fluence = 1.25x10^5 to 4.0x10^{7}ions/cm^2 per run

During the V_{IN} = 3V SET tests, a total of 20,083 events were captured. The vast majority (19,848) were benign single pulse events, resulting in slightly lengthened or shortened LX pulses and less than a 1% perturbation of V_{OUT}. Representative benign SET events are shown in Figure 12. The remaining events were non-benign, and showed a strong flux dependence as was seen during the baseline V_{IN} = 5V ±10% SET testing. An example non-benign SET event is shown in Figure 13.



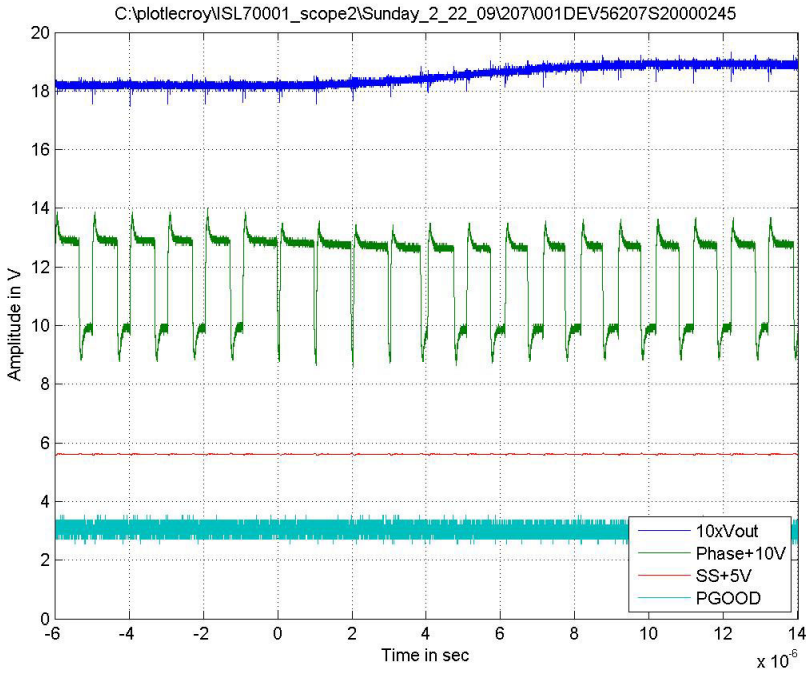
Note: Green trace shows one shortened LX pulse just before t = 0.



Note: Green trace on the right shows one lengthened LX pulse just before t = 0.

Note: In both cases V_{OUT} perturbation is < 1%.

Figure 12. Typical benign SET at LET = 43.2MeV/mg/cm^2



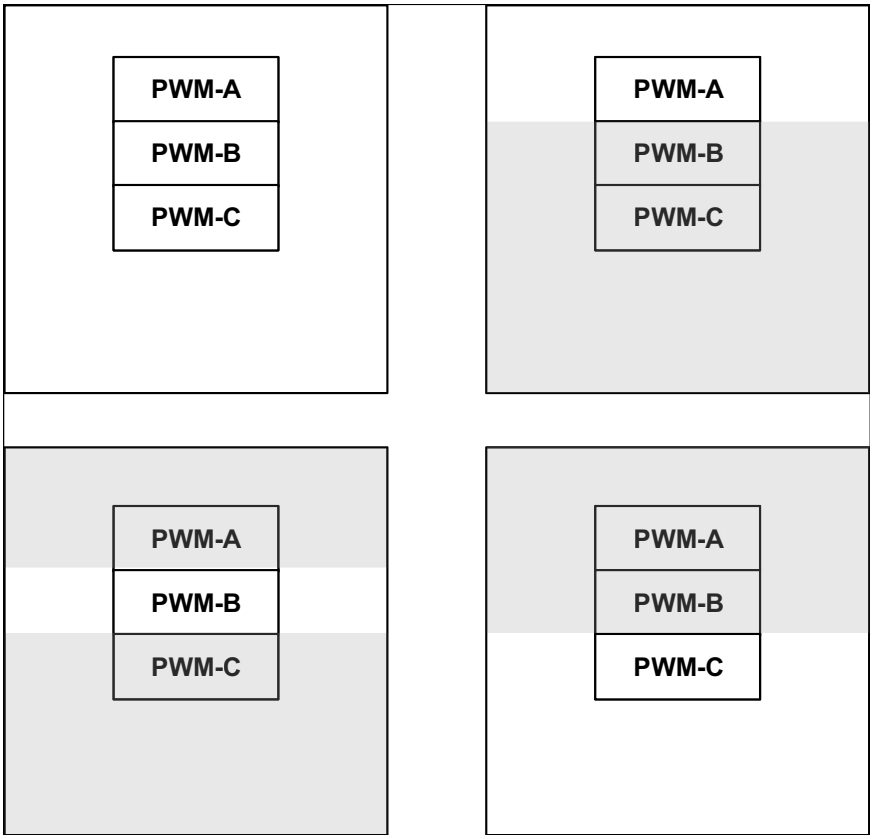
Note: Green trace shows four full-width LX pulses.
Blue trace shows an ~5% increase in VOUT.

Figure 13. Non-Benign SET at LET = 43.2MeV/mg/cm^2

2.4 Follow-Up SET Testing

The intent of follow-up SET testing was to prove (or disprove) the theory that non-benign SET events seen during baseline SET testing were the result of high flux test rates that would not be encountered in a natural Space environment. If flux test rates are high enough, it is possible that two of the three redundant PWM control loops would receive an ion strike within a short interval of time. If that interval of time is less than the recovery time (up to 1ms) of a redundant PWM control loop, the redundancy would be defeated and non-benign SETs could result.

To test this theory, a shielding approach was proposed. Two of the three redundant PWM control loops were shielded using three shielding patterns as shown in Figure 14.



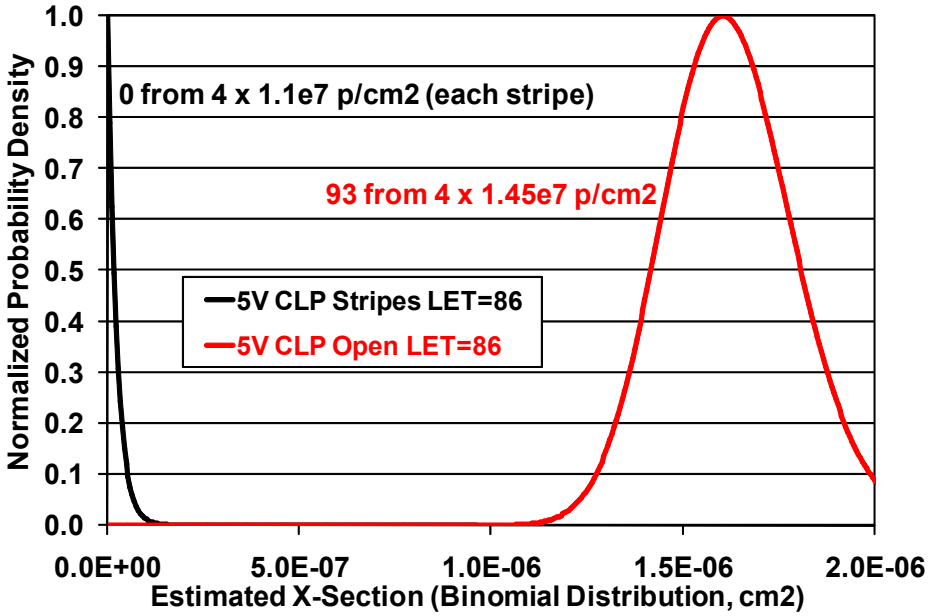
Note: Gray bars show shielding of two of the three redundant PWM control loops, while the third PWM control loop is exposed to the beam.

Figure 14. Proposed Shielding Patterns

Four units of each of the three shielding patterns shown in Figure 14 were prepared and irradiated to a fluence of $1.1x10^7$ions/cm^2. The combination of the 12 shielded units exposed the entire die, just not simultaneously, to a total fluence of $4.4x10^7$ions/cm^2. For comparison purposes, four unshielded units were each irradiated to a fluence of $1.45x10^7$ions/cm^2 for a total fluence of $5.8x10^7$ions/cm^2. The following are the other test conditions during testing of shielded and unshielded units:

- V_{IN} = 5V
- V_{OUT} = 1.8V
- I_{OUT} = 4A
- T_C = 25°C
- Ag Ions at 60° incident angle
- Effective LET = 86.4MeV/mg/cm^2

Testing showed there were no non-benign SETs captured during irradiation of the shielded units, but there were 93 non-benign SETs captured during irradiation of the non-shielded units. Figure 15 provides estimated cross-sections of the shielded and unshielded units and offers proof that the non-benign SETs are the result of high flux test rates. Therefore, it can be concluded that the redundant PWM control loops are effective in limiting SETs to less than a single LX pulse disturbance and an output voltage (V_{OUT}) perturbation of less than 1%.



Note: This offers proof that non-benign SETS are the result of high flux test rates.

Figure 15. Estimated Cross-Sections of Shielded (Black) and Unshielded (Red) Units Assuming a Binomial Distribution

During follow-up SET testing, a few SEFIs were observed. All SEFIs were captured with V_{OUT} = 1.8V, I_{OUT} = 4A and T_C = 25°C. Figure 16 shows a representative SEFI capture.

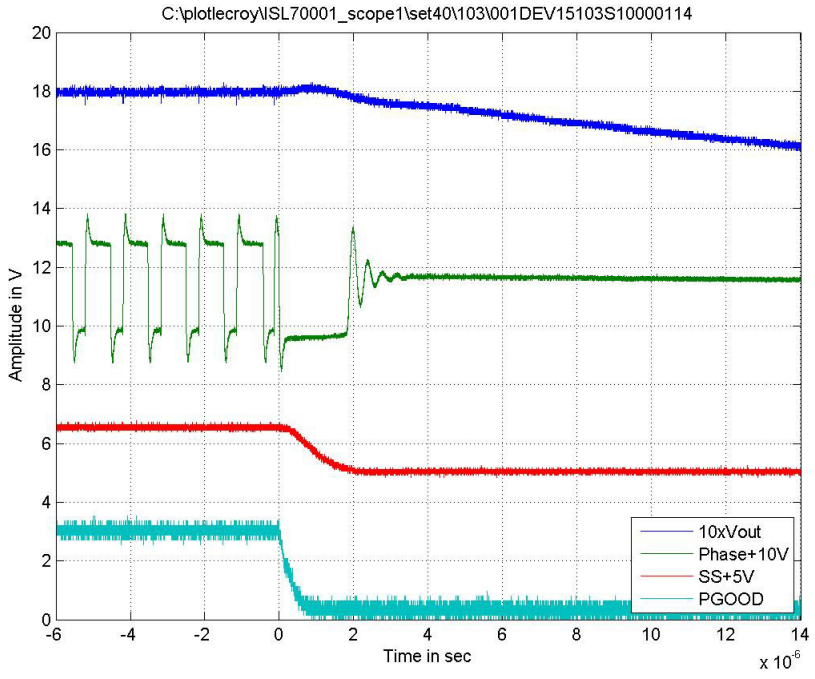
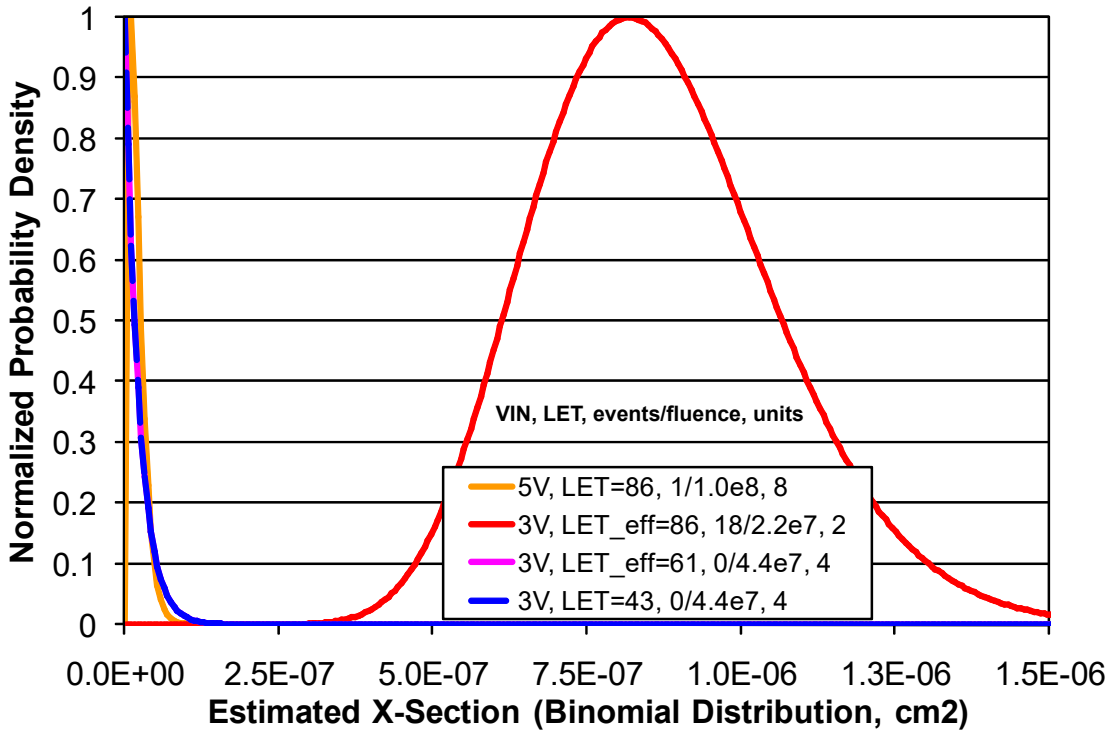


Figure 16. Representative SEFI Capture

The green trace shows LX pulses abruptly terminating. The blue trace shows VOUT decaying. The red trace shows a soft-start discharge. The Aqua trace shows a PGOOD fault. The device then proceeds through a normal soft-start and output voltage recovery with no external intervention (not shown).

Figure 17 shows the test conditions and provides an estimate of SEFI cross-section.



Note: With a 95% confidence level, cross-sections are estimated as follows: Orange trace: <6.5x10^{-8}cm^2. Red trace: <1.4x10^{-6}cm^2. Pink trace: <1.1x10^{-7}cm^2. Blue trace: <1.1x10^{-7}cm^2.

Figure 17. SEFI Test Conditions and Estimated Cross-Sections Assuming a Binomial Distribution

3. Conclusions

The ISL70001SRH SEE test results clearly demonstrate the value of a hardened by design approach. SEL/SEB/SEGR immunity is assured to an effective LET of 86.4MeV/mg/cm^2 at an input voltage up to 5.7V, an output current up to 7A and a case temperature up to 125°C. The triple redundant PWM control loops plus majority voter are highly effective in limiting SETs to less that one LX pulse perturbation and less than 1% perturbation of the output voltage to an effective LET of 86.4MeV/mg/cm^2. Several SEFIs were observed at an effective LET = 86.4MeV/mg/cm^2, with all but one occurring at an input voltage of 3V. In all cases, the device recovered normally with no user intervention required. More importantly, the cross-sections of the SEFIs were shown to be quite small.

4. Revision History

Revision	Date	Description
1.0	May 26, 2021	Initial release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/