ISL70005SEH, ISL73005SEH

SEE Test Report

Introduction

The intense proton and heavy ion environment encountered in space applications can cause a variety of Single Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Latch-Up (SEL), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. This report discusses the results of SEE testing performed on the ISL70005SEH product. The ISL70005SEH is offered with radiation assurance screening to 100krad(Si) at 50 to 300rad(Si)/s and 75krad(Si) at 10mrad(Si)/s. This report also applies to the ISL73005SEH part, which is the same silicon die offered with radiation assurance screening to only 75krad(Si) at 10mrad(Si)/s.

SEE Summary

The ISL70005SEH proved to be free of SEB and SEL at supply voltages up to 6.0V and a case temperature of 125°C when irradiated with normal incidence gold for a Linear Energy Transfer (LET) of 86MeV·cm^2/mg. The buck output was loaded with 3.5A, and the LDO was loaded with ±1.2A.

The buck regulator exhibited SET defined by output voltage deviations of ±36mV (±2% on the 1.8V output with 1.8A load) with a cross-section of 764µm^2 when irradiated with normal incidence argon for an LET of 8.5MeV·cm^2/mg. The precipitating disturbances were up to two switching periods at the 1MHz switching frequency when using a 1µH output inductor and a 150µF output capacitor.

The LDO did not produce any SET defined as ±18mV deviations (±2% on the 0.9V output) when irradiated with normal incidence argon for a LET of 8.5MeV·cm^2/mg. A 150µF output capacitor was used, and loading was up to ±0.9A.

Part Description

The ISL70005SEH is a radiation hardened dual output Point-of-Load (POL) regulator combining the high efficiency of a synchronous buck regulator with a Low Dropout (LDO) regulator in a single integrated circuit. This device is suited for systems with 3.3V to 5V power buses and can support continuous output load currents of 3A for the buck regulator and ±1A for the LDO.

The buck regulator uses a voltage mode control architecture and switches at a resistor adjustable frequency from 100kHz to 1MHz. Externally adjustable loop compensation allows for an optimum balance between stability and output dynamic performance. The internal synchronous power switches are optimized for high efficiency and excellent thermal performance.

The LDO is completely configurable independent of the switching regulator. It uses NMOS pass devices and the chip bias voltage (L_VCC) to drive the gate of the upper device, enabling the LDO to function with inputs less than 1V. The LDO can sink and source up to 1A continuously, making it an ideal choice to power DDR memory.

The ISL70005SEH offers programmable soft-start and enable functions along with a power-good indicator for ease of supply rail sequencing and other housekeeping requirements. In addition, the ISL70005SEH incorporates fault protection for the regulators. The protection circuits include over-temperature, input undervoltage, output undervoltage, and output overcurrent. The ISL70005SEH is available in a space saving 28 Ld ceramic dual flatpack package or in die form, and is specified to operate across the military temperature range of T_A = -55°C to +125°C.

The SEE testing of the ISL70005SEH was done on three versions that differed only in the metal layers (versions identified as A01, A03, and A04). The masks prior to metal were the same for all versions although the versions do represent different wafer lots. Because the production version is the A04, the results from that version are focused on. However, the results from the other versions can be cited as well because the silicon design is

common to all three versions, and the results from the versions provide some information on manufacturing variability.

The ISL70005SEH samples tested for this report were from silicon lots and wafers as follows:

- A01 lot 1YFHB00000 wafer V3BW6XW,
- A03 lot 1Z92B00000 wafer AXIBXZW
- A04 lot 1KJWB00000 wafer A3IBVUW

The samples were packaged without lids to allow irradiation, and only room temperature testing of the parts was done. No burn-in stressing was done on the parts.

Reference Documentation

For a full list of related documents, visit our website:

- ISL70005SEH and ISL73005SEH device pages

1. SEE Testing

1.1 Objective

The testing was intended to find the limits of the supply voltages and load currents set by the onset of destructive single event effects (SEGR, SEB, or SEL) at a LET of 86MeV·cm^2/mg (normal incidence gold). Additional testing was intended to identify and quantify SETs and SEFIs occurring on the output voltages. The SET studies included irradiation with normal incidence gold (86MeV·cm^2/mg), silver (43MeV·cm^2/mg), copper (20MeV·cm^2/mg), and argon (8.5MeV·cm^2/mg).

1.2 Facility

SEE testing was done at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute in College Station Texas. This facility is coupled to a K500 superconducting cyclotron that can supply a wide range of ion species and flux. The testing referred to in this report was done on August 31, 2018 - September 4, 2018, May 11-14, 2019, and June 7-10, 2019.

1.3 Setup

The ISL70005SEH was SEE evaluated using a general-purpose engineering evaluation board that allowed various application configurations to be used. The specific configurations changed with the type of testing. For destructive SEE testing (collectively called SEB herein), the buck and LDO were operated separately but concurrently (stand-alone mode). For the SET testing, the buck and LDO were operated in both a cascaded configuration (DDR), and with the buck disabled and the LDO independent (stand-alone).

For the SEB testing, the buck was configured to operate with a 1MHz switching frequency and an output of 3.15V (3.5V for the A01 variant) using an inductor of 2.2µH and input and output capacitors of 150µF (AVX TPME157K016R0030 with maximum ESR of 30mΩ). The inductor value was selected to set the ripple current (peak-to-peak) to about 20% of the device DC current of 3.5A under test. An electronic load was used for A01 testing, and a 0.9Ω resistor was used for the A03 and A04. A snubber to limit ringing was placed on the switching node, B_LX, with a 2.6Ω resistor and a 2.2nF capacitor. The supply voltage (B_PVIN and B_VCC) was started at 6.0V and incremented by 0.1V until the part exhibited permanent changes or until 6.4V was achieved. The monitored parameters for the buck are the first three listed in Table 1.

Table 1. Monitored Parameters and Failure Criteria for the ISL70005SEH SEB Testing

Parameter Monitored	Measurement Conditions: As irradiated except for the following.	Failure Criteria
Buck Output Voltage (3.15V)	Zero load current	±1%
Buck Standby Current	Buck disabled	±10%
Buck LX Output Leakage Current	Disabled with LX at biased to 2.5V	±10%
LDO Output Voltage (nominally 0.6 V)	Regulating unloaded (60µA)	±1%
LDO Control Input Current (I_L_VCC)	Enabled unloaded (60µA)	±10%
LDO Output Leakage Current	Disabled, L_OUT = 0.6 V (60µA)	±10%

For SEB testing, the LDO was configured for an output of 0.6V from the 0.6V reference voltage (VREF). The LDO output capacitor was 150µF with a maximum ESR of 30mΩ. The LDO had an external 1.2V supply provided to the power input (L_VIN). A 0.5Ω load to either GND or to L_VIN was provided to set the LDO current to ±1.2A. The LDO monitored parameters are listed in Table 1 as the last three items.

For SET testing, the ISL70005SEH was configured in one of two ways. The first way was a DDR configuration with the buck generating a 1.8V output and the LDO generating a 0.9V output based on a one-half divider reference from the buck. Both the buck and the LDO had output capacitors of 150µF and 30mΩ maximum ESR. The outputs were tested at 1.8A on the buck (1Ω) and ±1mA (900Ω) on the LDO. The second configuration only operated the LDO with an output of 0.9V based on a 1.5x gain of the internal 0.6V reference and an external 1.8V input supply. In this second configuration, the LDO was operated sinking and sourcing 900mA. It was found that to provide stable operation at these current levels, an additional 22µF ceramic capacitor was needed directly across

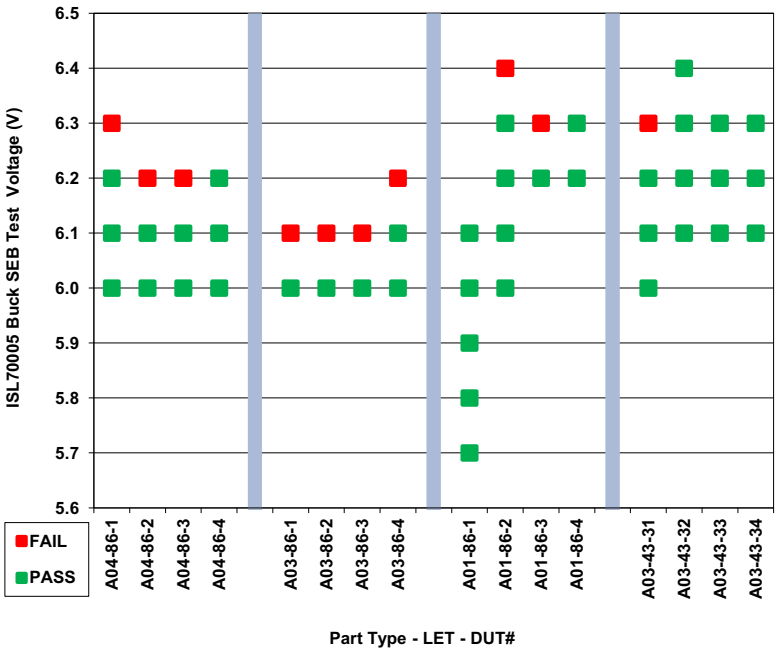
the LDO output and power ground pins. The buck was not operated in this second configuration. The input supply was operated at both 3.0V and 4.5V during the SET testing.

2. Results

2.1 Buck SEB and SEL

SEB and SEL testing of the ISL70005SEH was done on three successive part variants, the A01, A03, and A04. These three variants also represent three distinct wafer processing lots. The variability seen in the three versions for SEB testing likely represents manufacturing variability. The buck design was slightly modified between the A01 and the A03 with a logic change impacting the soft-start behavior into a precharged load. The A03 and A04 were identical buck designs with changes limited to the LDO design. A quick summary of the SEB and SEL results for the buck is presented in Figure 1. All four A04 DUTs tested at 86MeV·cm^2/mg passed at 6.1V supply. All four of the A03 DUTs passed at 6.0V. At 43MeV·cm^2/mg, four A03 DUTs tested passed at 6.2V supply voltage. In the original testing, three of four A01 parts passed testing at 6.2V; and the first part had testing terminated at 6.1V for TID limitation. The A01 parts had testing done at 0A of load current (not shown) before the 3.5A tests at each voltage and passed those 0A tests at the voltages where the 3.5A tests failed. These A01 results are taken as proof that the loaded condition is the worst-case for buck SEB so that the A03 and A04 only saw loaded SEB testing.

SEB testing on a DUT was terminated on either of two criteria. First, accumulation of total ionizing dose limited testing to only five exposures on a single DUT. Second, if a DUT exceeded the lowest failure level of equivalent DUTs, testing was terminated.



Note: Each result marker represents 1x10^{7}ion/cm^2 irradiation with either normal incidence gold for 86MeV·cm^2/mg or normal incidence silver for 43MeV·cm^2/mg..

Figure 1. SEB/SEL Buck Testing PASS/FAIL Summary

SEB (to include SEL) of the A04 was tested with normal incidence gold for 86MeV·cm^2/mg at a case temperature of 125°C ±10°C, and a buck load of 3.5A at an output voltage of approximately 3.15V (3.5V for A01). SEB testing consisted of irradiation at a buck supply voltage (VIN = B_VCC = B_PVIN) of 6.0V and proceeding in 0.1V increments until failure or 6.4V was reached. Both before and after irradiation three parameters (Table 1) were monitored to look for signs of either SEL or SEB. The results of this testing for the A04 part are presented in Table 2 on page 5. Failures to the criteria at the top of the columns are indicated with bold and red text. These failure results were basically the same as for the other versions in that failures were always for increases in the buck standby current.

Table 2. ISL70005SEH A04 Buck SEB and SEL Testing Results for Normal Incidence Gold at LET = 86MeV·cm^2/mg and 125°C ±10°C Case Temperature

Type- DUT	V_{IN} (V)	V_{OUT} at I_{OUT} = 0A (V) ±1%		I_IN Disabled at I_{OUT} = 0A (mA) ±10%		LX Leakage Disabled at 2.5V (µA) ±10%	
		Pre	Delta	Pre	Delta	Pre	Delta
A04-1	6.0	3.116	0.0%	6.20	-2%	82	0%
A04-1	6.1	3.116	-0.1%	6.16	1%	82	0%
A04-1	6.2	3.115	-0.1%	6.18	0%	82	0%
A04-1	6.3	3.113	0.0%	6.29	456%	82	0%
A04-2	6.0	3.105	0.0%	5.91	0%	82	0%
A04-2	6.1	3.104	0.0%	5.99	2%	82	0%
A04-2	6.2	3.104	0.0%	6.30	218%	82	0%
A04-3	6.0	3.132	0.0%	6.21	0%	82	0%
A04-3	6.1	3.129	0.1%	6.32	7%	82	0%
A04-3	6.2	3.130	0.0%	6.91	30%	82	0%
A04-4	6.0	3.120	0.0%	6.23	0%	82	0%
A04-4	6.1	3.119	0.0%	6.26	-1%	82	0%
A04-4	6.2	3.119	0.1%	6.41	0%	82	0%

Note: Each entry represents change across an irradiation of 1x10^{7}ion/cm^2.

2.2 LDO SEB and SEL

Although the two regulators were not coupled except for the supply voltages (B_VCC, B_PVIN, and L_VCC), which have a 150µF from B_PVIN to ground and 1µF from the VCC supplies to ground, SEB testing of the LDO was done at the same time as the buck SEB testing. The LDO output was set to 0.6V from a 0.6V input using VREF as reference. The power input to the LDO (L_VIN) was externally supplied with 1.2V and the output was loaded to either sourcing or sinking 1.2A. The results for testing the LDO with 86MeV·cm^2/mg are presented in Table 3 on page 6.

The LDO did not register any SEB or SEL failures in the testing represented in Table 3. Only the control voltage, L_VCC, was supplied with the buck test voltage. The output pass devices, both NMOS, were only stressed at 0.6V. However, these output devices are the same type as used in the low side of the buck output, so the buck testing provides stressing of this device type at the same test voltage. Therefore, the buck results provide validation of the LDO power biasing. In normal operation, the LDO output cannot reach the voltages imposed on the buck as the output must be 1.5V below L_VCC for operation. At the same time, the supply of L_VIN with the higher voltages limits the LDO current due to thermal considerations. Therefore, regular application configurations should never tax the LDO power terminals with voltages approaching those tested for the buck. It is concluded that the LDO is immune to SEB and SEL to the voltages that proved good for the buck (6.1V for 86MeV·cm^2/mg). The A01 and A03 LDO testing (with A03 at 43MeV·cm^2/mg irradiation) did not yield anything of note beyond the testing reported in Table 3. Therefore, in all cases the SEB and SEL failure limitation was for the buck and not the LDO.

Table 3. ISL70005SEH A04 SEB and SEL Testing of the LDO Loaded with ±1.2A at a 0.6V Output from a 1.2V Supply

DUT	L_VCC (LVIN = 1.2 V)	L_IOUT (A)	L_OUT L_IOUT = 60µA (V) ±2%		I_L_VCC Enabled, L_IOUT = 60µA (mA) ±25%		I_L_OUT Disabled at 0.6V (µA) ±25%	
			Pre	Delta	Pre	Delta	Pre	Delta
A04-1	6.0	+1.2	0.597	0%	5.529	0%	43	0%
A04-1	6.1	+1.2	0.597	0%	5.603	0%	43	0%
A04-1	6.2	+1.2	0.598	0%	5.663	0%	43	0%
A04-1	6.3	+1.2	0.598	0%	5.740	0%	43	0%
A04-2	6.0	+1.2	0.597	0%	5.521	0%	43	0%
A04-2	6.1	+1.2	0.597	0%	5.573	0%	43	0%
A04-2	6.2	+1.2	0.597	0%	5.640	0%	43	0%
A04-3	6.0	-1.2	0.598	0%	5.891	0%	43	0%
A04-3	6.1	-1.2	0.598	0%	5.956	0%	43	0%
A04-3	6.2	-1.2	0.598	0%	6.010	0%	43	0%
A04-4	6.0	-1.2	0.599	0%	5.862	0%	43	0%
A04-4	6.1	-1.2	0.599	0%	6.035	-1%	43	0%
A04-4	6.2	-1.2	0.599	0%	5.999	0%	43	0%

Note: The irradiations were $1x10^7$ion/cm^2 of normal incidence gold for 86MeV·cm^2/mg.

2.3 Buck SEFI

ISL70005SEH testing for general SET revealed a small number of SEFIs when irradiated with normal incidence gold (86MeV·cm^2/mg). These events led to a collapse of the output, BVOUT, toward ground. A total of 113 SEFI were encountered for the 16 irradiation runs of the A03 and A04 at a supply voltage of 3.0V. The total fluence for the runs was $1.6x10^8$ion/cm^2 and leads to an average cross-section of 71µm^2. The maximum cross-section was 130µm^2 (13 SEFI in $1x10^7$ion/cm^2). Only three SEFI were encountered when operating at 4.5V for a maximum cross-section of 20µm^2 and an average of cross-section of 1.9µm^2. There were no SEFI recorded for LET of 43MeV·cm^2/mg and lower. All but four of the SEFI at 3.0V exhibited immediate, spontaneous restart through either a hiccup or a single soft-start cycle. The four SEFI that did not immediately recover did recover after a few seconds under irradiation. It is speculated that the recoveries in these cases were due to subsequent ion strikes, so in actual operation a power cycle would be required to recover operation. These SEFI requiring power cycle then represent an average cross-section of 2.5µm^2. The power-good signal (B_PG) indicated the SEFI in all cases.

The three types of SEFI are presented in Figure 2 through Figure 4. The first two types represent spontaneous recovery events that exhibited a sudden shutdown of the buck output followed by a restart with a normal soft-start. In the first type (Figure 2), a normal hiccup cycle was encountered with a dummy soft-start cycle. In the second case (Figure 3), the dummy soft-start cycle was skipped, and the part went right into an active soft-start cycle. One SEFI of each of the first two types were seen at 4.5V operation in $1.6x10^8$ion/cm^2.

The power-cycle SEFI is third type of SEFI (Figure 4), and was rare with a cross-section of 2.5µm^2 at 3.0V and 86MeV·cm^2/mg. There was no spontaneous recovery from these events, and a power cycle is required to recover normal operation. The state at the end of Figure 4 persisted for at least another 7ms (the end of capture). There are other characteristics of these power-cycle SEFI that should be noted. The first is that the B_SS (Buck Soft-Start) stayed high even while BVOUT has collapsed. B_PG (Buck Power-Good) does however report that the SEFI occurred by being pulled low. It is also evident from the discharge rate of BVOUT that the low-side FET was on during the SEFI. This could lead to a destructive event if the output capacitance stored enough energy. In the

testing done, the 1.8V output into the 150µF capacitor with a 1µH inductor did not provide enough energy to damage the buck. One of these non-spontaneously recovering SEFI events was observed at 86MeV·cm^2/mg and 4.5V operation (in 1.6x10^{8}ions/cm^2), while none were seen for 43MeV·cm^2/mg and below.

The jeopardy of these power-cycle SEFI is therefore limited primarily to operation below 4.5V while in the presence of ions with a LET greater than 43MeV·cm^2/mg. Even at the extreme of 3.0V operation and 86MeV·cm^2/mg, the cross-section is a minuscule 2.5µm^2. Using a 43MeV·cm^2/mg threshold and a 2.5µm^2 saturation cross-section, CRÈME96 simulations predict events per device-day of less than 1.4x10^{-10} for Geosynchronous Earth Orbit (GEO). This translates to roughly an event once every twenty million years. The case of all SEFI (130µm^2), the bulk of which are self-recovering, predicts events once every fifteen thousand years. The SEFI do not seem to represent a practical limitation for the part given the improbability of the events.

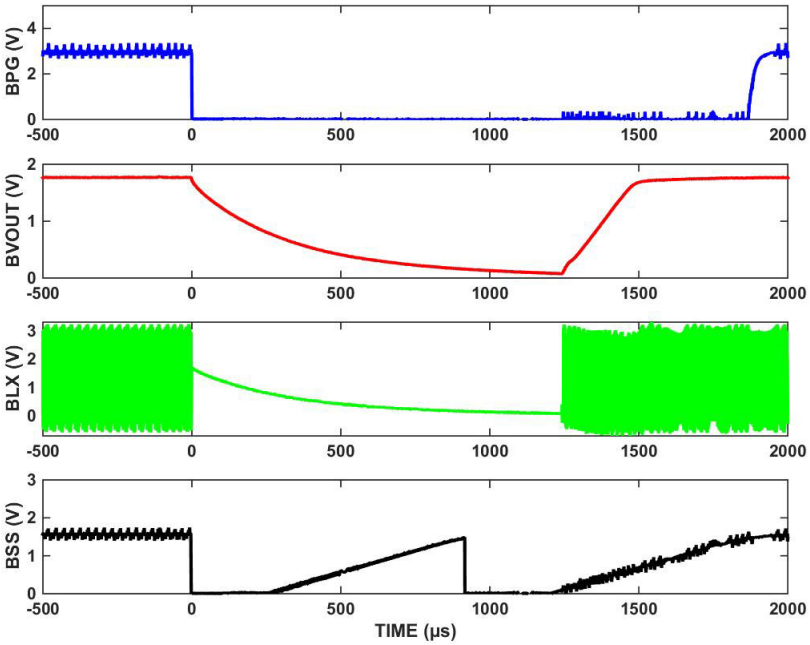


Figure 2. Normal Buck Hiccup SEFI

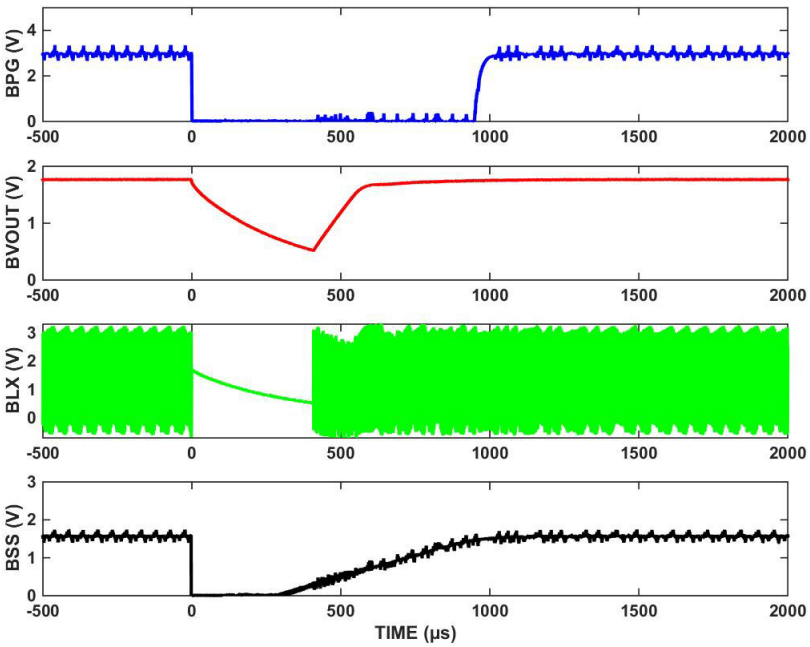


Figure 3. Buck Soft-Start SEFI

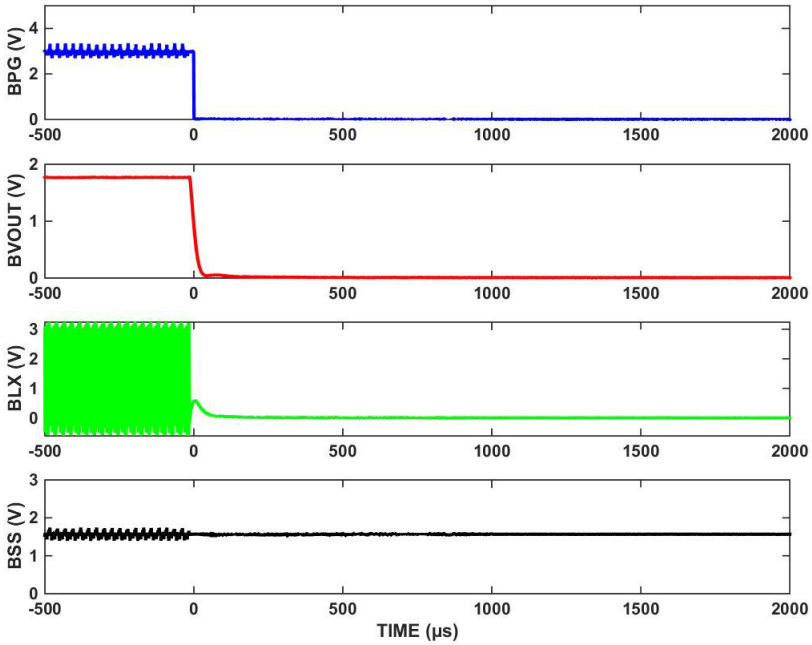


Figure 4. Power-Cycle Buck SEFI

Because the buck design is the same on ISL70005SEH versions A03 and A04, the results from SEE testing of these parts were combined for the buck SEFI. The combined SEFI numbers are presented in Table 4.

Table 4. Buck SEFI Type Counts for A03 and A04 SET Runs of 1x10^{7}ion/cm^2 at 86MeV·cm^2/mg and 3.0V

DUT-RUN	Hiccup SEFI		Soft-Start SEFI		Power Cycle SEFI	
	A03	A04	A03	A04	A03	A04
5-401	2	6	2	0	1	0
5-404	5	2	2	2	0	1
6-405	9	3	1	3	0	0
6-408	9	9	1	3	0	0
7-409	2	0	3	2	0	0
7-412	6	4	1	2	1	0
8-413	11	3	2	2	0	0
8-416	3	5	3	1	0	1
Mean X-Section (µm^2)	49.4		18.8		2.5	

2.4 Buck SET

Because storage of a captured oscilloscope trace takes a finite time, the number of captured events counted on the oscilloscope may not represent the total events caused by the raw fluence. The oscilloscope is blind to new SET events while it is storing the previous event. This can be corrected by subtracting from the exposure time the total time consumed by the storage of the captured events, which means the effective fluence tested was less than the raw irradiation fluence measured. A correction was applied to all the captures to extract effective cross-sections as outlined below.

- X-SECTION = (COUNT*1E8)/((FLUENCE/LIVE_TIME)*(LIVE_TIME-COUNT/RATE+COUNT*SPAN))
- X-SECTION = The calculated corrected cross-section of the captured SET events (µm^2)
- COUNT = Oscilloscope count of SET captures in an irradiation run
- FLUENCE = The raw fluence delivered in an irradiation run (ion/cm^2)
- LIVE_TIME = The time over which the FLUENCE was delivered (seconds)

- RATE = Rate at which the oscilloscope captures events when constantly triggered (captures/second)
- SPAN = The time span of the capture window (seconds)

To find the RATE, a 1MHz square wave was used as the triggering signal and the oscilloscopes were set up for the same conditions as used in the actual SET captures. Then, the oscilloscopes were set to capture and store traces for one minute, which was done five times for each oscilloscope configuration to be used in SET testing. These runs had considerable variation due to the oscilloscope system servicing background activities and so being unavailable to store captures. The average rates were used to calculate the corrected cross-sections. These corrections became large for cases where the rate of raw captures was large. The largest correction for A04 was 166% (from 32300µm^2 to 85900µm^2) for DUT18 at 86MeV·cm^2/mg in the LDO stand-alone configuration and -900mA load on the LDO.

The first configuration for testing the buck and LDO for SET had the buck supplying the LDO with both its power input (1.8V) and its reference voltage (0.9V) using a voltage divider. This configuration is the DDR configuration. The buck was operating at 1MHz with an inductor of 1µH. Both the buck and the LDO had output bulk capacitors of 150µF with a 30mΩ ESR specification (AVX TPME157K016R0030). The buck SETs were defined as a BVOUT deviation of ±36mV (±2%) from the equilibrium output. An oscilloscope was set to trigger on the ±36mV SET definition and the traces were stored for later analysis. The oscilloscope capture was from 20µs before the trigger point to 80µs after trigger. The cross-sections for the A04 as previously calculated for the buck with a ±36mV SET trigger on BVOUT are presented in Table 5. The cross-section corrections ranged from 3.6% to 21.3% for the 86MeV·cm^2/mg values.

Because one difference between condition groupings was the LDO current setting, the buck SET really had eight tests at each input voltage. All the buck SETs were captured with oscilloscope 1, so that potential source of difference was not active. However, each irradiation run did have a different oscilloscope trigger setting to accommodate small differences in the output voltage. Also, each of the first three LET represent different parts and boards tested, while the last two LET use the same DUTs.

Table 5. A04 Buck V_{OUT} ±36mV (±2%, Scope1) SET Cross-Sections with B_VOUT = 1.8V, B_IOUT = 1.8A

LET (MeV·cm^2/mg) =	86		43		20		8.5	
Conditions	**DUT**	**µm^2**	**DUT**	**µm^2**	**DUT**	**µm^2**	**DUT**	**µm^2**
V_{IN} = 3.0V L_IOUT = -1mA	5	5,560	9	2,151	13	0	13	--
	6	5,452	10	2,703	14	10	14	--
	7	8,783	11	5,227	15	0	15	--
	8	5,764	12	3,910	16	0	16	--
V_{IN} = 4.5V L_IOUT = -1mA	5	10,984	9	8,034	13	1,909	13	668
	6	10,372	10	7,465	14	2,246	14	750
	7	**12,969**	11	12,121	15	1,903	15	679
	8	12,372	12	8,416	16	1,833	16	885
V_{IN} = 4.5V L_IOUT = +1mA	5	11,022	9	7,209	13	1,868	13	770
	6	9,869	10	6,893	14	2,194	14	700
	7	11,670	11	12,243	15	2,082	15	669
	8	10,916	12	8,790	16	2,131	16	988
V_{IN} = 3.0V L_IOUT = +1mA	5	3,968	9	1,397	13	30	13	--
	6	4,841	10	2,296	14	0	14	--
	7	**5,951**	11	4,342	15	0	15	--
	8	4,223	12	3,128	16	0	16	--

Note: V_{IN} is all of B_VCC, L_VCC, and B_PVIN. Each entry represents 1x10^{7}ion/cm^2 of raw fluence at normal incidence. Bold entries provided example SET plots in Figure 5 through Figure 10.

It is interesting to note that the SET counts were higher for the case of a 4.5V supply than for a 3.0V supply. This likely results from the smaller buck duty-cycle at 4.5V supply (40% versus 60% at 3.0V) so that the same time

perturbation on the switching pulse represents a larger proportional change in duty-cycle when at 4.5V supply. Because the LDO load current was one of the conditions and should not impact the buck SET performance, there were only two buck conditions, with two irradiations for each DUT.

The SET cross-sections showed a strong dependency on the LET of the ions, but even at 8.5MeV·cm^2/mg the buck SET at ±36mV with a 4.5V supply had a cross-section of average 764µm^2. No LET threshold for the ±36mV buck SET with a 4.5V supply was identified except that it was below 8.5MeV·cm^2/mg. Extrapolating from the mean cross-section values leads to a projected threshold of 1.5MeV·cm^2/mg. The SETs at 3.0V supply were extremely small at 20MeV·cm^2/mg with an average of 5µm^2. The 3.0V condition was not tested at 8.5MeV·cm^2/mg due to the anticipation of even lower cross-section than at the higher LET.

The captured buck SET traces were post-processed with MATLAB® to extract characterization data on the SETs. To reduce the high frequency noise a 51-point Gaussian digital filter was applied to the captures (2ns sampling interval), providing a weighted moving average of the data. The collection of 544 SET for DUT7 at 86MeV·cm^2/mg with conditions of 3.0V and -1mA (bold text in Table 5) were processed to select the twenty extreme SET cases. The SEFI SET were removed from the collection of captures evaluated for SET. The extreme SET cases, ten largest and ten smallest as measured by the product of time and deviation, were composite plotted in Figure 5 on page 11 for the DUT7 case previously cited. The blue traces are for positive time-deviation products and the red traces are for negative time-deviation products. This collection of SET contained the largest magnitude SET encountered for the four DUTs tested at 86MeV·cm^2/mg over the 3.0V conditions. The choice of the time and deviation product to measure the SET was to eliminate large deviations without duration indicative of noise events. The largest positive SET was about 50mV and the largest negative SET was about 80mV. The peak of the SET events lasted less than 5µs but a 50µs recovery tail followed the actual SET.

The largest positive single SET is shown in Figure 6 on page 11 and has a maximum deviation of 52mV. (Figure 5 includes a SET that clearly is a double event, and this was not selected for further inspection). The event begins with what appears to be two full width B_LX pulses. This drives the output voltage higher. By the fourth pulse from the SET onset, the control loop generates a shortened pulse at the start of the recovery.

The largest negative SET is shown in Figure 7 on page 11 and has a deviation of -76mV. In this case, the SET begins with two shortened B_LX pulses that appear to be minimum width pulses. In response, the output voltage falls, and the control loop responds by lengthening the third, fourth, and fifth pulses. As with the positive SET, the actual SET event is limited to two B_LX pulses, then the control loop takes over and begins correcting for the SET.

The plots in Figure 5 through Figure 7 have complementing plots presented in Figure 8 through Figure 10 for the case of DUT7 at PVIN = 4.5V (1069 raw captures). The nature of the BVOUT SET changes slightly with the supply voltage increase from 3.0V to 4.5V. This change in voltage shifts the B_LX nominal duty-cycle from 60% down to 40% for the same BVOUT and skews the SET deviations more toward the positive as can be seen in Figure 8 on page 11 as compared to Figure 5. In Figure 5 (PVIN = 3.0 V), the largest event was in the negative direction, whereas in Figure 8 (PVIN = 4.5 V) the largest event was in the positive direction at 89mV. The extreme negative going deviation in Figure 8 was 64mV. Comparing the B_LX behaviors in Figure 6 and Figure 9 on page 11 reveals a strong similarity in the SET form on B_LX but shows a difference in the system response on BVOUT. Similarly, Figure 7 and Figure 10 show almost identical B_LX SET, but the different operating point manifests these SET slightly differently in the BVOUT response.

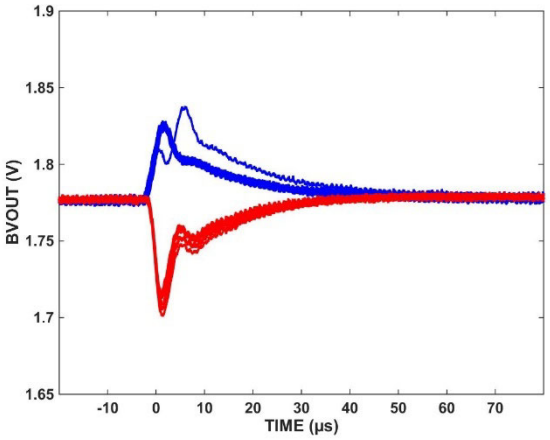


Figure 5. Extreme SET at 3.0V and LET = 86

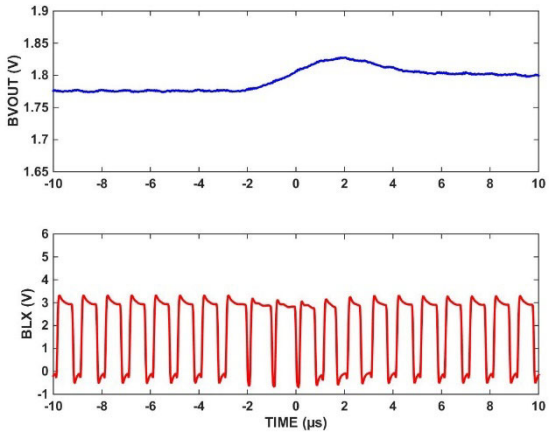


Figure 6. Maximum SET at 3.0V and LET = 86

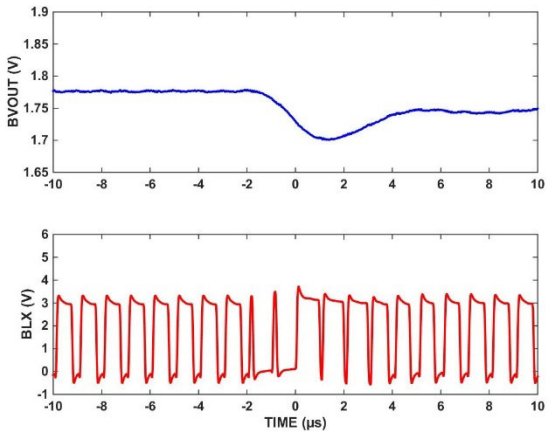


Figure 7. Minimum SET at 3.0V and LET = 86

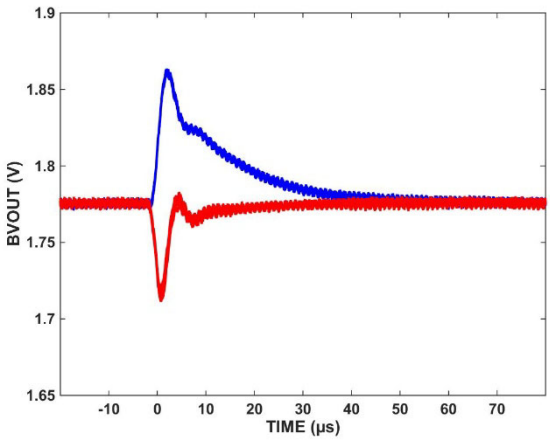


Figure 8. Extreme SET at 4.5V and LET = 86

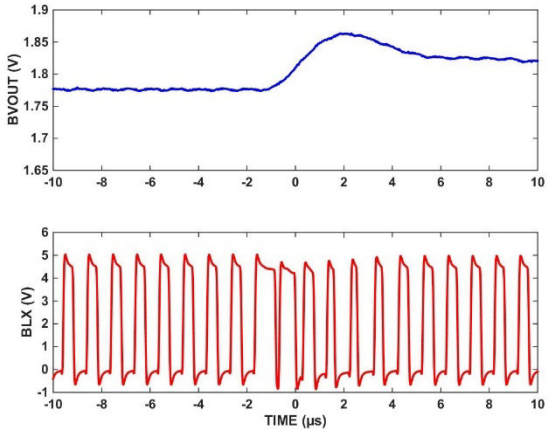


Figure 9. Maximum SET at 4.5V and LET = 86

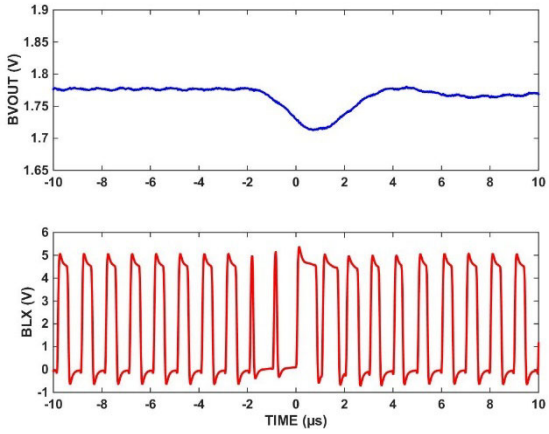
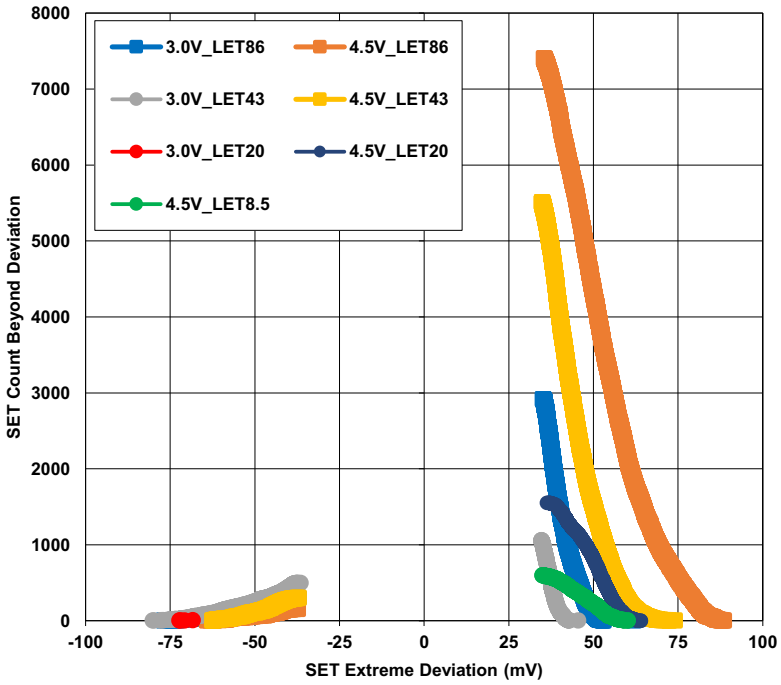


Figure 10. Minimum SET at 4.5V and LET = 86.

The buck SET extreme deviation distributions are shown in Figure 11. This plot counts the number of SET occurring, starting at the largest magnitudes both positive and negative, and plots the count on the vertical axis. The horizontal axis is the SET extreme deviation. Therefore, each SET is represented by a deviation and a cumulative SET count. The SET were defined as ±36mV deviation on the nominal 1.8V output. Smaller events were not counted nor captured. Each plotted condition represents $8x10^7$ion/cm^2 of raw fluence equally distributed over four DUTs. The negative going deviations were much less common than the positive deviations. The case for 86MeV·cm^2/mg and 4.5V supplies (4.5V_LET86) registered 7402 positive deviations for a raw cross-section of 9253µm^2. The 596 positive deviations for 8.5MeV·cm^2/mg irradiation at 4.5V indicate a raw cross-section of 750µm^2. The largest positive deviations ranged from 89mV for the 86MeV·cm^2/mg and 4.5V case to 60mV for the 8.5MeV·cm^2/mg and 4.5V case.



Note: Each condition represents the data for four DUTs each irradiated to $2x10^7$ion/cm^2 raw fluence at the LET indicated.

Figure 11. Buck SET Extreme Deviation Distributions by Test Conditions

The buck SET magnitudes and cross-sections both decreased with decreasing ion LET. At 8.5MeV·cm^2/mg only for the case of a 4.5V supply were any SET captured at the ±36mV trigger. The magnitudes ranged from the trigger value of 36mV to a maximum of about 60mV. The cross-section for all captured events was about 764µm^2. Although no negative SET are shown, this only means that the negative SET did not meet the trigger criteria of 36mV to be captured.

2.5 LDO SET

The LDO in the DDR configuration had the same type output capacitor as the buck (150µF, 30mΩ ESR, AVX TPME157K016R0030). The LDO SETs were monitored at the same time as the buck SET so some buck events cascaded to the LDO. The most notable were the buck SEFIs, and these were excluded from the LDO SET analysis. For the LDO, the SET definition was ±18mV (±2%) about the nominal equilibrium output of 0.9V. The capture counts with the correction as described for the buck SET in DDR configuration yielded the cross-sections in Table 6 on page 13. The cross-section corrections here were generally 1-2% for the 86MeV·cm^2/mg cases.

Table 6. LDO V_{OUT} ±18mV (Scope2) Raw SET Cross-Sections for DDR Configuration: B_VOUT = 1.8V, B_IOUT = 1.8A, L_OUT = 0.9V

LET (MeV·cm²/mg)	86		43		20		8.5	
Conditions	DUT	µm²	DUT	µm²	DUT	µm²	DUT	µm²
V_{IN} = 3.0V L_IOUT = -1mA	5	880	9	0	13	0	13	--
	6	972	10	0	14	0	14	--
	7	666	11	10	15	0	15	--
	8	1073	12	10	16	0	16	--
V_{IN} = 4.5V L_IOUT = -1mA	5	1198	9	110	13	0	13	0
	6	1956	10	70	14	0	14	0
	7	1115	11	90	15	0	15	0
	8	1537	12	80	16	0	16	0
V_{IN} = 4.5V L_IOUT = +1mA	5	1160	9	0	13	10	13	0
	6	1042	10	0	14	0	14	0
	7	1176	11	0	15	0	15	0
	8	1342	12	0	16	0	16	0
V_{IN} = 3.0V L_IOUT = +1mA	5	906	9	0	13	0	13	--
	6	1062	10	0	14	0	14	--
	7	1115	11	0	15	0	15	--
	8	1084	12	10	16	0	16	--

The LDO was also SET tested in the stand-alone configuration where the buck was disabled. The LDO was supplied with a L_VIN = 1.8V and used a gain of 1.5 from the internal 0.6V reference to output 0.9V. Therefore, the power input and LDO output were the same voltage as in the DDR configuration. The load currents tested in the stand-alone case were sourcing and sinking 900mA. The SET criterion was set to ±18mV deviation on the output for the stand-alone case, just as with the DDR. The capture counts with the correction as described for the buck SET in DDR configuration yielded the cross-sections in Table 7.

The cross-sections for the LDO in stand-alone configuration were much larger than for the DDR configuration. Because of the high capture rates, the cross-section corrections ranged up to the 166% case for the largest cross-section. There is no known reason to explain this difference in cross-sections; therefore, the stand-alone SET must be considered the worst-case cross-sections for the LDO. In both cases, SET (defined as ±18mV criterion) disappeared for 20MeV·cm²/mg irradiation. The DDR SETs were nearly gone at 43MeV·cm²/mg irradiation while the stand-alone case still produced considerable cross-sections.

Table 7. LDO V_{OUT} ±18mV (±2%, Scope1) SET Cross-Sections for the Stand-Alone Configuration

LET (MeV·cm²/mg) =	86		43		20		8.5	
Conditions	DUT	µm²	DUT	µm²	DUT	µm²	DUT	µm²
V_{IN} = 3.0V L_IOUT = -900mA	17	38140	21	19098	25	--	28	--
	18	85975	22	28931	26	0	25	--
	19	40280	23	29248	27	0	26	--
	20	33317	24	18960	28	0	27	--
V_{IN} = 4.5V L_IOUT = -900mA	17	37960	21	18417	25	0	28	--
	18	71252	22	29859	26	0	25	--
	19	32874	23	29226	27	0	26	--
	20	28240	24	18473	28	0	27	--

Table 7. LDO V_{OUT} ±18mV (±2%, Scope1) SET Cross-Sections for the Stand-Alone Configuration (Continued)

LET (MeV·cm²/mg) =	86		43		20		8.5	
Conditions	DUT	µm²	DUT	µm²	DUT	µm²	DUT	µm²
V_{IN} = 4.5V L_IOUT = +900mA	17	32159	21	16357	25	0	28	--
	18	49404	22	21856	26	0	25	--
	19	28134	23	15497	27	0	26	--
	20	25976	24	15097	28	0	27	--
V_{IN} = 3.0V L_IOUT = +900mA	17	31337	21	18525	25	0	28	--
	18	58744	22	29162	26	0	25	--
	19	29047	23	15189	27	0	26	--
	20	25276	24	15401	28	0	27	--

The entries for DUT18 (in red text) were suspicious in their large SET counts and cross-sections. Post-irradiation inspection of the board for DUT18 revealed that the LDO output capacitor had a cold solder joint. This contributed extra series resistance to the output capacitance. The impact of this extra resistance can easily be seen in Figure 12. DUT18 had a unique distribution that included significantly more SET and significantly larger SET. DUT18 was omitted from further SET analysis for the stand-alone LDO configuration.

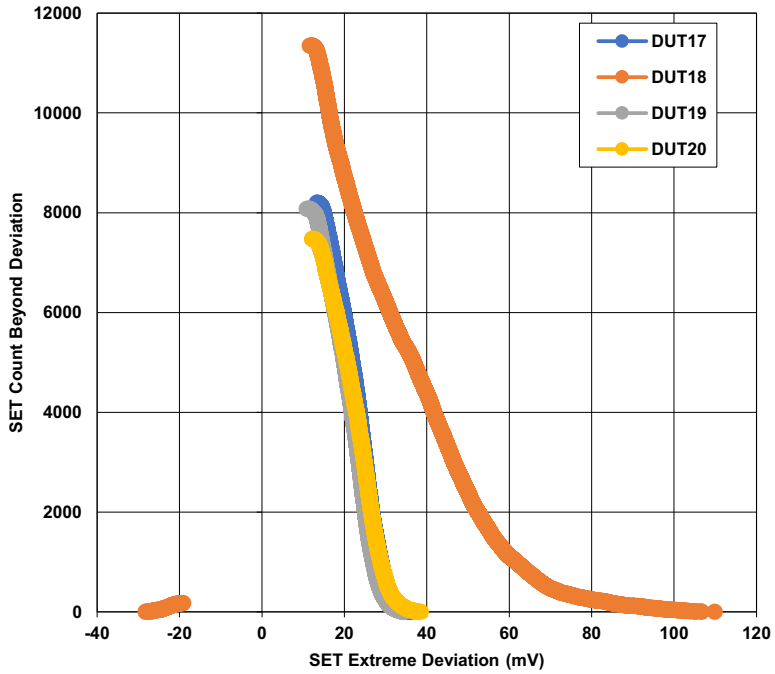


Figure 12. SET Extreme Deviation Composite Distributions by DUT for the 86MeV·cm²/mg Irradiations of the Stand-Alone LDO

Post processing the LDO SET with a MATLAB® routine included a 51-point Gaussian digital filter (2ns sample time). A composite plot of the extreme filtered SET (ten positive and ten negative) is plotted in Figure 13 on page 15 for the DDR configuration souring 1mA with a 4.5V supply. The SET deviations range up to about 30mV in Figure 13, and no negative deviations were captured. As always, the lack of negative deviations merely indicates that no negative deviations attained the trigger level of 18mV.

The composite plot of the extreme SET for the stand-alone LDO case with 3.0V supply and -900mA load at 86MeV·cm²/mg is presented in Figure 14 on page 15. In this case the positive SET deviations go up to 34mV with a minimum of 13mV, and again no negative deviations are captured. Note also that the noise created by the buck is clearly visible in Figure 13 for the DDR case but does not appear in Figure 14 for the stand-alone configuration.

The SET deviation distributions for the four bias conditions of the DDR configuration are presented in Figure 15 on page 15. Each bias condition has combined in it the SET deviations for the four DUTs tested. Both bias variables appear to exert an influence on the SET populations. The sense of the current load, either ±1mA, determines the sense of the resulting SET deviations. Sourcing current (+1mA) leads to positive deviations, while sinking current (-1mA) leads to negative deviations. This would appear to be the result of which side of the dead zone the part is initially biased. The dead zone is an output voltage region inside of which neither sourcing nor sinking correction current is imposed. For sourcing current (+1mA) the part is biased at the low side of the dead zone leaving an extra 10mV for a positive SET to move before a correction response is encountered. Conversely, for sinking current (-1mA) the part is biased on the high side of the dead zone and a negative SET has the dead zone width added to it. The L_VCC supply voltage also appears to influence the magnitude and probability of the SET. The supply of 4.5V distributions go to ±30mV whereas the 3.0V cases only go to about ±20mV deviations.

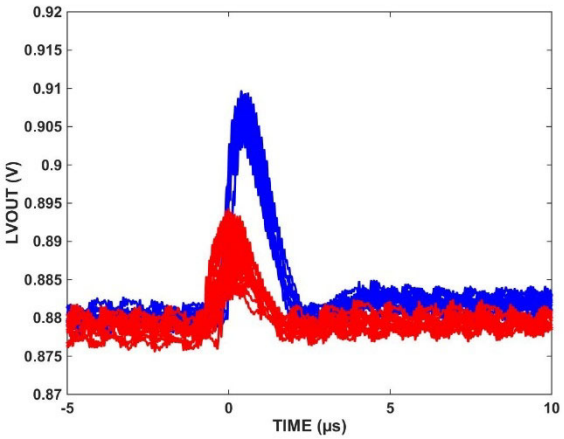


Figure 13. LDO-DDR Extreme SET for 4.5V and Sourcing 1mA with 86MeV·cm^2/mg (DUT6)

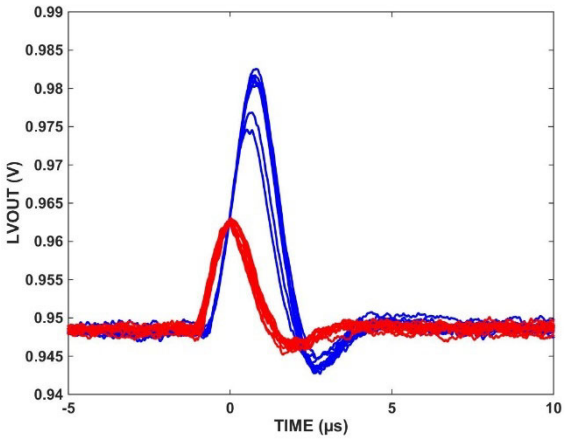
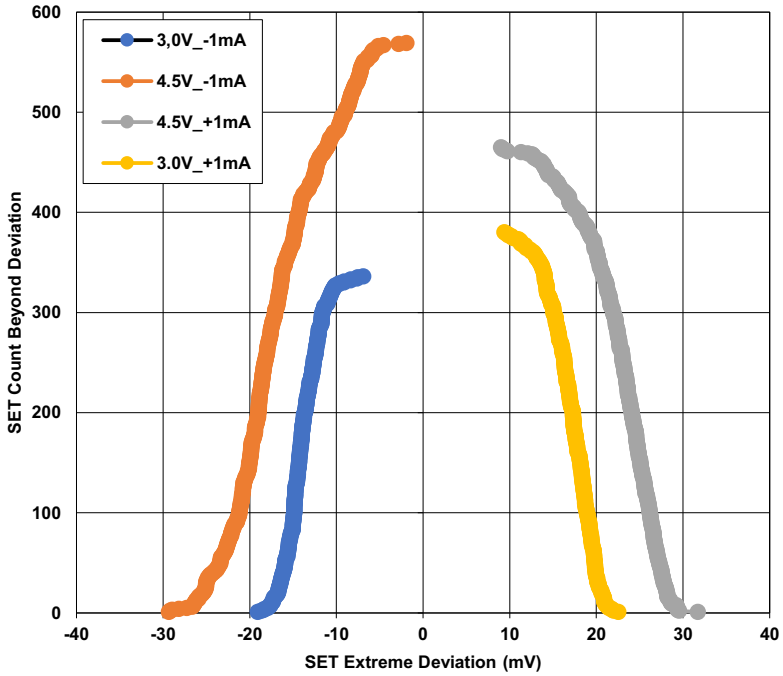


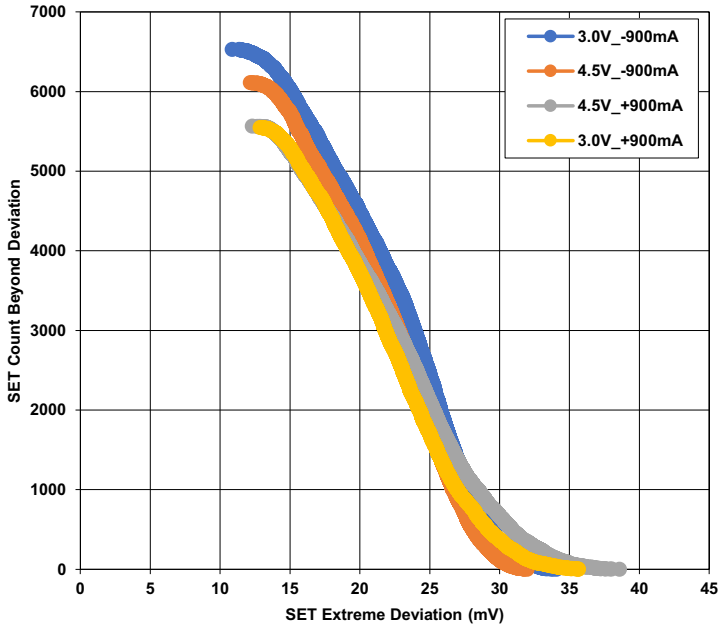
Figure 14. LDO Stand-Alone Extreme SET for 3.0V and Sinking 900mA with 86MeV·cm^2/mg (DUT17)



Note: Each case is the composite results for four parts tested.

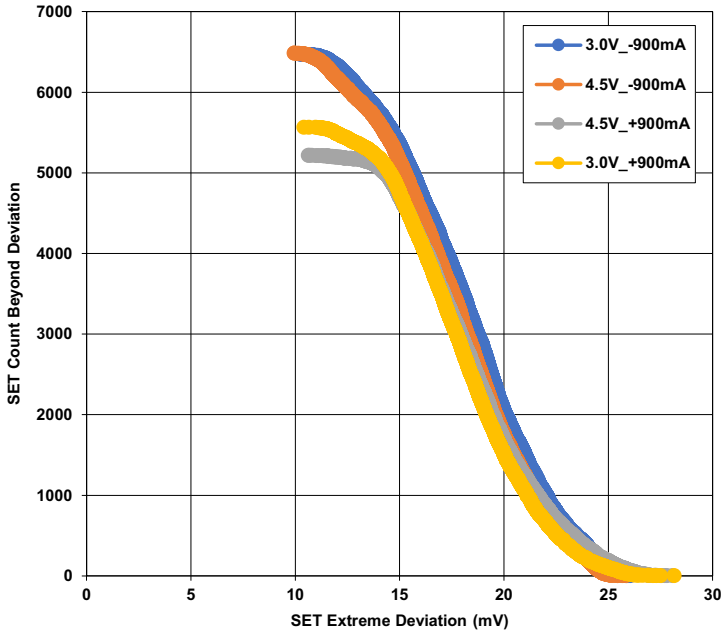
Figure 15. LDO-DDR SET Magnitude Distributions for the Four Bias Cases

Figure 16 shows the SET distributions for the four biasing conditions of the stand-alone LDO testing based on the data for the three good DUTs. All SET deviations for all four biases were in the positive sense. This contrasts with the data taken at low load currents for the DDR configuration. In fact, the biasing changes made little if any difference to the SET distributions obtained. The largest SET seen was 39mV with captures going down to about 13mV of deviation. At 43MeV·cm^2/mg the maximum SET deviation was 28mV.



Note: Each case is the composite results for three parts tested (DUT17, DUT19, DUT20) at 1x10^7 ion/cm^2 for each part.

Figure 16. LDO Stand-Alone SET Magnitude Distributions for the Four Bias Cases at 86MeV·cm^2/mg



Note: Each case is the composite results for three parts tested (DUT17, DUT19, DUT20) at 1x10^7 ion/cm^2 for each part.

Figure 17. LDO Stand-Alone SET Magnitude Distributions for the Four Bias Cases at 43MeV·cm^2/mg

3. Discussion and Conclusions

The ISL70005SEH proved to be SEB and SEL immune up to a supply voltage of 6.0V for irradiation with normal incidence Au for 86MeV·cm^2/mg. The testing was done with a case temperature of 125°C ±10°C and a buck load of approximately 3.5A at 3.15V, and an LDO load of ±1.2A at 0.6V output. The parts proved to be SEB and SEL immune to a supply voltage of 6.2V when irradiated with normal incidence silver for 43MeV·cm^2/mg under the same operating conditions. No SEL events were observed. SEB limits were set by permanent changes observed in the buck standby current.

Exceedingly rare buck SEFI events (interruption in the switching and collapse of the output voltage) were observed during SET testing at 86MeV·cm^2/mg. These SEFI registered a maximum cross-section of 130µm^2. The mean cross-section obtained was 71µm^2. No SEFIs were observed at 43MeV·cm^2/mg up to 1.6x10^{8}ion/cm^2. Of these SEFI events, 96% (109/113) recovered spontaneously with a soft-start cycle. Using a 43MeV·cm^2/mg threshold and a 130µm^2 saturation cross-section, CRÈME96 predicts that these buck SEFI should occur less than once every fifteen thousand years in geosynchronous Earth orbit.

Buck SET as defined by a ±36mV (±2%) deviation trigger on the 1.8V output produced event cross-sections up to 22,206µm^2 at 86MeV·cm^2/mg. The range of the SET perturbations was +90mV to -80mV (+5.0% and -4.4%) with the 150µF (30mΩ ESR) and 1µH output filter and 1MHz operation. Larger output filter components are expected to proportionally reduce the SET perturbations as long as the ESR reduces as well. The SET with gold irradiation were limited to three B_LX pulses at the 1MHz switching frequency. The perturbed pulses were either minimum or maximum duty-cycle. At argon with an LET of 8.5MeV·cm^2/mg, the ±36mV cross-section dropped to a maximum of 988µm^2 and the maximum perturbation dropped to 60mV (3.3%). With argon, the B_LX transients were limited to two precipitating pulses, again either minimum or maximum duty-cycle at the 1MHz switching frequency.

The SET for the LDO had different results depending on how the parts were operating. In all cases, the SET definition was a ±18mV (±2%) change in the nominal 0.9V output. In the DDR configuration at 86MeV·cm^2/mg, the LDO exhibited a maximum cross-section of 1956µm^2. However, in the stand-alone configuration the LDO was found to have a maximum cross-section of 40280µm^2. These results were obtained with output capacitors of 150µF (30mΩ ESR). As with the buck it is expected that a larger capacitance and smaller ESR reduce the SET magnitudes. This difference between DDR and stand-alone results is not understood. Many SET were close to the trigger definition of ±18mV and small changes in magnitude would lead to large changes in captured SET counts and therefore differing calculated cross-sections. The ±18mV LDO SET disappeared entirely at 20MeV·cm^2/mg irradiation.

4. Revision History

Rev.	Date	Description
1.01	Nov 4, 2022	Updated header on page 1.
1.00	Oct 21, 2019	Initial release

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