ISL70023SEH, ISL73023SEH

Introduction

This report documents the results of low and high dose rate total dose testing and subsequent high temperature biased annealing of the ISL70023SEH and ISL73023SEH 100V, 60A N-Channel enhancement mode GaN transistor. The tests were conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of dose rate, bias, or anneal sensitivity. Parts were irradiated under three different bias conditions:

- T_{OFF} – gate and source grounded; drain connected to 84V ±4V
- T_{ON} – gate connected to 4.5V ±10%; drain and source connected to ground
- All pins grounded at Low Dose Rate (LDR) and at High Dose Rate (HDR)

Figure 2, Figure 3, and Figure 4 show the bias schematics for each of these test conditions. The ISL70023SEH is rated at 100krad(Si) at HDR (50rad – 300rad(Si)/s) and at 75krad(Si) at LDR (0.01rad(Si)/s) and is acceptance tested on a lot-by-lot basis to these limits. The ISL73023SEH is rated at 75krad(Si) at LDR (0.01rad(Si)/s) and is acceptance tested to these limits. Both parts use the same die and the dataset reported in this document applies to both.

Product Description

The ISL70023SEH is a 100V N-channel enhancement mode GaN power transistor. Applications for these devices include commercial aerospace, medical, and nuclear power generation. GaN's exceptionally high electron mobility and low temperature coefficient allows for a very low $r_{DS(ON)}$ of 5mΩ (typical), while its lateral device structure and majority carrier diode provide an exceptionally low Q_G of 14nC (typical) and zero Q_{RR}. The end result is a device that can operate at a higher switching frequency with more efficiency while reducing the overall solution size.

The ISL70023SEH operates across the -55°C to +125°C temperature range and is offered in a hermetically sealed Surface Mount Device (SMD) 4-pin package. Manufacturing in a MIL-PRF-38535 like flow results in best-in-class power transistors, which are ideally suited for high reliability applications.

Related Literature

For a full list of related documents, visit our website

- ISL70023SEH, ISL73023SEH product pages
- MIL-STD-883 Test Method 1019

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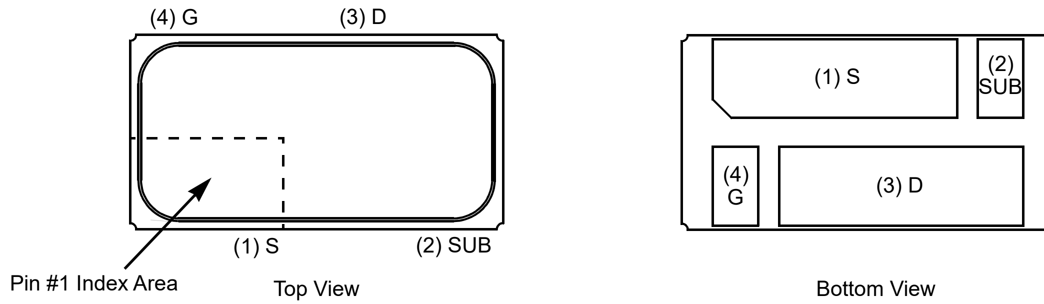
1. Pin Configuration



Note: The ESD triangular mark is indicative of Pin #1. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

Figure 1. ISL70023SEH Pinout Configuration

Table 1. ISL70023SEH Pin Descriptions

Pin Number	Pin Name	Description
1	S	Source connection for the GaN FET.
2	SUB	Substrate connection for the GaN FET, which is internally shorted in to source. Tie this pin to source on the PCB.
3	D	Drain connection for the GaN FET.
4	G	Gate connection for the GaN FET. Minimize trace inductance from driver to reduce over-stressing the gate.
NA	Lid	Internally tied to the source pin.

2. Test Description

2.1 Irradiation Facilities

HDR testing was performed at 167.5rad(Si)/s using a Gammacell industry standard irradiator located in the Palm Bay, Florida Renesas facility. LDR testing was performed at 0.01rad(Si)/s using the Renesas Palm Bay Hopewell Designs N40 panoramic irradiator. Both irradiators use PbAl spectrum hardening filters to shield the test board and devices under test against low energy secondary gamma radiation. Biased irradiation and annealing were performed on all samples following irradiation, at +100°C for 168 hours in a small temperature chamber.

2.2 Test Fixturing

Figure 2, Figure 3, and Figure 4 show the configurations used for biased irradiation at both dose rates.

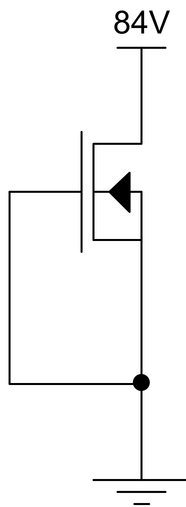


Figure 2. ISL70023SEH TID Bias Schematics (T_{OFF})

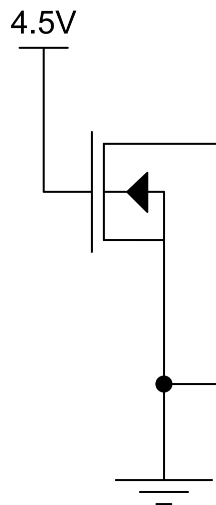


Figure 3. ISL70023SEH TID Bias Schematics (T_{ON})

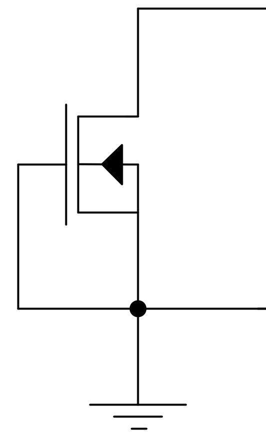


Figure 4. ISL70023SEH TID Bias Schematics (Grounded)

2.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature outside the irradiator, using production Automated Test Equipment (ATE) with datalogging at each downpoint.

2.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 20 samples irradiated at LDR under T_{OFF} bias, 20 samples irradiated at LDR under T_{ON} bias, 20 samples irradiated at LDR with all pins grounded, 16 samples irradiated at HDR under T_{OFF} bias, 16 samples irradiated at HDR under T_{ON} bias, and 16 samples irradiated at HDR with all pins grounded. At anneal, the parts irradiated with all leads grounded were split, with half of units biased in the T_{OFF} configuration and half of the units biased in the T_{ON} configuration. The worst case of the two data points was plotted. Three control units were used.

The ISL70023SEH HDR samples were drawn equally from two wafer lots: QUALJSC2 and QUALJSC3. The LDR samples were drawn equally from wafer lots QUALJSD3 and QUALJSD4. All samples were packaged in the hermetic 42mm^2 4-pin surface mount package (code J4.A). Samples were processed through the standard burn-in cycle before irradiation.

2.5 Downpoints

Downpoints for the LDR tests were 0, 10, 30, 50, and 75krad(Si). Downpoints for the HDR tests were 0, 30, 50, 100, and 150krad(Si). All irradiations were followed by a 168 hour high temperature anneal at +100°C under bias.

3. Test Results

3.1 Attributes Data

Table 2 summarizes the results of the ISL70023SEH total dose testing.

Table 2. ISL70023SEH Total Dose Test Attributes Data

Dose Rate (rad(Si)/s)	Bias	Sample Size	Downpoint	Pass[1]	Fail
0.01	T_{OFF}, Figure 2	20	Pre-irradiation	20	
			10krad(Si)	20	0
			30krad(Si)	20	0
			50krad(Si)	20	0
			75krad(Si)	20	0
			Anneal	20	0
0.01	T_{ON}, Figure 3	20	Pre-irradiation	20	
			10krad(Si)	20	0
			30krad(Si)	20	0
			50krad(Si)	20	0
			75krad(Si)	20	0
			Anneal	20	0
0.01	GND, Figure 4	20	Pre-irradiation	20	
			10krad(Si)	20	0
			30krad(Si)	20	0
			50krad(Si)	20	0
			75krad(Si)	20	0
			Anneal	20	0
167.5	T_{OFF}, Figure 2	16	Pre-irradiation	16	
			10krad(Si)	16	0
			30krad(Si)	16	0
			50krad(Si)	16	0
			75krad(Si)	16	0
			Anneal	16	0

Table 2. ISL70023SEH Total Dose Test Attributes Data (Cont.)

Dose Rate (rad(Si)/s)	Bias	Sample Size	Downpoint	Pass[1]	Fail
167.5	T_{ON}, Figure 3	16	Pre-irradiation	16	
			10krad(Si)	16	0
			30krad(Si)	16	0
			50krad(Si)	16	0
			75krad(Si)	16	0
			Anneal	16	0
167.5	GND, Figure 4	16	Pre-irradiation	16	
			10krad(Si)	16	0
			30krad(Si)	16	0
			50krad(Si)	16	0
			75krad(Si)	16	0
			Anneal	16	0

1. A Pass indicates a sample that passes all datasheet limits.

3.2 Key Parameter Listing

Figure 3 lists 11 key parameters that are indicative of part performance. These parameters are plotted in Figure 5 through Figure 15. All limits are taken from the *ISL70023SEH datasheet*. See the datasheet for further detail.

Table 3. ISL70023SEH Key Total Dose Datasheet Parameters (T_A = 25°C)

Figure	Symbol	Parameter	Limit, Low	Limit, High	Unit	Conditions
5	I_{DSS}	Drain-Source Leakage Current	-	1.1	mA	V_{DS} = 80V, V_{GS} = 0V
6	I_{GSX}	Drain-Gate Leakage Current	-0.7	-	mA	V_{DS} = 80V, V_{GS} = 0V
7	I_{GSS}	Gate-Source Forward Leakage	-	9	mA	V_{GS} = 5V
8		Gate-Source Reverse Leakage	-0.7	-	mA	V_{GS} = -4V
9	$V_{GS(th)}$	Gate Threshold Voltage	0.7	2.5	V	V_{DS} = V_{GS}, I_D = 12mA
10	$r_{DS(ON)}$	Drain-Source On Resistance	-	12	mΩ	V_{GS} = 5V, I_D = 25A
11	V_{SD}	Source-Drain Forward Voltage	0.7	3.0	V	I_S = 0.5A, V_{GS} = 0V
12	Q_{GD}	Gate-Drain Charge	-	12	nC	V_{DS} = 50V, I_D = 25A
13	Q_{GS}	Gate-Source Charge	-	5	nC	V_{DS} = 50V, I_D = 25A
14	Q_G	Total Gate Charge	-	25	nC	V_{DS} = 50V, I_D = 25A, V_{GS} = 5V
15	C_{OSS}	Output Capacitance	-	1250	pF	V_{DS} = 50V, V_{GS} = 0V

3.3 Key Parameters Variables Data

The plots in Figure 5 through Figure 15 illustrate the TID response of the key datasheet parameters outlined in Key Parameter Listing. The plots show the average tested values of the key parameters shown in Table 3 as a function of total dose for each of the three irradiation conditions (T_{OFF}, T_{ON}, and GND) at HDR and LDR. For example, the legend LDR_Toff indicates the average LDR response for parts biased in the T_{OFF} configuration. PA_L on the graphs stands for Post-Anneal Low Dose and PA_H represents the Post-Anneal High Dose results. Note that the worst case of the two bias configurations of the samples that were irradiated with all terminals grounded, as described in Experimental Matrix, is plotted. The plots also include error bars at each downpoint, representing the minimum and maximum measured values of the samples, although in some plots the error bars are not visible due to their values as compared to the scale of the graph. Also, in some plots the datasheet limit, which are set by temperature, are not shown to better display the actual measurements, which are orders of magnitude less.

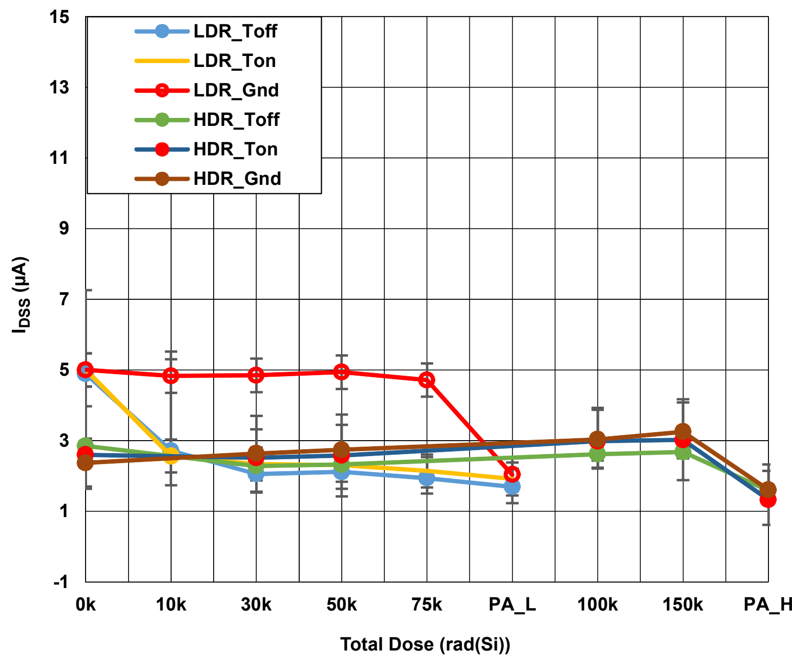


Figure 5. ISL70023SEH drain-to-source leakage current, I_{DSS}, with V_{DS} = 80V and V_{GS} = 0V, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit, which is set by temperature, is 1100µA maximum, but is not shown to better display the actual measurements, which are orders of magnitude less.

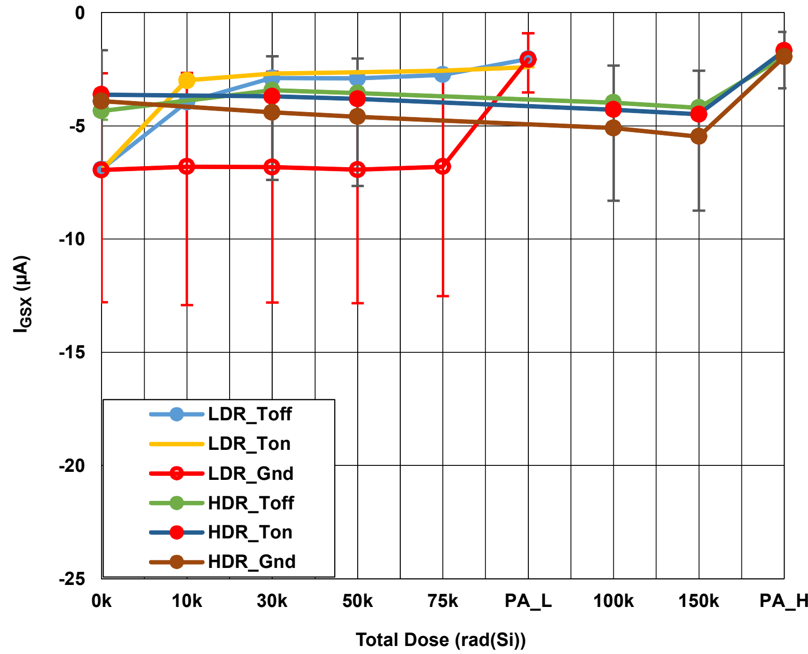


Figure 6. ISL70023SEH drain-to-gate leakage current, I_{GSX}, with V_{DS} = 80V and V_{GS} = 0V, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit, which is set by temperature, is -700µA minimum, but is not shown to better display the actual measurements, which are orders of magnitude less.

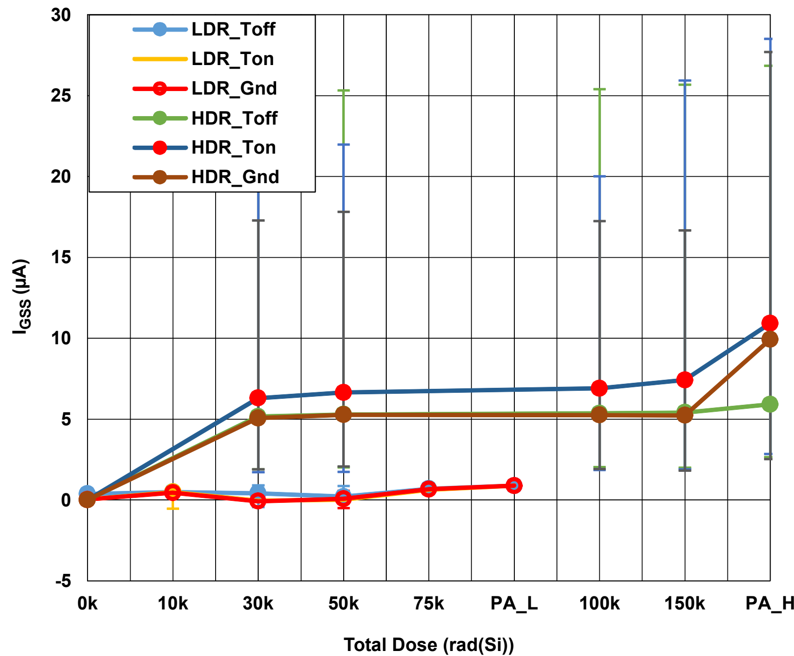


Figure 7. ISL70023SEH gate-to-source forward leakage current, I_{GSS}, with V_{GS} = 5V, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit, which is set by temperature, is 9000µA maximum, but is not shown to better display the actual measurements, which are orders of magnitude less.

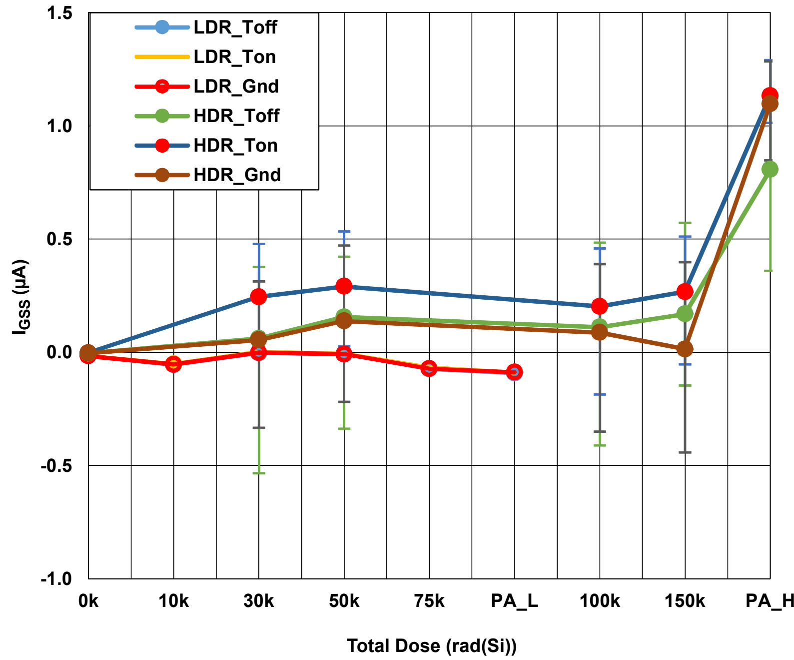


Figure 8. ISL70023SEH gate-to-source reverse leakage current, I_{GSS}, with V_{GS} = -4V, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit, which is set by temperature, is -700µA minimum, but is not shown to better display the actual measurements, which are orders of magnitude less.

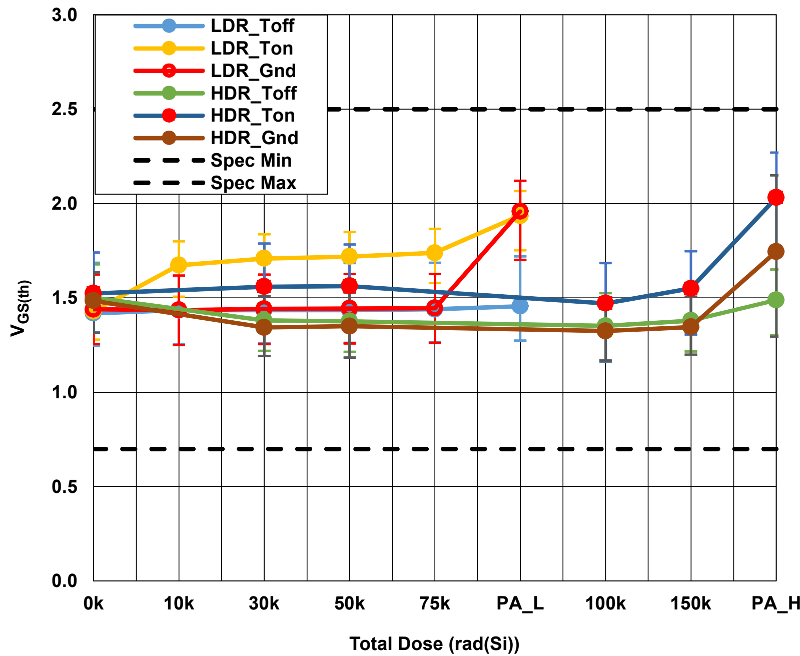


Figure 9. ISL70023SEH gate threshold voltage, $V_{GS(th)}$, with V_{DS} = V_{GS}, I_{DS} = 12mA, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limits are 0.7V minimum and 2.5V maximum.

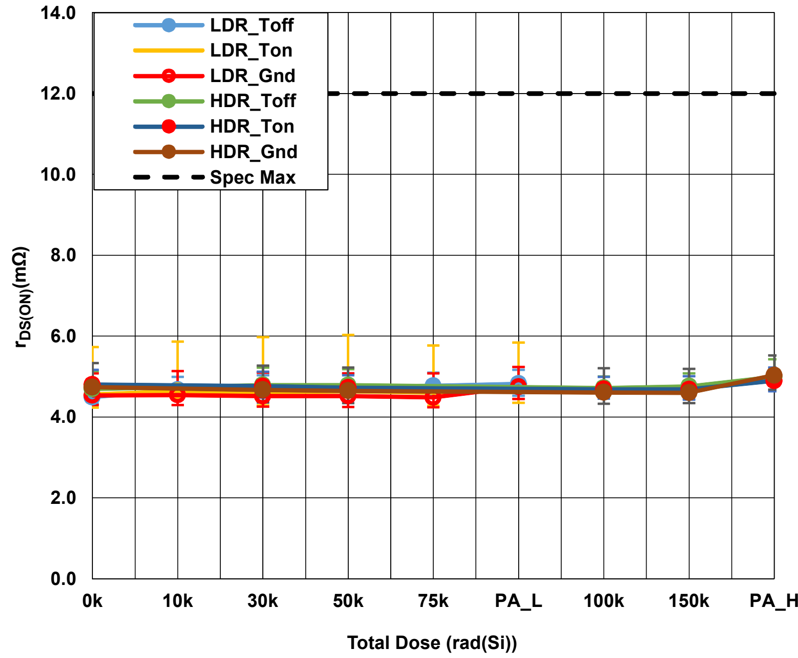


Figure 10. ISL70023SEH drain-to-source On-Resistance, $r_{DS(ON)}$, with V_{GS} = 5V, I_D = 25A, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit is 12mΩ maximum.

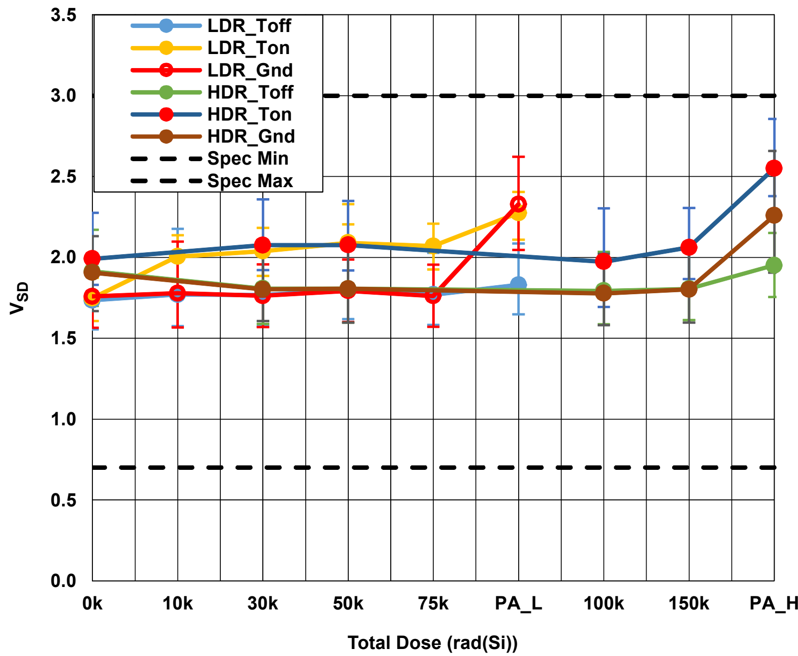


Figure 11. ISL70023SEH source-to-drain forward voltage, V_{SD}, with I_S = 0.5A, V_{GS} = 0V, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limits are 0.7V minimum and 3.0V maximum.

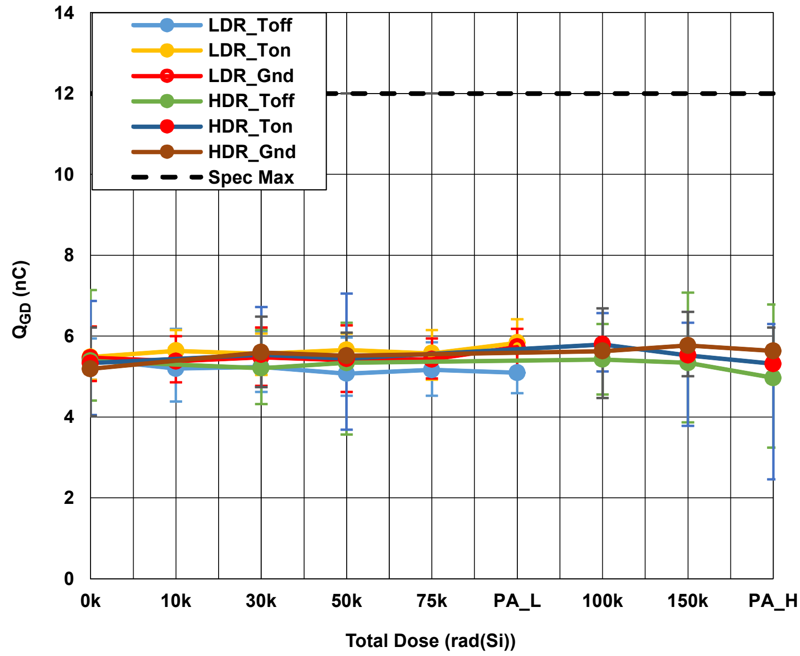


Figure 12. ISL70023SEH gate-to-drain charge, Q_{GD}, with V_{DS} = 50V, I_D = 25A, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit is 12nC maximum.

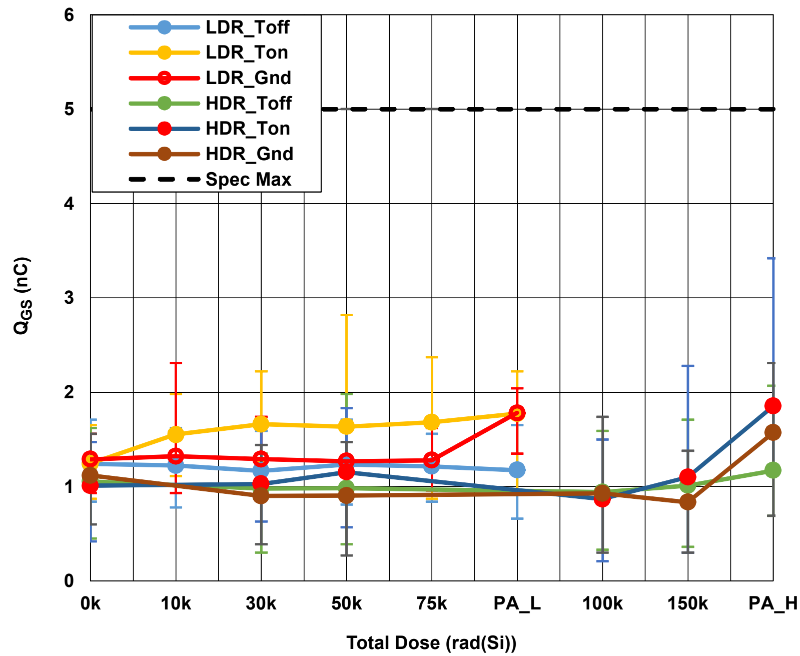


Figure 13. ISL70023SEH gate-to-source charge, Q_{GS}, with V_{DS} = 50V, I_D = 25A, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit is 5nC maximum.

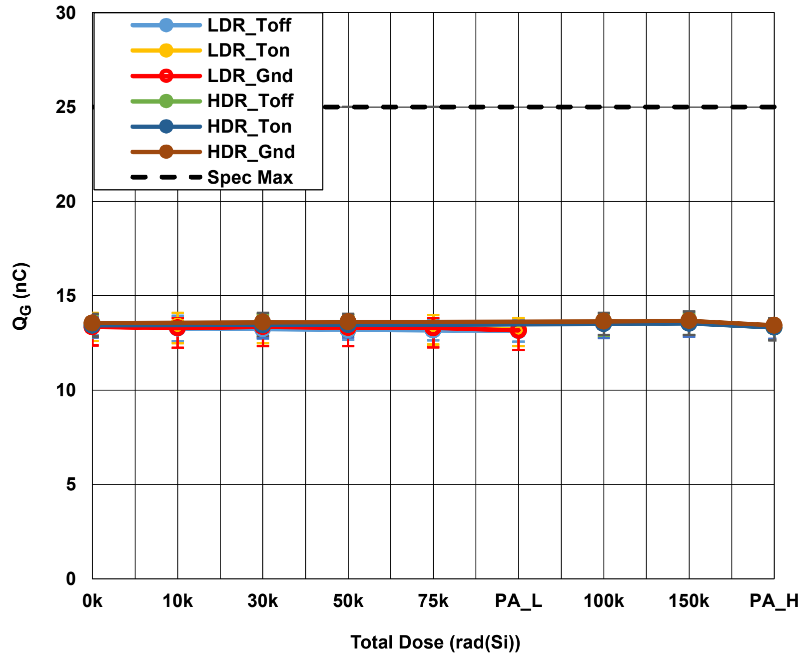


Figure 14. ISL70023SEH total gate charge, Q_G, with V_{DS} = 50V, I_D = 25A, V_{GS} = 5V, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit is 25nC maximum.

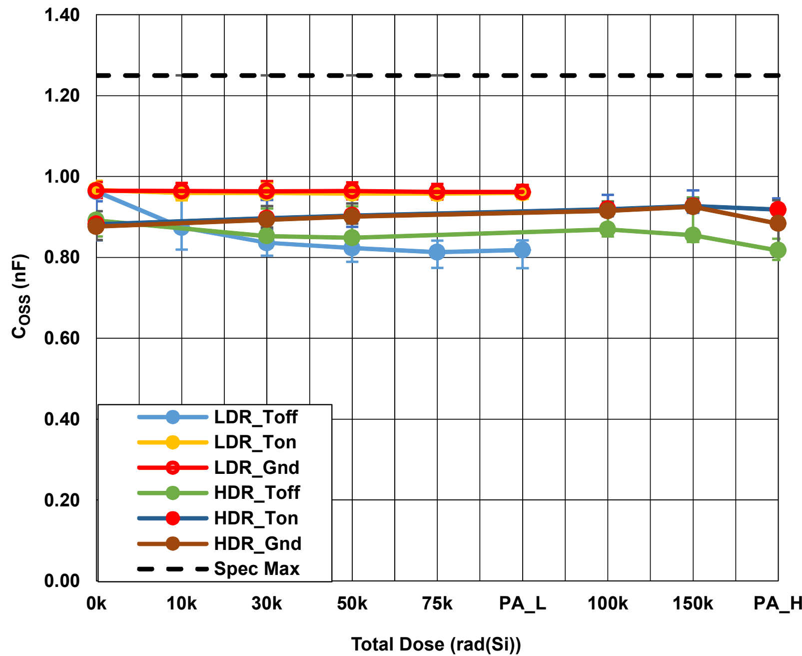


Figure 15. ISL70023SEH output capacitance, C_{OSS}, with V_{DS} = 50V, V_{GS} = 0V, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit is 1250pF maximum.

4. Discussion and Conclusion

We report the results of an LDR and HDR total dose test of the ISL70023SEH 100V, 60A N-Channel enhancement mode GaN transistor. All irradiations were followed by a 168-hour anneal at +100°C under bias. Attributes Data summarizes the attributes data for the test. Key Parameter Listing summarizes the 11 critical parameters for the part. Key Parameters Variables Data provides plots of the total dose and anneal response for the critical parameters.

All parameters remained well within the datasheet limits at all downpoints and showed only slight differences in total dose response between LDR and HDR irradiations (see Figure 7 and Figure 9). In Figure 9 and Figure 13, the LDR_Ton configuration response differs somewhat from the others. Anneal sensitivity is present in some parameters, with the samples biased in the T_{ON} configuration, including the parts that were exposed in the GND bias configuration, showing more shift than the parts biased in the T_{OFF} configuration.

This anneal sensitivity is most clearly illustrated in Figure 9 and Figure 11, where the slightly negative shifts of the threshold voltage and source-to-drain forward voltage, respectively, during irradiation change to a positive shift during anneal. These negative shifts during irradiation are likely caused by trapped holes in the AlGaN layer, and the positive post-anneal shifts are probably caused by the release of those trapped holes, and/or their neutralization be electrons from the channel. The T_{ON} bias configuration exacerbates this shift.

The gate-to-source charge (Figure 13) also reflects these exposure-bias differences and post anneal shifts. Because this parameter is extracted from the device's voltage/current measurements, this response is expected.

5. Revision History

Rev.	Date	Description
1.00	Nov 28, 2022	Applied new template. Added ISL73023SEH information on page 1.
0.00	Dec 4, 2017	Initial release

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TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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