ISL71148SLH

Low Dose Rate Total Ionizing Dose Testing of the ISL71148SLH 8-Channel 14-Bit 900/480ksps SAR ADC

Introduction

This report summarizes the results of the low dose rate (LDR) total ionizing dose (TID) testing of the ISL71148SLH, a radiation hardened 8-channel 14-bit 900/480ksps successive approximation register (SAR) analog-to-digital converter (ADC). The test was conducted to assess the total dose hardness of the part and to provide an estimate of the bias sensitivity. Parts were irradiated either under bias or with all pins grounded at an LDR (0.01rad(Si)/s) to 100krad(Si) followed by a 168-hour biased anneal at 100ºC. The ISL71148SLH is rated to 75krad(Si) at LDR and is acceptance tested on a wafer-by-wafer basis to the datasheet limits.

Product Description

The ISL71148SLH is a radiation hardened 8-channel high precision 14-bit, 900/480ksps SAR ADC. The ADC core is preceded by eight fully differential analog input channels, a buffered 8-to-1 multiplexer, and a Programmable Gain Amplifier (PGA). The device features a peak signal-to-noise ratio of 83.2dBFS when operating at 900ksps. With the PGA enabled, sampling rates up to 480ksps are supported. The PGA can be bypassed to increase the sample rate to 900ksps.

The product features 900/480ksps throughput with no data latency, excellent linearity, and dynamic accuracy. The ISL71148SLH offers a high-speed SPI-compatible serial interface that supports logic ranging from 2.2V to 3.6V using a separate digital I/O supply pin.

The ISL71148SLH offers a separate low-power mode (LPM) pin that reduces power dissipation at lower sample rates. An external reference with a supported input range of 2.4V to 2.6V determines the analog input signal range.

The ISL71148SLH operates across the military temperature range from -55ºC to +125ºC and is available in a 48-lead Thin Quad Flat-Pack (TQFP). The pin assignments for the ISL71148SLH are shown in Figure 1, and the pin descriptions are shown in Table 1.

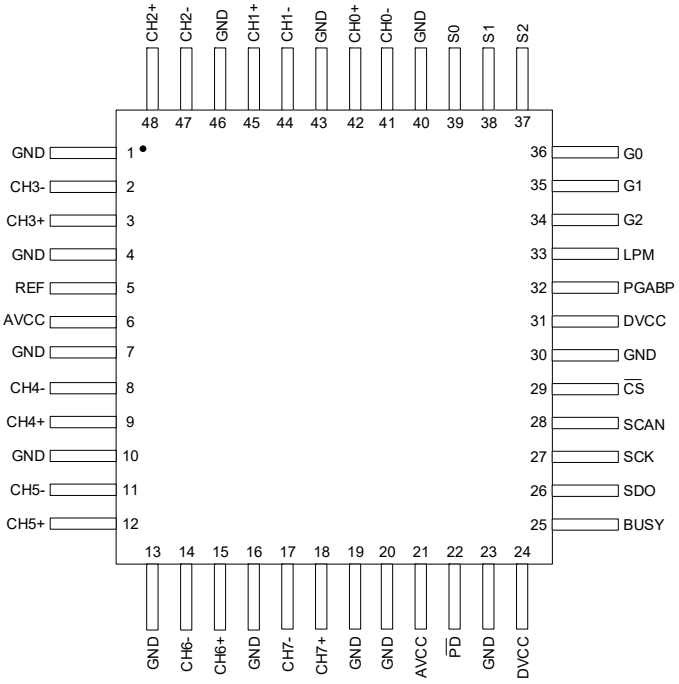


Figure 1. ISL71148SLH Pin Assignments

Table 1. ISL71148SLH Pin Descriptions

Pin Number	Pin Name	Description
1, 4, 7, 10, 13, 16, 19, 20, 23, 30, 40, 43, 46	GND	Analog and digital supply ground. Tie directly to the PCB ground plane (GND).
6, 21	AVCC	Analog supply. The supply range is 4.5V to 5.5V. Bypass this pin to GND with a 10µF ceramic capacitor.
5	REF	Reference Input. The input range of REF is 2.4V to 2.6V. The voltage at the REF pin (V_{REF}) defines the input range of each Analog Input Channel as 0V to $V_{REF.}$ Bypass REF to GND with a 10µF ceramic capacitor.
2	CH3-	Analog Input Channel Pairs. CH0± to CH7± are eight fully differential input channel pairs. Each Analog Input Channel pin may be driven within the voltage range from 0V to V_{REF}.
3	CH3+	
8	CH4-	
9	CH4+	
11	CH5-	
12	CH5+	
14	CH6-	
15	CH6+	
17	CH7-	
18	CH7+	
41	CH0-	
42	CH0+	
44	CH1-	
45	CH1+	
47	CH2-	
48	CH2+	
22	$\overline{PD}$	Power-Down Low Input. When this input is logic low, the chip is powered down. If this occurs during a conversion, the conversion is halted, and the SDO pin is placed in Hi-Z. DV_{CC} determines logic levels. This pin has an internal 500kΩ pull-up resistor to $DV_{CC.}$
24, 31	DVCC	Digital I/O supply. Voltage range on this pin is 2.2V to 3.6V. DV_{CC} is nominally set to the same supply voltage as the host interface (2.5V or 3.3V). Bypass DVCC to GND with 0.1µF capacitor.
25	BUSY	Busy output. A logic high indicates a conversion is in progress. The BUSY indicator returns low following the completion of a conversion. DV_{CC} determines logic levels.
26	SDO	Serial data output. The current conversion result is serially shifted on this pin on the rising edges of SCK, Most Significant Bit (MSB) first to Least Significant Bit (LSB) last. The data stream comprises of 14 bits of conversion data followed by the channel select and gain select bits corresponding to the conversion result. DV_{CC} determines logic levels.
27	SCK	Serial data clock input. When $\overline{CS}$ is low and the BUSY indicator is low, the conversion result is shifted out on SDO on the rising edges of SCK, MSB first to LSB last. DV_{CC} determines logic levels. SCK should be held low when it is not being asserted.
28	SCAN	Channel scan input. When this input is logic high, the internal sequencer controls the channel selected. CH0 is the first channel selected following the rising edge of SCAN. Each subsequent channel is selected on each new rising edge of $\overline{CS}$. DV_{CC} determines logic levels.

Table 1. ISL71148SLH Pin Descriptions (Cont.)

Pin Number	Pin Name	Description
29	$\overline{CS}$	Convert Start Low input. A falling edge on this input completes the sampling process and starts a new conversion. The conversion is timed using an internal oscillator. The device automatically powers down following the conversion process. The logic state of the $\overline{CS}$ pin controls the state of the SDO pin. A logic high on the $\overline{CS}$ pin disables the SDO pin driver, and the SDO pin impedance is Hi-Z. A logic low on the $\overline{CS}$ pin enables the SDO driver (unless $\overline{PD}$ is low) and allows data to be read out following a conversion. This pin should be held low at power-up and when in power-down or when the device is inactive.
32	PGABP	PGA bypass mode input. When this input is logic high, the PGA is bypassed, and the input buffer/multiplexer directly drives the ADC. The maximum throughput rate is increased to 900ksps. DV_{CC} determines logic levels.
33	LPM	Low-power mode input. When this input is logic high, the acquisition time is directly controlled by the $\overline{CS}$ pin logic state held high. The ADC is automatically powered down between conversion to reduce power consumption for lower sample rates. This pin is a device configuration pin and should not be switched dynamically during operation.
34	G2	Logic Inputs. These three pins program the gain of the PGA. The G2, G1, and G0 logic inputs are latched internally on the rising edge of the $\overline{CS}$. DV_{CC} determines logic levels.
35	G1	
36	G0	
37	S2	Channel selection logic inputs. These three pins select the input channel passed through the input multiplexer to the PGA (or ADC if the PGA is bypassed). The S2, S1, and S0 logic inputs are latched internally on the rising edge of $\overline{CS}$. DV_{CC} determines logic levels.
38	S1	
39	S0	

Contents

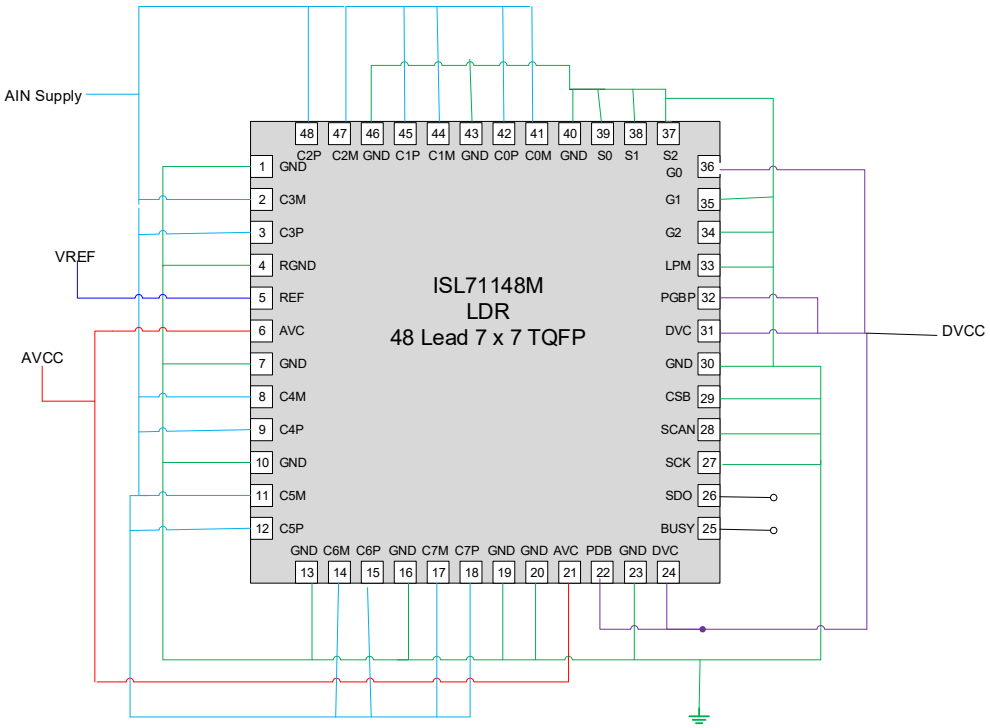
1. Test Description

1.1 Irradiation Facility

LDR testing was performed at 0.01rad(Si)/s using a Hopewell Designs N40 vault-type LDR irradiator in the Palm Bay, Florida, Renesas facility. A PbAl box was used to shield the test fixture and devices under test against low energy, secondary gamma radiation. Post-irradiation anneals were performed under bias in a small temperature chamber.

1.2 Test Fixturing

Figure 2 shows the configuration used for the biased LDR testing and anneals.



Power Up Sequencing
1) VCC1 / AVCC = 5.5V
2) VCC 2 / DVCC = 3.6V
3)VCC3 / VREF = 2.6V
4) VCC4 / AIN = 1.3V

Reverse above for Power Down

Figure 2. ISL71148SLH LDR Bias Configuration

1.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE) with data logging at each downpoint. Downpoint electrical testing was performed at room temperature.

1.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of twelve samples irradiated at LDR under bias and twelve irradiated at LDR with all pins grounded. All parts were also subject to a 168-hour, 100ºC biased anneal. Three control units were used.

The ISL71148SLH samples were drawn from three wafers in wafer lot F6W628. All samples were packaged in the standard 48-lead Thin Quad Flat-Pack.

1.5 Downpoints

Planned irradiation downpoints for the LDR test were 0krad(Si), 10krad(Si), 30krad(Si), 50krad(Si), 60krad(Si), 75krad(Si), and 100krad(Si). A 168-hour high temperature anneal at 100ºC under bias followed the LDR irradiations.

2. Results

LDR TID testing of the ISL71148SLH is complete. All tested parameters passed the datasheet limits. Table 2 summarizes the results.

2.1 Attributes Data

Table 2. ISL71148SLH Attributes Data

Dose Rate (rad(Si)/s)	Condition	Sample Size	Downpoint	Pass[1]	Fail
0.01	Biased (Figure 2)	12	Pre-irradiation	12	0
			10krad(Si)	12	0
			30krad(Si)	12	0
			50krad(Si)	12	0
			60krad(Si)	12	0
			75krad(Si)	12	0
			100krad(Si)	12	0
			Anneal	12	0
0.01	Grounded	12	Pre-irradiation	12	0
			10krad(Si)	12	0
			30krad(Si)	12	0
			50krad(Si)	12	0
			60krad(Si)	12	0
			75krad(Si)	12	0
			100krad(Si)	12	0
			Anneal	12	0

1. A Pass indicates a sample that passes all datasheet limits.

2.2 Variables Data

The plots in Figure 3 through Figure 62 illustrate the LDR response of the selected parameters shown in Table 3 in the Appendix. The plots show the average tested values of the parameters as a function of the total dose for each of the irradiation conditions, biased and grounded, plus a 168-hour, 100ºC biased anneal. The plots also include error bars at each down-point, representing the minimum and maximum measured values of the samples. However, in some plots, the error bars might not be visible due to their values compared to the scale of the graph.

Some graphs and captions state that they are the average; this denotes that the average of the measurements of multiple channels or pins was plotted. The error bars on these graphs represent the maximum and minimum measured values across all the channels or pins. Additionally, some parameters were only tested on CH0, as per the datasheet, and their graphs and captions state that they are CH0.

Unless otherwise specified, AV_{CC} = 5V and DV_{CC} = 2.5V.

After irradiation to each level up to 100krad(Si) and the subsequent anneal, all samples passed the datasheet limits.

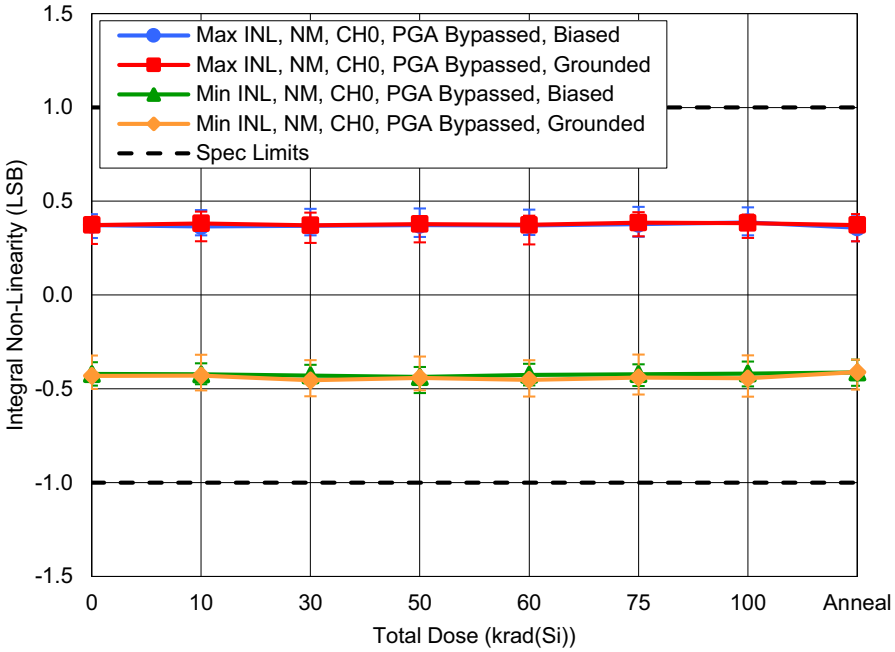


Figure 3. ISL71148SLH CH0 minimum and maximum integral non-linearity (INL) in normal operating mode (NM) with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -1LSB and a maximum of 1LSB.

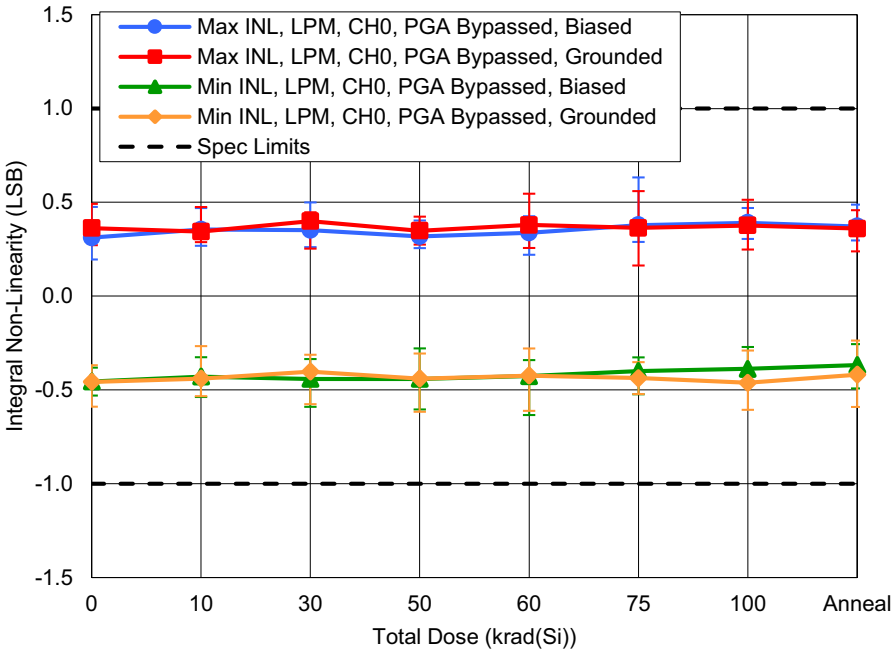


Figure 4. ISL71148SLH CH0 minimum and maximum integral non-linearity (INL) in low-power mode (LPM) with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -1LSB and a maximum of 1LSB.

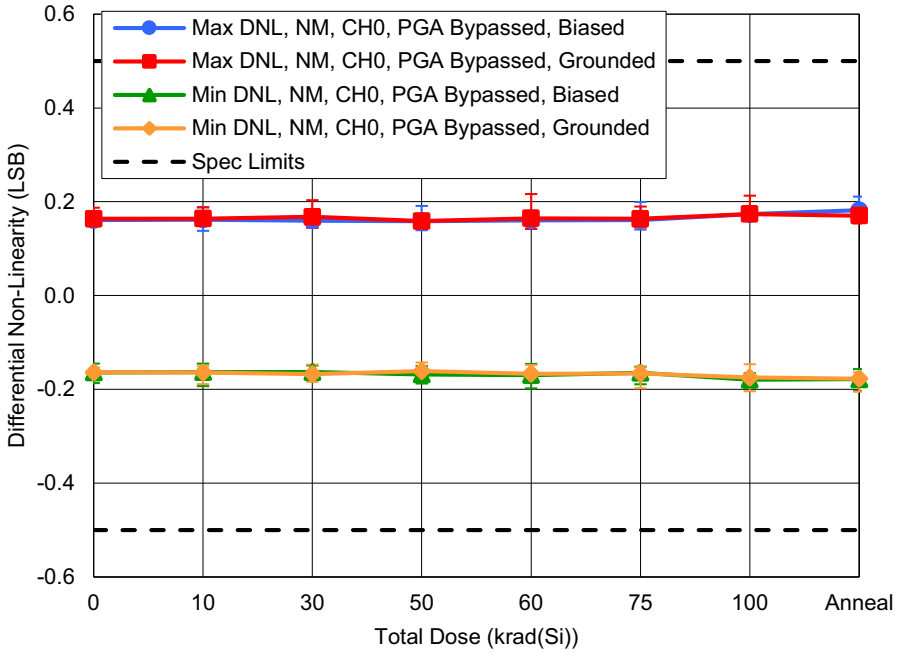


Figure 5. ISL71148SLH CH0 minimum and maximum differential non-linearity (DNL) in normal operating mode with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -0.5LSB and a maximum of 0.5LSB.

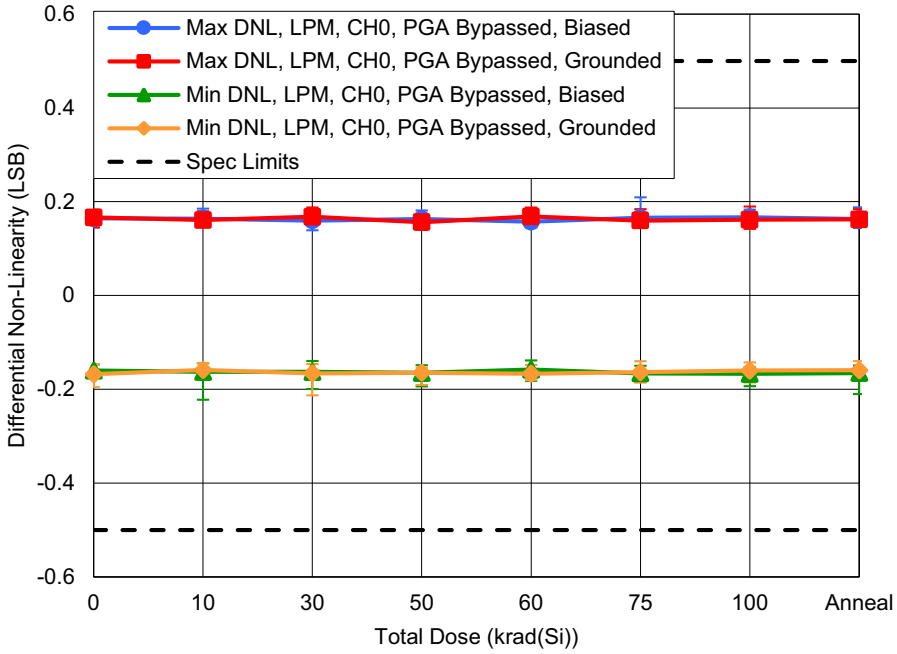


Figure 6. ISL71148SLH CH0 minimum and maximum differential non-linearity (DNL) in low-power mode with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -0.5LSB and a maximum of 0.5LSB.

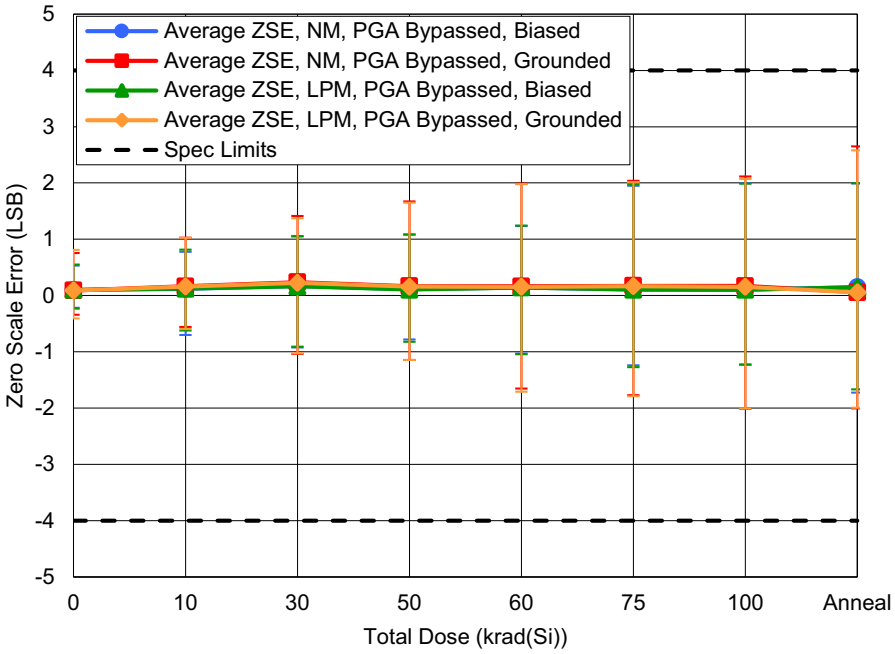


Figure 7. ISL71148SLH average zero-scale error (ZSE) in normal operating mode or low-power mode with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -4LSB and a maximum of 4LSB.

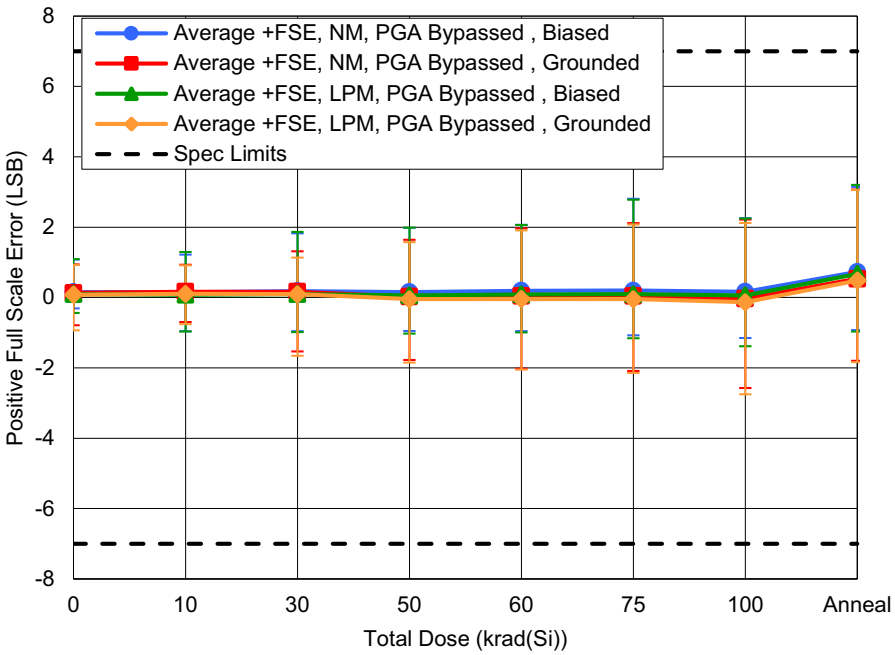


Figure 8. ISL71148SLH average positive full-scale error (+FSE) in normal operating mode or low-power mode with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -7LSB and a maximum of 7LSB.

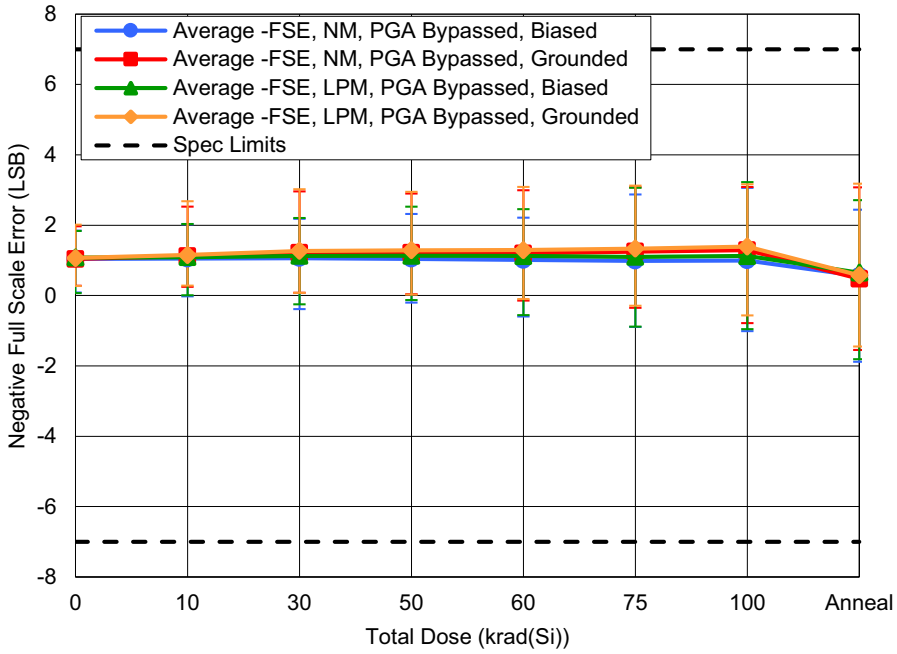


Figure 9. ISL71148SLH average negative full-scale error (-FSE) in normal operating mode or low-power mode with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -7LSB and a maximum of 7LSB.

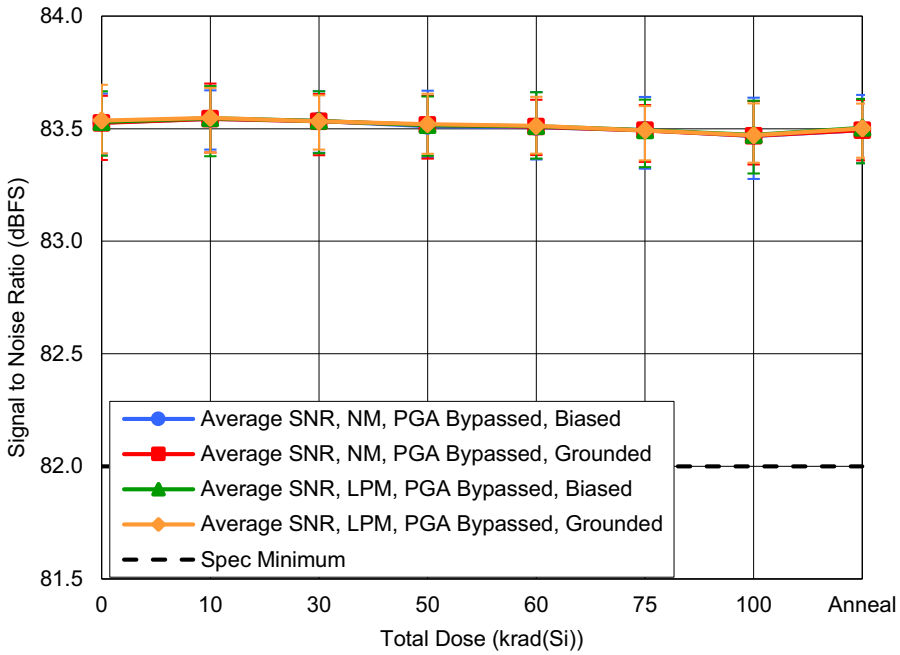


Figure 10. ISL71148SLH average signal-to-noise ratio (SNR) in normal operating mode or low-power mode with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 82dBFS.

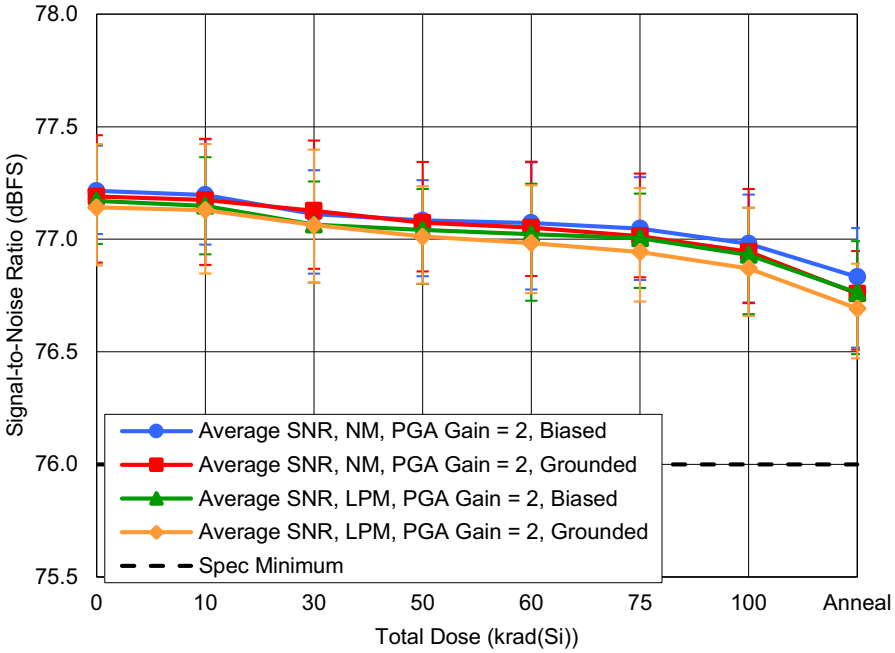


Figure 11. ISL71148SLH average signal-to-noise ratio (SNR) in normal operating mode or low-power mode with AV_{CC} = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 76dBFS.

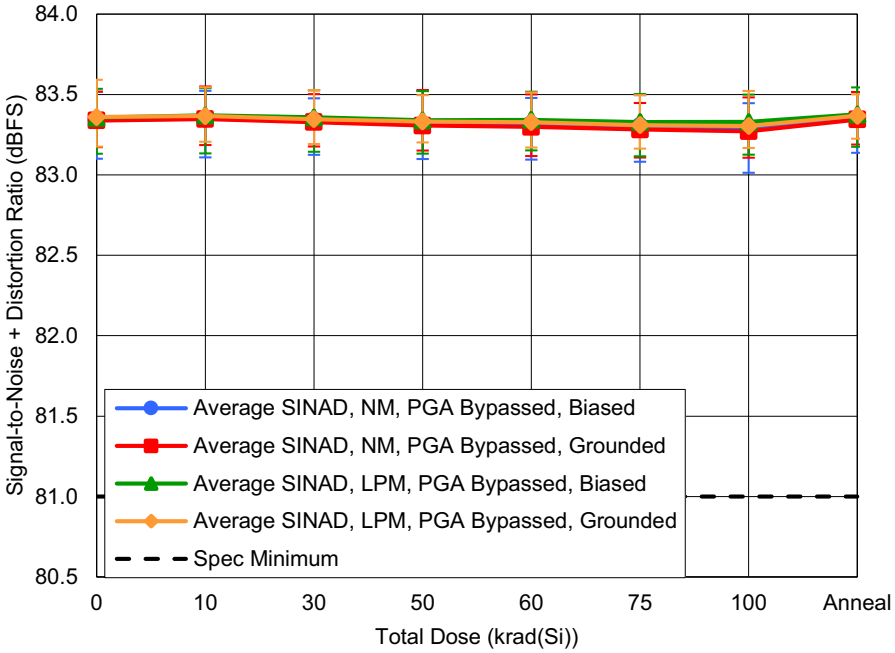


Figure 12. ISL71148SLH average signal to noise + distortion ratio (SINAD) in normal operating mode or low-power mode with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 81dBFS.

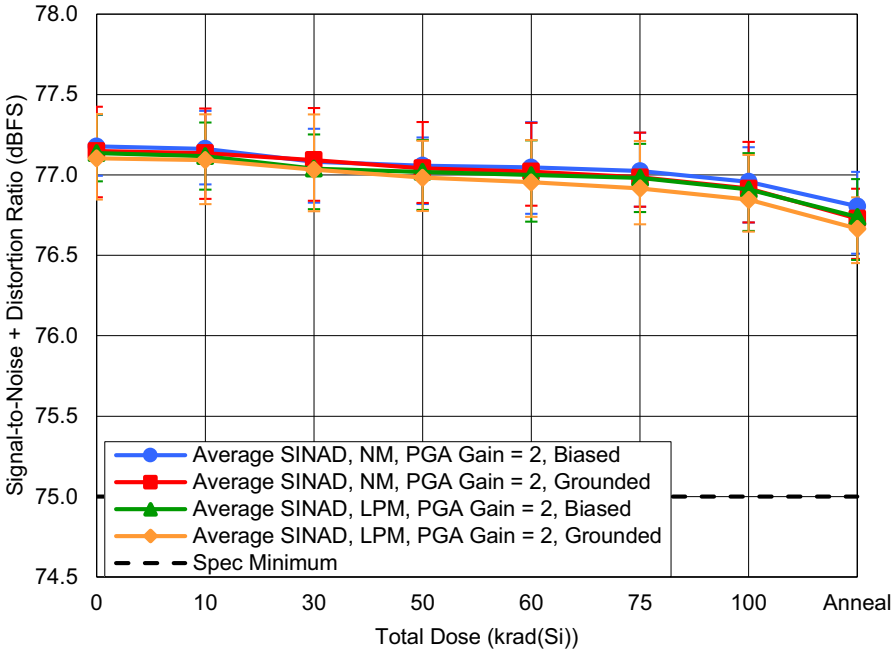


Figure 13. ISL71148SLH average signal to noise + distortion ratio (SINAD) in normal operating mode or low-power mode with AV_{CC} = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 75dBFS.

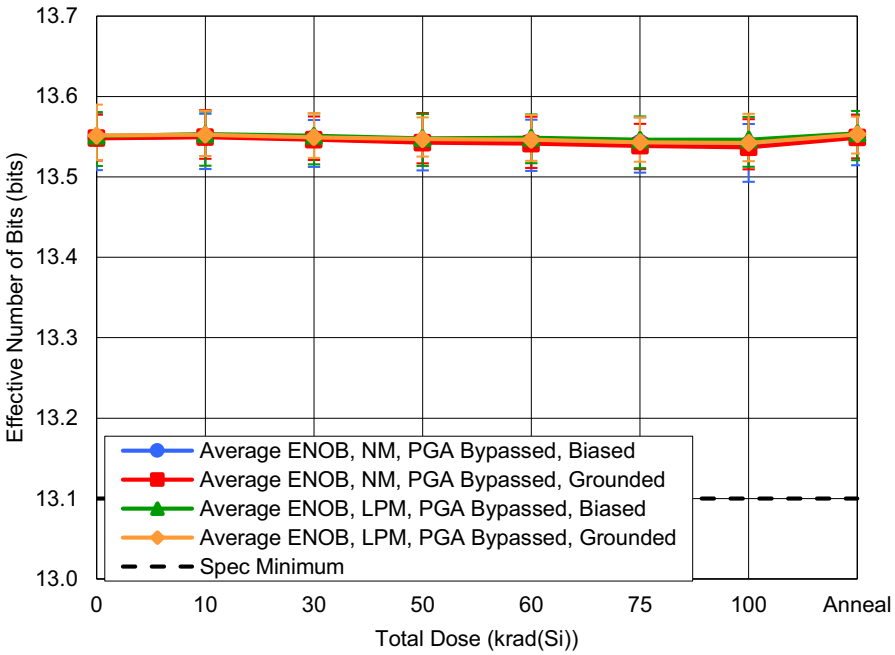


Figure 14. ISL71148SLH average effective number of bits (ENOB) in normal operating mode or low-power mode with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 13.1bits.

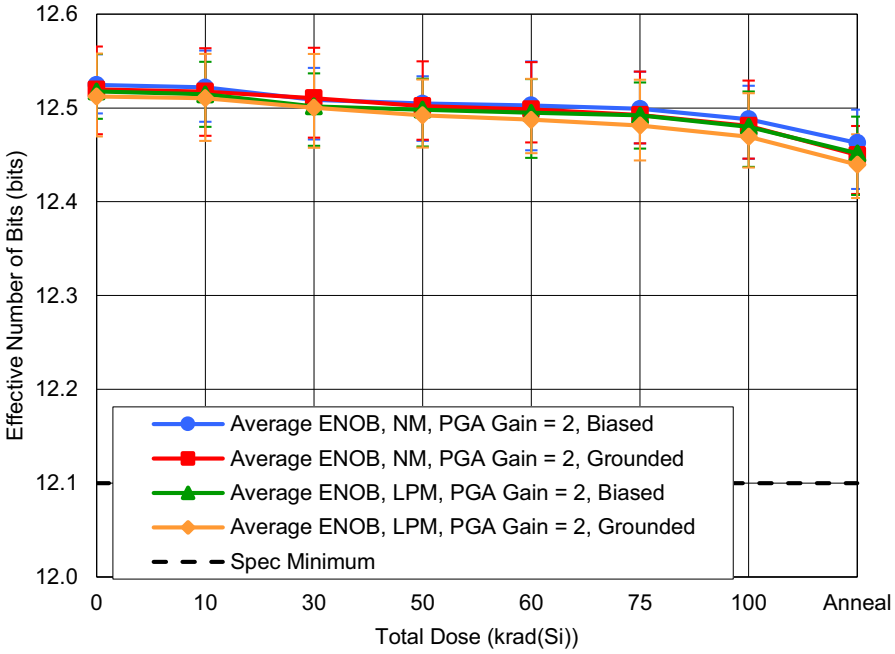


Figure 15. ISL71148SLH average effective number of bits (ENOB) in normal operating mode or low-power mode with AV_{CC} = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 12.1bits.

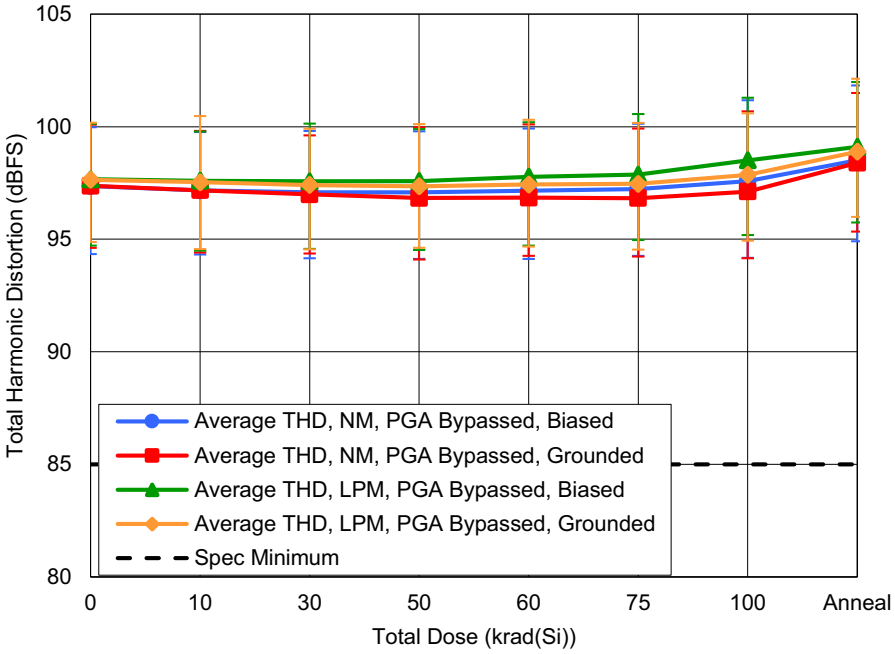


Figure 16. ISL71148SLH average total harmonic distortion (THD) in normal operating mode or low-power mode with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 85dBFS.

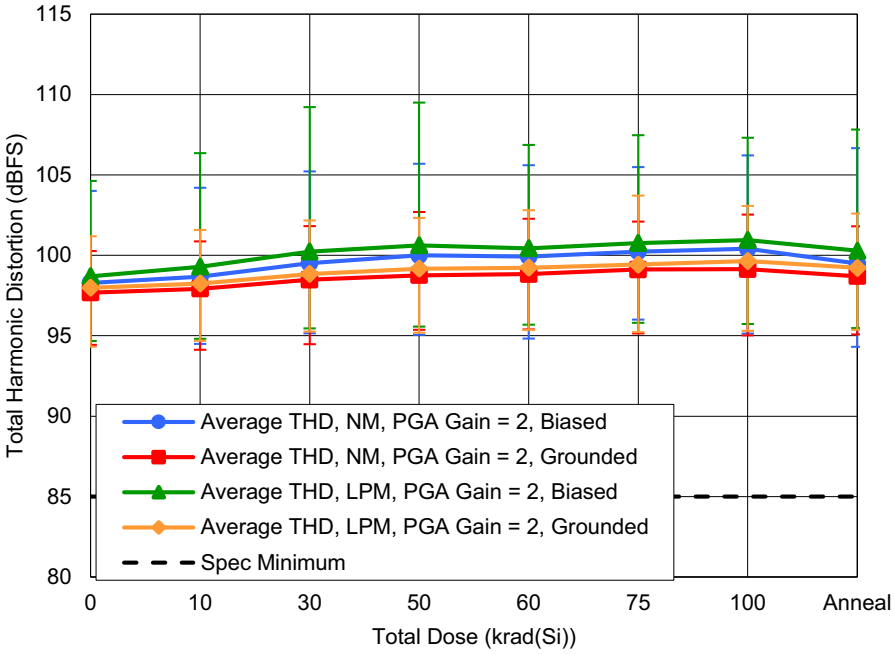


Figure 17. ISL71148SLH average total harmonic distortion (THD) in normal operating mode or low-power mode with AV_{CC} = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 85dBFS.

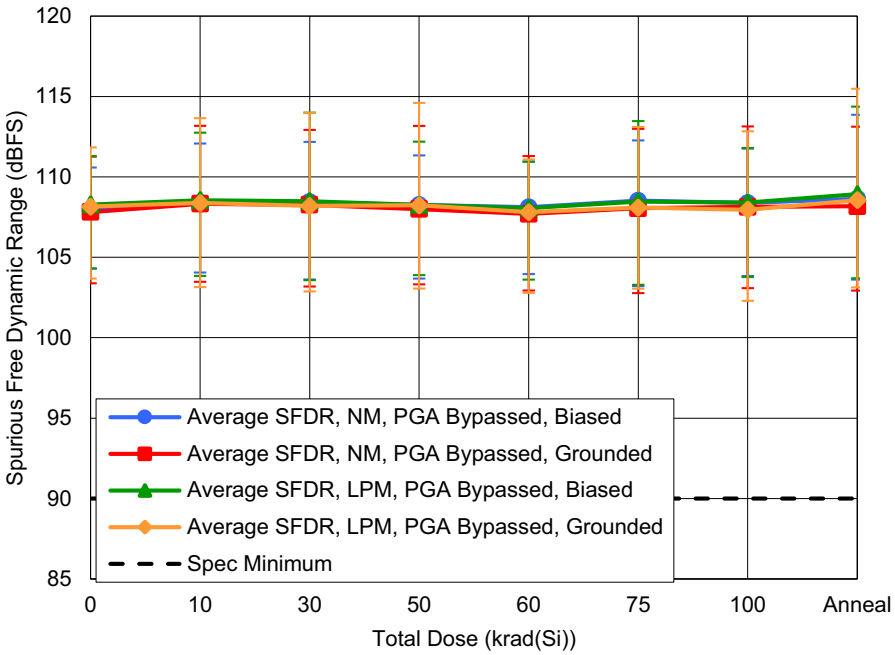


Figure 18. ISL71148SLH average spurious free dynamic range (SFDR) in normal operating mode or low-power mode with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 90dBFS.

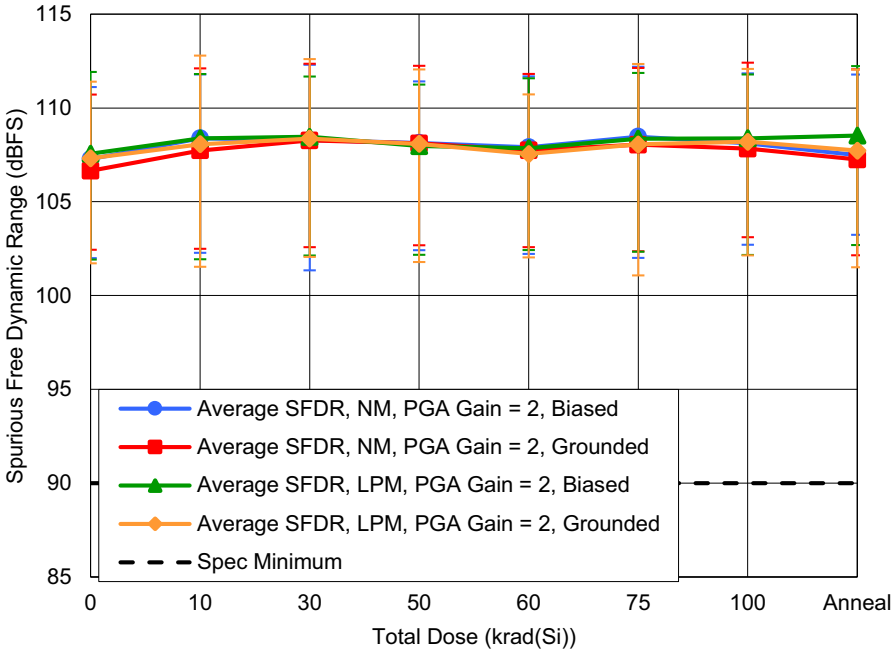


Figure 19. ISL71148SLH average spurious free dynamic range (SFDR) in normal operating mode or low-power mode with AV_{CC} = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limit is a minimum of 90dBFS.

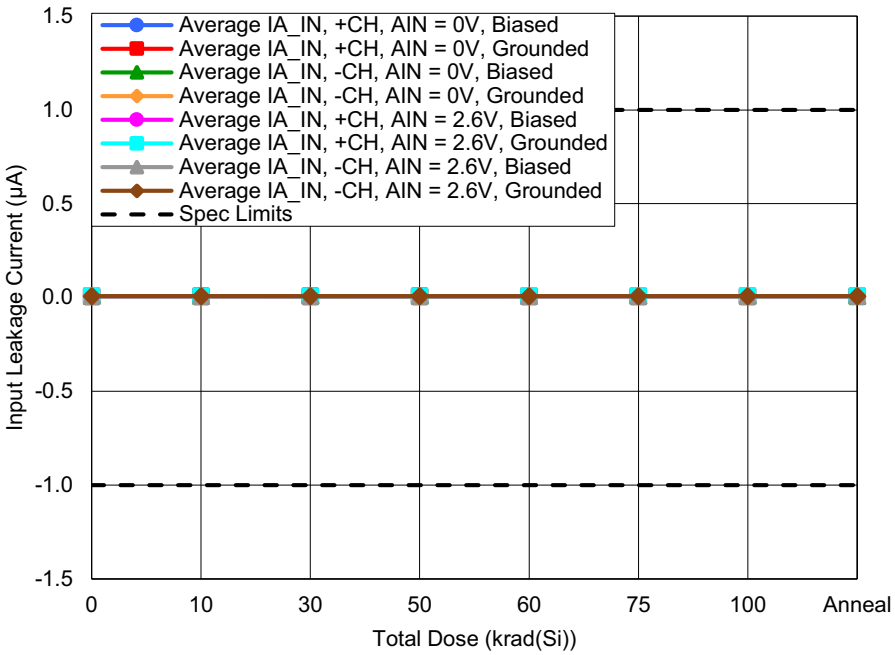


Figure 20. ISL71148SLH average input leakage current (IA_{IN}) with A_{IN} = 0V or 2.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all channels. The datasheet limits are a minimum of -1µA and a maximum of 1µA.

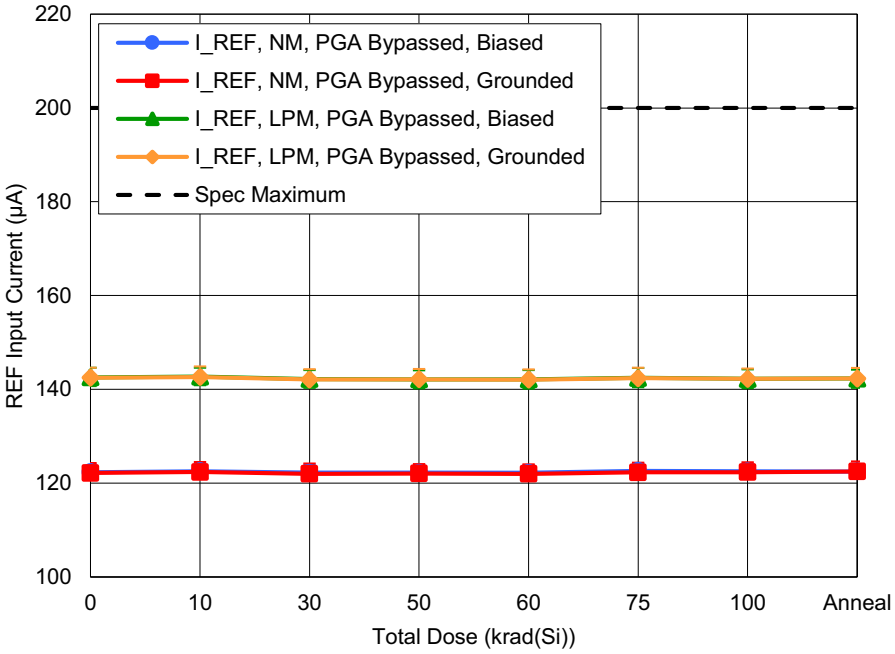


Figure 21. ISL71148SLH REF input current (I_{REF}) in normal operating mode or low-power mode with V_{REF} = 2.6V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 200µA.

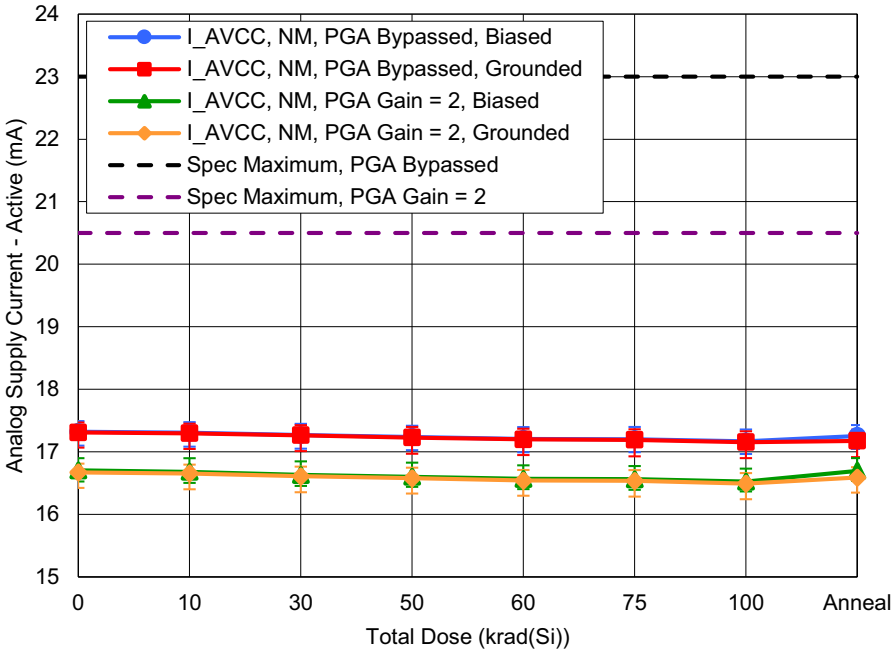


Figure 22. ISL71148SLH analog supply current – active (I_{AVCC}) in normal operating mode with AV_{CC} = 5V and with PGA bypassed and f_{SAMP} = 900.901ksps or with PGA Gain = 2 and f_{SAMP} = 483.092ksps as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are maximums of 23mA with PGA bypassed and 20.5mA with PGA Gain = 2.

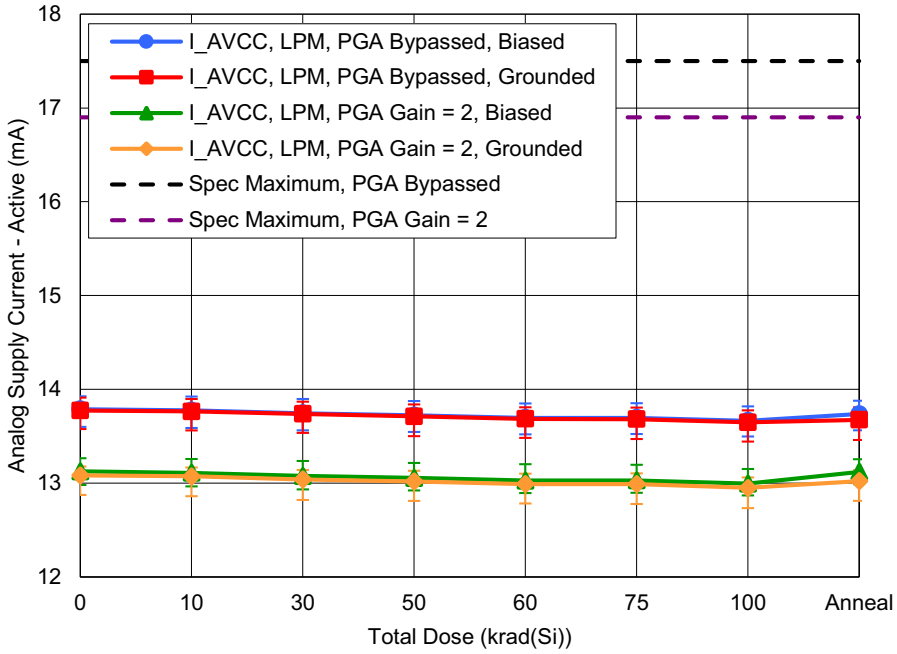


Figure 23. ISL71148SLH analog supply current – active (I_{AVCC}) in low-power mode with AV_{CC} = 5V and with PGA bypassed and f_{SAMP} = 670ksps or with PGA Gain = 2 and f_{SAMP} = 413.223ksps as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are maximums of 17.5mA with PGA bypassed and 16.9mA with PGA Gain = 2.

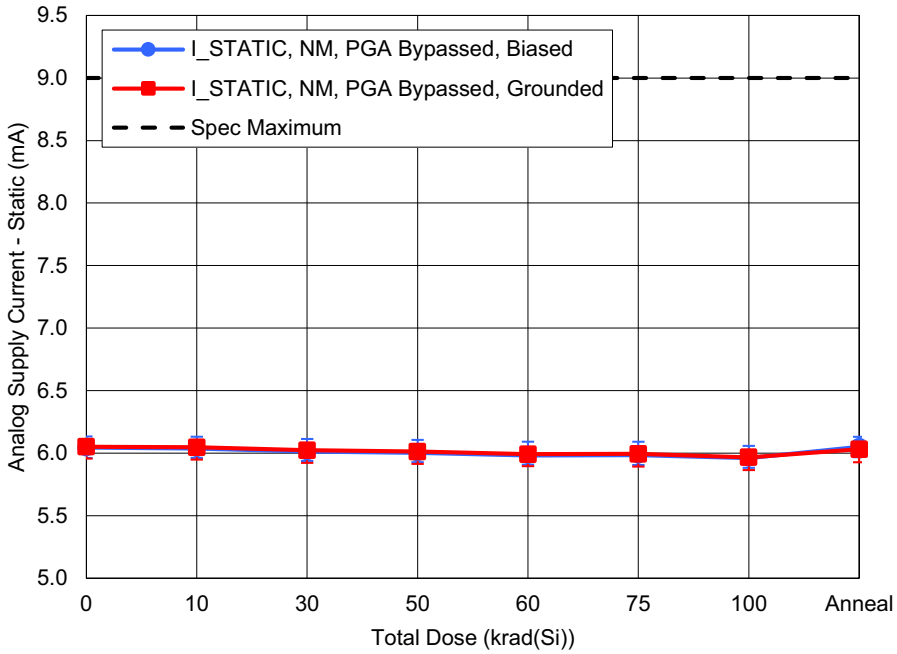


Figure 24. ISL71148SLH analog supply current – static (I_{STATIC}) in normal operating mode with AV_{CC} = 5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 9mA.

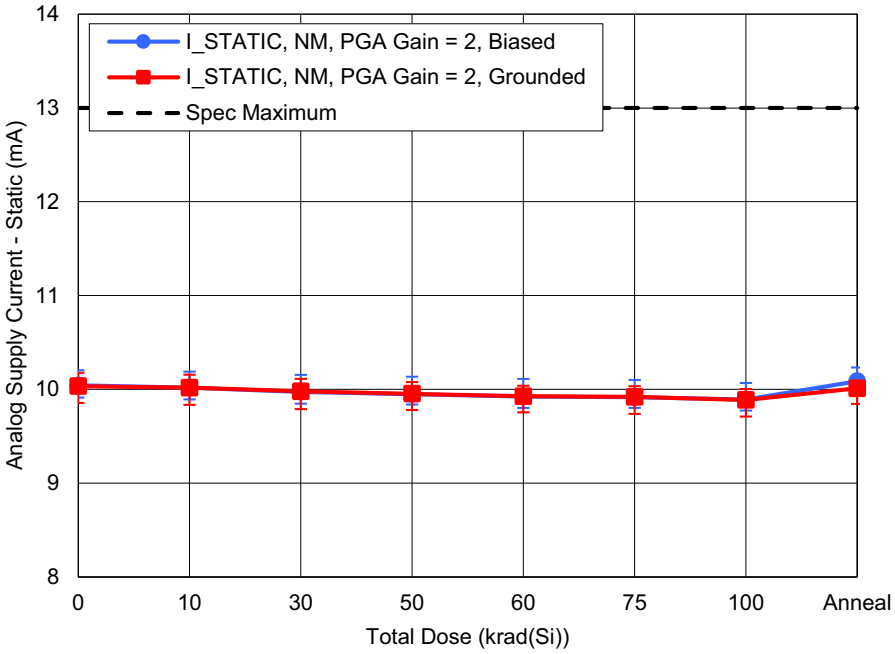


Figure 25. ISL71148SLH analog supply current – static (I_{STATIC}) in normal operating mode with AV_{CC} = 5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 13mA.

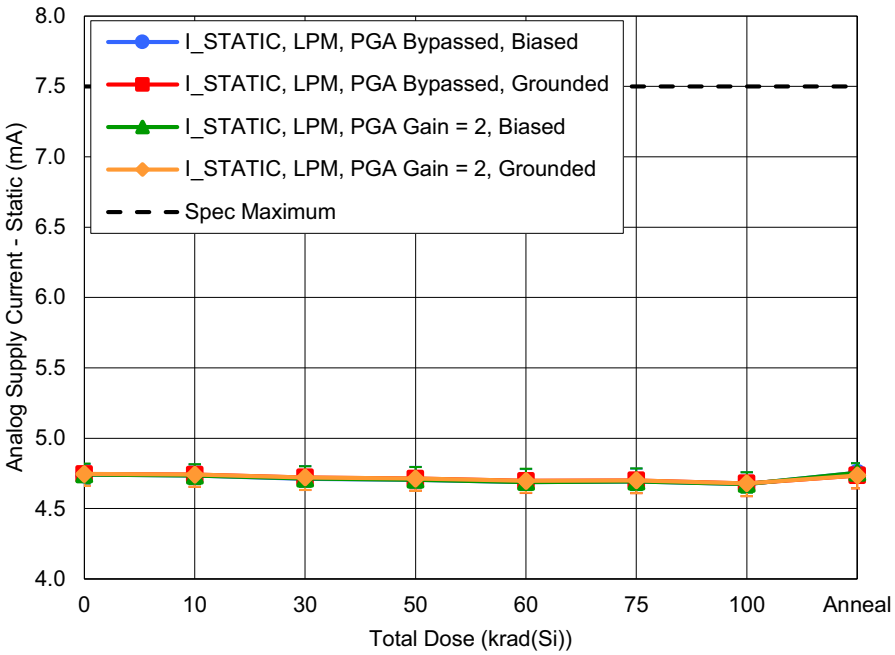


Figure 26. ISL71148SLH analog supply current – static (I_{STATIC}) in low-power mode with AV_{CC} = 5V and PGA Gain = 2 or bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 7.5mA for both conditions.

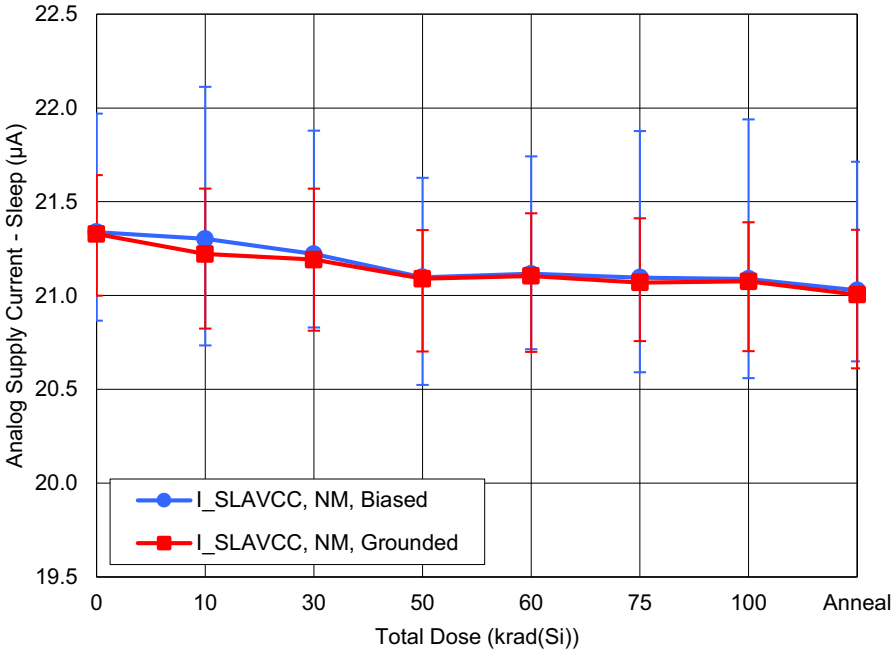


Figure 27. ISL71148SLH analog supply current – sleep (I_{SLAVCC}) in normal operating mode with AV_{CC} = 5V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. There are no datasheet limits for this parameter, but the typical value is 20µA.

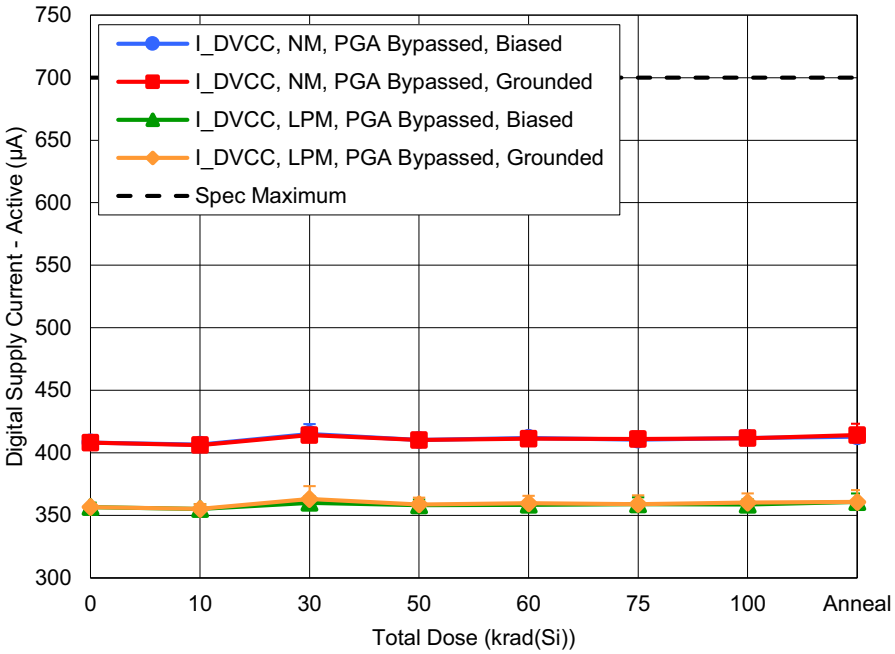


Figure 28. ISL71148SLH digital supply current – active (I_{DVCC}) in normal operating mode or low-power mode with DV_{CC} = 2.5V, f_{SCK} = 50MHz, and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 700µA.

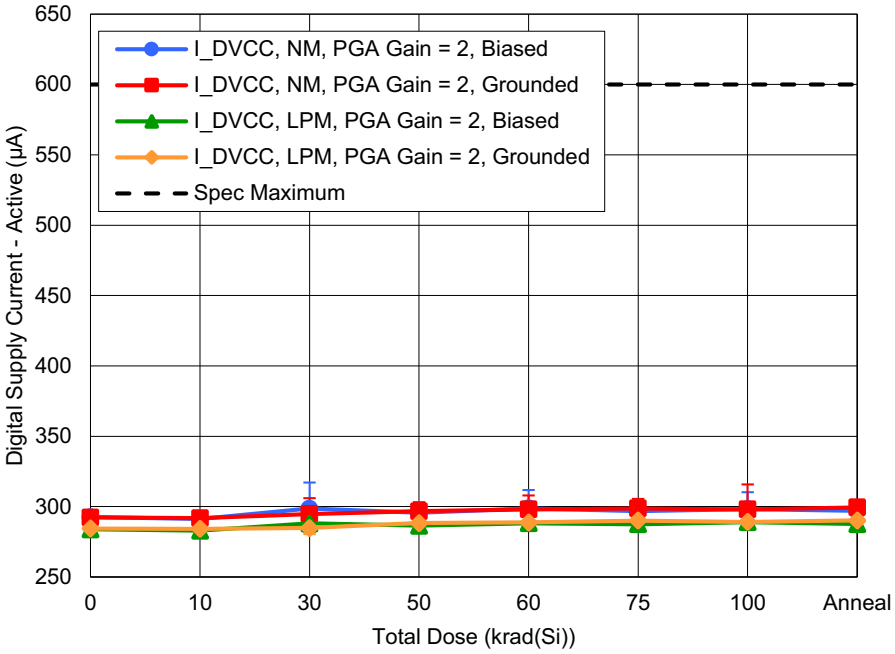


Figure 29. ISL71148SLH digital supply current – active (I_{DVCC}) in normal operating mode or low-power mode with DV_{CC} = 2.5V, f_{SCK} = 50MHz, and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 600µA.

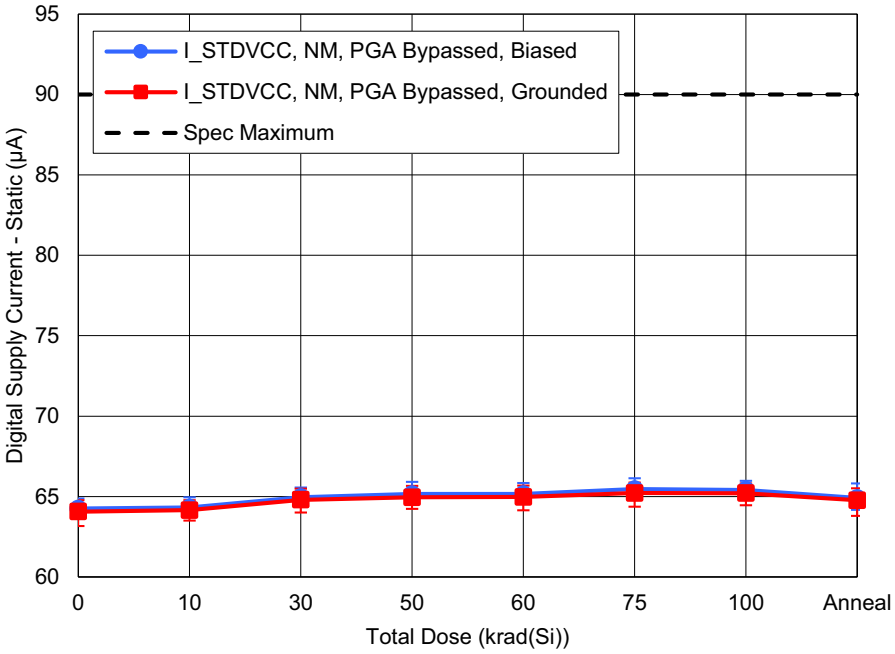


Figure 30. ISL71148SLH digital supply current – static (I_{STDVCC}) in normal operating mode with DV_{CC} = 2.5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 90µA.

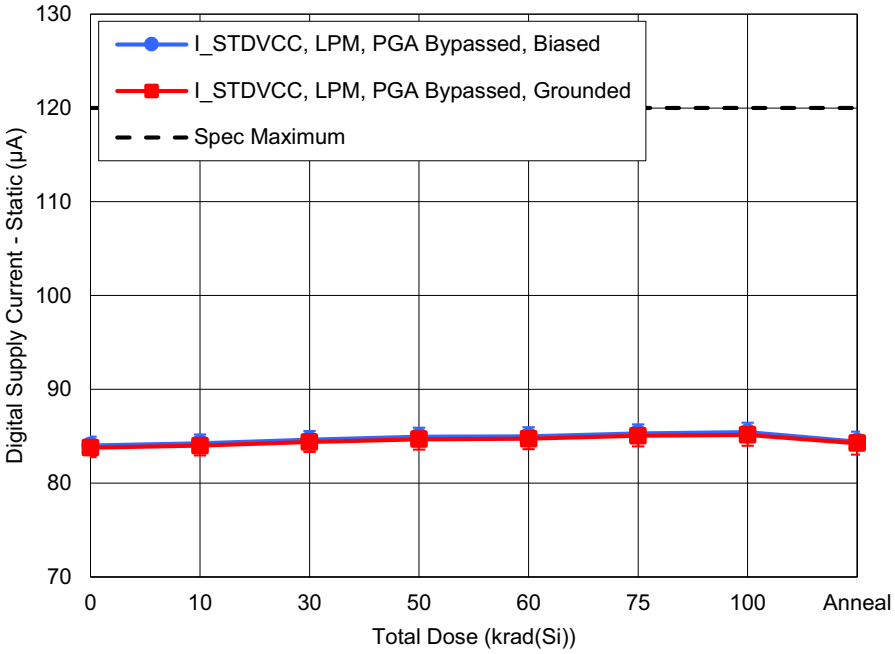


Figure 31. ISL71148SLH digital supply current – static (I_{STDVCC}) in low-power mode with DV_{CC} = 2.5V and PGA bypassed as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 120µA.

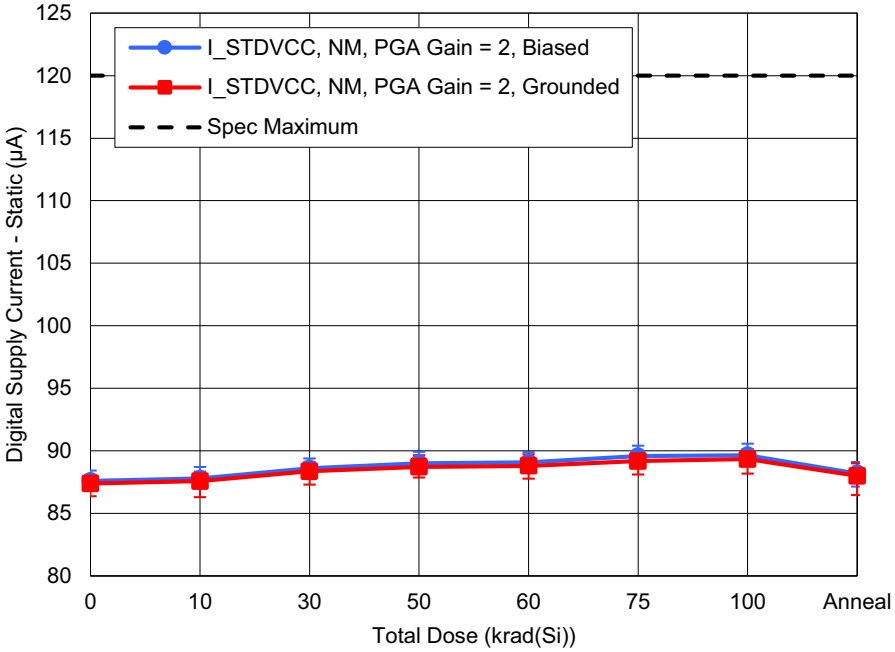


Figure 32. ISL71148SLH digital supply current – static (I_{STDVCC}) in normal operating mode with DV_{CC} = 2.5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 120µA.

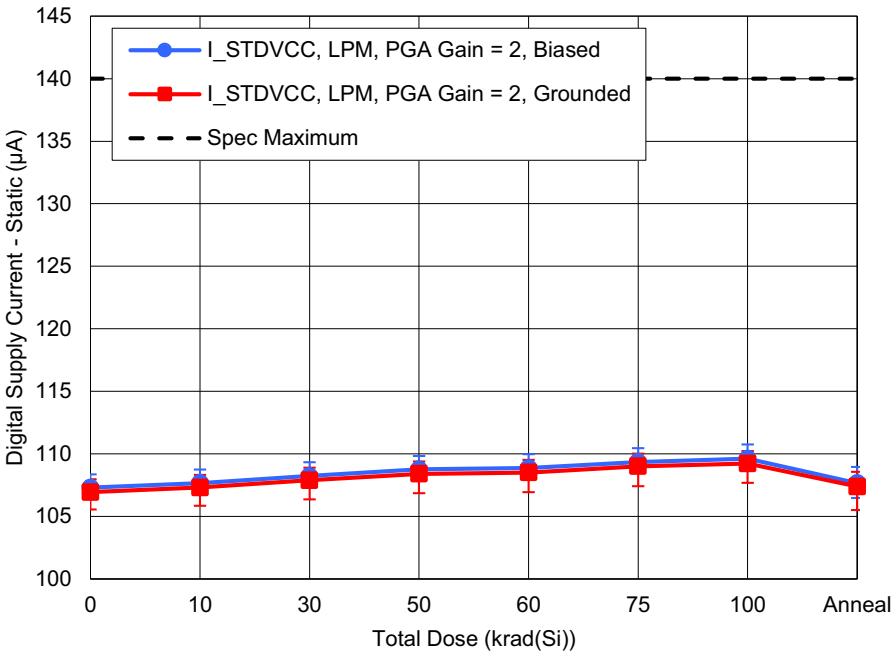


Figure 33. ISL71148SLH digital supply current – static (I_{STDVCC}) in low-power mode with DV_{CC} = 2.5V and PGA Gain = 2 as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits is a maximum of 140µA.

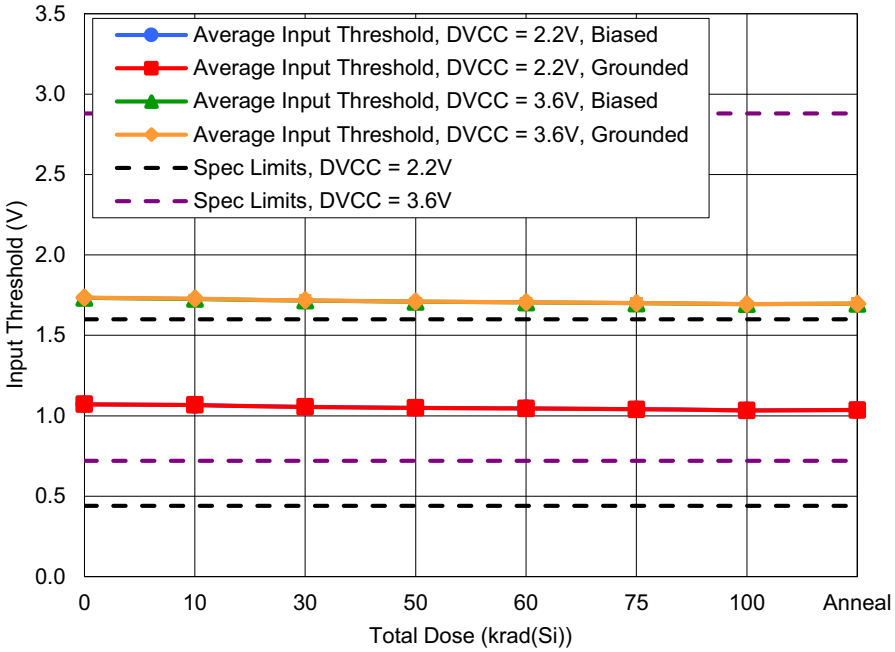


Figure 34. ISL71148SLH high-level input (V_{IH}) and low-level input (V_{IL}) with DV_{CC} = 2.2V or 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are minimums of 1.76V when DV_{CC} = 2.2V and 2.88V when DV_{CC} = 3.6V, and maximums of 440mV when DV_{CC} = 2.2V and 720mV when DV_{CC} = 3.6V.

Note: The datasheet reports the minimum voltages that are assured to be registered as logic high inputs. The measured values are the actual maximum voltages required to be registered as logic high inputs, so the datasheet limits are the maximums of the measured values. Similarly, the datasheet reports the maximum voltages that are assured to be registered as logic low inputs. The measured values are the actual minimum voltages required to be registered as logic low inputs, so the datasheet limits are the minimums of the measured values.

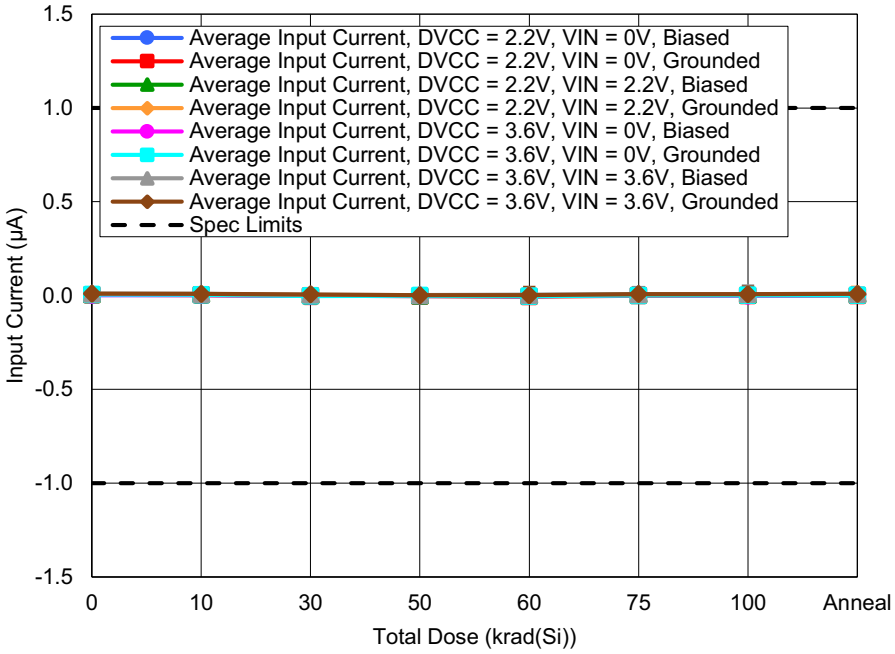


Figure 35. ISL71148SLH average input current ($\overline{CS}$, SCK, PGABP, S2, S1, S0, G2, G1, G0) (I_{IN}) with DV_{CC} = 2.2V and V_{IN} = 2.2V and 0V or DV_{CC} = 3.6V and V_{IN} = 3.6V and 0V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all pins. The datasheet limits are a minimum of -1µA and a maximum of 1µA.

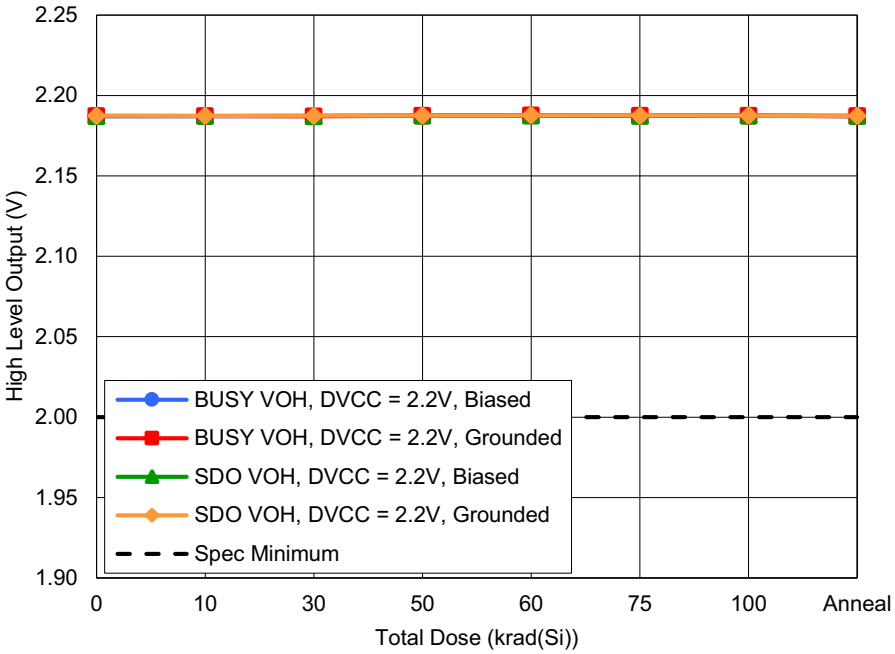


Figure 36. ISL71148SLH high-level output (V_{OH}) with DV_{CC} = 2.2V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of 2V.

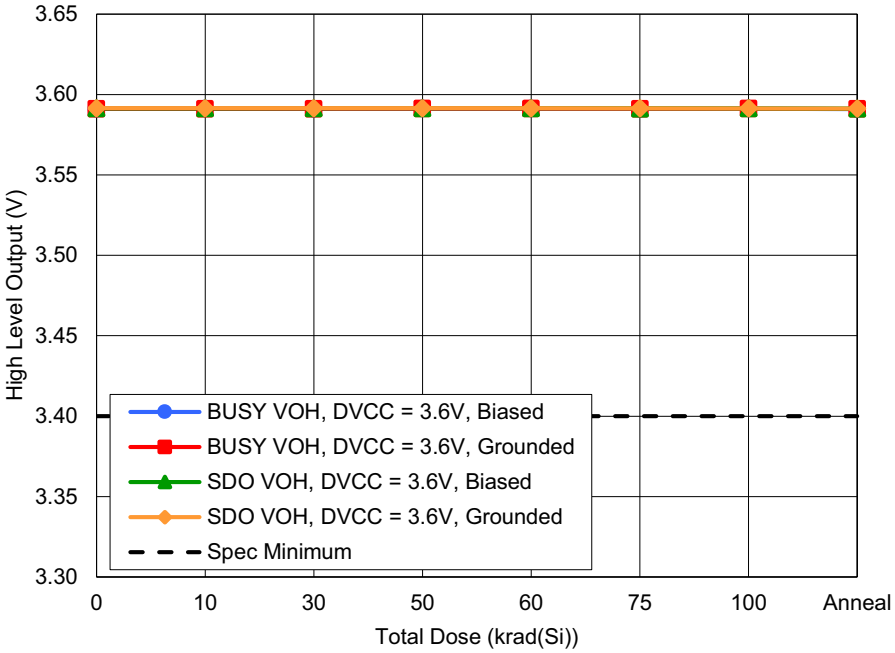


Figure 37. ISL71148SLH high-level output (V_{OH}) with DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of 3.4V.

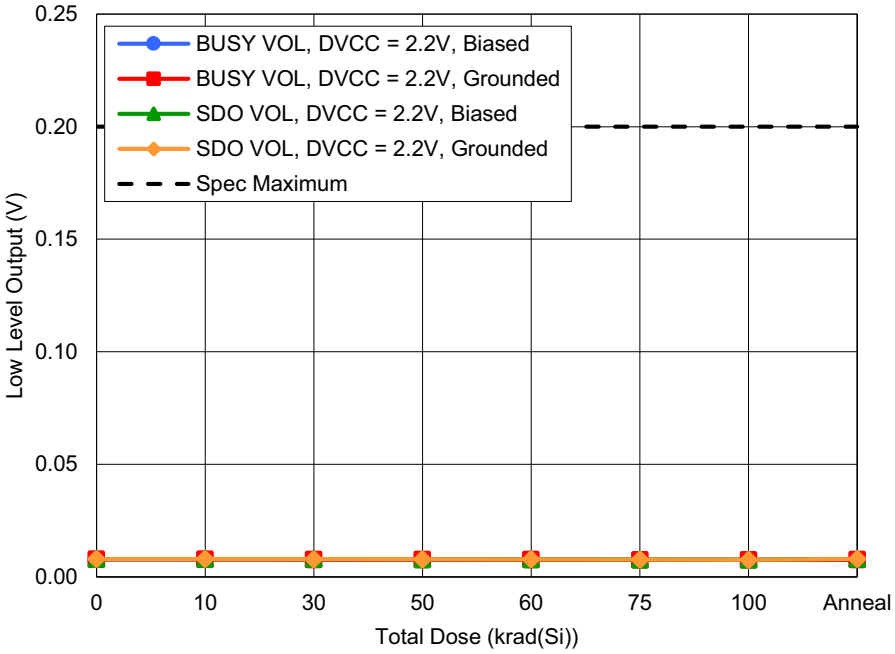


Figure 38. ISL71148SLH low-level output (V_{OL}) with DV_{CC} = 2.2V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 0.2V.

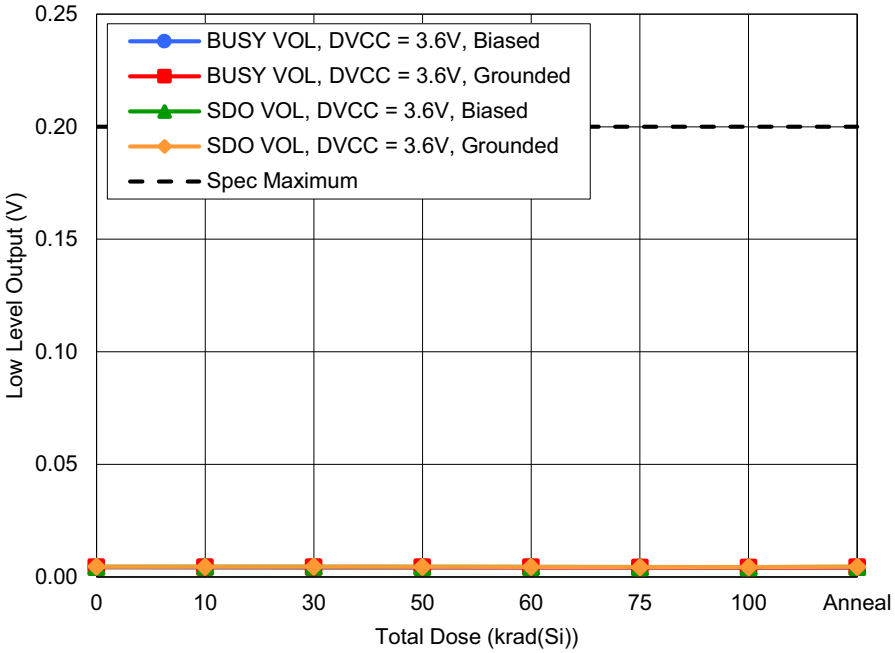


Figure 39. ISL71148SLH low-level output (V_{OL}) with DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 0.2V.

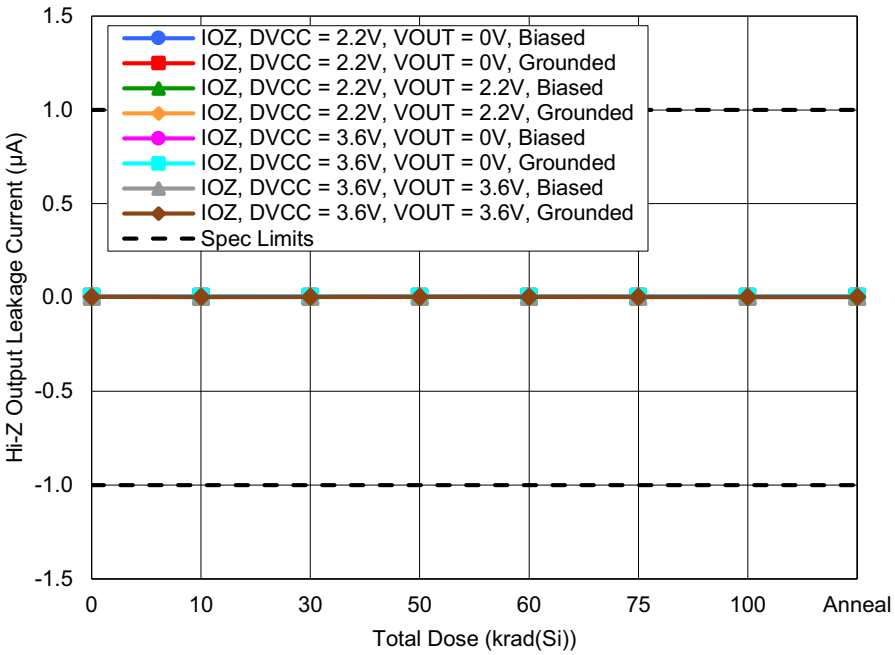


Figure 40. ISL71148SLH Hi-Z output leakage current (I_{OZ}) with DV_{CC} = 2.2V and V_{OUT} = 2.2V and 0V or DV_{CC} = 3.6V and V_{OUT} = 3.6V and 0V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -1µA and a maximum of 1µA.

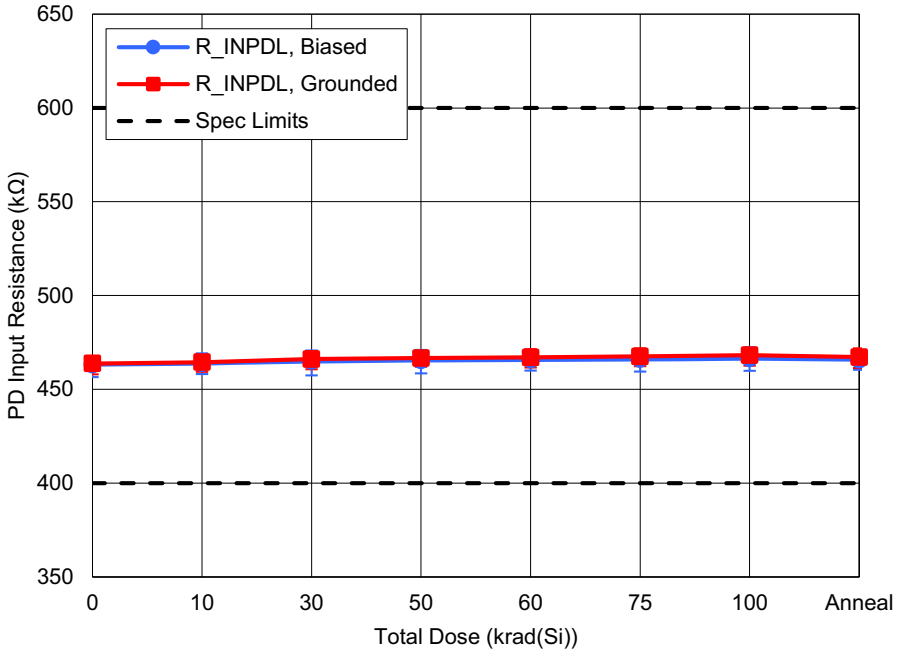


Figure 41. ISL71148SLH $\overline{PD}$ input resistance (R_{INPDL}) as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 400kΩ and a maximum of 600kΩ.

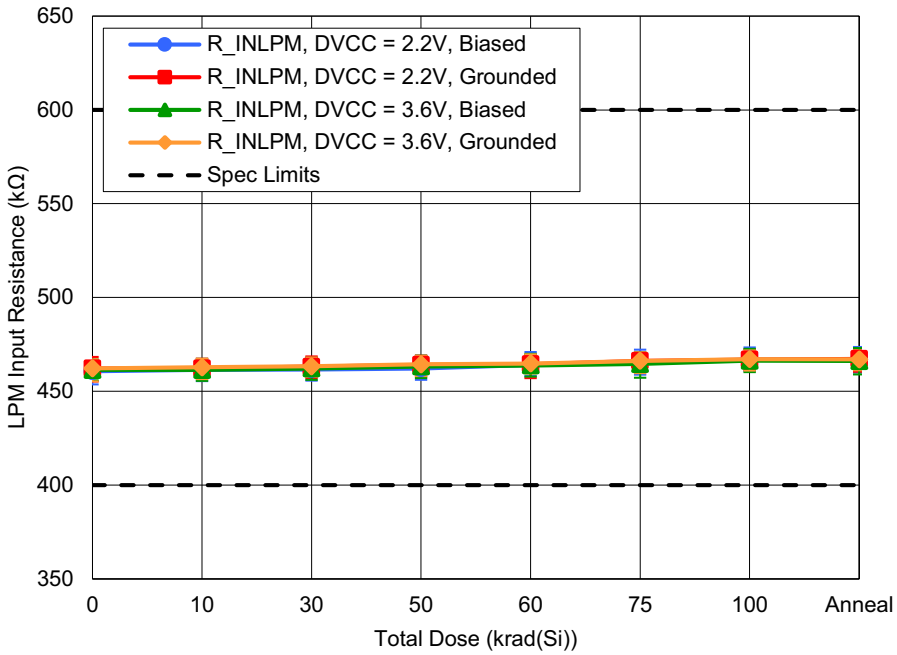


Figure 42. ISL71148SLH LPM input resistance (R_{INLPM}) with DV_{CC} = 2.2V or 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 400kΩ and a maximum of 600kΩ.

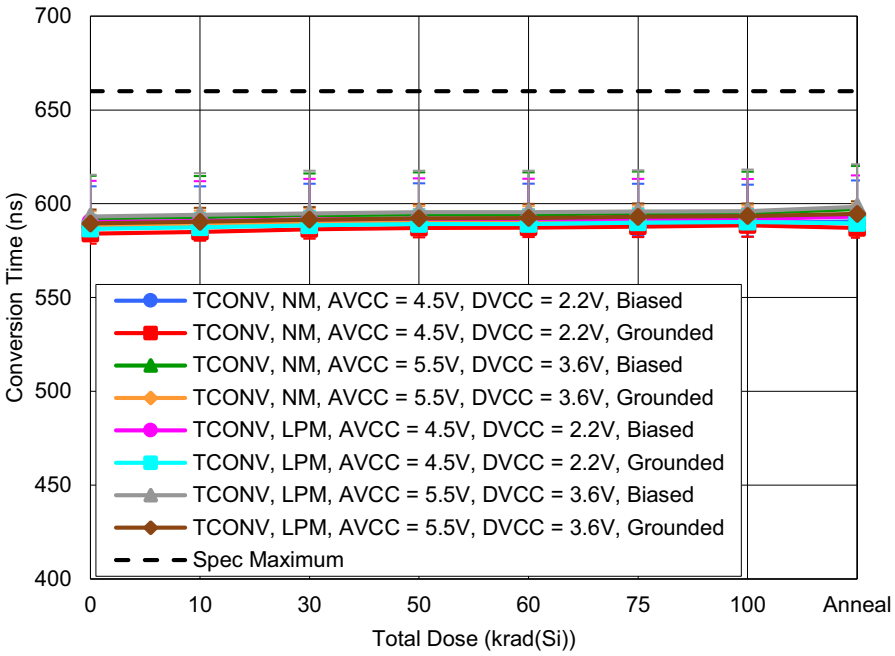


Figure 43. ISL71148SLH conversion time (t_{CONV}) in normal operating mode or low-power mode with PGA bypassed and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 660ns.

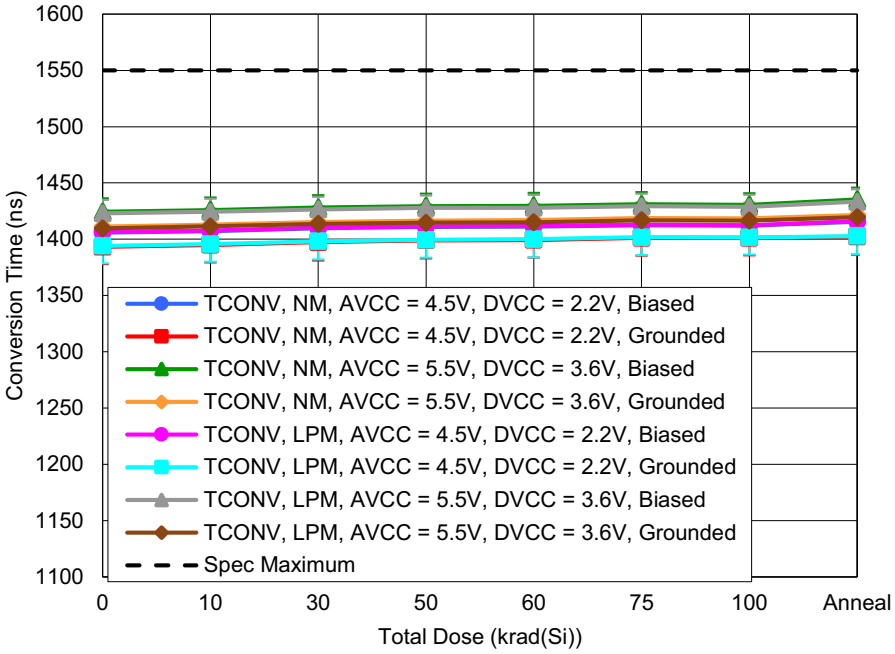


Figure 44. ISL71148SLH conversion time (t_{CONV}) in normal operating mode or low-power mode with PGA Gain = 2 and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 1550ns.

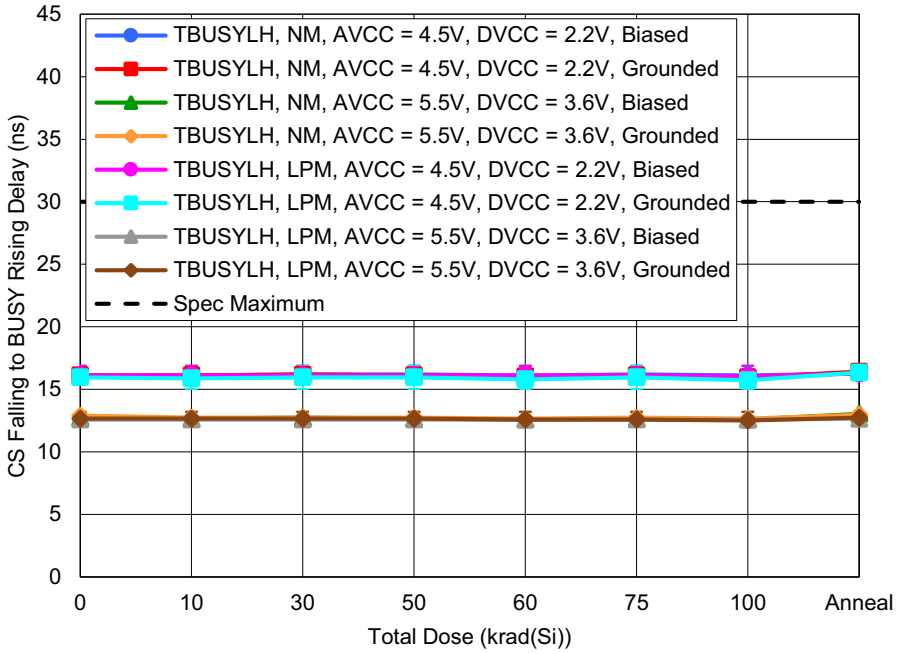


Figure 45. ISL71148SLH $\overline{CS}\downarrow$ to BUSY $\uparrow$ (t_{BUSYLH}) in normal operating mode or low-power mode with PGA bypassed, C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 30ns.

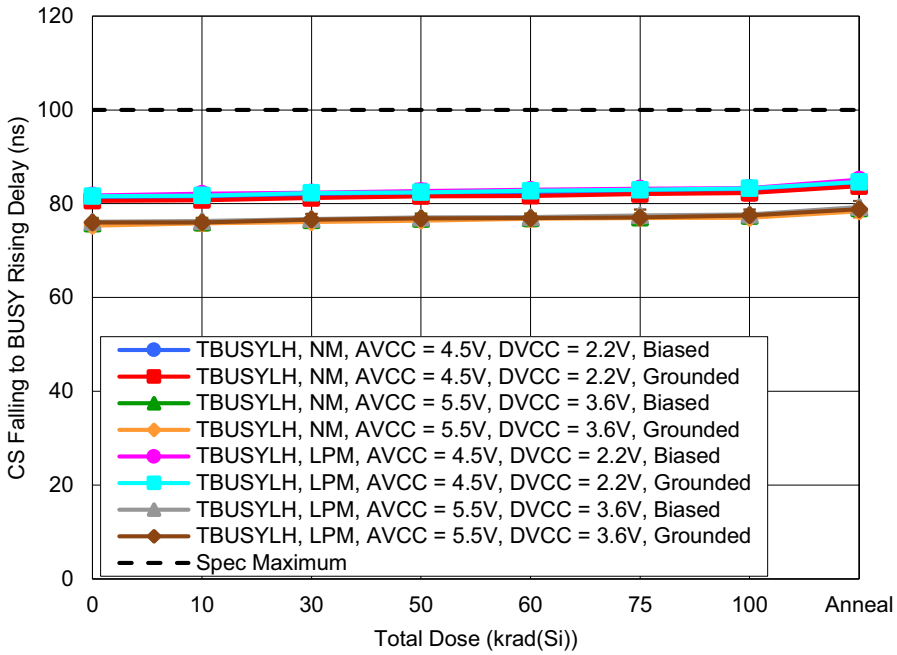


Figure 46. ISL71148SLH $\overline{CS}\downarrow$ to BUSY $\uparrow$ (t_{BUSYLH}) in normal operating mode or low-power mode with PGA Gain = 2, C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 100ns.

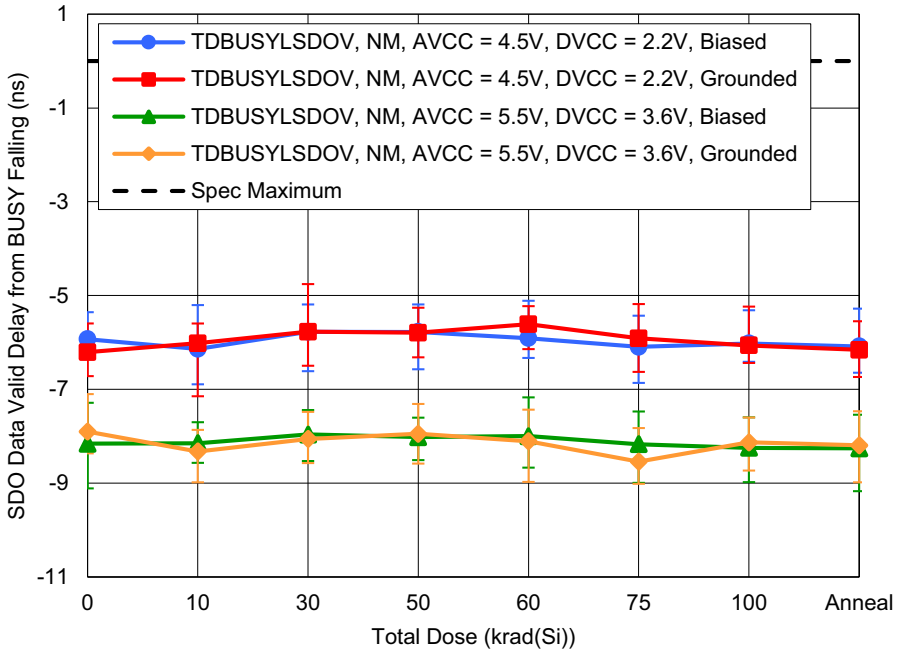


Figure 47. ISL71148SLH SDO Data Valid Delay from BUSY ↓ ($t_{DBUSYLSDOV}$) in normal operating mode with C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 0ns.

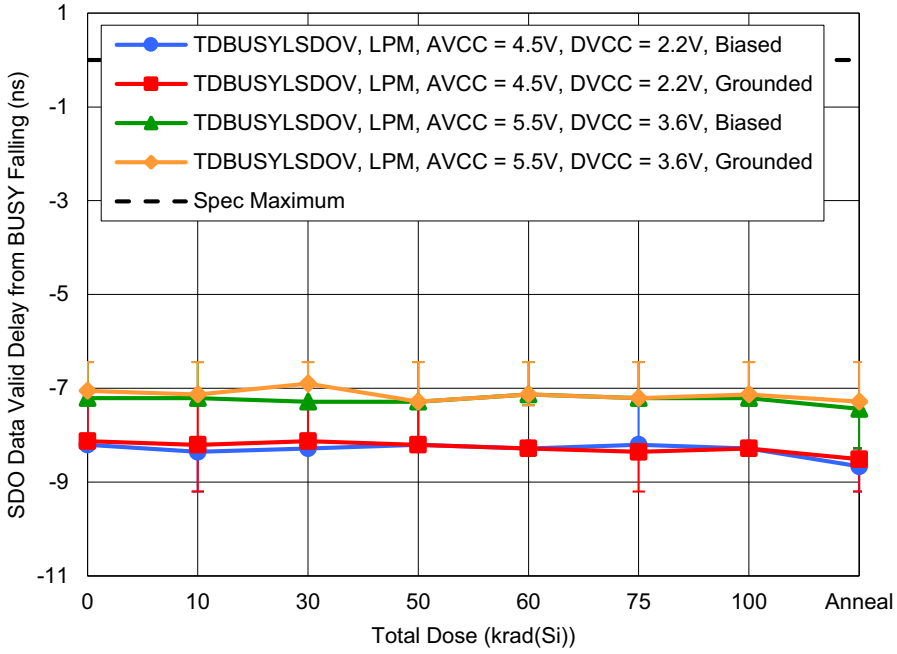


Figure 48. ISL71148SLH SDO Data Valid Delay from BUSY ↓ ($t_{DBUSYLSDOV}$) in low-power mode with C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 0ns.

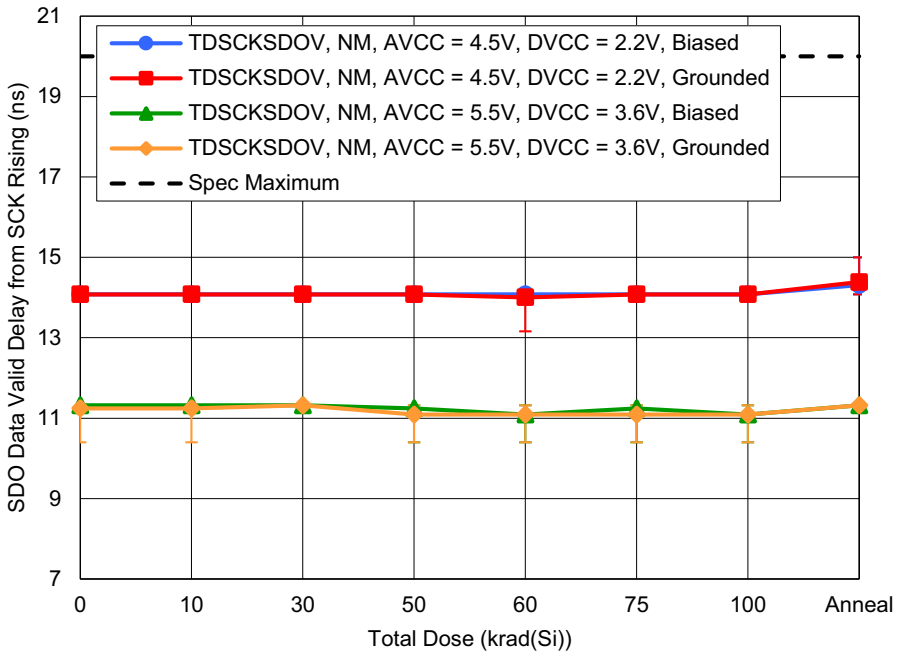


Figure 49. ISL71148SLH SDO Data Valid Delay from SCK ↑ ($t_{DSCKSDOV}$) in normal operating mode with C_L = 10pF, and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 20ns.

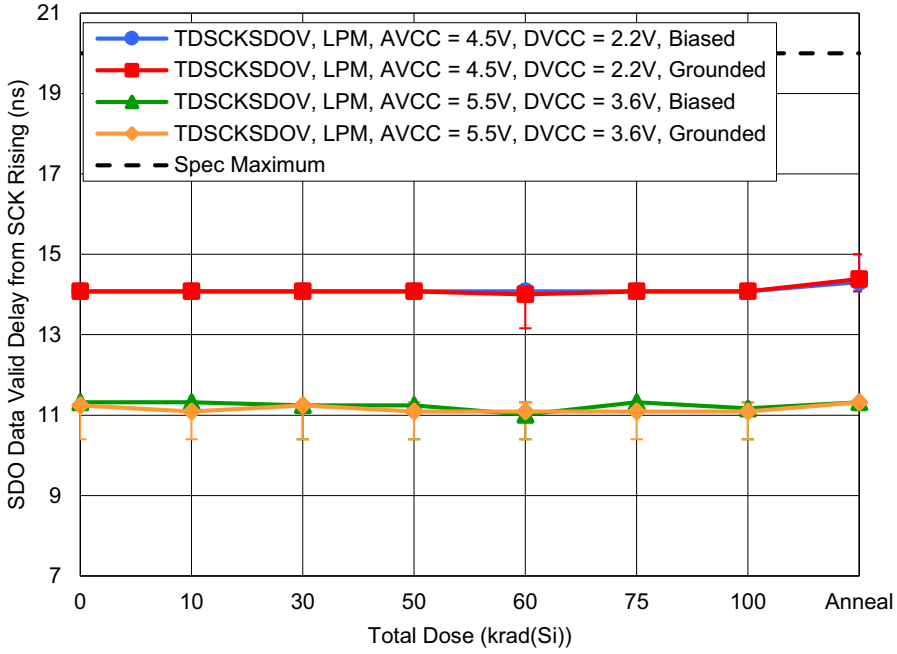


Figure 50. ISL71148SLH SDO Data Valid Delay from SCK ↑ ($t_{DSCKSDOV}$) in low-power mode with C_L = 10pF, and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 20ns.

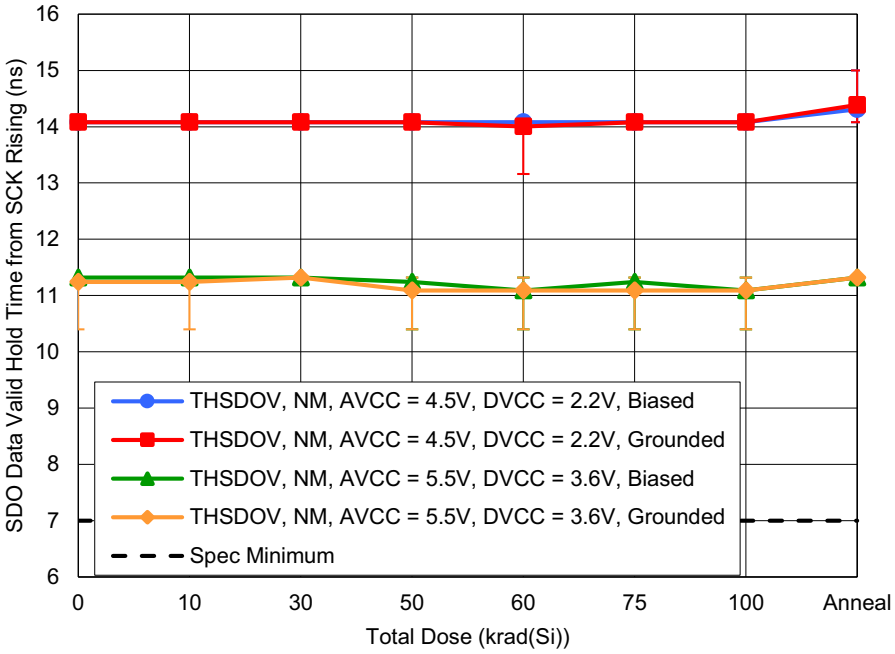


Figure 51. ISL71148SLH SDO Data Valid Hold Time from SCK ↑ (t_{HSDOV}) in normal operating mode with C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of 7ns.

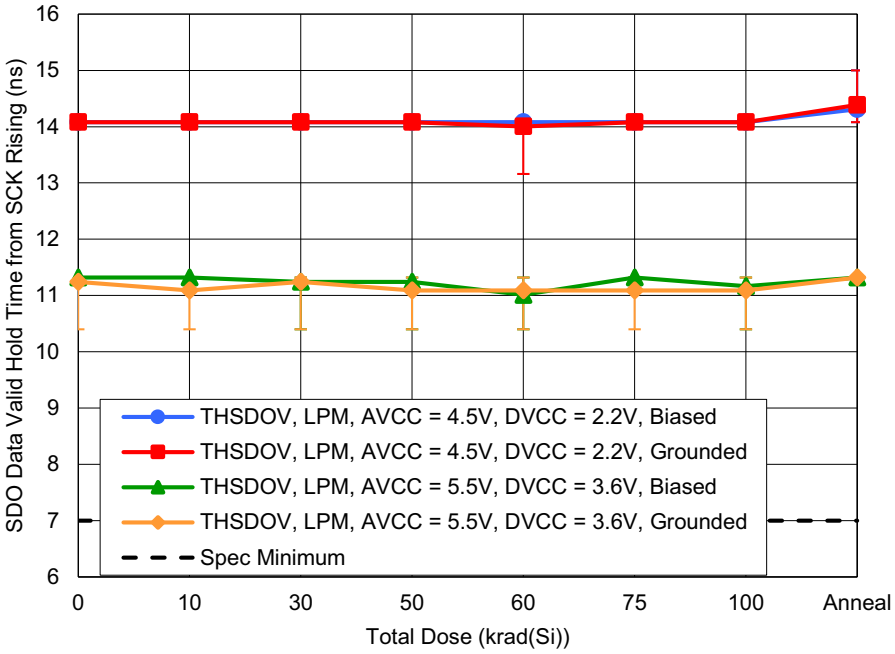


Figure 52. ISL71148SLH SDO Data Valid Hold Time from SCK ↑ (t_{HSDOV}) in low-power mode with C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of 7ns.

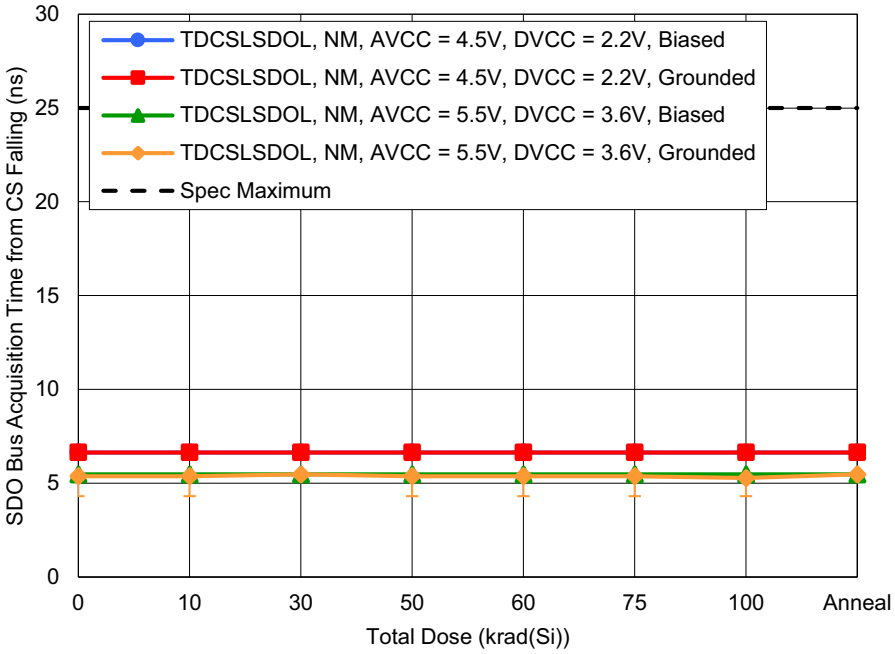


Figure 53. ISL71148SLH SDO Bus Acquisition Time from $\overline{CS}\downarrow$ ($t_{DCSLSDOL}$) in normal operating mode with C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 25ns.

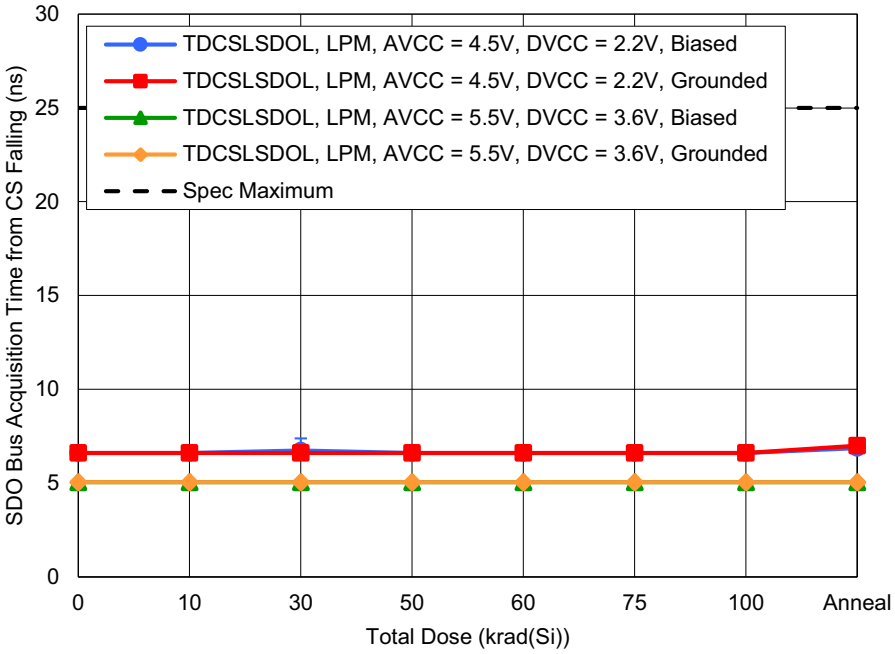


Figure 54. ISL71148SLH SDO Bus Acquisition Time from $\overline{CS}\downarrow$ ($t_{DCSLSDOL}$) in low-power mode with C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 25ns.

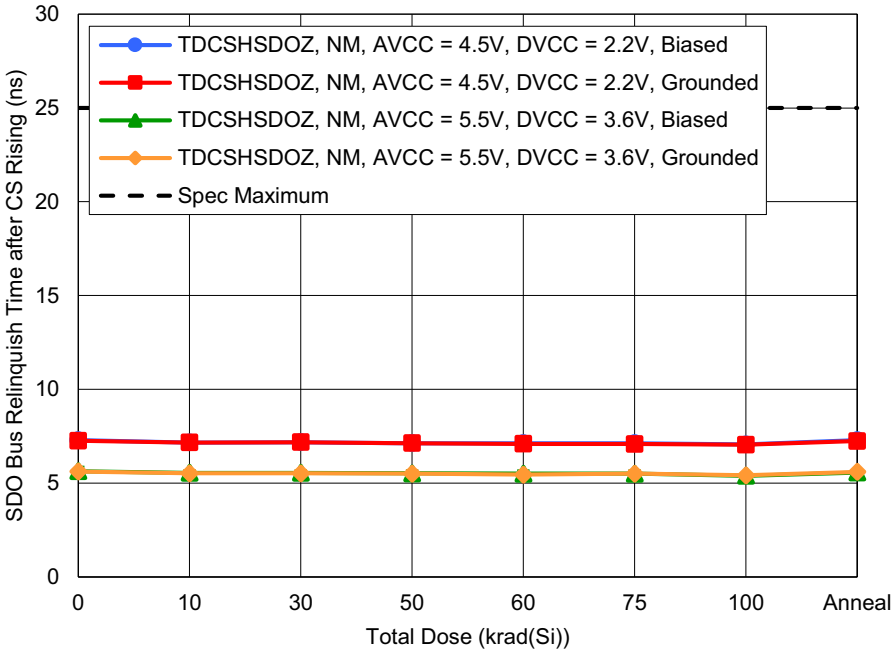


Figure 55. ISL71148SLH SDO Bus Relinquish Time after $\overline{CS}$ ↑ ($t_{DCSHSDOZ}$) in normal operating mode with C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 25ns.

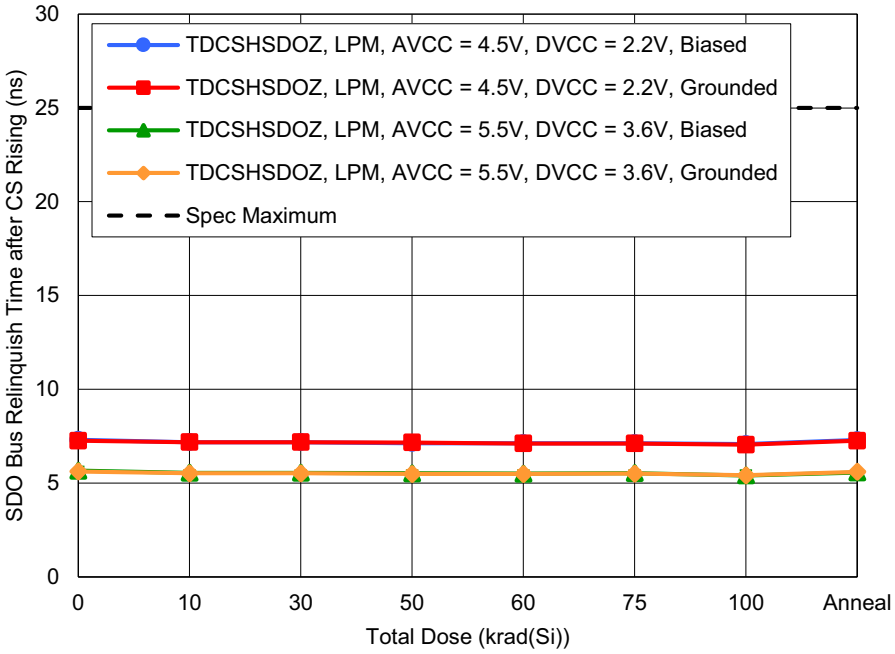


Figure 56. ISL71148SLH SDO Bus Relinquish Time after $\overline{CS}$↑ ($t_{DCSHSDOZ}$) in low-power mode with C_L = 10pF and with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 25ns.

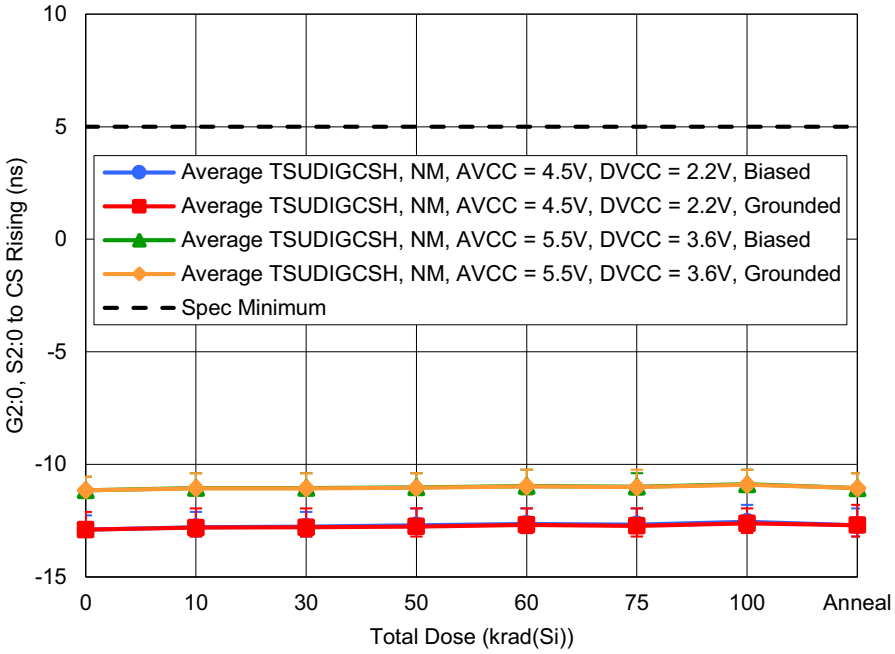


Figure 57. ISL71148SLH average G2:0, S2:0 to $\overline{CS}$↑ ($t_{SUDIGCSH}$) in normal operating mode with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all pins. The datasheet limit is a minimum of 5ns. *Note:* the measured values are the actual maximum required hold times, so the datasheet limits are the maximums of the measured values.

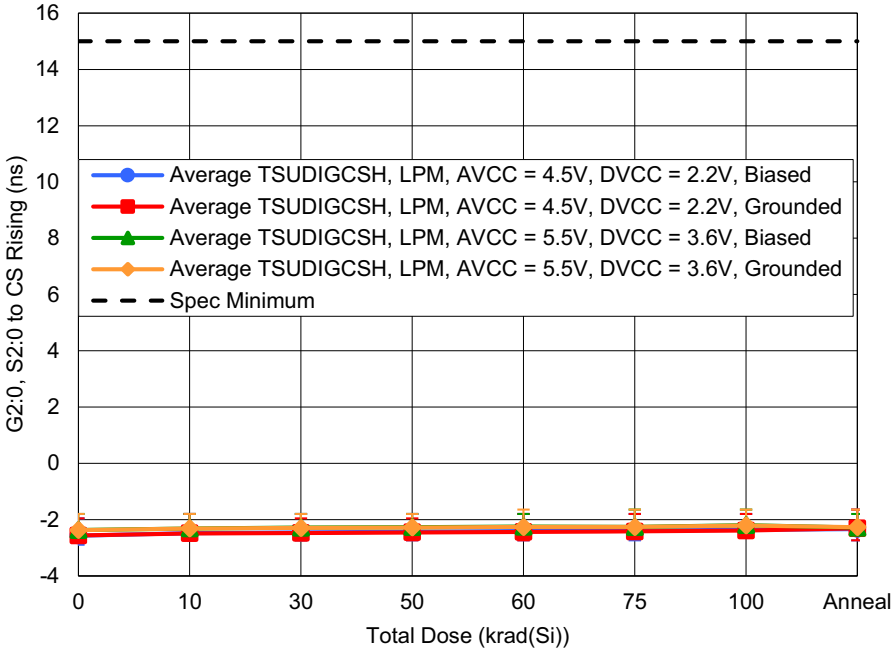


Figure 58. ISL71148SLH average G2:0, S2:0 to $\overline{CS}$↑ ($t_{SUDIGCSH}$) in low-power mode with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all pins. The datasheet limit is a minimum of 15ns. *Note:* the measured values are the actual maximum required hold times, so the datasheet limits are the maximums of the measured values.

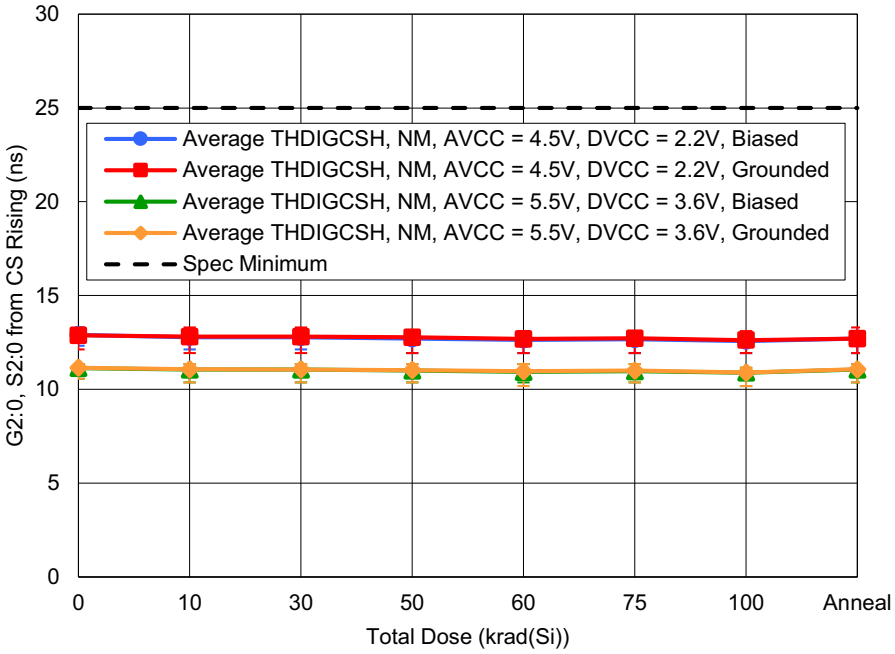


Figure 59. ISL71148SLH average G2:0, S2:0 from $\overline{CS}\uparrow$ ($t_{HDIGCSH}$) in normal operating mode with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all pins. The datasheet limit is a minimum of 25ns. *Note:* the measured values are the actual maximum required hold times, so the datasheet limits are the maximums of the measured values.

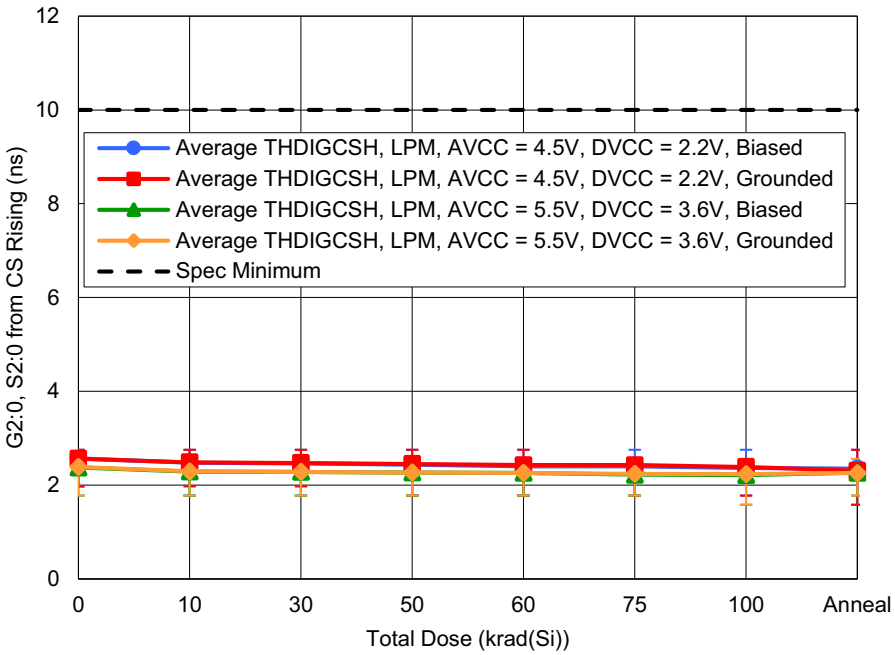


Figure 60. ISL71148SLH average G2:0, S2:0 from $\overline{CS}\uparrow$ ($t_{HDIGCSH}$) in low-power mode with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values across all pins. The datasheet limit is a minimum of 10ns. *Note:* The measured values are the actual maximum required hold times, so the datasheet limits are the maximums of the measured values.

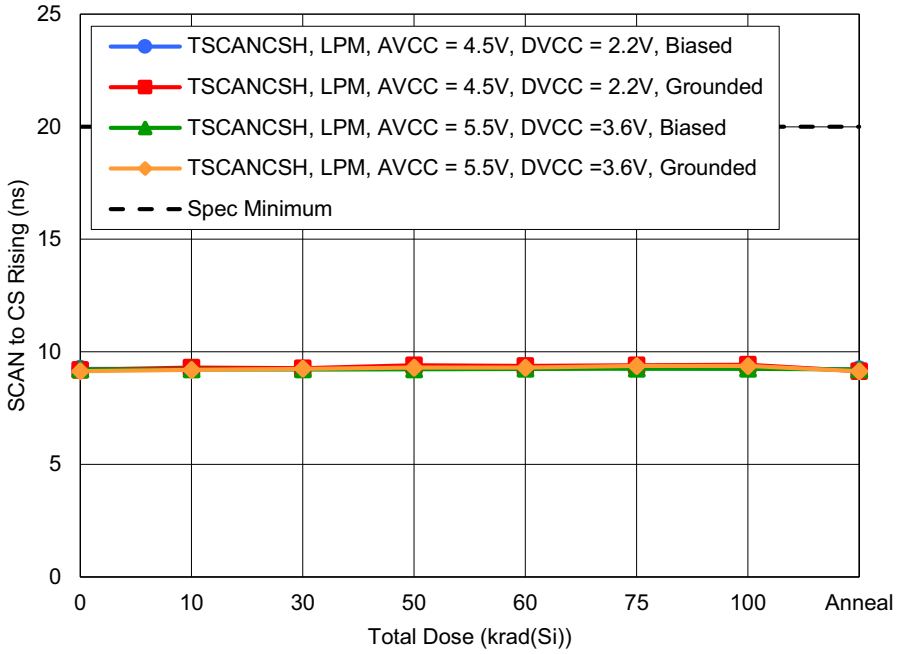


Figure 61. ISL71148SLH SCAN to $\overline{CS}\uparrow$ ($t_{SCANCSH}$) in low-power mode with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a minimum of 20ns. *Note:* The measured values are the actual maximum required hold times, so the datasheet limits are the maximums of the measured values.

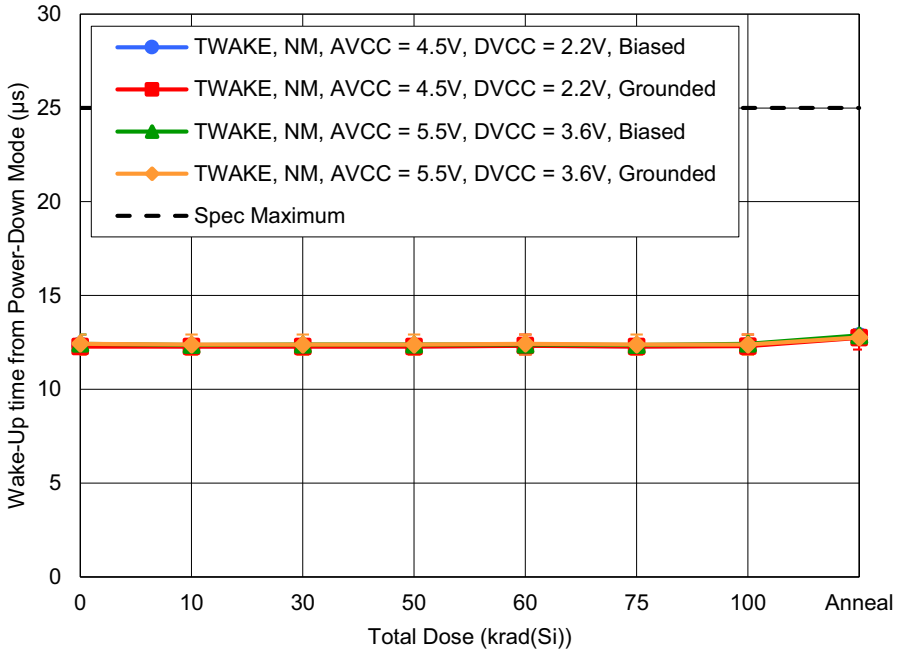


Figure 62. ISL71148SLH wake-up time from power-down mode (t_{WAKE}) in normal operating mode (but results also apply to LPM) with AV_{CC} = 4.5V and DV_{CC} = 2.2V or AV_{CC} = 5.5V and DV_{CC} = 3.6V as a function of LDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 25µs.

3. Discussion and Conclusion

This document reports the results of the LDR TID testing of the ISL71148SLH radiation tolerant 8-channel 14-bit 900/480ksps SAR ADC. Biased and grounded samples were irradiated to 100krad(Si) at an LDR of 0.01rad(Si)/s, followed by a 168-hour anneal at 100ºC under bias. All datasheet parameters passed at all downpoints. No evidence of bias dependence was observed.

4. Revision History

Revision	Date	Description
1.00	Apr 22, 2024	Initial release.

Appendix

Table 3 lists the datasheet parameters that are considered indicative of part performance. These parameters are plotted in Figure 3 through Figure 62. All limits are taken from the ISL71148SLH datasheet, which may also have more details on test conditions.

Table 3. ISL71148SLH Datasheet Total Dose Parameters (T_A = 25ºC)

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
3	Integral Non-Linearity	INL	Normal Mode; PGA Bypassed; AV_{CC} = 5V	-1	1	LSB
4			LPM; PGA Bypassed; AV_{CC} = 5V			
5	Differential Non-Linearity	DNL	Normal Mode; PGA Bypassed; AV_{CC} = 5V	-0.5	0.5	LSB
6			LPM; PGA Bypassed; AV_{CC} = 5V			
7	Zero-Scale Error	ZSE	Normal Mode; PGA Bypassed; AV_{CC} = 5V	-4	4	LSB
			LPM; PGA Bypassed; AV_{CC} = 5V			
8	Positive Full-Scale Error	+FSE	Normal Mode; PGA Bypassed; AV_{CC} = 5V	-7	7	LSB
			LPM; PGA Bypassed; AV_{CC} = 5V			
9	Negative Full-Scale Error	-FSE	Normal Mode; PGA Bypassed; AV_{CC} = 5V	-7	7	LSB
			LPM; PGA Bypassed; AV_{CC} = 5V			
10	Signal-to-Noise Ratio	SNR	Normal Mode; PGA Bypassed; AV_{CC} = 5V	82	-	dBFS
			LPM; PGA Bypassed; AV_{CC} = 5V			
11			Normal Mode; PGA Gain = 2; AV_{CC} = 5V	76	-	
			LPM; PGA Gain = 2; AV_{CC} = 5V			
12	Signal-to-Noise + Distortion Ratio	SINAD	Normal Mode; PGA Bypassed; AV_{CC} = 5V	81	-	dBFS
			LPM; PGA Bypassed; AV_{CC} = 5V			
13			Normal Mode; PGA Gain = 2; AV_{CC} = 5V	79	-	
			LPM; PGA Gain = 2; AV_{CC} = 5V			
14	Effective Number of Bits	ENOB	Normal Mode; PGA Bypassed; AV_{CC} = 5V	13.1	-	bits
			LPM; PGA Bypassed; AV_{CC} = 5V			
15			Normal Mode; PGA Gain = 2; AV_{CC} = 5V	12.8	-	
			LPM; PGA Gain = 2; AV_{CC} = 5V			
16	Total Harmonic Distortion	THD	Normal Mode; PGA Bypassed; AV_{CC} = 5V	85	-	dBFS
			LPM; PGA Bypassed; AV_{CC} = 5V			
17			Normal Mode; PGA Gain = 2; AV_{CC} = 5V	85	-	
			LPM; PGA Gain = 2; AV_{CC} = 5V			

Table 3. ISL71148SLH Datasheet Total Dose Parameters (T_A = 25ºC) (Cont.)

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
18	Spurious Free Dynamic Range	SFDR	Normal Mode; PGA Bypassed; AV_{CC} = 5V	90	-	dBFS
			LPM; PGA Bypassed; AV_{CC} = 5V			
19			Normal Mode; PGA Gain = 2; AV_{CC} = 5V	90	-	
			LPM; PGA Gain = 2; AV_{CC} = 5V			
20	Input Leakage Current	IA_{IN}	A_{IN} = 0V, 2.6V	-1	1	µA
21	REF Input Current	I_{REF}	Normal Mode, LPM; PGA Bypassed; V_{REF} = 2.6V	-	200	µA
22	Analog Supply Current – Active	I_{AVCC}	Normal Mode; PGA Bypassed; AV_{CC} = 5V; f_{SAMP} = 900.901ksps	-	23	mA
			Normal Mode; PGA Gain = 2; AV_{CC} = 5V; f_{SAMP} = 483.092ksps	-	20.5	
23			LPM; PGA Bypassed; AV_{CC} = 5V; f_{SAMP} = 670ksps	-	17.5	
			LPM; PGA Gain = 2; AV_{CC} = 5V; f_{SAMP} = 413.223ksps	-	16.9	
24	Analog Supply Current – Static	I_{STATIC}	Normal Mode; PGA Bypassed; AV_{CC} = 5V; $\overline{CS}$ held low	-	9	mA
25			Normal Mode; PGA Gain = 2; AV_{CC} = 5V; $\overline{CS}$ held low	-	13	
26			LPM; PGA Bypassed; AV_{CC} = 5V; $\overline{CS}$ held low	-	7.5	
			LPM; PGA Gain = 2; AV_{CC} = 5V; $\overline{CS}$ held low			
27	Analog Supply Current – Sleep	I_{SLAVCC}	Normal Mode; AV_{CC} = 5V; $\overline{PD}$ held low	-	-	µA
28	Digital Supply Current – Active	I_{DVCC}	Normal Mode; PGA Bypassed; DV_{CC} = 2.5V; f_{SCK} = 50MHz	-	700	µA
			LPM; PGA Bypassed; DV_{CC} = 2.5V; f_{SCK} = 50MHz			
29			Normal Mode; PGA Gain = 2; DV_{CC} = 2.5V; f_{SCK} = 50MHz	-	600	
			LPM; PGA Gain = 2; DV_{CC} = 2.5V; f_{SCK} = 50MHz			
30	Digital Supply Current – Static	I_{STDVCC}	Normal Mode; PGA Bypassed; DV_{CC} = 2.5V; $\overline{CS}$ held low	-	90	µA
31			LPM; PGA Bypassed; DV_{CC} = 2.5V; $\overline{CS}$ held low	-	120	
32			Normal Mode; PGA Gain = 2; DV_{CC} = 2.5V; $\overline{CS}$ held low	-	120	
33			LPM; PGA Gain = 2; DV_{CC} = 2.5V; $\overline{CS}$ held low	-	140	

Table 3. ISL71148SLH Datasheet Total Dose Parameters (T_A = 25ºC) (Cont.)

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
34	High-Level Input	V_{IH}	DV_{CC} = 2.2V, 3.6V	0.8 × DV_{CC}	-	V
	Low-Level Input	V_{IL}	DV_{CC} = 2.2V, 3.6V	-	0.2 × DV_{CC}	V
35	Input Current ($\overline{CS}$, SCK, SCAN, PGABP, S2, S1, S0, G2, G1, G0)	I_{IN}	DV_{CC} = 2.2V; V_{IN} = 0V, 2.2V	-1	1	µA
			DV_{CC} = 3.6V; V_{IN} = 0V, 3.6V			
36	High-Level Output	V_{OH}	DVCC = 2.2V;DV_{CC} – Output; I_O = -500µA	2	-	V
37			DVCC = 3.6V; DV_{CC} – Output; I_O = -500µA	3.4	-	
38	Low Level Output	V_{OL}	DVCC = 2.2V; I_O = 500µA	-	0.2	V
39			DVCC = 3.6V; I_O = 500µA			
40	Hi-Z Output Leakage Current	I_{OZ}	DV_{CC} = 2.2V, 3.6V; V_{OUT} = 0V to DV_{CC}	-1	1	µA
41	$\overline{PD}$ Input Resistance	R_{INPDL}	Internal pull-up resistance to DV_{CC}	400	600	kΩ
42	LPM Input Resistance	R_{INLPM}	Internal pull-down resistance to GND; DV_{CC} = 2.2V, 3.6V	400	600	kΩ
43	Conversion Time	t_{CONV}	Normal Mode; PGA bypassed; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; BUSY output high time	-	660	ns
			LPM; PGA bypassed; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; BUSY output high time			
44			Normal Mode; PGA enabled; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; BUSY output high time	-	1550	
			LPM; PGA enabled; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; BUSY output high time			
45	$\overline{CS}$ ↓ to BUSY ↑	t_{BUSYLH}	Normal Mode; PGA bypassed; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; C_L = 10pF	-	30	ns
			LPM; PGA bypassed; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; C_L = 10pF			
46			Normal Mode; PGA Gain = 2; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; C_L = 10pF	-	100	
			LPM; PGA Gain = 2; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; C_L = 10pF			

Table 3. ISL71148SLH Datasheet Total Dose Parameters (T_A = 25ºC) (Cont.)

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
47	SDO Data Valid Delay from BUSY ↓	$t_{DBUSYLSDOV}$	Normal Mode; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; C_L = 10pF	-	0	ns
48			LPM; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; C_L = 10pF			
49	SDO Data Valid Delay from SCK ↑	$t_{DSCKSDOV}$	Normal Mode; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; C_L = 10pF	-	20	ns
50			LPM; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; C_L = 10pF			
51	SDO Data Valid Hold Time from SCK ↑	t_{HSDOV}	Normal Mode; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; C_L = 10pF	7	-	ns
52			LPM; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; C_L = 10pF			
53	SDO Bus Acquisition Time from $\overline{CS}$ ↓	$t_{DCSLSDOL}$	Normal Mode; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; C_L = 10pF	-	25	ns
54			LPM; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; C_L = 10pF			
55	SDO Bus Relinquish Time after $\overline{CS}$ ↑	$t_{DCSHSDOZ}$	Normal Mode; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; C_L = 10pF	-	25	ns
56			LPM; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V; C_L = 10pF			
57	G2:0, S2:0 to $\overline{CS}$ ↑	$t_{SUDIGCSH}$	Normal Mode; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V	5	-	ns
58			LPM; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V	15	-	
59	G2:0, S2:0 from $\overline{CS}$ ↑	$t_{HDIGCSH}$	Normal Mode; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V	25	-	ns
60			LPM; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V	10	-	
61	SCAN to $\overline{CS}$ ↑	$t_{SCANCSH}$	LPM; AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V	20	-	ns
62	Wake-Up time from Power-Down Mode	t_{WAKE}	Normal Mode (but results apply to LPM); AV_{CC} = 4.5V, 5.5V; DV_{CC} = 2.2V, 3.6V	-	25	µs

Related Literature

For a full list of related documents, visit our website:

- ISL71148SLH device page
- MIL-STD-883 test method 1019

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