ISL71831SEH

Single Event Effects (SEE) Testing

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Introduction

The intense proton and heavy ion environment encountered in space applications can cause a variety of Single Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Gate Rupture (SEGR) and Single Event Burnout (SEB). SEE can lead to system-level performance issues including disruption, degradation and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. This report discusses the results of SEE testing performed on the Intersil ISL71831SEH 32:1 analog multiplexer (MUX) designed for space applications.

Product Description

The ISL71831SEHVF is a 32:1 analog multiplexer (MUX) that operates with supply voltages from 3V to 5.5V and input overvoltage capability to +7V. The part is also “cold spare” capable; i.e., inputs of an unpowered part do not leak more than 1µA to +7V. The ISL71831SEHVF is fabricated in a proprietary Intersil bonded wafer SOI BiCMOS process (P6SOI).

The ISL71830SEHVF is a 16-channel MUX based on the 32-channel ISL71831SEHVF. Since the 16-channel ISL71830SEHVF is constructed with all the same design blocks as the 32-channel ISL71831SEHVF, the results reported. here for the 32-channel ISL71831SEHVF are closely related to the performance of the ISL71830SEHVF reported separately.

Product Documentation

- ISL71831SEH datasheet
- Standard Microcircuit Drawing (SMD): 5962-15248

SEE Test Objectives

The ISL71831SEH was tested to determine its susceptibility to destructive single event effects (SEGR and SEB, collectively referred to by SEB herein) and to characterize its Single Event Transient (SET) behavior over various conditions. The ISL71831SEH parts tested came from lot J69526.1, manufactured on Intersil's proprietary P6SOI process.

SEE Test Facility

Testing was performed at the Texas A&M University (TAMU) Cyclotron Institute heavy ion facility. This facility is coupled to a K500 superconducting cyclotron, which is capable of generating a wide range of test particles with the various energy, flux and fluence levels needed for advanced radiation testing. Details on the test facility can be found on the TAMU Cyclotron website. Testing was carried out on March 20, 2015 and May 30, 2015.

SEE Test Set-Up

SEE testing is carried out with the sample in an active configuration. A schematic of the ISL71831SEH SEE test fixture is shown in Figure 1. The test circuit is configured to accept variable supply voltage and two groupings of input voltages. The addressing of input IN22 is accomplished with VD1 low and VD2 high. With both VD1 and VD2 high the switches are all disabled. When VIN22 is selected, the output is set to half of VIN22 by a resistor divider formed from VIN22 to GND through VOUT. Of the remaining inputs, the odd numbered ones are connected to VINO and the even numbered ones are connected to VINE.

The ISL71831SEH samples in standard ceramic flatpack packages without lids were assembled on boards for irradiation. A 20-foot coaxial cable was used to connect the test fixture to a switch box in the control room, which contained all of the monitoring equipment.

Digital multimeters were used to monitor pertinent voltages and currents. LeCroy waveRunner 4-channel digital oscilloscopes were used to capture and store SET traces at VOUT that exceeded the oscilloscope's ±20mV AC trigger setting.

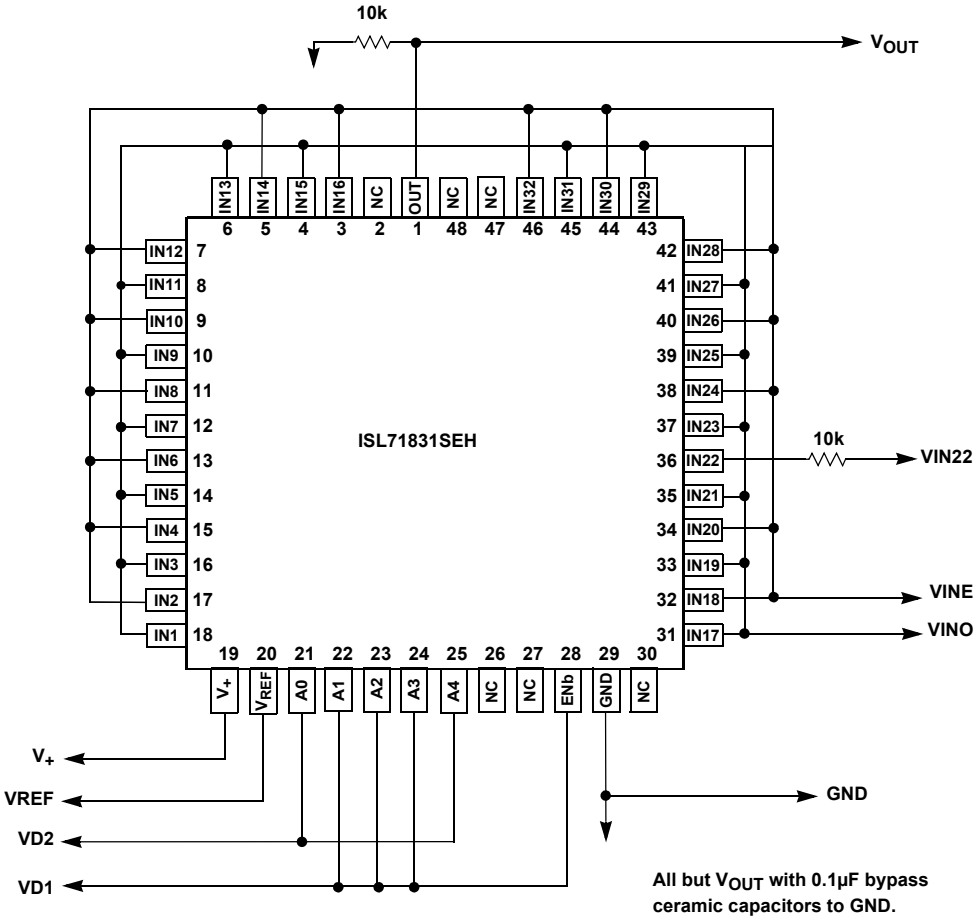

FIGURE 1. SCHEMATIC OF THE ISL71831SEHVF SEE TESTING CONFIGURATION

SEE Damage (SEB) Testing

For the destructive SEE (SEB) tests, conditions were selected to maximize the electrical and thermal stresses on the Device Under Test (DUT), thus insuring worst-case conditions. Two SEB tests were run with the conditions listed in Table 1. The supply voltage was set to the levels of 6V and 6.3V. The input voltages were split between the supply rail (VINO) and ground (VINE). Case temperature was maintained at +125°C ±10°C by controlling the current flowing into a resistive heater bonded to the underside of the board. Four DUTs were irradiated with 2.114GeV Pr ions at 10° incidence resulting in an effective surface LET = 60MeV • cm^2/mg.

The normal range into silicon for these Pr ions after 40 mm of air is about 118µm with a Bragg peak range of 37µm. More detail can be found on the TAMU Cyclotron website. These conditions guaranteed ions transited all active device volume in this SOI process (about 10µm depth). Each irradiation was to a fluence of $4x10^6$ ion/cm^2. The currents into each of the voltage supplies was measured before and after each irradiation to look for changes indicative of permanent damage to the part.

TABLE 1. SEB TESTING CONDITIONS

NUMBER OF TESTS	EFFECTIVE LET (MeV • cm^2/mg)	TCASE (°C)	V_+	VINO (V)	VINE (V)	VIN22 (V)	VREF (V)	VD1 (V)	VD2 (V)
Test 1	59 at 10°	+125	6	6	0	6	6	0	6
Test 2	59 at 10°	+125	6.3	6.3	0	6.3	6.3	0	6.3

NOTE: Irradiation was with 2.114GeV Pr at 10° incidence for effective LET = 60MeV • cm^2/mg to a fluence of $4x10^6$ ions/cm^2.

As none of the supply currents reported in Table 2 changed by more than measurement repeatability, it is inferred that they indicate no damage occurred due to the exposure to the ions. Based on this, it is concluded that the part is immune to destructive SEE effects under the conditions tested in Table 1. Table 2 is represented as percentage change in Table 3.

TABLE 2. SEB MONITOR PARAMETERS FOR TESTING AT EFFECTIVE LET = 60MeV•cm^2/mg AND T_{CASE} = +125°C

MONITORED PARAMETER (V)			OUT (V)	I+ (nA)	I_{INO} (nA)	I_{REF} (µA)	ID2 (nA)
DUT1	6	Pre	2.99	24.9	77	125	3.3
		Post	2.99	24.2	–	125	3.2
	6.3	Pre	3.14	26.9	92	125	3.5
		Post	3.14	27.0	92	125	3.4
DUT2	6	Pre	2.99	57.6	188	125	3.4
		Post	2.99	58.3	189	125	3.2
	6.3	Pre	3.14	65.0	259	125	3.3
		Post	3.14	66.4	263	125	3.3
DUT3	6	Pre	2.99	37.3	137	125	3.1
		Post	2.99	37.9	138	125	3.3
	6.3	Pre	3.14	41.7	168	126	3.2
		Post	3.14	41.8	168	126	3.1
DUT4	6	Pre	2.99	46.6	187	125	3.3
		Post	2.99	47.2	192	125	3.4
	6.3	Pre	3.14	52.5	231	126	3.4
		Post	3.14	52.5	232	125	3.4

NOTE: Each irradiation was to a fluence of 4x10^6 ions/cm^2.

TABLE 3. PARAMETER CHANGES IN PERCENTAGE FOR THE IRRADIATIONS WITH EFFECTIVE LET = 60MeV•cm^2/mg to 4x10^6 Ions/cm^2 PER RUN

		V_{OUT} (V)	IV_+ (nA)	IVINO (nA)	IVREF (µA)	IVD2 (nA)
DUT1	6V	0%	-3%	-	0%	-3%
	6.3V	0%	0%	0%	0%	-3%
DUT2	6V	0%	1%	1%	0%	-6%
	6.3V	0%	2%	2%	0%	0%
DUT3	6V	0%	2%	1%	0%	6%
	6.3V	0%	0%	0%	0%	-3%
DUT4	6V	0%	1%	3%	0%	3%
	6.3V	0%	0%	0%	0%	0%

NOTE: It should be noted that two units tested at 6.5V and 60MeV•cm^2/mg registered damage, specifically on IVREF and IVD2.

SET Testing of ISL71831SEH 32:1 Analog MUX

SET testing was done on four samples of the ISL71831SEH. Testing started with 10° incident praseodymium (Pr) for effective LET = 60MeV•cm^2/mg and with the SET detection threshold set to ±20mV deviation on V_{OUT}. Three separate conditions as shown in Table 4 were applied to each of the four parts tested. Tests 1 and 2 looked for SET on V_{OUT} with IN22 selected, while Test 3 looked at V_{OUT} with all switches disabled. Addressing inputs were put at the respective V_{IL} and V_{IH} levels to test for addressing upsets. The first test, Test 1, tested the part operating at the bottom of the recommended supply voltage range, 3V. The second test exercised the part at the maximum of the supply voltage range, 5.5V. In the third case, Test 3, with the upper supply voltage, the switches were disabled by the addressing so that the output was pulled to ground. In all cases the V_{REF} was set to the minimum of the recommended operating range of 3V to minimize the noise margin in the addressing circuits. The lower noise margins makes the addressing most susceptible to an SEE leading to an address change SET.

Table 5 summarizes the SET counts for each test by DUT and then reports the nominal SET cross section for the complement of all four DUT's. The cross sections reported are the nominal found by dividing the event counts by the total fluence generating those counts.

Post processing of the captured SET oscilloscope traces, including some digital filtering, generated the composite plots in Figures 2, 3 and 4 for the effective LET = 60MeV•cm^2/mg case. These plots show the composite of the 20 largest and 20 longest events for each polarity of the extreme deviation so they reflect the worst 80 SET observed in the run. The first two SET. Figures 2 and 3, show the SET with IN22 selected and driven from V_+, 3V and 5.5V respectively, while OUT is connected to GND, both connections through 10kΩ resistors. Figure 4 shows the VOUT SET with all switches disabled and V_+ at 5.5V.

The SET in Figure 2 show somewhat larger negative going events of the OUT node. The positive going SET are somewhat more consistent. In no cases does it appear that an address change occurred since the terminal voltages are within ±50mV of the DC V_{OUT} level.

At the higher supply of 5.5V there seems to be a balance between the positive and negative SET with both exhibiting peak magnitudes of about 75mV and capacitance charging magnitudes of about 20mV. Again there is no indication of an addressing SET occurring since the SET magnitudes do not approach either extreme (±2.75V) that would apply for an address disruption.

The SET plots in Figure 4 exhibit an asymmetry favoring large SET in the positive direction. This is to be expected since the nominal output is a ground due to the testing conditions. With that exception, the SET do not look particularly different from those in Figures 2 or 3.

TABLE 4. SET TESTING CONDITIONS

NUMBER OF TESTS	V_+ (V)	V_{REF} (V)	VD1 (V)	VD2 (V)	VINO (V)	VINE (V)	VIN22 (V)	~OUT (V)
Test 1	3	3	0.9	2.1	3	0	3	1.50
Test 2	5.5	3	0.9	2.1	5.5	0	5.5	2.75
Test 3	5.5	3	2.1	2.1	5.5	0	5.5	0

TABLE 5. ±20mV SET COUNTS ON V_{OUT} FOR TESTING OF THE ISL71831SEH.

TESTS CONFIGURATIONS	DUT1 ±20mV EVENT COUNTS	DUT2 ±20mV EVENT COUNTS	DUT3 ±20mV EVENT COUNTS	DUT4 ±20mV EVENT COUNTS	TOTAL ±20mV SET CROSS SECTION (cm^2)
Test 1	115	102	101	94	2.6E-05
Test 2	144	112	113	134	3.1E-05
Test 3	59	66	73	68	1.7E-05

NOTE: LET was 60MeV•cm^2/mg and fluence of $4x10^6$ ions/cm^2 per run.

Composite Plots

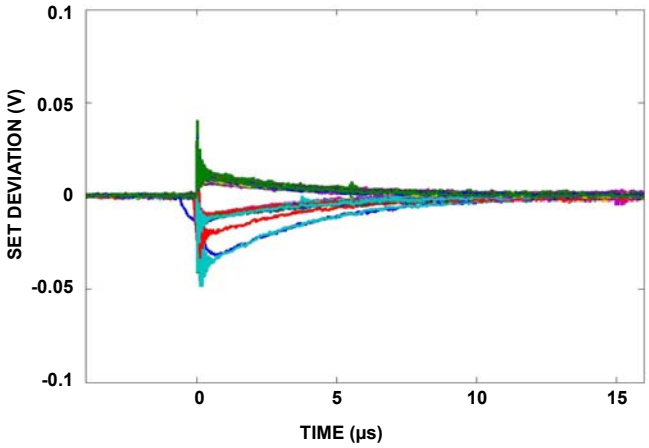

FIGURE 2A.

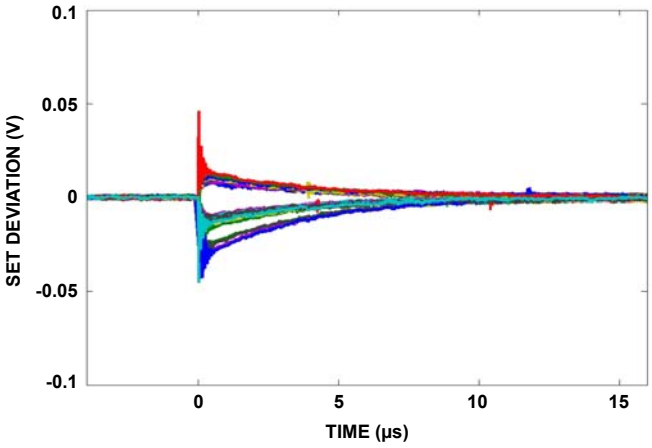

FIGURE 2B.

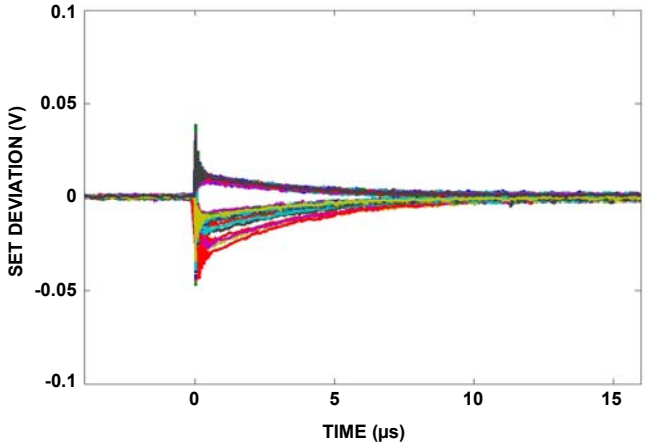

FIGURE 2C.

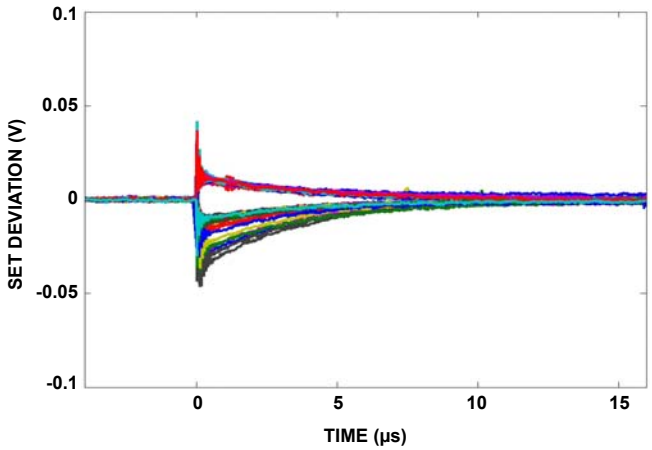

FIGURE 2D.

FIGURE 2. Composite plots of extreme V_{OUT} SET for effective LET = 60MeV • cm^2/mg for DUT 1 through 4 and Test 1, 3V supply and IN22 selected. Each run was to $4x10^6$ ions/cm^2. Post processing selected the 20 largest and longest SET with both positive and negative deviations; not all of 80 such plots were unique.

Composite Plots (Continued)

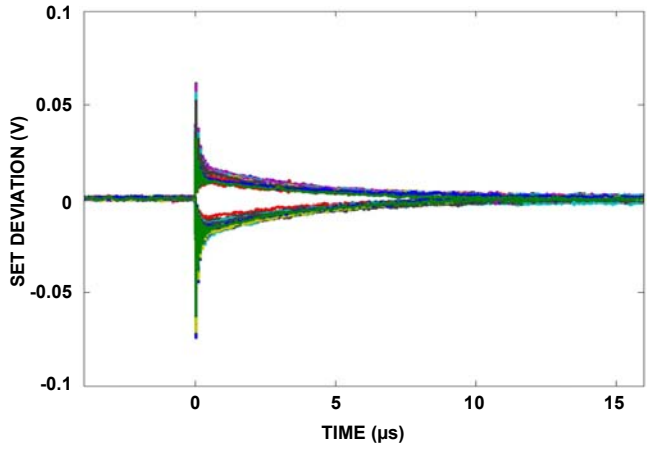

FIGURE 3A.

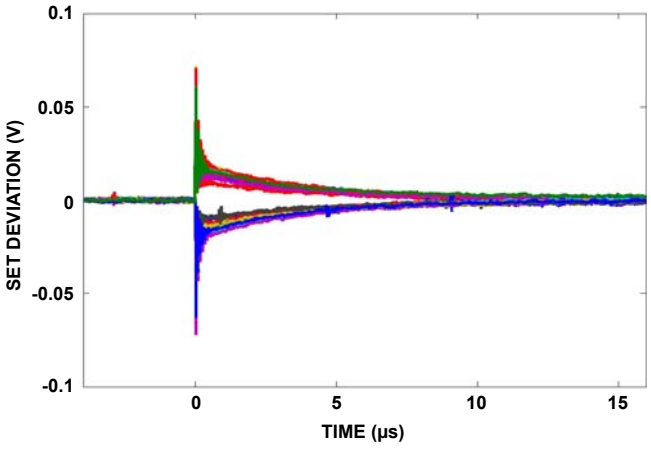

FIGURE 3B.

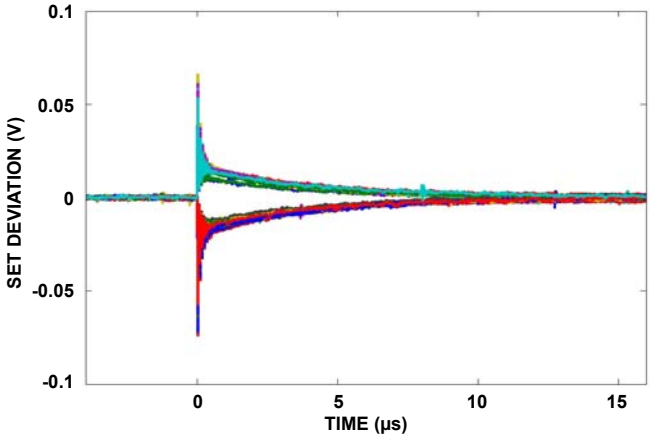

FIGURE 3C.

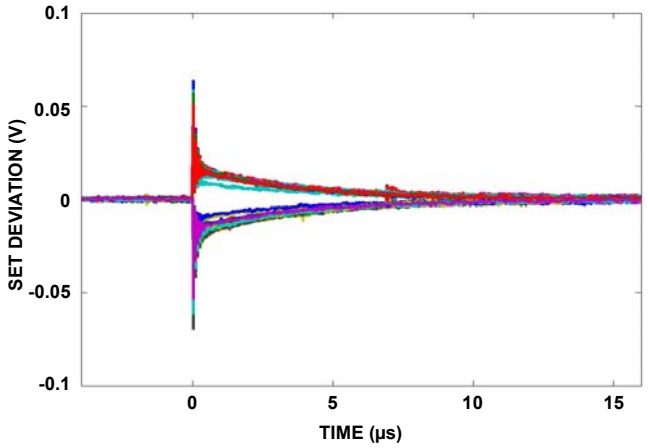

FIGURE 3D.

FIGURE 3. Composite plot of SET for effective LET = 60MeV • cm^2/mg for DUT 1 through 4 and Test 2, 5.5V supply with IN22 selected. Each run was to $4x10^6$ ions/cm^2. Post processing selected the 20 largest and longest SET in both positive and negative deviations; not all of the 80 such plots were unique.

Composite Plots (Continued)

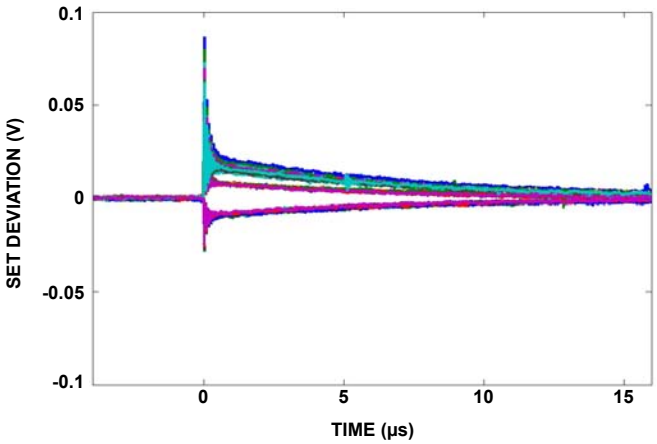

FIGURE 4A.

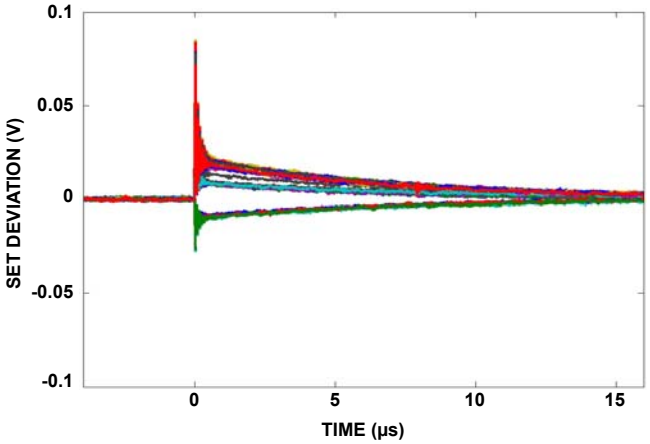

FIGURE 4B.

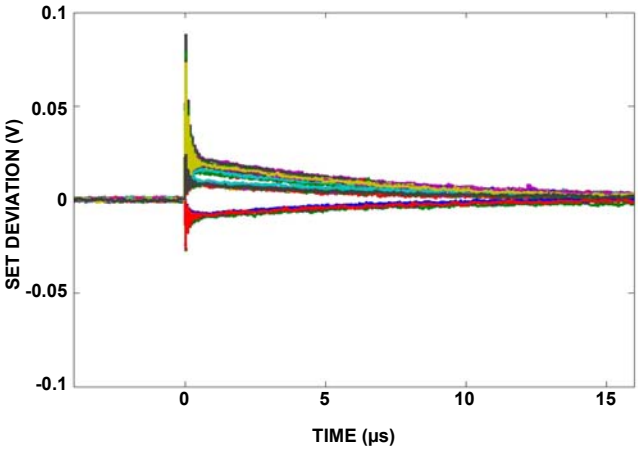

FIGURE 4C.

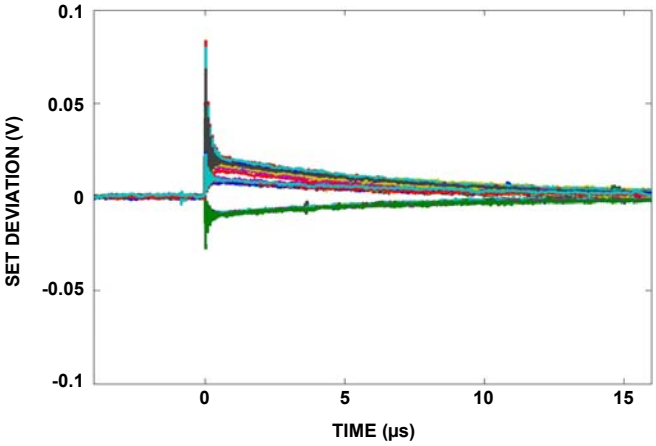

FIGURE 4D.

FIGURE 4. Composite plot of SET for effective LET = 60MeV • cm^2/mg for DUT 1 through 4 and Test 3, 5.5 V supply and switches disabled. Each run was to $4x10^6$ ions/cm^2. Post processing selected the 20 largest and longest SET in both positive and negative deviations; not all of the 80 such plots were unique.

Discussion and Conclusions

SEL and SEB

Testing with 10º incident Pr for effective LET = 60MeV • cm^2/mg did not result in any indications of SEB or SEGR at applied voltages up to 6.3V for the supplies and inputs. The 2.114GeV Pr had a range into silicon of 117µm and a Bragg Range of 37µm putting the Bragg peak well into the inactive handle wafer of the SOI part. Functionality and operational currents monitored did not change as a result of the irradiations carried out at a case temperature of +125ºC ±10ºC. It should be noted however that two devices were damaged when tested at 6.5V. A minimal interpretation of the possible SEB/SEGR cross section is less than $1.8x10^{-7}cm^2$ to a 95% confidence at LET = 60MeV • cm^2/mg for the voltages up to 6.3V. This is all tantamount to saying that under normal operating conditions the ISL71831SEH is not susceptible to SEB or SEGR failures at up to effective LET = 60MeV • cm^2/mg and operating voltages to 6.3V.

SET Results

In SET testing no indication of an addressing upset was noted. However, SET testing did result in events exceeding the ±20mV detection threshold. The total cross section indicated by the SET capture counts topped out at $3.1x10^5/cm^2$ at effective LET = 60MeV • cm^2/mg. The number of SET ±20mV captures was weakly dependent on supply voltage with 3V yielding slightly fewer captured SET than with 5.5V. It appears the SET result from instantaneous coupling of the output to the supply rails. All SET captured were within ±100mV spike deviation. The charging of the V_{OUT} node was generally less than ±50mV.

The observed output SET had decay times of about 15µs. This is likely set by the capacitive loading on V_{OUT} (about 700pF from the cabling) and the resistance setting the nominal voltage (5kΩ). Thus predicted 3.5µs time constant is consistent with that observed. This is important since the application will determine this decay constant and hence the SET duration.

It should be noted that Test 3 where the switches were disabled, the positive SET were larger than the negative as would be expected since V_{OUT} was pulled to ground. In any case, the largest positive SET were still within 100mV.

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