ISL73006SLH

High Dose Rate Total Ionizing Dose Testing of the ISL73006SLH 18V, 1A Point-of-Load Regulator

Introduction

This report summarizes the results of high dose rate (HDR) total ionizing dose (TID) testing of the ISL73006SLH, a radiation hardened, 18V, 1A Point-of-Load (POL) regulator. The test was conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of the bias sensitivity. Parts were irradiated either under bias or with all pins grounded at HDR (68rad(Si)/s) to 150krad(Si) followed by a 168-hour biased anneal at 100ºC. The ISL73006SLH is rated to 75krad(Si) at low dose rate (LDR) and is acceptance tested on a wafer-by-wafer basis to the datasheet limits. The ISL73006SLH is not rated for HDR.

Product Description

The ISL73006SLH is a radiation hardened POL buck regulator that provides up to 1A of output current capability with an input voltage ranging from 3V to 18V or 3V to 16.5V in a heavy ion environment. The device uses constant frequency peak current mode control architecture for fast loop transient response. The device uses internal compensation or an external Type II compensation to optimize performance and stabilize the loop. The ISL73006SLH has a default switching frequency of 500kHz.

The ISL73006SLH integrates high-side (P-Channel) and low-side (N-Channel) power FETs. There are options for external or internal compensation and slope control that can be implemented with minimum external components, reducing the BOM count and design complexity.

The ISL73006SLH includes a comprehensive suite of operational features and protections, including preset undervoltage, overvoltage, overcurrent protections, power-good, soft-start, and over-temperature.

The ISL73006SLH operates across the temperature range of -55°C to +125°C and is available in a 10-lead ceramic dual in-line flat package (CDFP) and die form. The pin assignments for the ISL73006SLH are shown in Figure 1, and the pin descriptions are shown in Table 1.

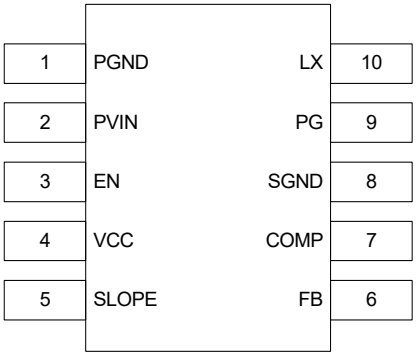


Figure 1. ISL73006SLH Pin Assignments

Table 1. ISL73006SLH Pin Descriptions

Pin Number	Pin Name	Description
1	PGND	Power-ground connection. Ground return for the low-side power MOSFET.
2	PVIN	Power Input. Supplies the power switches of the buck converter.
3	EN	Enable input. This is a comparator-type input with a rising threshold of 1.2V. Bypass this pin to the PCB ground plane with a 10nF ceramic capacitor to mitigate SEE. The pin can be tied to a maximum of 5V.

Table 1. ISL73006SLH Pin Descriptions (Cont.)

Pin Number	Pin Name	Description
4	VCC	Linear regulator output from PVIN to provide an internal bias supply rail of up to 5V. Bypass this pin to the PCB ground plane with a 2.2µF ceramic or low ESR Tantalum capacitor for stability, SEE, and noise mitigation. VCC is not intended to bias external circuits.
5	SLOPE	Slope Compensation. Connect a resistor from this pin to GND to externally set the slope compensation. This pin is a current source of 12µA into the external resistor. Connect the SLOPE pin to VCC to use the default internal slope compensation voltage of 1.2V. If not connected to VCC, add a 1nF capacitor from this pin to ground for SEE mitigation.
6	FB	Error Amplifier inverting input. Connect a resistor divider from VOUT to GND with the midpoint driving the FB pin.
7	COMP	Error Amplifier output. The external compensation network is connected from this pin to GND. Tie this pin to VCC to use the internal Error Amplifier compensation setup.
8	SGND	Signal ground. The ground is associated with the internal control circuitry. Connect this pin directly to the PCB ground plane at a single point. Pin 8 is connected to the thermal flash on the package bottom and the lid.
9	PG	Power-good output. The pin is an open-drain logic output pulled to SGND when the output is outside of the PGOOD range. The pin can be pulled to any voltage up to the PVIN absolute maximum limit. Renesas recommends using a nominal 1kΩ to 10kΩ pull-up resistor. Bypass this pin to the PCB ground plane with a 100pF capacitor for SEE mitigation.
10	LX	Switch node connection. Connect this pin to the output filter inductor. Internally, this pin is connected to the common node of the synchronous MOSFET power switches.

Contents

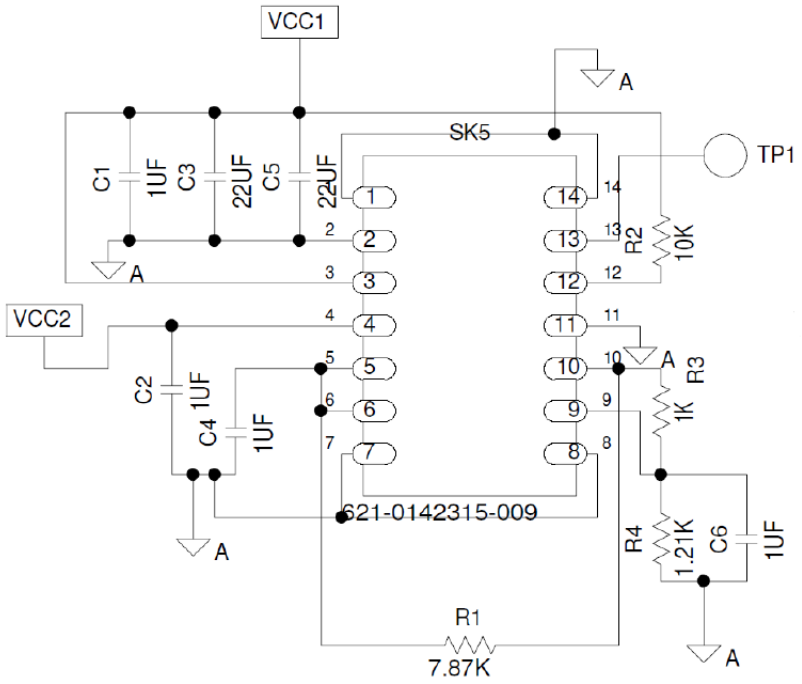
1. Test Description

1.1 Irradiation Facility

HDR testing was performed on June 8, 2023 at a dose rate of 68rad(Si)/s using a Gammacell 220 irradiator. The irradiator is located in the Palm Bay, Florida Renesas facility. A PbAl box was used to shield the test fixture and devices under test against low energy, secondary gamma radiation. Post-irradiation anneals were performed under bias in a small temperature chamber.

1.2 Test Fixturing

Figure 2 shows the configuration used for the biased HDR testing and for the anneal.



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VOLTAGES AND SEQUENCING:

1. VCC1 = V1 = 18.0V
2. VCC2 = V2 = 5.0V

REVERSE THE ORDER FOR POWER DOWN:

1. VCC2 = V2 = 0.0V
2. VCC1 = V1 = 0.0V

Figure 2. ISL73006SLH Irradiation Bias Configuration

1.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE) with data logging at each downpoint. Downpoint electrical testing was performed at room temperature.

1.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of four samples irradiated at HDR under bias and four samples irradiated at HDR with all pins grounded. All parts were also subject to a 168-hour, 100ºC biased anneal. Two control units were used.

The ISL73006SLH samples were drawn from wafer lots F6V359, F6V360, and F6V361. All samples were packaged in the standard 10 Ld CDFP.

1.5 Downpoints

The irradiation downpoints were 0krad(Si), 30krad(Si), 50krad(Si), 75krad(Si), 100krad(Si), and 150krad(Si). The irradiations were followed by a 168-hour high-temperature anneal at 100ºC under bias.

2. Results

TID testing of the ISL73006SLH is complete. All tested parameters passed the datasheet limits. Table 2 summarizes the results.

2.1 Attributes Data

Table 2. ISL73006SLH Attributes Data

Dose Rate (rad(Si)/s)	Condition	Sample Size	Downpoint	Pass[1]	Fail
68	Biased (Figure 2)	4	Pre-irradiation	4	0
			30krad(Si)	4	0
			50krad(Si)	4	0
			75krad(Si)	4	0
			100krad(Si)	4	0
			150krad(Si)	4	0
			Anneal	3	1[2]
68	Grounded	4	Pre-irradiation	4	0
			30krad(Si)	4	0
			50krad(Si)	4	0
			75krad(Si)	4	0
			100krad(Si)	4	0
			150krad(Si)	4	0
			Anneal	4	0

1. A Pass indicates a sample that passes all datasheet limits.
2. One device had a slight parametric failure on the Feedback Voltage Accuracy (V_{FB}) during the anneal following HDR irradiation. See Figure 11.

2.2 Variables Data

The plots in Figure 3 through Figure 44 illustrate the HDR response of the selected parameters shown in Table 3 in the Appendix. The plots show the average tested values of the parameters as a function of the total dose for each of the irradiation conditions, biased and grounded, plus a 168-hour, 100ºC biased anneal. The plots also include error bars at each down-point, representing the minimum and maximum measured values of the samples, although in some plots the error bars might not be visible due to their values compared to the scale of the graph.

All samples passed the datasheet limits after irradiation at HDR up to 150krad(Si). One sample had a slight parametric failure on the Feedback Voltage Accuracy (V_{FB}) during the anneal following irradiation at HDR as seen in Figure 11. The HDR data is provided for guidance only as the ISL73006SLH is only acceptance tested to 75krad(Si) at LDR.

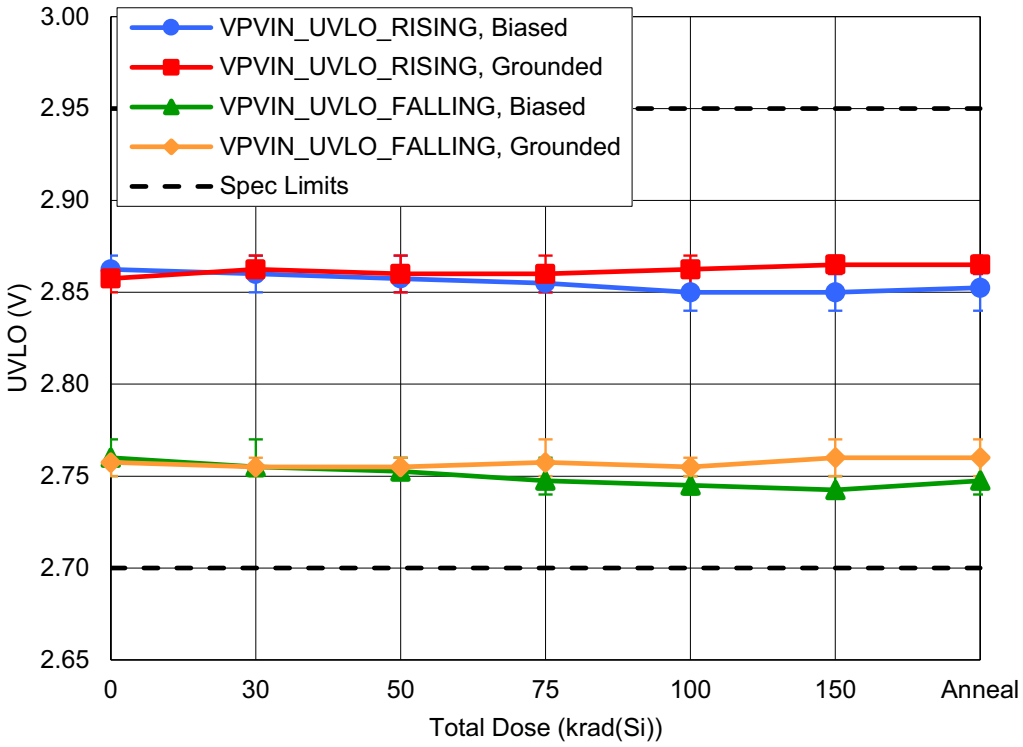

Figure 3. ISL73006SLH Rising and Falling Undervoltage Lockout (V_{PIN_UVLO}) as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 2.7V for Falling Undervoltage Lockout and a maximum of 2.95V for Rising Undervoltage Lockout.

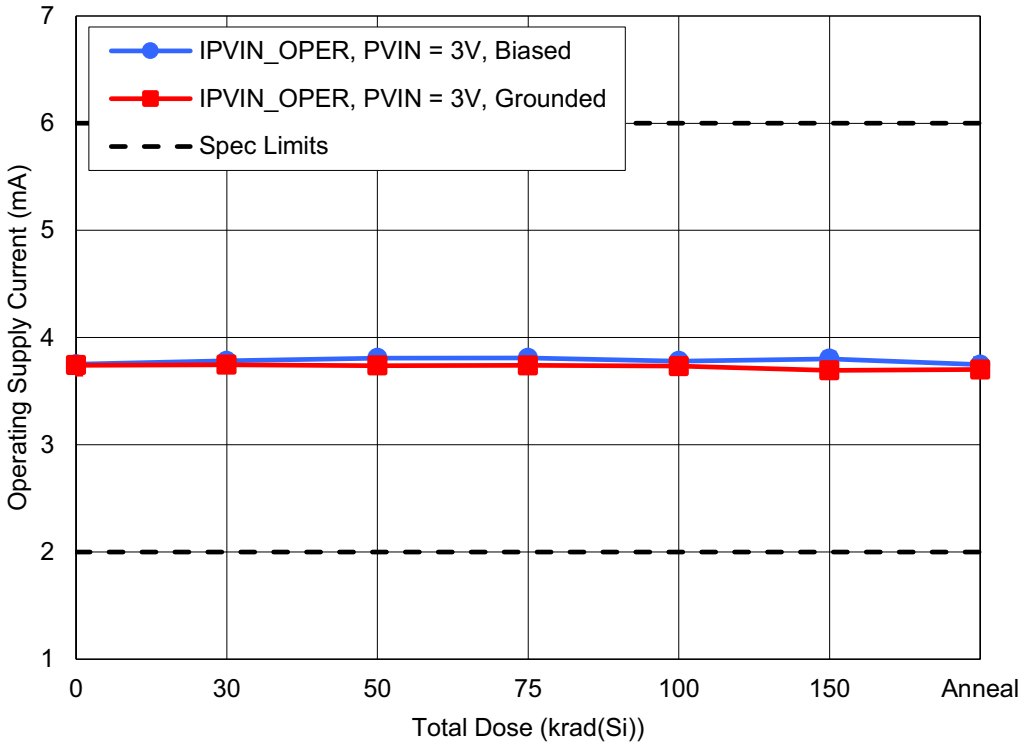

Figure 4. ISL73006SLH Operating Supply Current (I_{PVIN_OPER}) with PVIN = 3V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 2mA and a maximum of 6mA.

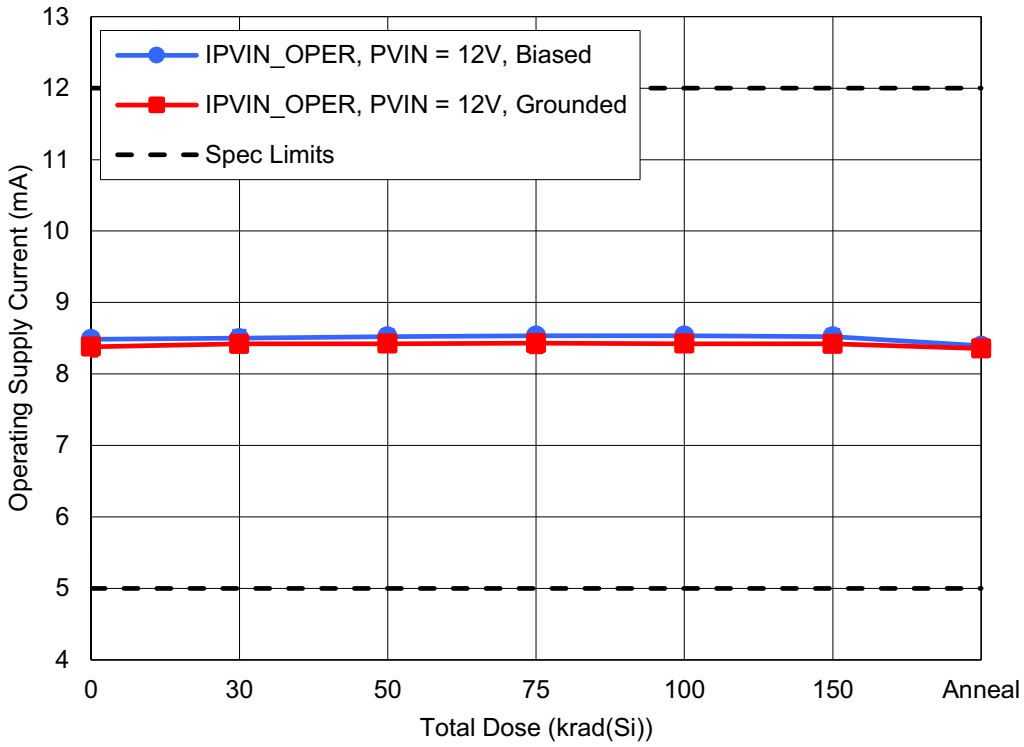

Figure 5. ISL73006SLH Operating Supply Current (I_{PVIN_OPER}) with PVIN = 12V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 5mA and a maximum of 12mA.

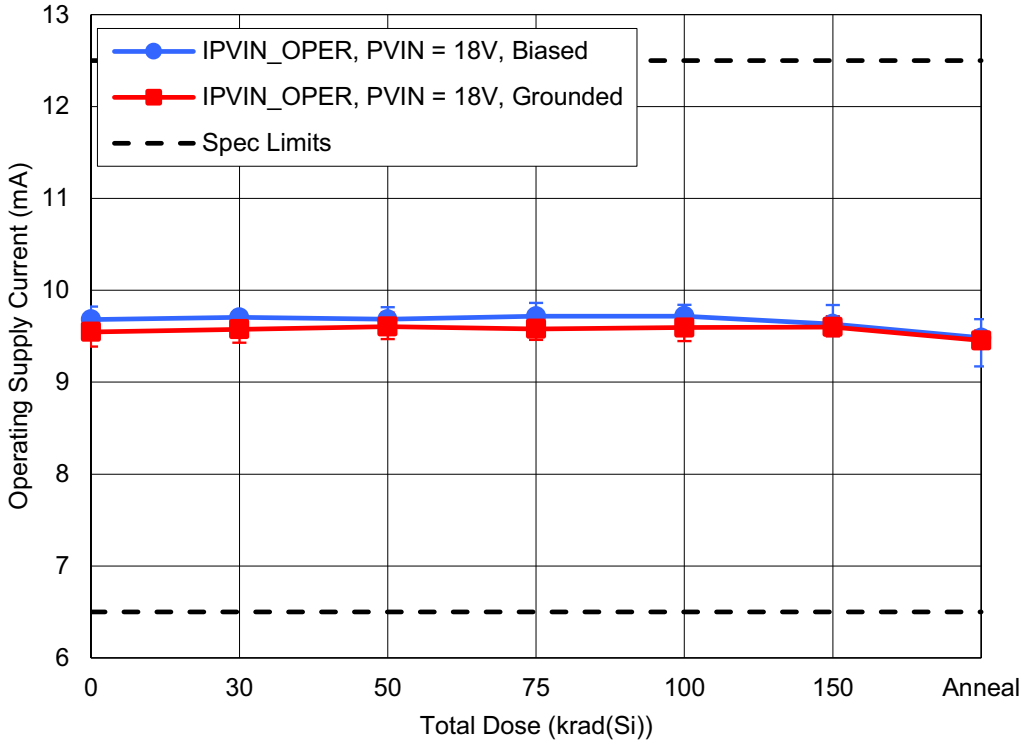

Figure 6. ISL73006SLH Operating Supply Current (I_{PVIN_OPER}) with PVIN = 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 6.5mA and a maximum of 12.5mA.

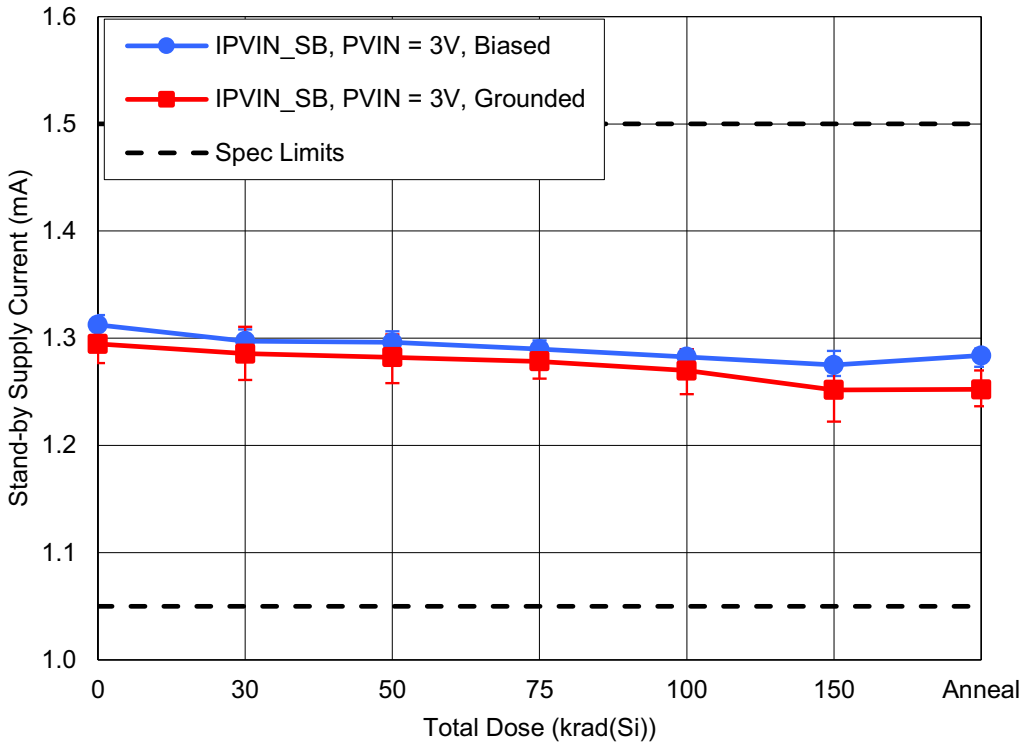

Figure 7. ISL73006SLH Stand-by Supply Current (I_{PVIN_SB}) with PVIN = 3V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.05mA and a maximum of 1.5mA.

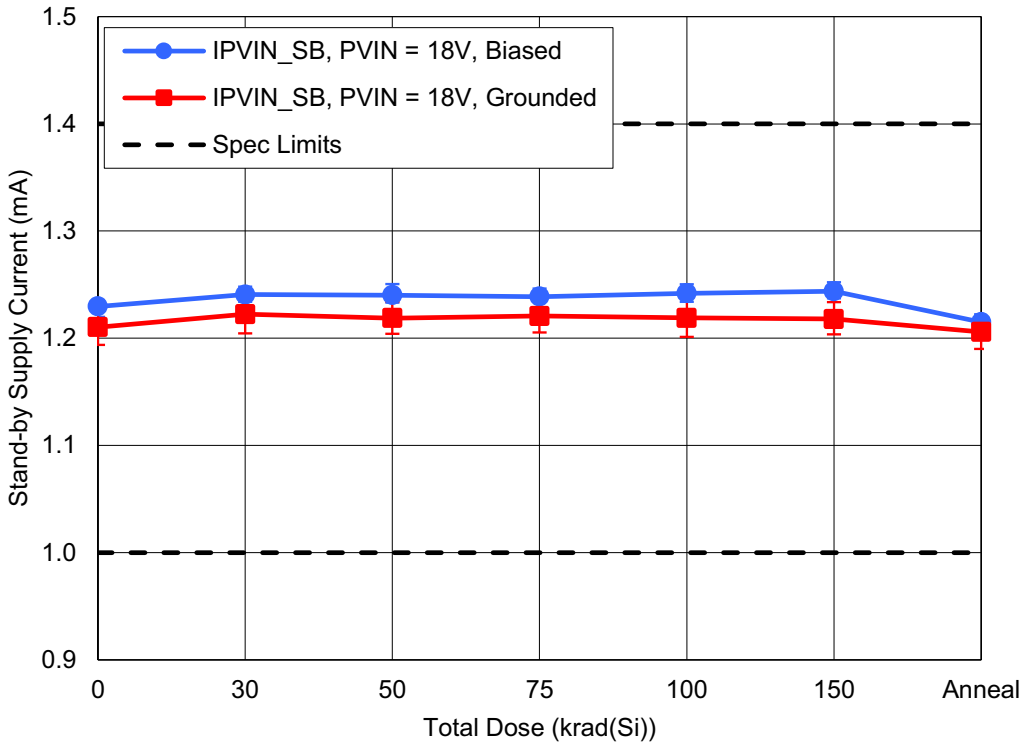

Figure 8. ISL73006SLH Stand-by Supply Current (I_{PVIN_SB}) with PVIN = 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1mA and a maximum of 1.4mA.

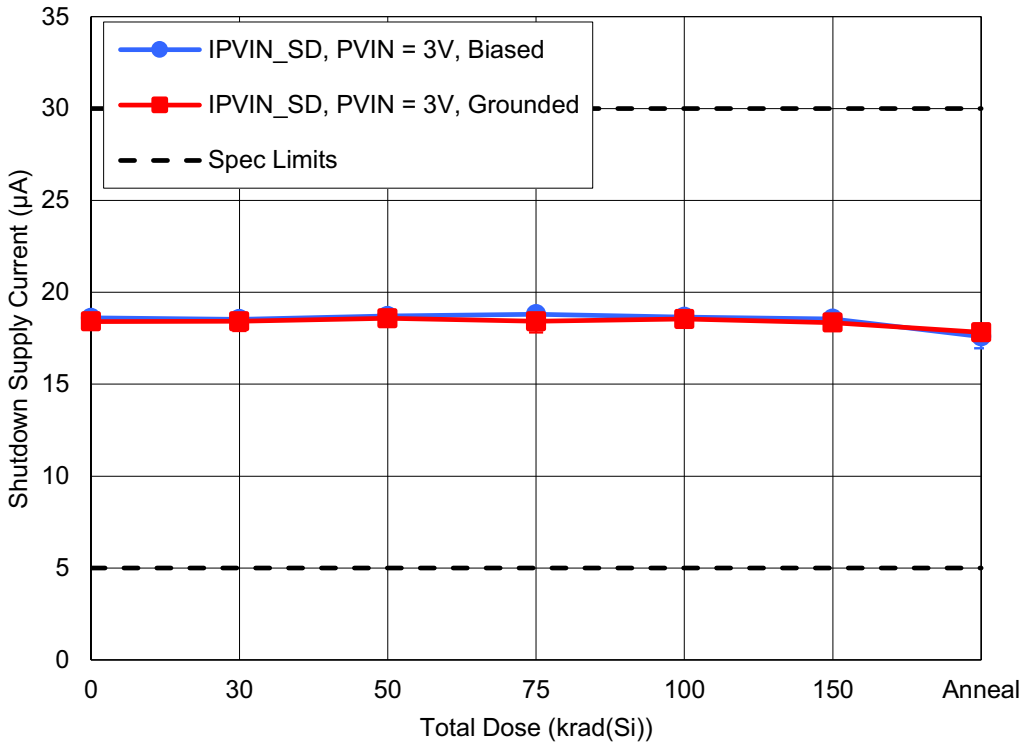

Figure 9. ISL73006SLH Shutdown Supply Current (I_{PVIN_SD}) with PVIN = 3V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 5µA and a maximum of 30µA.

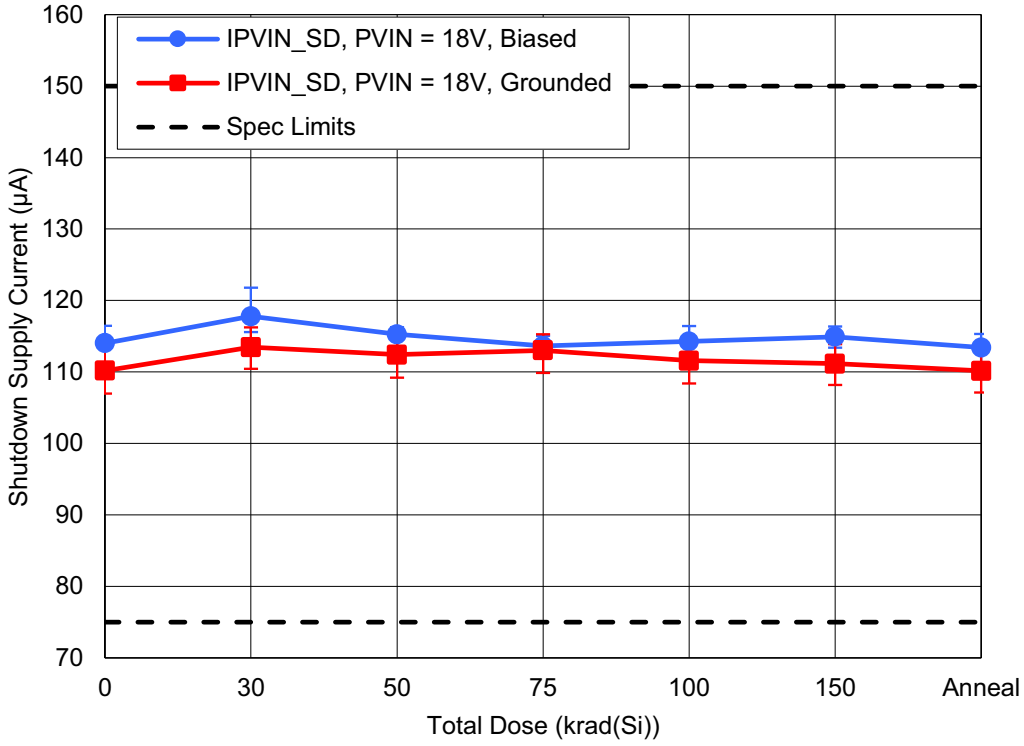

Figure 10. ISL73006SLH Shutdown Supply Current (I_{PVIN_SD}) with PVIN = 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 75µA and a maximum of 150µA.

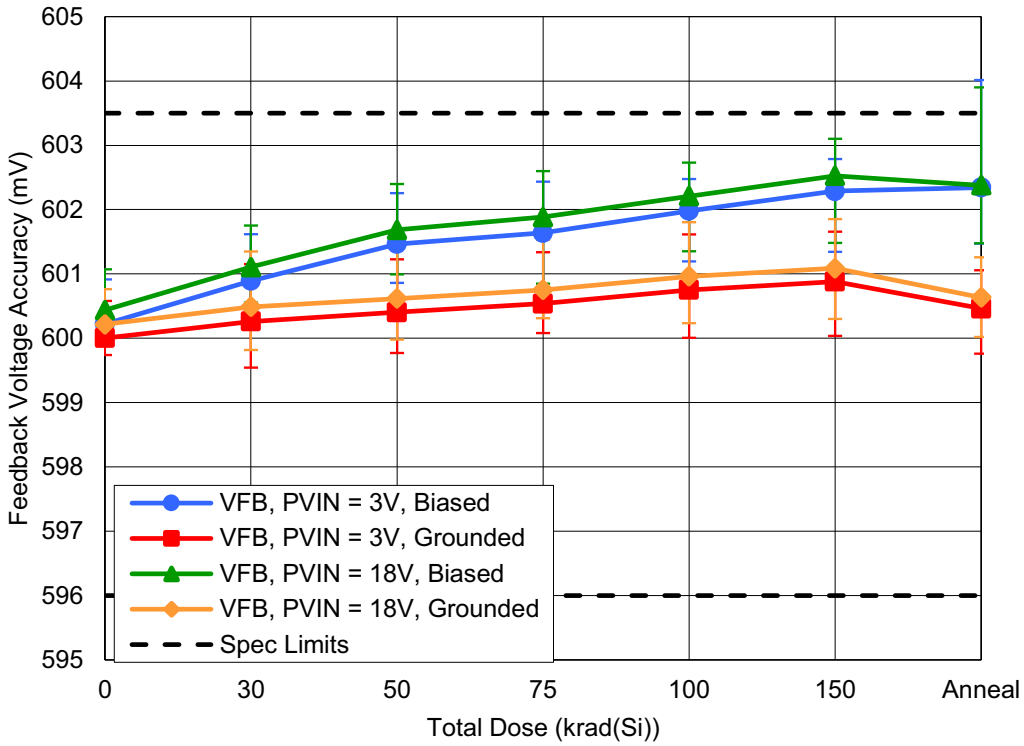

Figure 11. ISL73006SLH Feedback Voltage Accuracy (V_{FB}) with PVIN = 3V or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 596mV and a maximum of 603.5mV. One device experienced a slight parametric failure during the anneal for both PVIN = 3V and 18V.

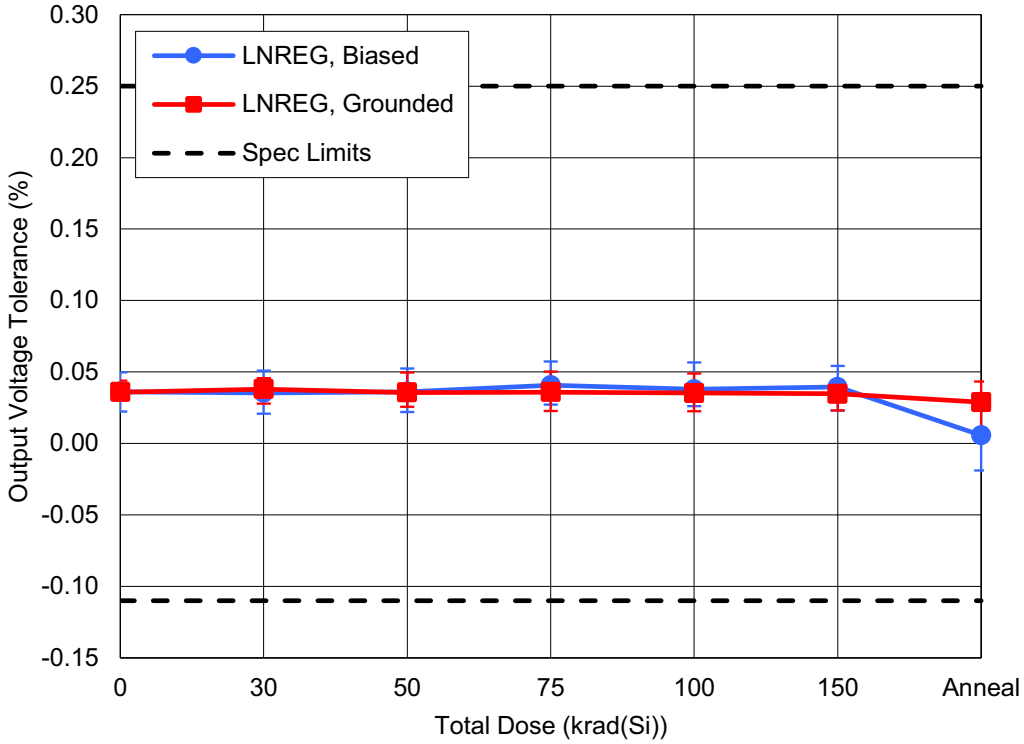

Figure 12. ISL73006SLH Output Voltage Tolerance Over Input Voltage Range (LNREG) as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -0.11% and a maximum of 0.25%.

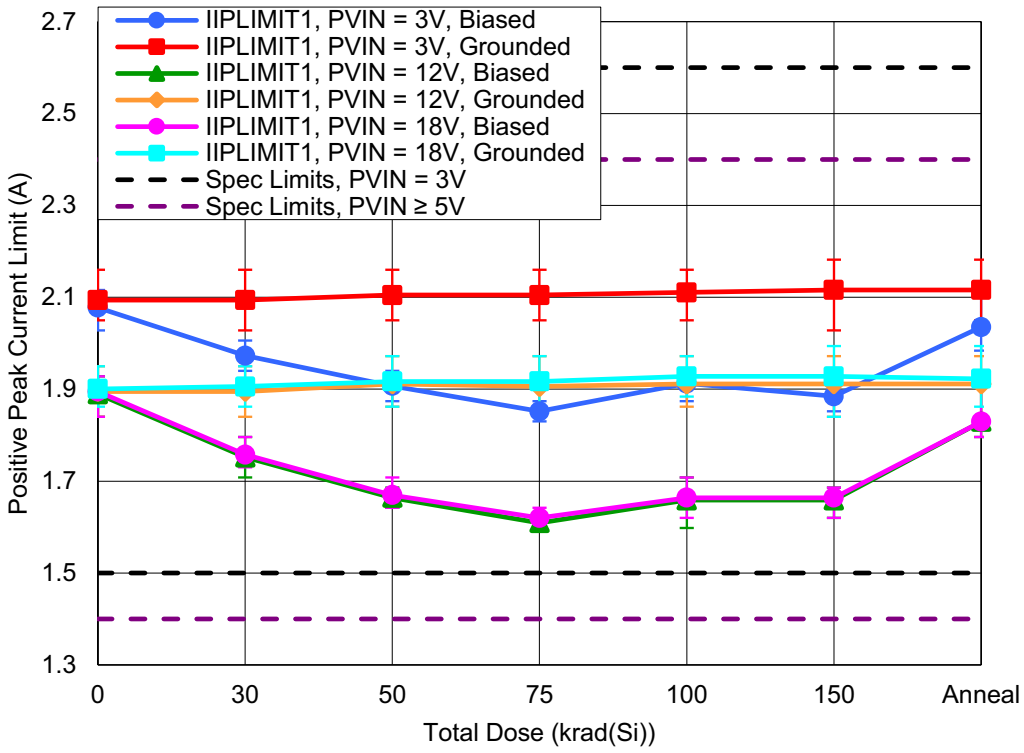

Figure 13. ISL73006SLH Positive Peak Current Limit ($I_{IPLIMIT1}$) with PVIN = 3V, 12V, or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.5A and a maximum of 2.6A when PVIN = 3V or a minimum of 1.4A and a maximum of 2.4A when PVIN ≥ 5V.

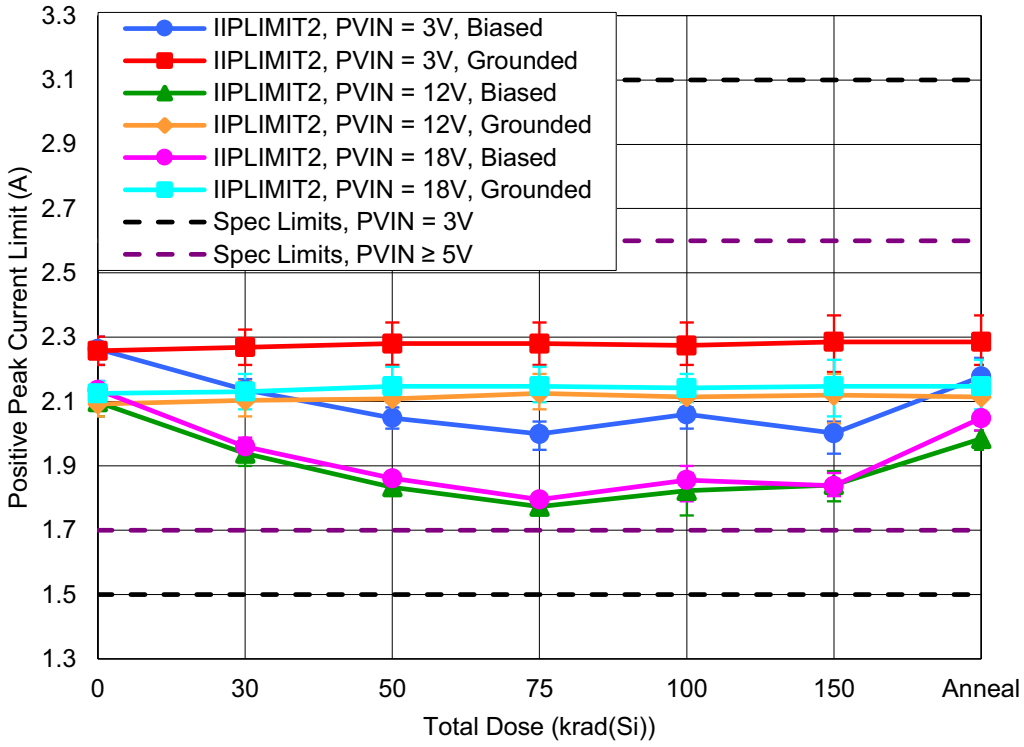

Figure 14. ISL73006SLH Positive Peak Current Limit ($I_{IPLIMIT2}$) with PVIN = 3V, 12V, or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.5A and a maximum of 3.1A when PVIN = 3V or a minimum of 1.7A and a maximum of 2.6A when PVIN ≥ 5V.

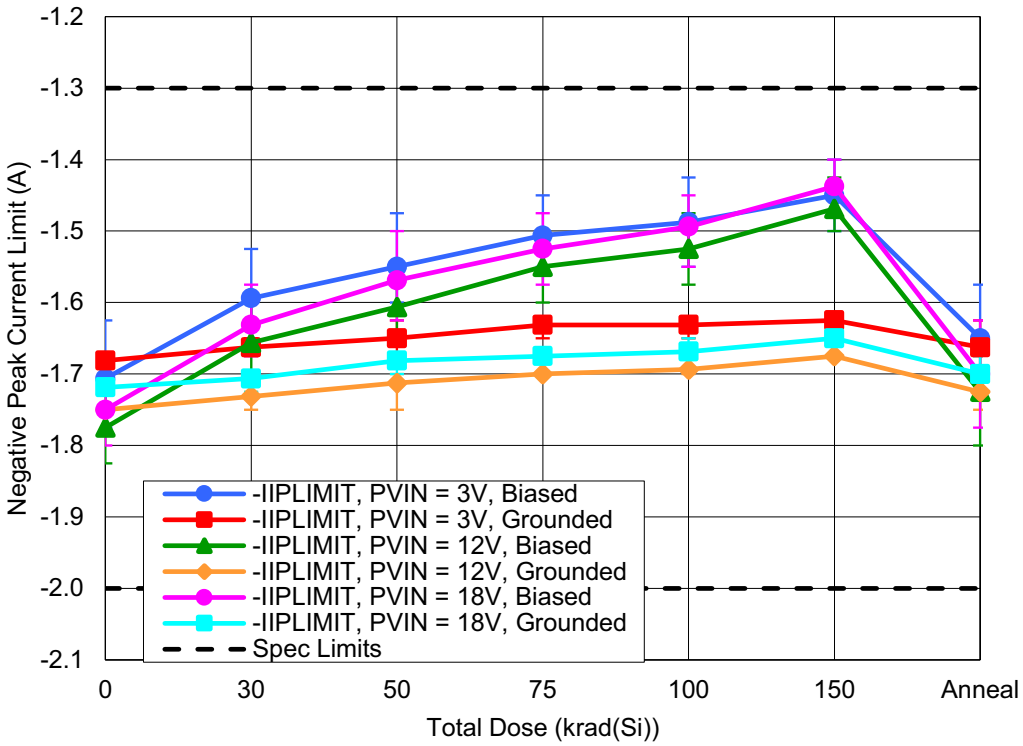

Figure 15. ISL73006SLH Negative Peak Current Limit ($-I_{IPLIMIT}$) with PVIN = 3V, 12V, or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -2A and a maximum of -1.3A.

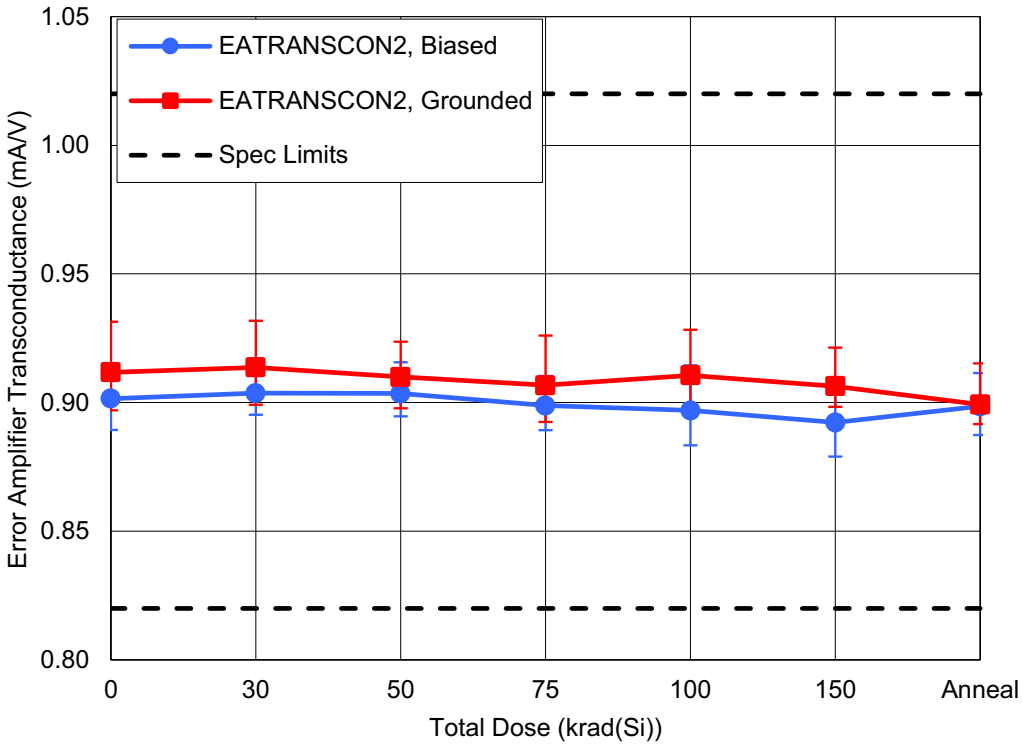

Figure 16. ISL73006SLH External Error Amplifier Transconductance ($EA_{transcon2}$) as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.82mA/V and a maximum of 1.02mA/V.

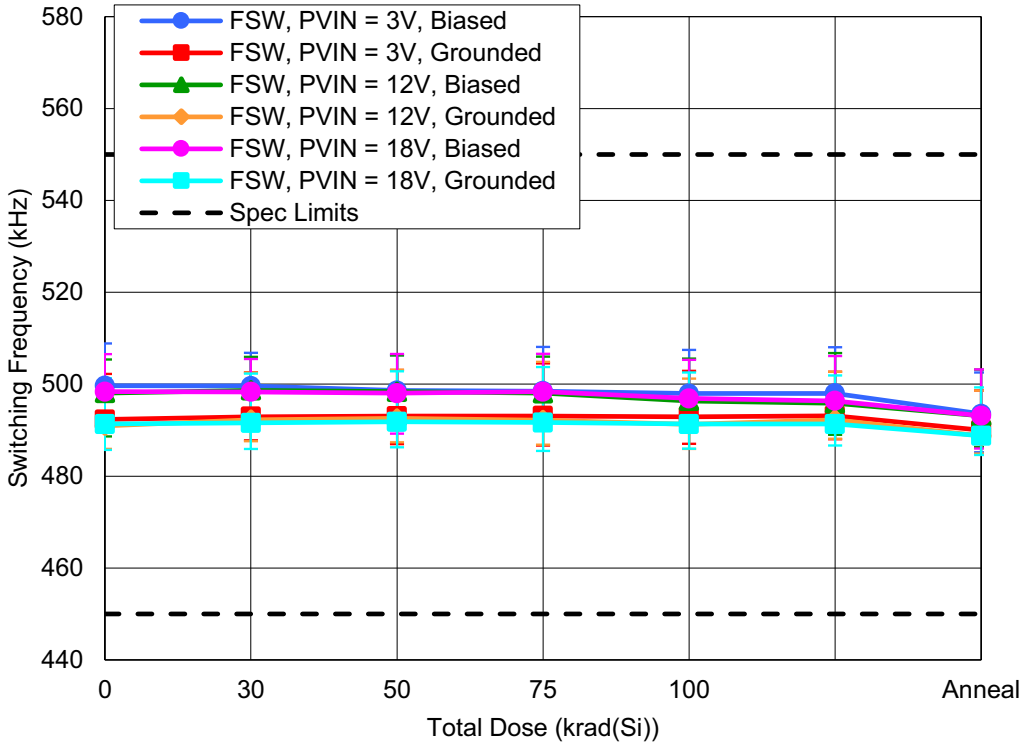

Figure 17. ISL73006SLH Switching Frequency (f_{SW}) with PVIN = 3V, 12V, or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 450kHz and a maximum of 550kHz.

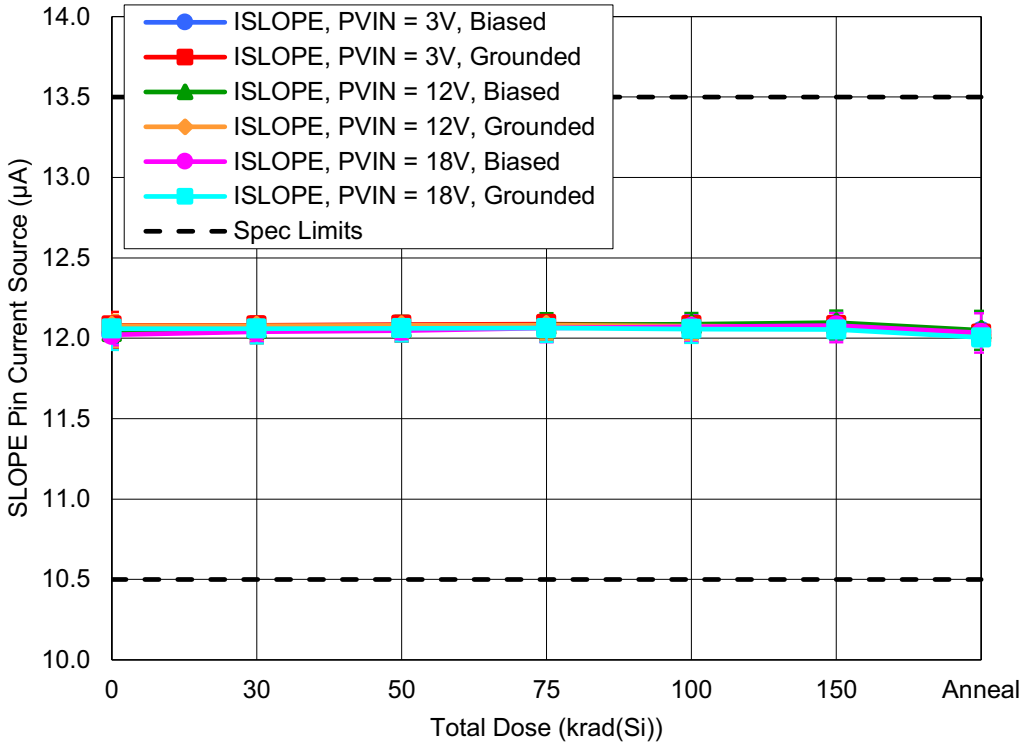

Figure 18. ISL73006SLH SLOPE Pin Current Source (I_{SLOPE}) with PVIN = 3V, 12V, or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 10.5µA and a maximum of 13.5µA.

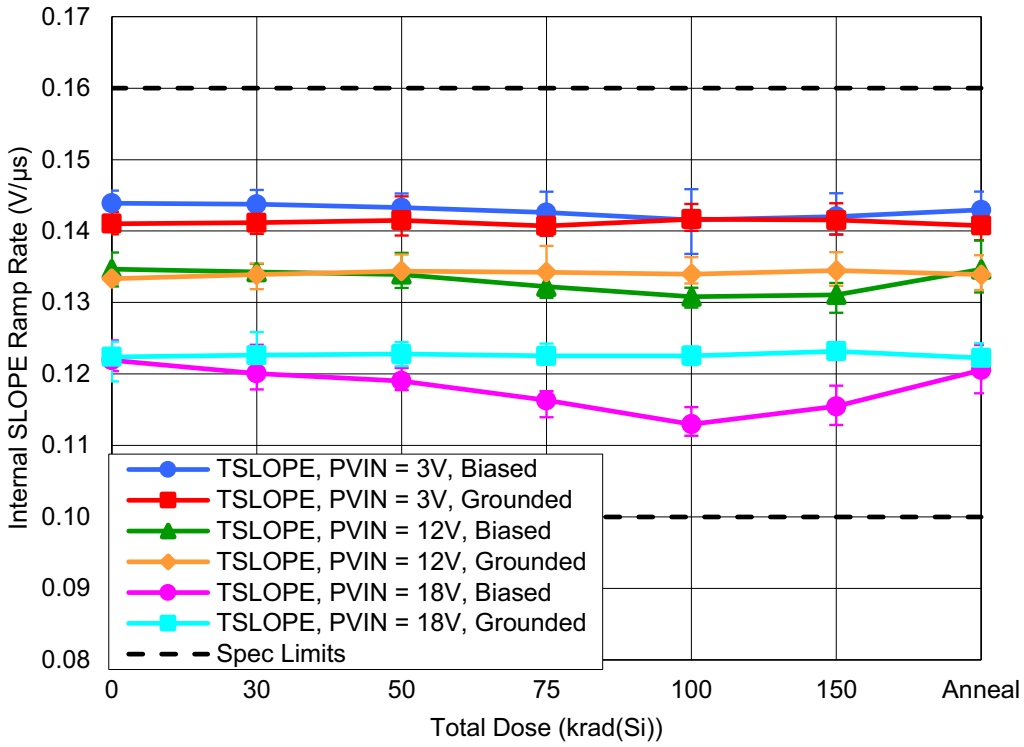

Figure 19. ISL73006SLH Internal SLOPE Ramp Rate (t_{SLOPE}) with PVIN = 3V, 12V, or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.1V/µs and a maximum of 0.16V/µs.

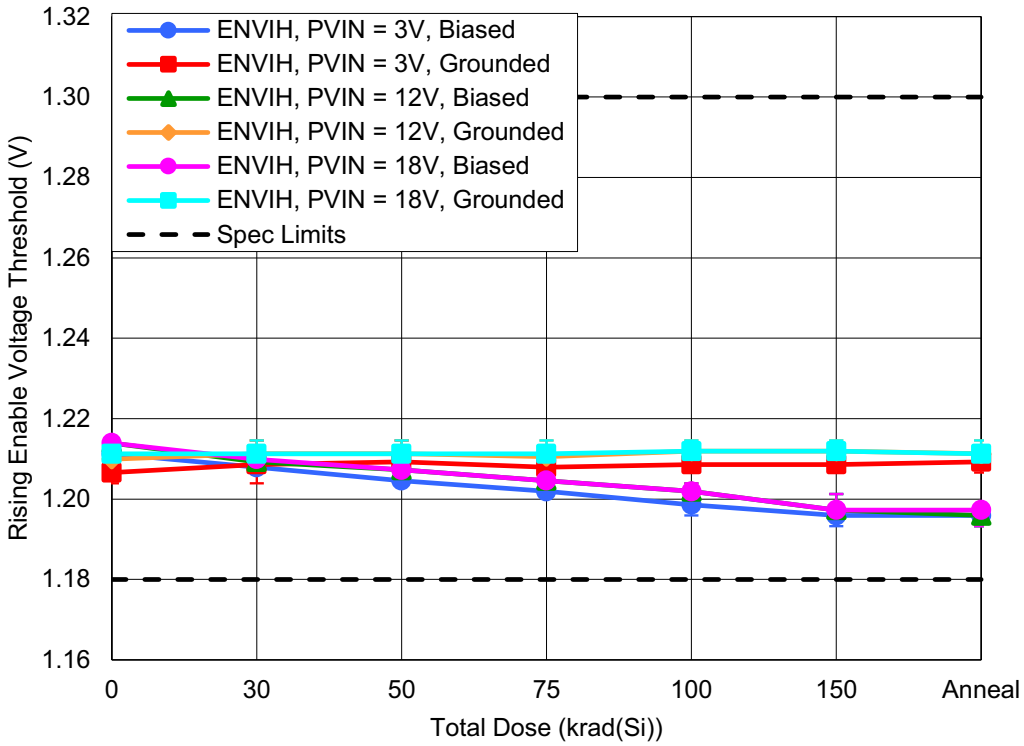

Figure 20. ISL73006SLH Rising Enable Voltage Threshold (EN_{VIH}) with PVIN = 3V, 12V, or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.18V and a maximum of 1.3V.

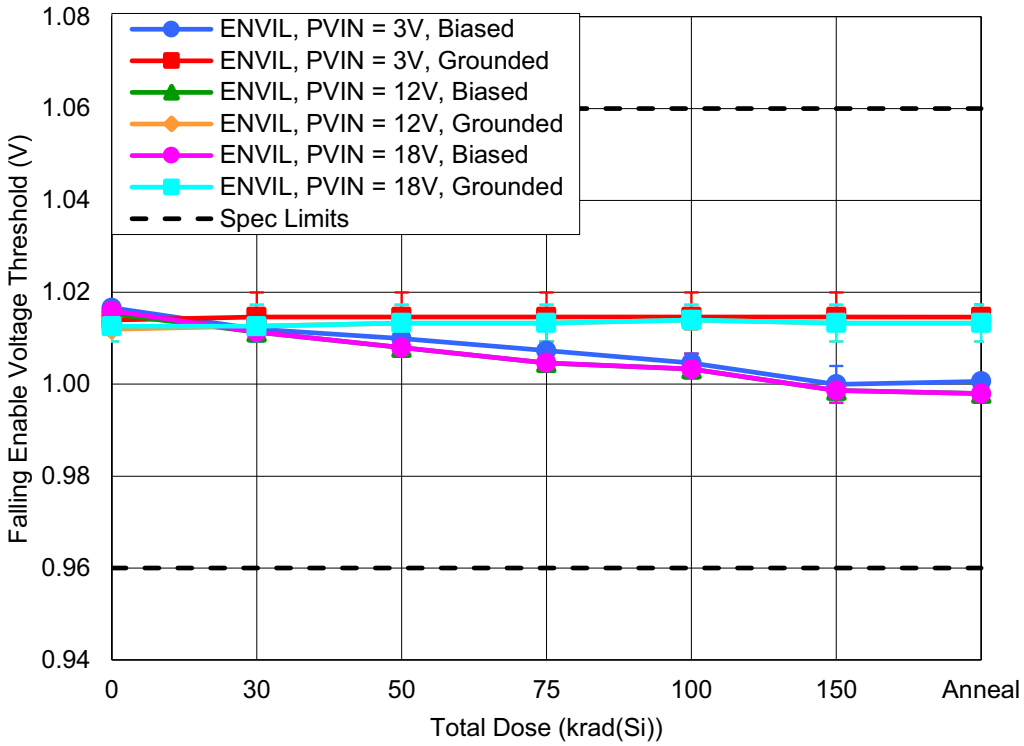

Figure 21. ISL73006SLH Falling Enable Voltage Threshold (EN_{VIL}) with PVIN = 3V, 12V, or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.96V and a maximum of 1.06V.

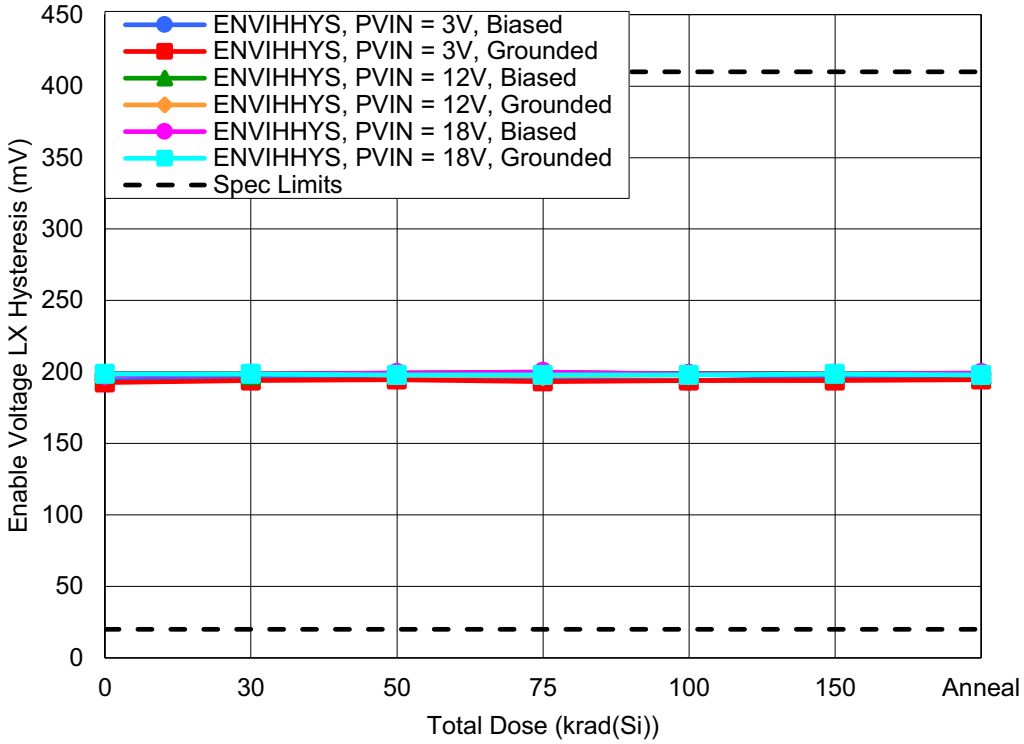

Figure 22. ISL73006SLH Enable Voltage LX Hysteresis (EN_{VIHhys}) with PVIN = 3V, 12V, or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 20mV and a maximum of 410mV.

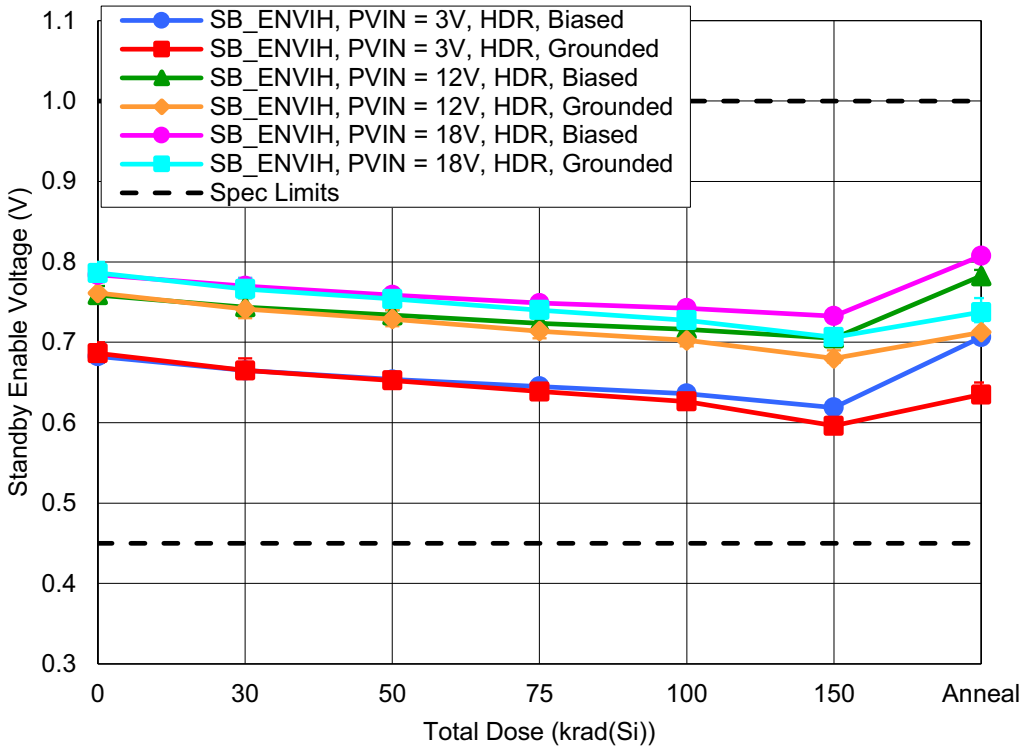

Figure 23. ISL73006SLH Standby Enable Voltage (SB_EN_{VIH}) with PVIN = 3V, 12V, or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.45V and a maximum of 1V.

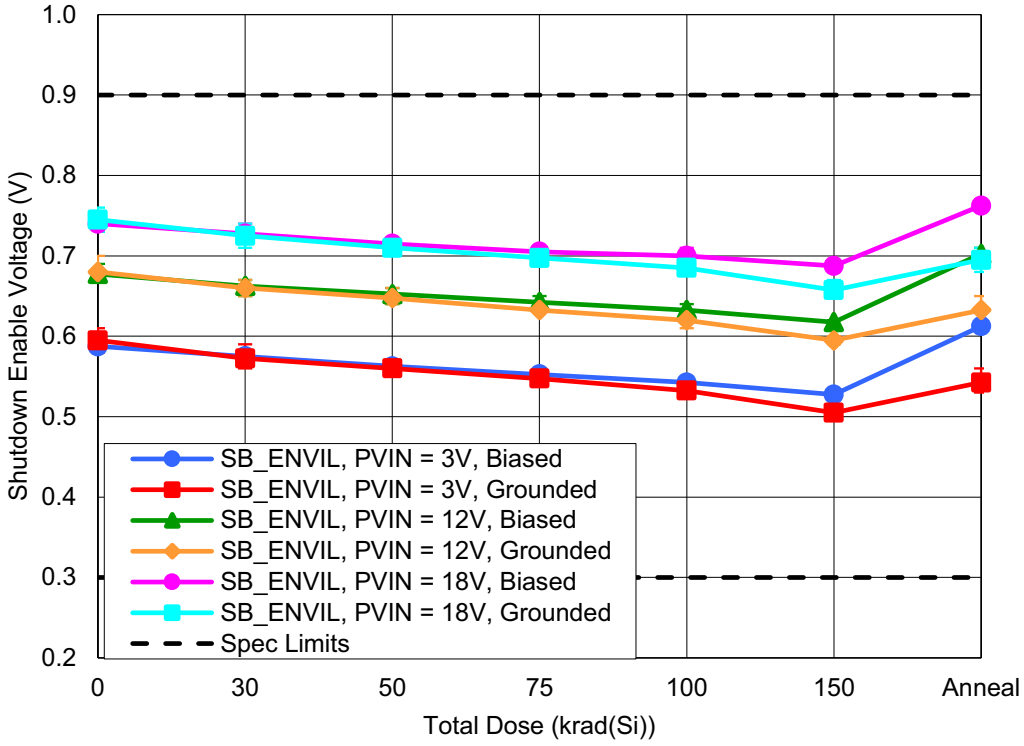

Figure 24. ISL73006SLH Shutdown Enable Voltage (SB_EN_{VIL}) with PVIN = 3V, 12V, or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 0.3V and a maximum of 0.9V.

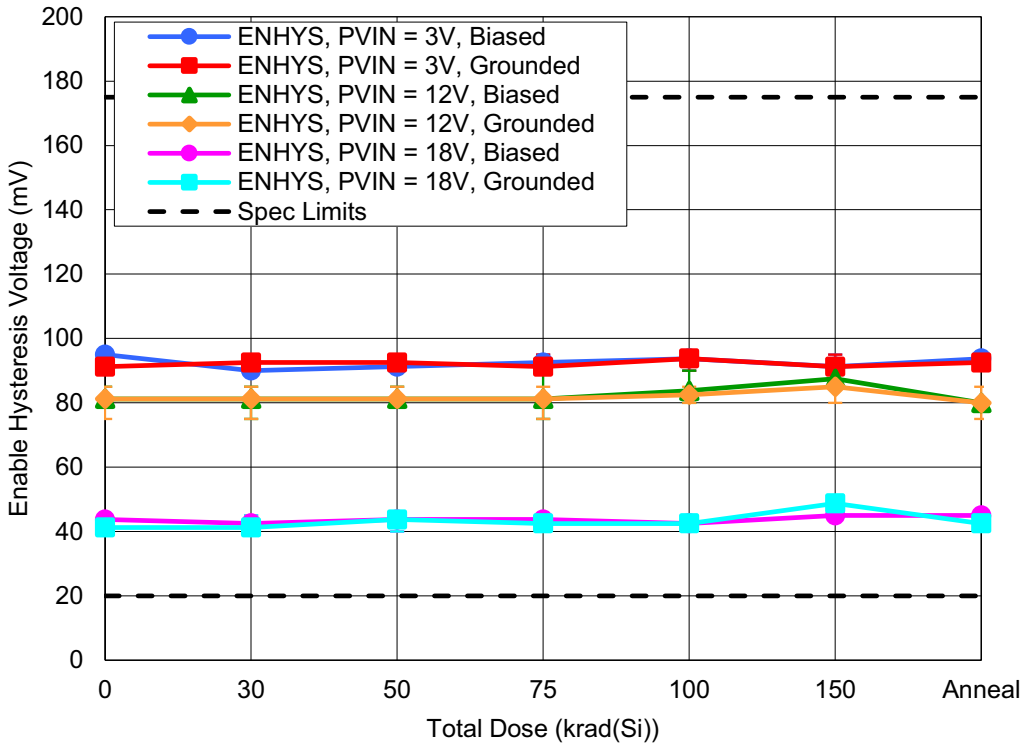

Figure 25. ISL73006SLH Enable Hysteresis Voltage (EN_{HYS}) with PVIN = 3V, 12V, or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 20mV and a maximum of 175mV.

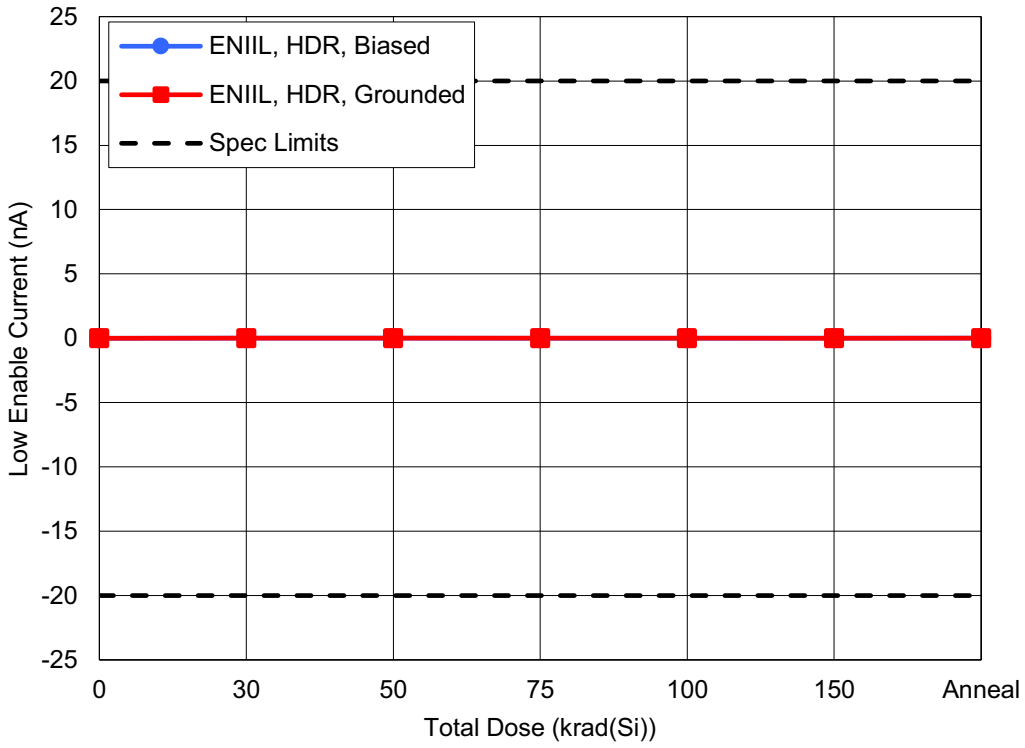

Figure 26. ISL73006SLH Low Enable Current (EN_{IIL}) as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of -20nA and a maximum of 20nA.

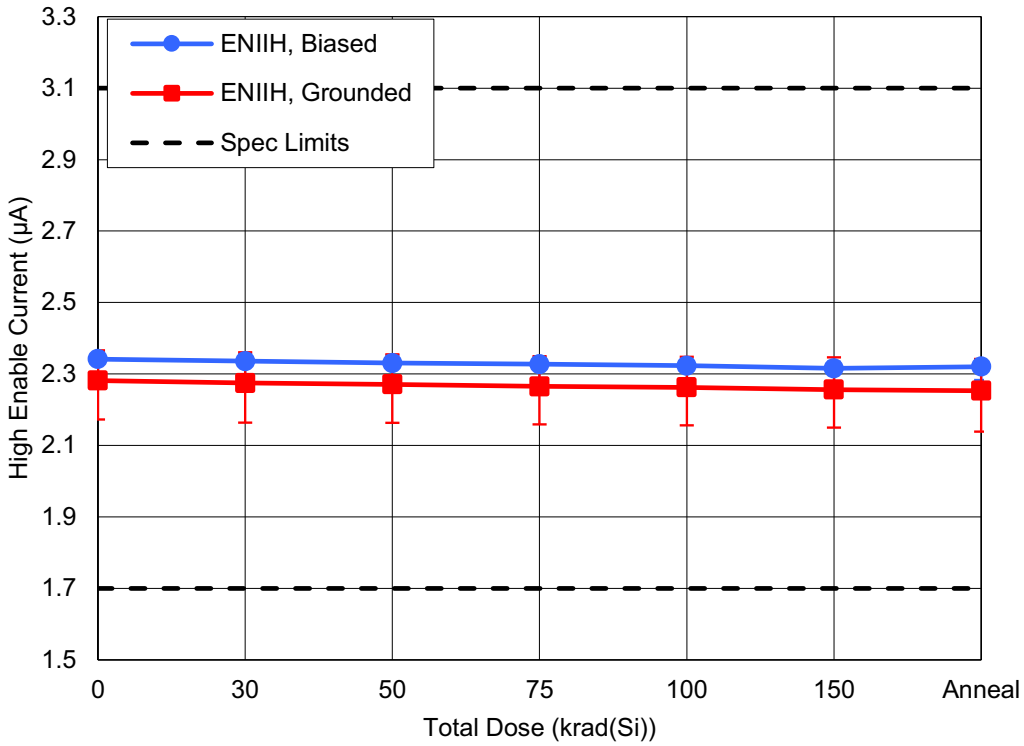

Figure 27. ISL73006SLH High Enable Current (EN_{IIH}) as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.7µA and a maximum of 3.1µA.

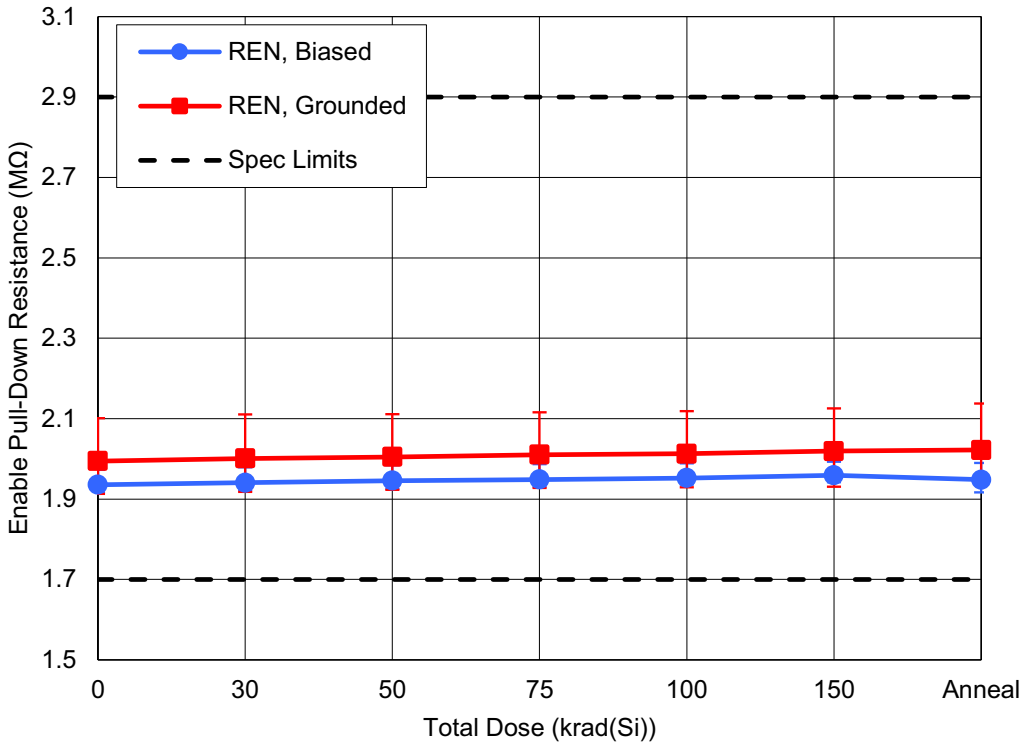

Figure 28. ISL73006SLH Enable Pull-Down Resistance (R_{EN}) with PVIN = 12V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.7MΩ and a maximum of 2.9MΩ.

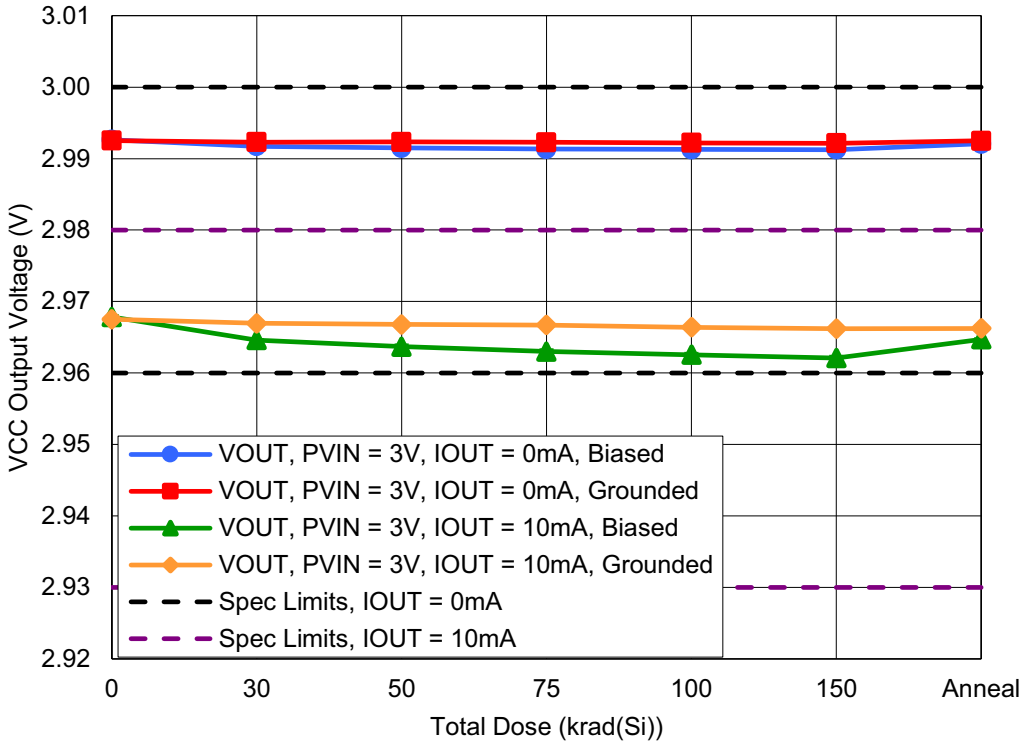

Figure 29. ISL73006SLH VCC Output Voltage ($VOUT_{3V,0mA}$,$VOUT_{3V,10mA}$) with PVIN = 3V, and with I_{OUT} = 0mA or 10mA as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 2.96V and a maximum of 3V when I_{OUT} = 0mA or a minimum of 2.93V and a maximum of 2.98V when I_{OUT} = 10mA.

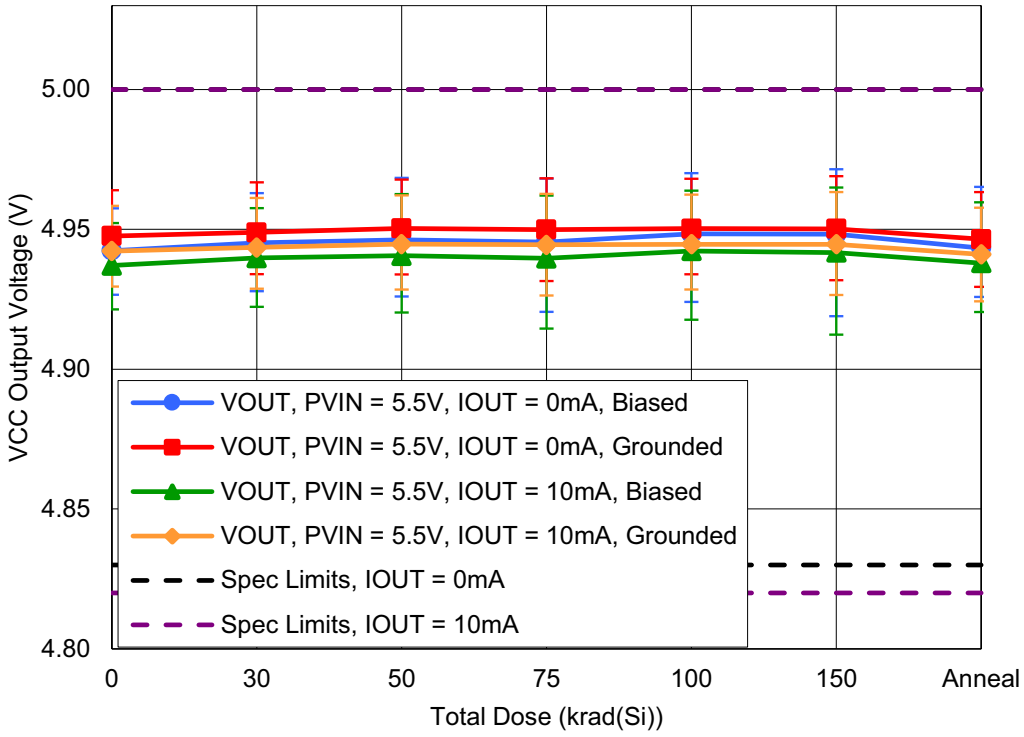

Figure 30. ISL73006SLH VCC Output Voltage ($VOUT_{5V,0mA}$,$VOUT_{5V,10mA}$) with PVIN = 5.5V, and with I_{OUT} = 0mA or 10mA as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 4.83V and a maximum of 5V when I_{OUT} = 0mA or a minimum of 4.82V and a maximum of 5V when I_{OUT} = 10mA.

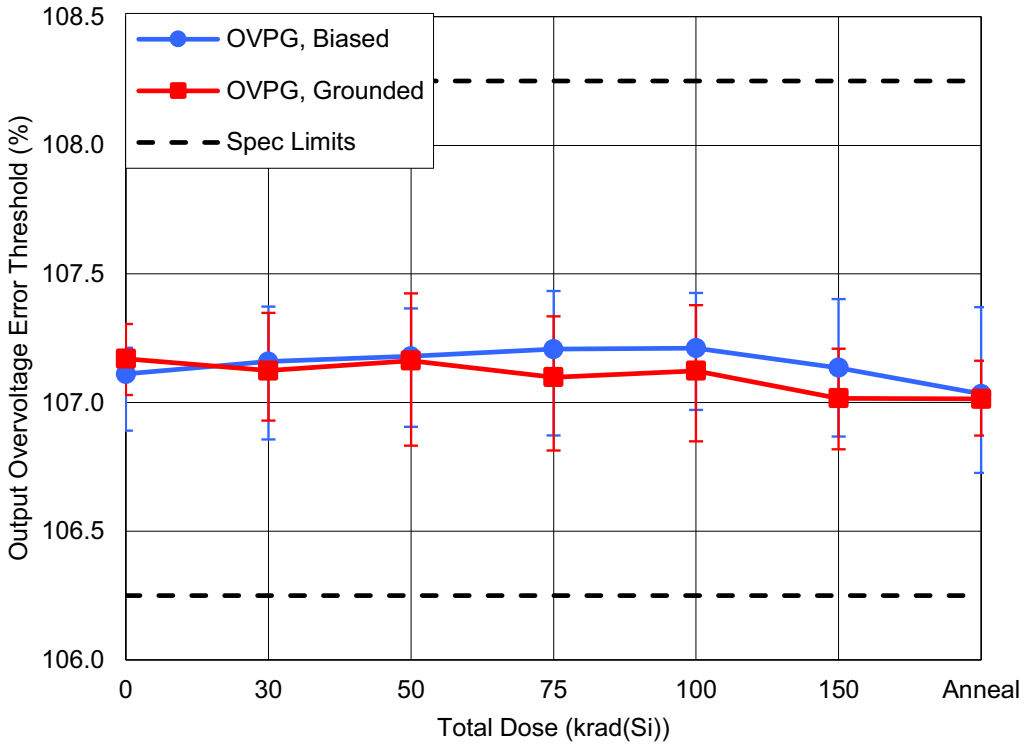

Figure 31. ISL73006SLH Output Overvoltage Error Threshold (OVPG) with PVIN = 5V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 106.25% and a maximum of 108.25%.

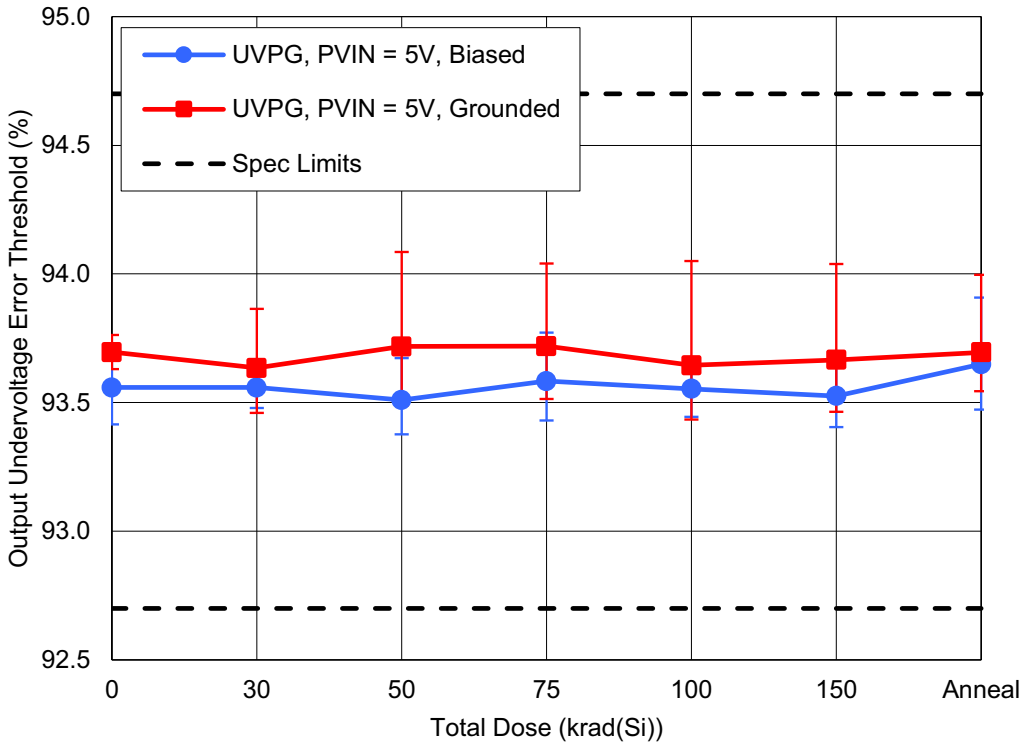

Figure 32. ISL73006SLH Output Undervoltage Error Threshold (UVPG) with PVIN = 5V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 92.7% and a maximum of 94.7%.

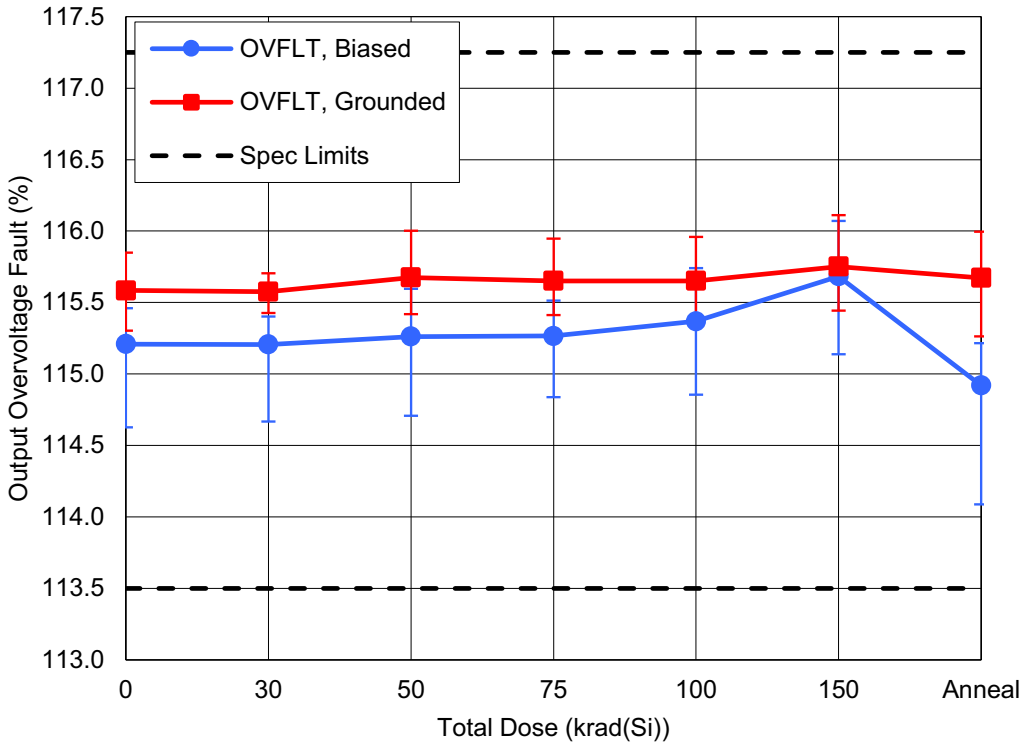

Figure 33. ISL73006SLH Output Overvoltage Fault (OV_{flt}) as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 113.5% and a maximum of 117.25%.

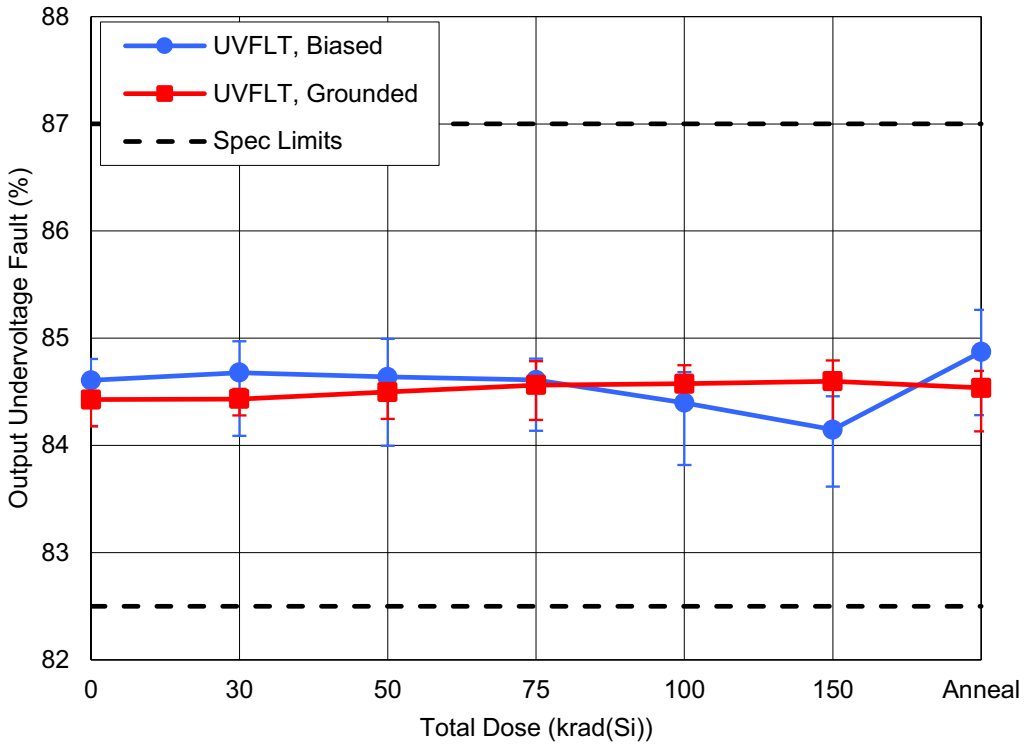

Figure 34. ISL73006SLH Output Undervoltage Fault (UV_{flt}) as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 82.5% and a maximum of 87%.

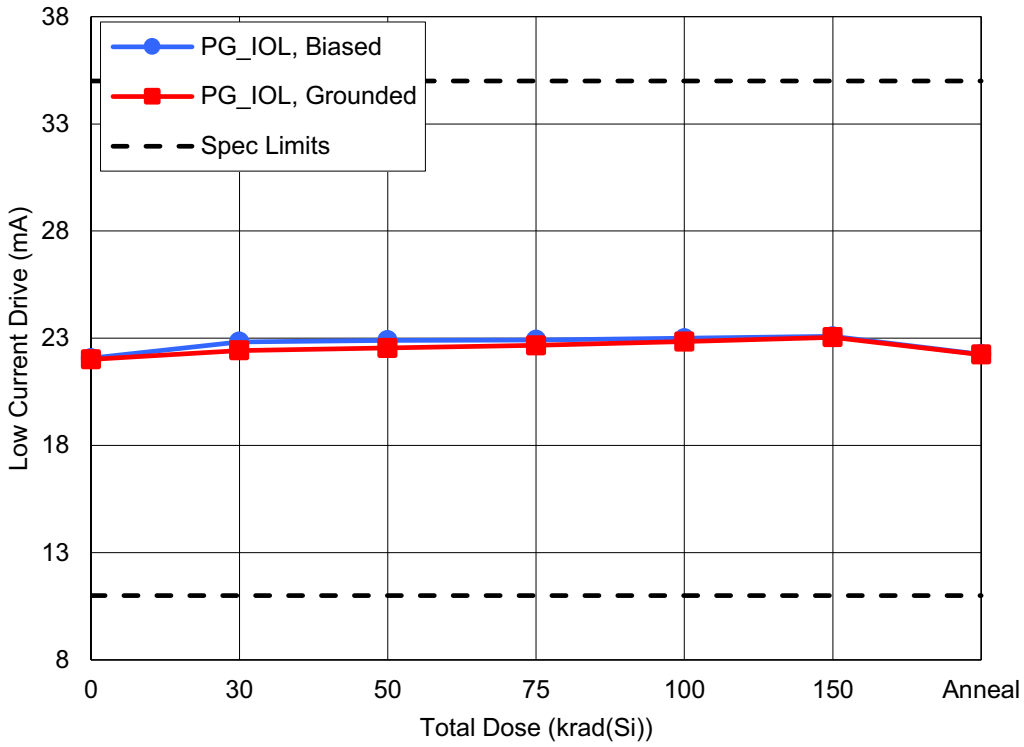

Figure 35. ISL73006SLH Low Current Drive (PG_I_{OL}) with PVIN = 3V, PG = 0.4V, and EN = 0V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 11mA and a maximum of 35mA.

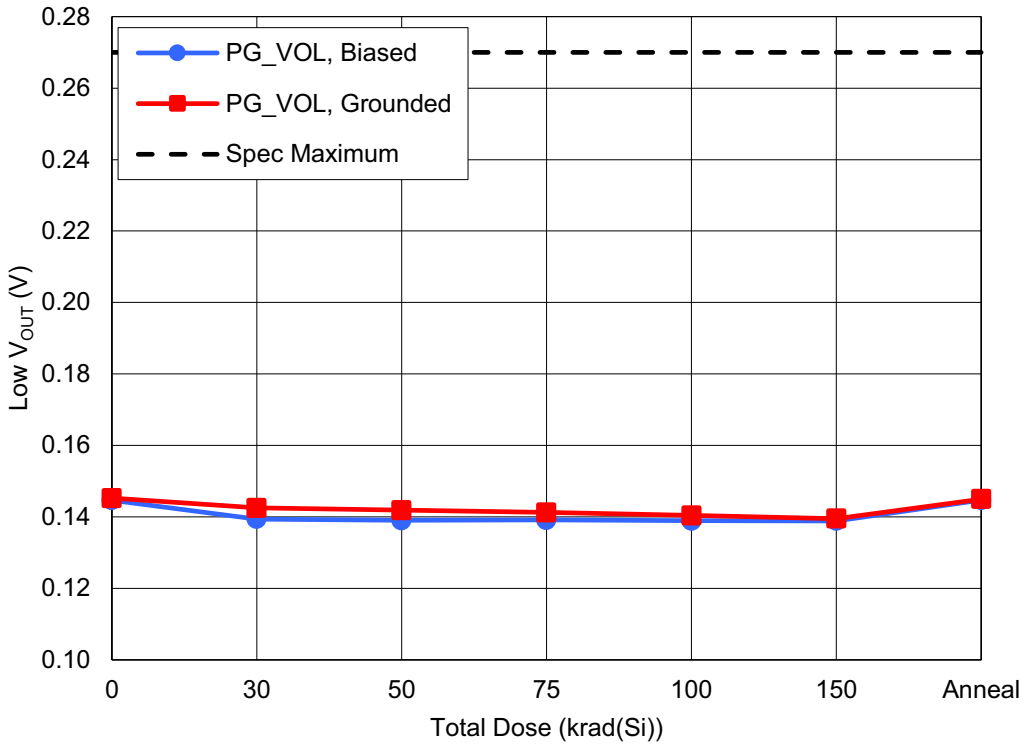

Figure 36. ISL73006SLH Low V_{OUT} (PG_V_{OL}) as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 0.27V.

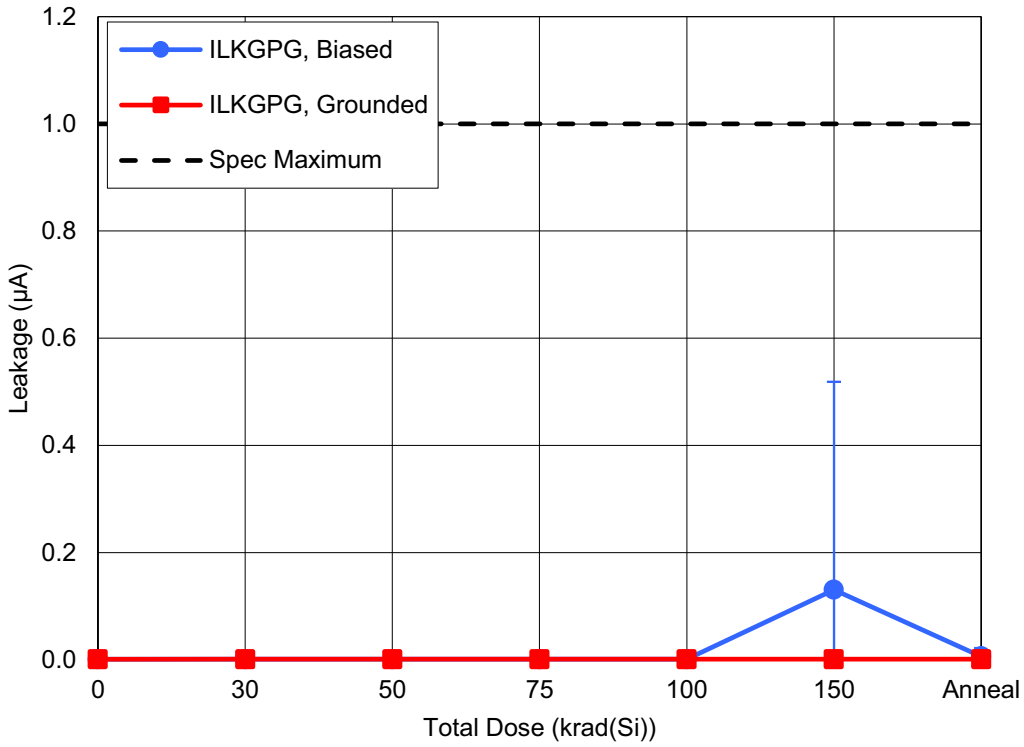

Figure 37. ISL73006SLH Leakage (I_{LKGPG}) with PVIN = PGOOD = 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 1µA.

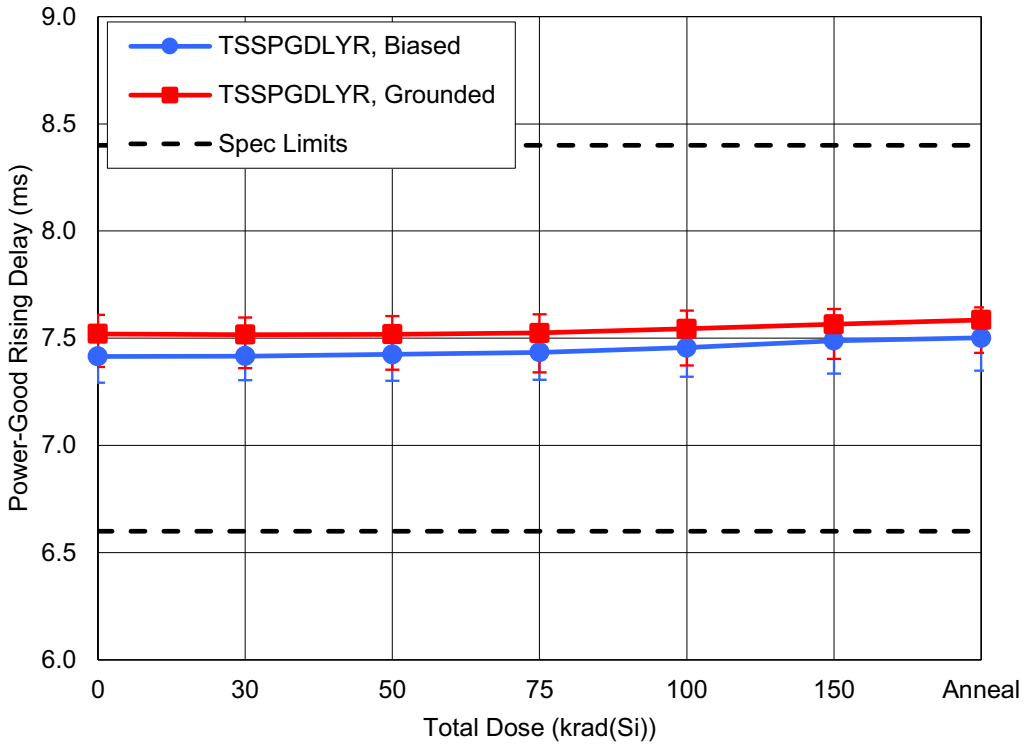

Figure 38. ISL73006SLH Power-Good Rising Delay ($t_{SSPGdlyr}$) with PVIN = 5.5V at 500kHz as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 6.6ms and a maximum of 8.4ms.

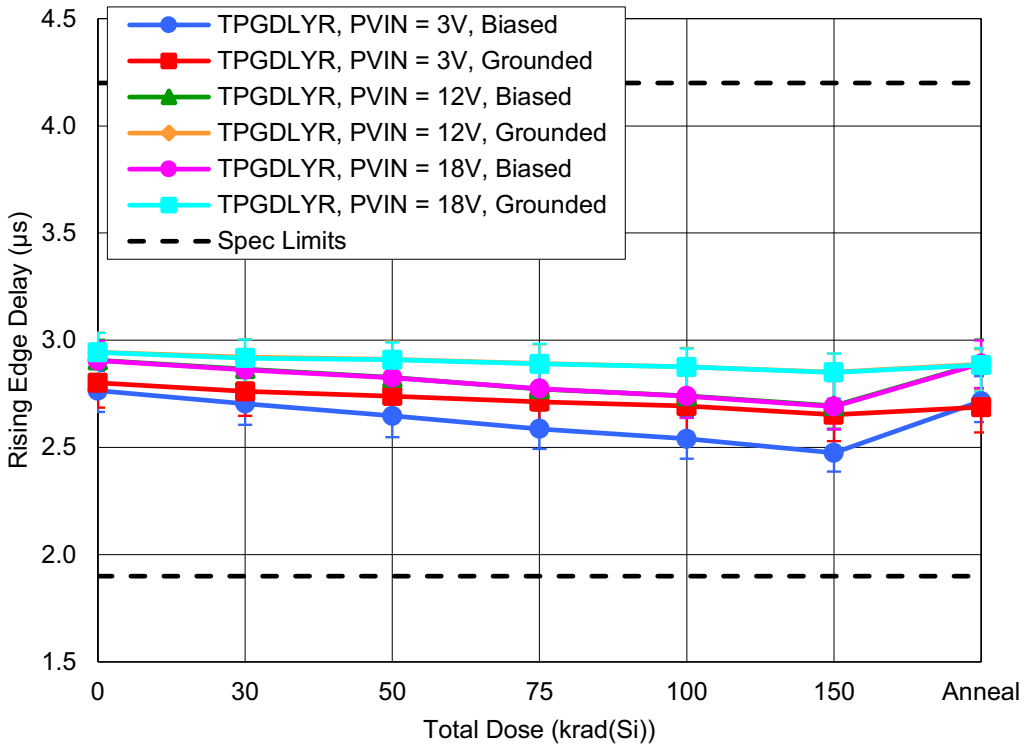

Figure 39. ISL73006SLH Rising Edge Delay (t_{PGdlyr}) with PVIN = 3V, 12V, or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 1.9µs and a maximum of 4.2µs.

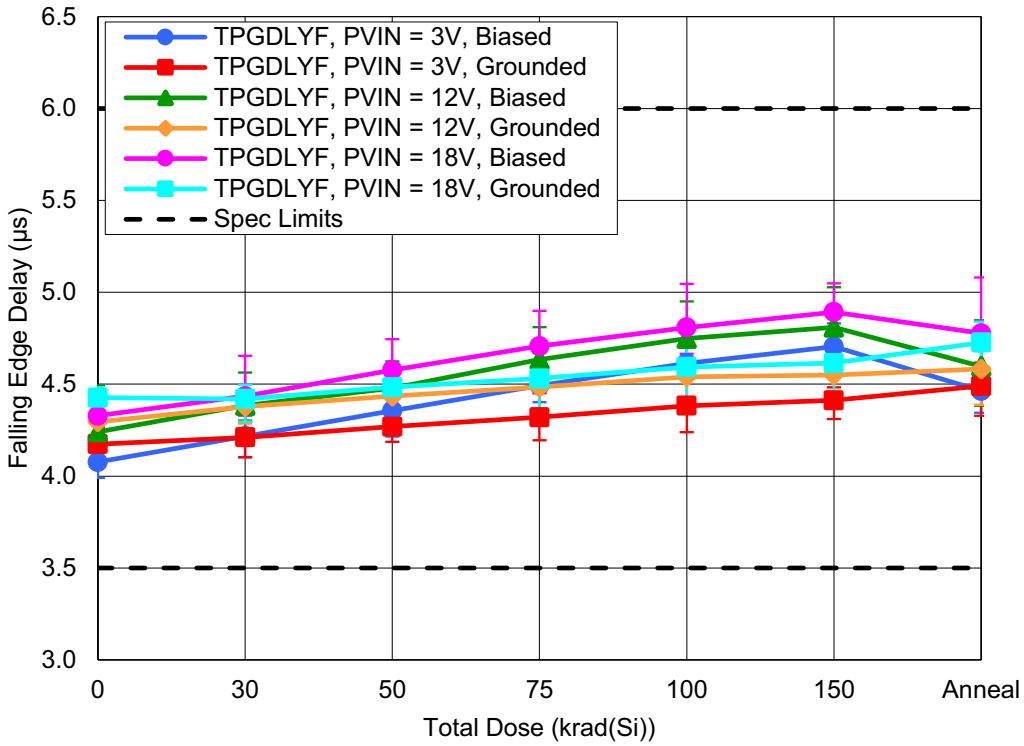

Figure 40. ISL73006SLH Falling Edge Delay (t_{PGdlyf}) with PVIN = 3V, 12V or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 3.5µs and a maximum 6µs.

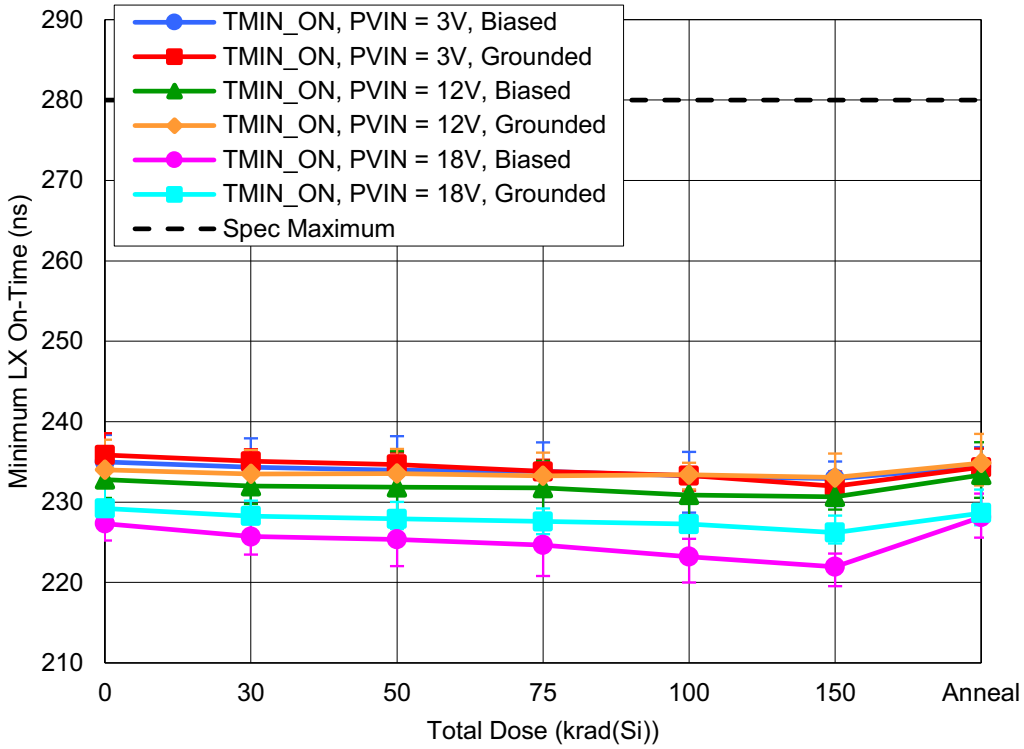

Figure 41. ISL73006SLH Minimum LX On-Time (t_{MIN_ON}) with PVIN = 3V, 12V or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 280ns.

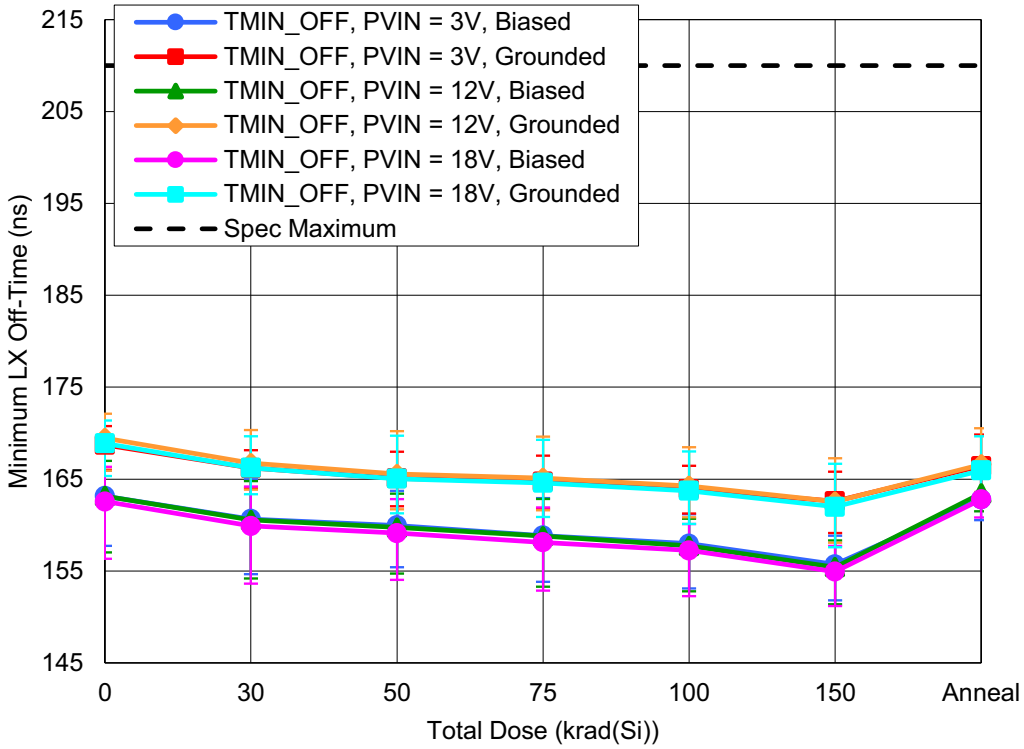

Figure 42. ISL73006SLH Minimum LX Off-Time (t_{MIN_OFF}) with PVIN = 3V, 12V or 18V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limit is a maximum of 210ns.

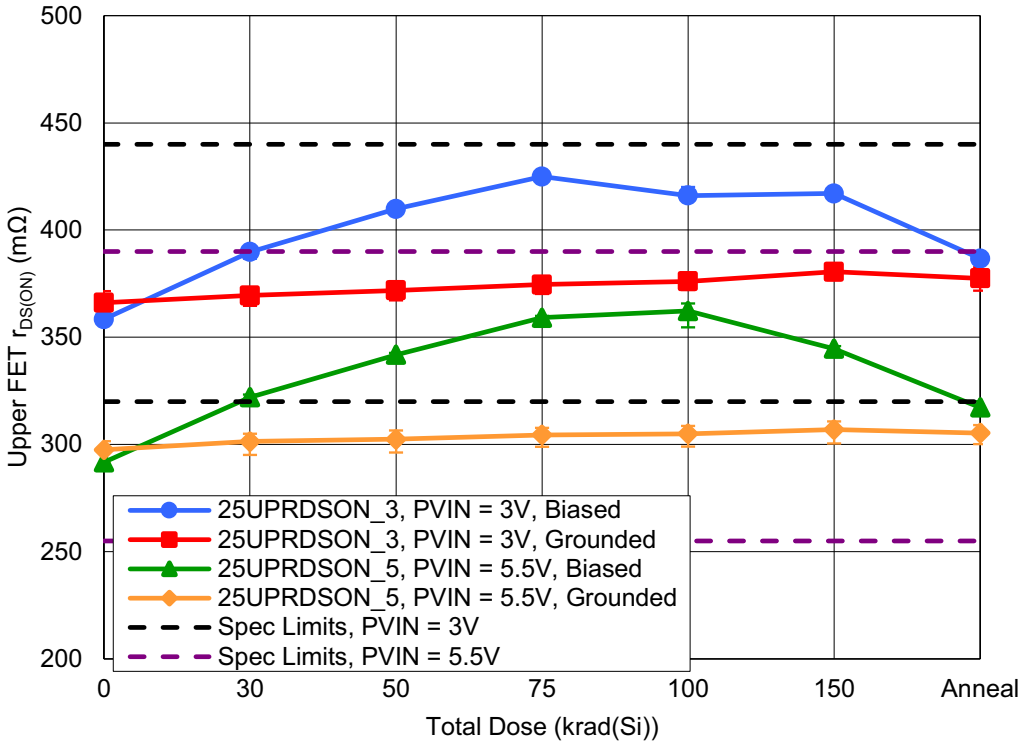

Figure 43. ISL73006SLH Post Rad CDFP Upper FET $r_{DS(ON)}$ ($25UPR_{DSON\_3}$, $25UPR_{DSON\_5}$) with PVIN = 3V or 5.5V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 320mΩ and a maximum of 440mΩ when PVIN = 3V or a minimum of 255mΩ and a maximum of 390mΩ when PVIN = 5.5V.

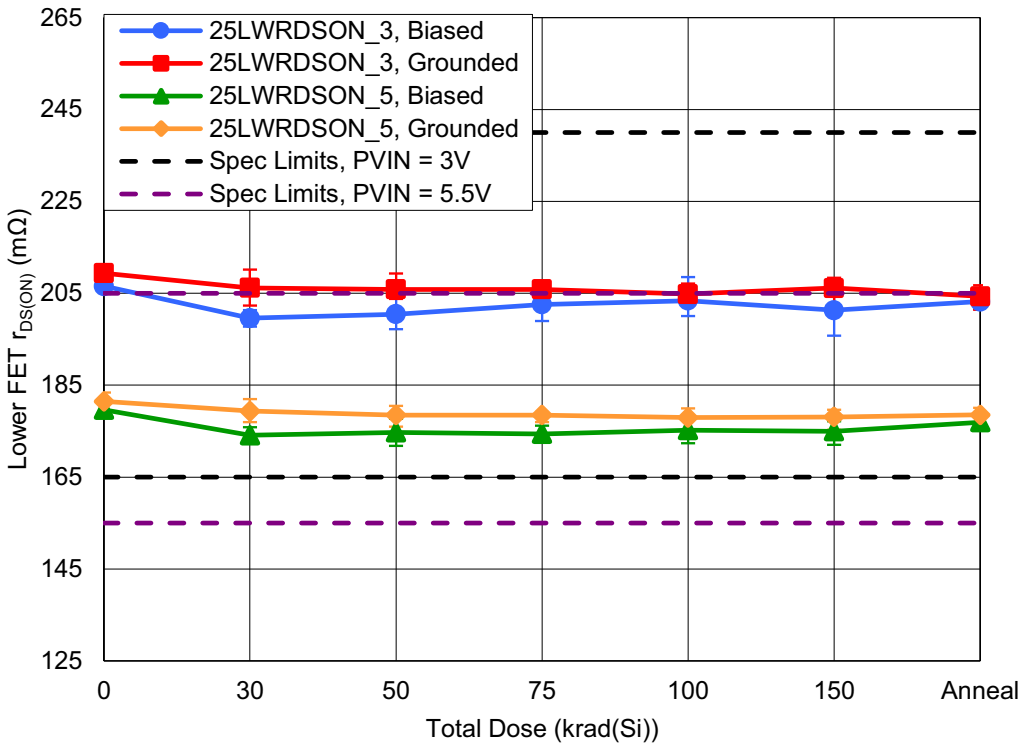

Figure 44. ISL73006SLH Post Rad CDFP Lower FET $r_{DS(ON)}$ ($25LWR_{DSON\_3}$, $25LWR_{DSON\_5}$) with PVIN = 3V or 5.5V as a function of HDR irradiation and anneal for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The datasheet limits are a minimum of 165mΩ and a maximum of 240mΩ when PVIN = 3V or a minimum of 155mΩ and a maximum of 205mΩ when PVIN = 5.5V.

3. Discussion and Conclusion

This document reports the results of the TID test of the ISL73006SLH radiation hardened 18V, 1A point of load regulator. The irradiation of biased and grounded samples to 150krad(Si) at HDR of 68rad(Si)/s was followed by a 168-hour anneal at 100ºC under bias. The data for samples irradiated at HDR are provided for guidance only as the ISL73006SLH is only acceptance tested to 75krad(Si) at LDR. All datasheet parameters passed at all downpoints except for one device which had a slight parametric failure on Feedback Voltage Accuracy (VFB) during the anneal following HDR irradiation. No evidence of bias dependence was observed. The ISL73006SLH is rated to 75krad(Si) at LDR and is acceptance tested on a wafer-by-wafer basis to the datasheet limits. The ISL73006SLH is not rated for HDR.

4. Revision History

Revision	Date	Description
1.00	Dec 13, 2023	Initial release.

Appendix

Table 3 lists the datasheet parameters that are considered indicative of part performance. These parameters are plotted in Figure 3 through Figure 44. All limits are taken from the ISL73006SLH datasheet, which may also have more details on test conditions.

Table 3. ISL73006SLH Datasheet Total Dose Parameters (TA = 25ºC)

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
3	Rising Undervoltage Lockout	V_{PVIN_UVLO}	EN = 2.25V	-	2.95	V
	Falling Undervoltage Lockout		EN = 2.25V	2.7	-	V
4	Operating Supply Current	I_{PVIN_OPER}	PVIN = 3V, EN = 2.25V, no load	2	6	mA
5			PVIN = 12V, EN = 2.25V, no load	5	12	
6			PVIN = 18V, EN = 2.25V, no load	6.5	12.5	
7	Stand-by Supply Current	I_{PVIN_SB}	PVIN = 3V, EN = 1V	1.05	1.5	mA
8			PVIN = 18V, EN = 1V	1	1.4	
9	Shutdown Supply Current	I_{PVIN_SD}	PVIN = 3V, EN = 0V	5	30	µA
10			PVIN = 18V, EN = 0V	75	150	
11	Feedback Voltage Accuracy	V_{FB}	PVIN = 3V or 18V	596	603.5	mV
12	Output Voltage Tolerance Over Input Voltage Range	LNREG	PVIN = 3V, 18V using servo loop	-0.11	0.25	%
13	Positive Peak Current Limit	$I_{IPLIMIT1}$	PVIN = 3V	1.5	2.6	A
			PVIN ≥ 5V	1.4	2.4	
14		$I_{IPLIMIT2}$	PVIN = 3V	1.5	3.1	
			PVIN ≥ 5V	1.7	2.6	
15	Negative Peak Current Limit	$-I_{IPLIMIT}$	PVIN = 3V, 12V, or 18V	-2	-1.3	A
16	External Error Amplifier Transconductance	$EA_{transcon2}$	PVIN = 5V, delta COMP current/delta FB Voltage (10mV)	0.82	1.02	mA/V
17	Switching Frequency	f_{SW}	PVIN = 3V, 12V, or 18V VSLOPE = 1.2V	450	550	kHz
18	SLOPE Pin Current Source	I_{SLOPE}	PVIN = 3V, 12V, or 18V	10.5	13.5	µA
19	Internal SLOPE Ramp Rate	t_{SLOPE}	PVIN = 3V, 12V, or 18V (V_{COMP} at 80%DC - V_{COMP} at 20%DC)/(t_{MIN_ON} at 80%DC - t_{MIN_ON} at 20%DC)	0.1	0.16	V/µs
20	Rising Enable Voltage Threshold	EN_{VIH}	PVIN = 3V, 12V, or 18V Enable Rising to LX Switching	1.18	1.3	V
21	Falling Enable Voltage Threshold	EN_{VIL}	PVIN = 3V, 12V, or 18V Enable Falling to LX Stops Switching	0.96	1.06	V
22	Enable Voltage LX Hysteresis	EN_{VIHhys}	PVIN = 3V, 12V, or 18V Enable Rising to LX Switching - Enable Falling to LX Stop Switching	20	410	mV
23	Standby Enable Voltage	SB_EN_{VIH}	PVIN = 3V, 12V, or 18V Enable Rising to VCC Enabled	0.45	1	V

Table 3. ISL73006SLH Datasheet Total Dose Parameters (TA = 25ºC)

Fig.	Parameter	Symbol	Test Conditions	Low Limit	High Limit	Unit
24	Shutdown Enable Voltage	SB_EN_{VIL}	PVIN = 3V, 12V, or 18V Enable Falling to VCC Disabled	0.3	0.9	V
25	Enable Hysteresis Voltage	EN_{HYS}	PVIN = 3V, 12V, or 18V Enable Rising to LX Switching - EN Falling to VCC Disable	20	175	mV
26	Low Enable Current	EN_{IIL}		-20	20	nA
27	High Enable Current	EN_{IIH}		1.7	3.1	µA
28	Enable (EN) Pull-Down Resistance	R_{EN}	PVIN = 12V	1.7	2.9	MΩ
29	VCC Output Voltage	$VOUT_{3V,0mA}$	PVIN = 3V, I_{OUT} = 0mA	2.96	3	V
		$VOUT_{3V,10mA}$	PVIN = 3V, I_{OUT} = 10mA	2.93	2.98	
30		$VOUT_{5V,0mA}$	PVIN = 5.5V, I_{OUT} = 0mA	4.83	5	
		$VOUT_{5V,10mA}$	PVIN = 5.5V, I_{OUT} = 10mA	4.82	5	
31	Output Overvoltage Error Threshold	OVPG	PVIN = 5V, FB as a % of V_{REF}	106.25	108.25	%
32	Output Undervoltage Error Threshold	UVPG	PVIN = 5V, FB as a % of V_{REF}	92.7	94.7	%
33	Output Overvoltage Fault	OV_{flt}	PVIN = 5V, FB as a % of V_{REF}	113.5	117.25	%
34	Output Undervoltage Fault	UV_{flt}	PVIN = 5V, FB as a % of V_{REF}	82.5	87	%
35	Low Current Drive	PG_I_{OL}	PVIN = 3V, PG = 0.4V, EN = 0V	11	35	mA
36	Low V_{OUT}	PG_V_{OL}	PVIN = 18V, FB = 0V, EN = 0V, IPG = 10mA	-	0.27	V
37	Leakage	I_{LKGPG}	PVIN = PG = 18V	-	1	µA
38	Power Good Rising Delay	$t_{SSPGdlyr}$	PVIN = 5.5V, from EN edge to PG high	6.6	8.4	ms
39	Rising Edge Delay	t_{PGdlyr}	PVIN = 3V, 12V, or 18V Return to regulation to PG response	1.9	4.2	µs
40	Falling Edge Delay	t_{PGdlyf}	PVIN = 3V, 12V, or 18V Out of regulation to PG response	3.5	6	µs
41	Minimum LX On-Time	t_{MIN_ON}	PVIN = 3V, 12V, or 18V Forced Min On-Time by COMP bias, No Load	-	280	ns
42	Minimum LX Off-Time	t_{MIN_OFF}	PVIN = 3V, 12V, or 18V Forced Min Off-Time by COMP bias, No Load	-	210	ns
43	Post Rad CDFP Upper FET $r_{DS(ON)}$	$25UPR_{DSON\_3}$	PVIN = 3.0V, I_{OUT} = 200mA	320	440	mΩ
		$25UPR_{DSON\_5}$	PVIN = 5.5V, I_{OUT} = 200mA	255	390	mΩ
44	Post Rad CDFP Lower FET $r_{DS(ON)}$	$25LWR_{DSON\_3}$	PVIN = 3.0V, I_{OUT} = 200mA	165	240	mΩ
		$25LWR_{DSON\_5}$	PVIN = 5.5V, I_{OUT} = 200mA	155	205	mΩ

Related Literature

For a full list of related documents, visit our website:

- ISL73006SLH device page
- MIL-STD-883 test method 1019

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