ISL73006SLH

Single Event Effects (SEE) Testing of the ISL73006SLH 18V, 1A Point-of-Load Regulator

Introduction

The intense proton and heavy-ion environment encountered in space applications can cause a variety of Single Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Latch-Up (SEL), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues, including disruption, degradation, and destruction. Individual electronic components should be characterized for predictable and reliable space system operation to determine their SEE response. This report discusses the SEE testing results performed on the ISL73006SLH product. The ISL73006SLH is offered with radiation assurance screening to 75krad(Si) at 10mrad(Si)/s.

SEE Summary

All SEE testing was performed with normal incidence gold for a LET of 86.3MeV·cm^2/mg at the surface of the device. The LET in the active silicon layer of the device ranged from 88.4MeV·cm^2/mg to 90.2MeV·cm^2/mg.

The ISL73006SLH was free of Destructive Single Event Effects (DSEE) under the following maximum parameter set: PVIN = 16.5V and VCC = 6.0V.

The regulator experienced SET events where V_{OUT} deviated beyond ±2% of its nominal value with a worst-case cross-section of 17.5µm^2. The maximum deviation in V_{OUT} was 2.33%. The maximum time until V_{OUT} returned within ±2% of its nominal value was 19.7µs.

A SEFI was defined as an event in which PG pulled low, and there was a loss of regulation in V_{OUT}. During a SEFI, the device enters a hiccup mode, and V_{OUT} regulation is restored with a spontaneous soft start. A total of 44 SEFIs were observed during testing for a cross-section of 8.41µm^2. PG was low for approximately 13ms during SEFIs. SEFIs for the ISL73006SLH were caused by a standard fault response with hiccup and soft-start.

Product Description

The ISL73006SLH is a radiation hardened Point-of-Load (POL) buck regulator that provides up to 1A of output current capability with an input voltage ranging from 3V to 18V and 3V to 16.5V in a heavy ion environment. The device uses constant frequency peak current mode control architecture for fast loop transient response. The device uses internal compensation or an external Type II compensation to optimize performance and stabilize the loop. The ISL73006SLH has a default switching frequency of 500kHz.

The ISL73006SLH integrates high-side (P-channel) and low-side (N-channel) power FETs. There are options for external or internal compensation and slope control that can be implemented with minimum external components, reducing the BOM count and design complexity.

The ISL73006SLH includes a comprehensive suite of operational features and protections, including preset undervoltage, overvoltage, overcurrent protections, power-good, soft-start, and over-temperature.

The ISL73006SLH operates across the temperature range of -55°C to +125°C and is available in a 10-lead ceramic dual in-line flat package (CDFP) and die form.

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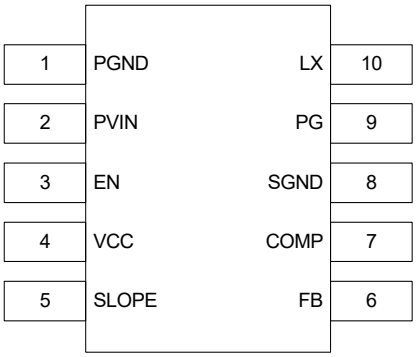

Figure 1. ISL73006SLH Pin Assignments

Table 1. ISL73006SLH Pin Descriptions

Pin Number	Pin Name	Description
1	PGND	Power-ground connection. Ground return for the low-side power MOSFET.
2	PVIN	Power Input. Supplies the power switches of the buck converter.
3	EN	Enable input. This input is a comparator-type input with a rising threshold of 1.2V. Bypass this pin to the PCB ground plane with a 10nF ceramic capacitor to mitigate SEE. This pin can be tied to a maximum of 5V.
4	VCC	Linear regulator output from PVIN to provide an internal bias supply rail of up to 5V. Bypass this pin to the PCB ground plane with a 2.2µF ceramic or low ESR Tantalum capacitor for stability, SEE, and noise mitigation. VCC is not intended to bias external circuits.
5	SLOPE	Slope Compensation. Connect a resistor from this pin to GND to externally set the slope compensation. This pin is a current source of 12µA into the external resistor. Connect the SLOPE pin to VCC to use the default internal slope compensation voltage of 1.2V. If not connected to VCC, add a 1nF capacitor from this pin to ground for SEE mitigation.
6	FB	Error Amplifier inverting input. Connect a resistor divider from VOUT to GND with the midpoint driving the FB pin.
7	COMP	Error Amplifier output. The external compensation network is connected from this pin to GND. Tie this pin to VCC to use the internal Error Amplifier compensation setup.
8	SGND	Signal ground. The ground is associated with the internal control circuitry. Connect this pin directly to the PCB ground plane at a single point. Pin 8 is connected to the thermal flash on the package bottom and the lid.
9	PG	Power-good output. The pin is an open-drain logic output pulled to SGND when the output is outside of the PGOOD range. The pin can be pulled to any voltage up to the PVIN absolute maximum limit. Renesas recommends using a nominal 1kΩ to 10kΩ pull-up resistor. Bypass this pin to the PCB ground plane with a 100pF capacitor for SEE mitigation.
10	LX	Switch node connection. Connect this pin to the output filter inductor. Internally, this pin is connected to the common node of the synchronous MOSFET power switches.

Contents

1. SEE Testing

1.1 Objective

The testing was intended to find the limits of the power input (PVIN) and linear regulator output (VCC) set by the onset of Destructive Single Event Effects (DSEE) at a LET of 86.3MeV·cm^2/mg (normal incidence gold). Additional testing was intended to identify and quantify SETs and SEFIs occurring in the output voltage of the ISL73006SLH. The SET and SEFI studies also consisted of irradiation with normal incidence gold (86.3MeV·cm^2/mg).

1.2 Facility

SEE testing was done at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute in College Station, Texas. This facility is coupled to a K500 superconducting cyclotron that can supply a wide range of ion species and flux. The SEE testing in this report was performed on August 22, 2023.

2. Results

2.1 DSEE Results

DSEE testing consisted of PVIN DSEE testing and VCC DSEE testing. V_{OUT} was set to 3.3V, EN = 5V, SLOPE and COMP were tied to VCC, and PG was pulled up to PVIN through a 10kΩ resistor. The output LC filter comprised a 15µH inductor and a 100µF bulk capacitor (ESR < 30mΩ). The test boards were configured to irradiate two devices simultaneously during a run.

2.1.1 PVIN

The purpose of the first component of DSEE testing was to find the maximum value of the power input voltage (PVIN) set by the onset of DSEEs at an ambient temperature of 25°C. An ambient temperature of 25°C was chosen because previous testing on a prior revision of the part with a lower overcurrent threshold indicated that this was a marginally worse temperature than a die temperature of 125°C for PVIN DSEE testing. For PVIN DSEE testing, I_{OUT} was switched between 0A and 1.1A at a frequency of 100Hz and a 50% duty cycle. VCC was bypassed to the PCB ground plane with a 2.7µF capacitor. PVIN was initially set to 14.7V and was incremented after each run up to a maximum voltage of 18.9V. Testing ended when the device underwent a DSEE or when PVIN reached 18.9V. The device was considered to have experienced a DSEE if the output voltage at no load changed by ±1% or the PVIN current at no load changed by ±1%.

The results of PVIN DSEE testing are displayed in Table 2. Devices began experiencing DSEEs with PVIN = 17.6V. Therefore, operate the device with a maximum value of PVIN = 16.5V to be robust against DSEE. The devices were monitored for SEFIs during PVIN DSEE testing. These results are also shown in Table 2. A total of 27 SEFIs were captured during PVIN DSEE testing. The characteristics of these SEFIs are discussed in the SEFI Results section.

Table 2. ISL73006SLH PVIN DSEE Test Results

PVIN (V)	Run #	DUT #	Result	Fluence (ions/cm^2)	V_{OUT} (±1%)			I_{PVIN} (±1%)			SEFI Count
					Pre (V)	Post (V)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)	
14.7	403	6	Pass	1E7	3.272	3.269	-0.09	7.66	7.69	0.39	4
		7	Pass	1E7	3.303	3.303	0.00	7.69	7.69	0.00	1
	408	11	Pass	1E7	3.312	3.306	-0.18	7.81	7.78	-0.38	1
		12	Pass	1E7	3.306	3.302	-0.12	7.79	7.74	-0.64	0

Table 2. ISL73006SLH PVIN DSEE Test Results (Cont.)

PVIN (V)	Run #	DUT #	Result	Fluence (ions/cm^2)	V_{OUT} (±1%)			I_{PVIN} (±1%)			SEFI Count
					Pre (V)	Post (V)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)	
15.6	404	6	Pass	1E7	3.270	3.271	0.03	7.7	7.7	0.00	3
		7	Pass	1E7	3.303	3.300	-0.09	7.69	7.68	-0.13	1
	409	11	Pass	1E7	3.311	3.311	0.00	7.81	7.81	0.00	1
		12	Pass	1E7	3.305	3.303	-0.06	7.75	7.76	0.13	5
16.5	405	6	Pass	1E7	3.272	3.275	0.09	7.7	7.74	0.52	2
		7	Pass	1E7	3.301	3.306	0.15	7.71	7.73	0.26	1
	410	11	Pass	1E7	3.311	3.308	-0.09	7.82	7.84	0.26	3
		12	Pass	1E7	3.301	3.302	0.03	7.78	7.79	0.13	0
17.6	406	6	Pass	1E7	3.276	3.276	0.00	7.74	7.74	0.00	3
		7	Pass	1E7	3.307	3.304	-0.09	7.75	7.75	0.00	1
	411	11	Fail	6.5E6	3.307	0.00	-100	7.84	3.2	-59.18	0
		12	Fail	9.2E6	3.301	0.00	-100	7.79	3.53	-54.69	1
18.9	407	6	Fail	3.65E6	3.275	0.00	-100	7.75	230	2867.74	0
		7	Fail	3.65E6	3.305	0.00	-100	7.78	14	79.95	0
	-	11	-	-	-	-	-	-	-	-	-
		12	-	-	-	-	-	-	-	-	-

2.1.2 VCC

The purpose of the second component of DSEE testing was to find the maximum value of the linear regulator output (VCC) set by the onset of DSEEs at a die temperature of 125°C. A die temperature of 125°C was chosen to exercise the control circuitry at the maximum die temperature. For VCC DSEE testing, the VCC supply was overdriven, so the internal regulator from PVIN was inactive, and the VCC current could be monitored directly. Additionally, I_{OUT} was set to 0A, and PVIN was set to 12V. VCC was initially set to 5.6V and was incremented after each run to a maximum voltage of 6.1V. Testing ended when the device underwent a DSEE or when VCC reached 6.1V. The device was considered to have experienced a DSEE if the output voltage at no load changed by ±1%, the PVIN current at no load changed by ±1%, or the VCC current at no load changed by ±1%.

The results of VCC DSEE testing are displayed in Table 3. DUT 2 experienced a DSEE when VCC = 6.1V. Therefore, operate the device with a maximum value of VCC = 6.0V to be robust against DSEE.

Table 3. ISL73006SLH VCC DSEE Test Results

VCC (V)	DUT #	Result	V_{OUT} (±1%)			I_{PVIN} (±1%)			I_{VCC} (±1%)		
			Pre (V)	Post (V)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
5.6	1	Pass	3.272	3.276	0.12	3.59	3.58	-0.28	4.905	4.919	0.29
	2	Pass	3.299	3.297	-0.06	3.56	3.53	-0.84	4.946	4.949	0.06
	9	Pass	3.280	3.284	0.12	3.43	3.44	0.29	4.788	4.761	-0.56
	12	Pass	3.289	3.289	0.00	3.52	3.54	0.57	4.916	4.904	-0.24

Table 3. ISL73006SLH VCC DSEE Test Results (Cont.)

VCC (V)	DUT #	Result	V_{OUT} (±1%)			I_{PVIN} (±1%)			I_{VCC} (±1%)		
			Pre (V)	Post (V)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)	Pre (mA)	Post (mA)	Δ (%)
5.8	1	Pass	3.277	3.277	0.00	3.61	3.61	0.00	5.573	5.563	-0.18
	2	Pass	3.298	3.300	0.06	3.62	3.62	0.00	5.601	5.595	-0.11
	9	Pass	3.285	3.285	0.00	3.55	3.55	0.00	5.419	5.424	0.09
	12	Pass	3.291	3.290	-0.03	3.62	3.61	-0.28	5.558	5.567	0.16
6.0	1	Pass	3.279	3.274	-0.15	3.68	3.69	0.27	6.249	6.258	0.14
	2	Pass	3.301	3.298	-0.09	3.71	3.71	0.00	6.279	6.276	-0.05
	9	Pass	3.287	3.296	0.27	3.61	3.62	0.28	6.107	6.162	0.90
	12	Pass	3.293	3.285	-0.24	3.69	3.69	0.00	6.247	6.231	-0.26
6.1	1	Pass	3.276	3.275	-0.03	3.8	3.83	0.79	6.878	6.835	-0.63
	2	Fail	3.30	3.303	0.09	3.9	3.9	0.00	6.884	7.756	12.67
	9	Pass	3.297	3.296	-0.03	3.65	3.67	0.55	6.513	6.478	-0.54
	12	Pass	3.287	3.290	0.09	3.74	3.75	0.27	6.578	6.563	-0.23

DSEE testing indicates that the device should be operated with the following maximum parameter set to be robust against DSEE: PVIN = 16.5V and VCC = 6.0V.

2.2 SET Results

For SET testing, devices were tested under eight different test conditions (TCs), as shown in Table 4. For all conditions, EN = 1.5V, VCC was bypassed to the PCB ground plane with a 2.7µF capacitor, PG was pulled up to PVIN through a 10kΩ resistor, and a load resistor (ROUT) was chosen such that the load current was 500mA. The test boards were configured to irradiate two devices simultaneously during a run. The ambient temperature was 25°C. A device experienced a SET when V_{OUT} deviated beyond ±2% of its nominal value. Triggers were set to capture events where PG dropped below 1V, or V_{OUT} deviated beyond ±2% of its nominal value to capture SEFIs and SETs, respectively.

Table 4. ISL73006SLH SET Test Conditions

Test Condition	# of Devices Tested	PVIN (V)	Slope	Comp	L_{OUT} (µH)	C_{OUT} (µF)	V_{OUT} (V)	R_{OUT} (Ω)
#1	4	3	VCC	VCC	6.8	68	1.8	3.6
#2	4	6						
#3	4	3	51.1kΩ	12.1kΩ, 3.9nF				
#4	4	6						
#5	4	10	VCC	VCC	15	47	3.3	6.6
#6	4	15						
#7	4	10	42.2kΩ	12.1kΩ, 4.7nF				
#8	4	15						

The results of SET testing for the ISL73006SLH are shown in Table 5.

Table 5. ISL73006SLH SET Test Results

Test Condition	Run #	DUT #	Fluence (ions/cm^2)	# of SETs	# of SEFIs
#1	430	27	1.0E7	0	0
		28	1.0E7	0	0
	432	29	1.0E7	0	0
		30	1.0E7	0	0
#2	431	27	1.0E7	0	0
		28	1.0E7	0	1
	433	29	1.0E7	0	0
		30	1.0E7	6	0
#3	434	25	1.0E7	0	0
		26	1.0E7	0	0
	436	23	1.0E7	0	0
		24	1.0E7	0	0
#4	435	25	1.0E7	0	2
		26	1.0E7	1	0
	437	23	1.0E7	0	0
		24	1.0E7	2	2
#5	438	37	1.0E7	0	0
		14	1.0E7	0	0
	440	31	1.0E7	0	0
		33	1.0E7	0	0
#6	439	37	1.0E7	0	1
		14	1.0E7	0	0
	441	31	1.0E7	1	1
		33	1.0E7	6	0
#7	442	29	1.0E7	1	0
		31	1.0E7	0	1
	444	30	1.0E7	0	0
		33	1.0E7	0	0
#8	443	29	1.0E7	0	1
		31	1.0E7	0	1
	445	30	1.0E7	0	0
		33	1.0E7	1	2

The results are summarized in Table 6.

Table 6. ISL73006SLH SET Test Results Summary

Test Condition	# of DUTs	Total Fluence (ions/cm^2)	# of SETs	SET σ (µm^2)	# of SEFIs
#1	4	4.0E7	0	2.5	0
#2	4	4.0E7	6	15	1
#3	4	4.0E7	0	2.5	0
#4	4	4.0E7	3	7.5	4
#5	4	4.0E7	0	2.5	0
#6	4	4.0E7	7	17.5	2
#7	4	4.0E7	1	2.5	1
#8	4	4.0E7	1	2.5	4
Worst Case	-	-	-	17.5	-

Of the 18 captures by the ±2% trigger, only 16 of the events were true SETs. Two events, one from TC #4 and one from TC #8, were double-ion strike events and are discussed separately.

Figure 2 through Figure 4 show scatter plots of the maximum V_{OUT} deviation in percentage of the nominal V_{OUT} voltage versus the SET recovery time in microseconds for test conditions #2, #4, and #6, respectively. The recovery time was defined as the duration V_{OUT} deviated beyond 2% of its nominal value. Some events had maximum V_{OUT} deviations of less than 2% and were triggered due to noise. The red lines indicate the 2% V_{OUT} deviation criteria. All the SETs resulted in positive deviations in V_{OUT}. The maximum SET V_{OUT} deviation was 2.33%, and only two of the 16 SETs had V_{OUT} deviations beyond 2.2%. The maximum recovery time was 19.7µs, and only three of the 16 SETs had recovery times longer than 15µs.

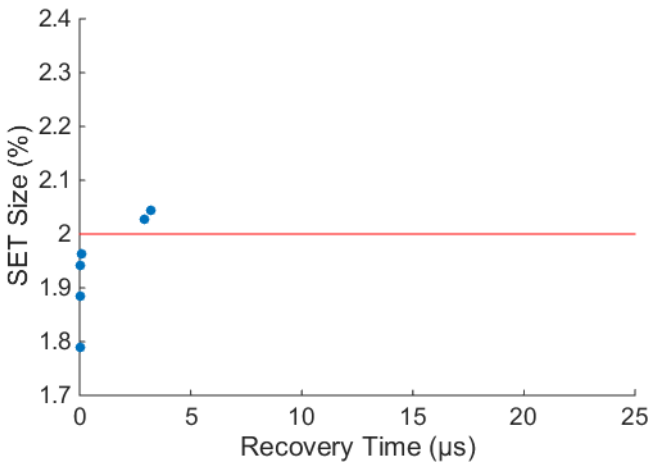

Figure 2. ISL73006SLH TC #2: V_{OUT} SET Size vs Recovery Time

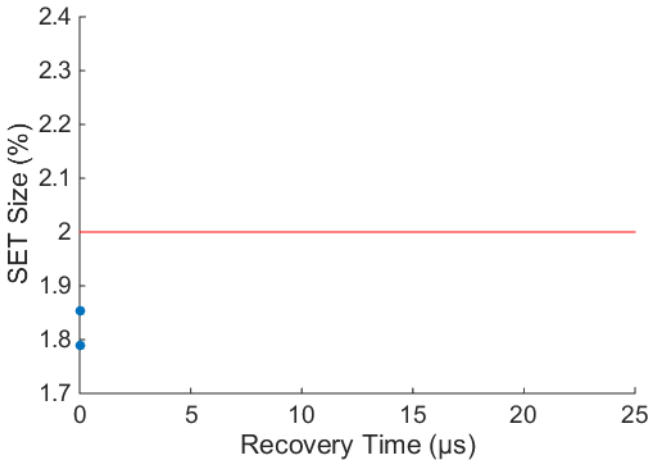

Figure 3. ISL73006SLH TC #4: V_{OUT} SET Size vs Recovery Time[1]

1. An event at (44.13µs, 2.71%) was a deviation in V_{OUT} caused by two ion strikes. Therefore, it is not a single event transient and was omitted from the plot.

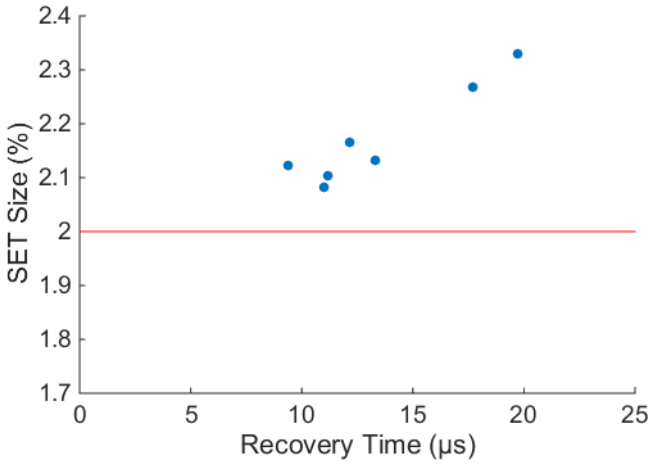

Figure 4. ISL73006SLH TC #6: V_{OUT} SET Size vs Recovery Time

TC #7 only had one SET event. This event had a V_{OUT} deviation of 2.08% and a recovery time of 15.95µs.

TC #8 also only had one event. This event had a V_{OUT} deviation of 2.45% and a recovery time of 33.51µs. However, this transient was caused by two separate ion strikes; therefore, it is not a single event transient.

Figure 5 shows the largest SET captured after applying a Gaussian filter by convolving the signal, sampled at a rate of one sample per 10ns, with an 11-point Gaussian window, with a width factor of 2.5. This SET occurred while the device was in TC #6; it had a V_{OUT} deviation of 2.33% and a recovery time of 19.7µs. During all of the SETs, there was a sharp increase in VCC (red) by approximately 0.1V. VCC recovered after 80µs. Judging by the timing of the events, it seems that the perturbation in VCC rippled into V_{OUT} (black), which peaked at a voltage more than 2% above its nominal voltage. V_{OUT} then recovered and returned to its nominal voltage. All 16 SETs had waveforms similar to Figure 5.

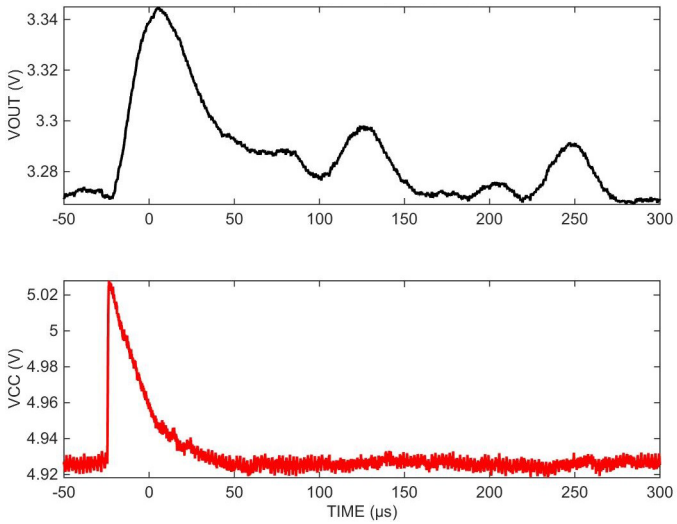

Figure 5. Typical SET Capture

TC #8 and TC#4 had events caused by double ion strikes. Both waveforms are similar to Figure 6. A Gaussian filter was applied to the waveforms in Figure 6 by convolving the signal, sampled at a rate of one sample per 10ns, with an 11-point Gaussian window with a width factor of 2.5. During the event, two distinct impulses on VCC (red) indicated two ion strikes. Each impulse increased V_{OUT} (black), leading to a larger V_{OUT} deviation and recovery time. Since these events involved multiple ion strikes, they were not single event transients. Double ion strike events are possible during SEE testing because the flux during SEE testing is much higher than typical fluxes encountered in space. Testing was performed with a flux of 5E4ions/cm2/s, which means, on average, five ions will strike every square centimeter of the device every 100µs. Therefore, multiple ions can strike the sensitive area of the device in close temporal proximity. However, this situation is virtually impossible in an ordinary space environment.

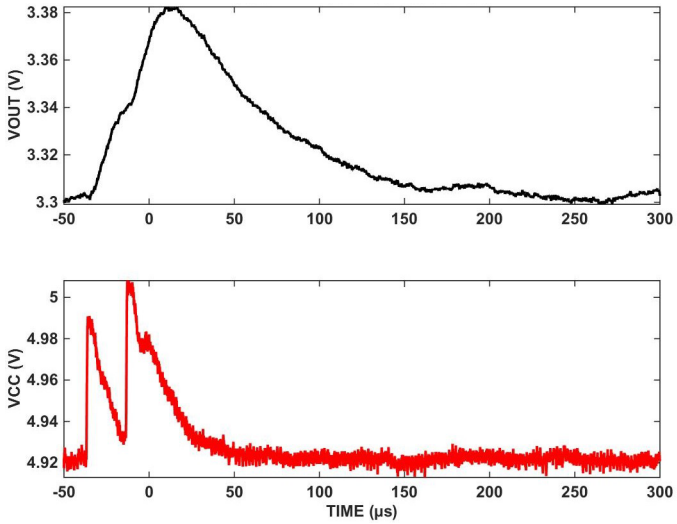

Figure 6. V_{OUT} Deviation from Multiple Ion Strikes

The maximum cross-section for SETs was 17.5µm^2. The largest deviation in V_{OUT} during a SET was 2.33%. The longest recovery time was 19.7µs.

A total of 12 SEFIs were captured during SET testing. The characteristics of the SEFIs are discussed in the SEFI Results section.

2.3 SEFI Results

A previous version of the part with a lower overcurrent limit had a high SEFI rate, so special SEFI testing was performed to verify that the new version of the ISL73006SLH had a low SEFI rate. For SEFI testing, four devices were tested with SLOPE connected to GND through a 41.7kΩ resistor, COMP connected to GND through a 12.1kΩ, 3.3nF RC filter, PVIN = 15.6V, V_{OUT} = 3.3V, and PG was pulled up to PVIN through a 10kΩ resistor. IOUT was switched between 0A and 1.1A at a frequency of 100Hz and a 50% duty cycle. The output LC filter comprised a 15µH inductor and a 100µF bulk capacitor (ESR < 30mΩ). The ambient temperature was 25°C. The test boards were configured such that two devices could be tested simultaneously during a run. The trigger was set to capture events in which PG dropped below 5V.

The results of SEFI testing are displayed in Table 7.

Table 7. ISL73006SLH SEFI Test Results

Run #	DUT #	Fluence (ions/cm^2)	# of SEFIs
401	4	1.0E7	3
	5	1.0E7	2
402	45	1.0E7	0
	46	1.0E7	0

A total of five SEFIs were captured during SEFI testing. The SEFI rates appear to be independent of operating conditions. Therefore, the total SEFI cross-section can be calculated as the total number of SEFIs captured during all testing of the ISL73006SLH over the total fluence. A total of 44 SEFIs were captured during testing to a fluence of 5.23E8ions/cm^2, so the SEFI cross-section is 8.41µm^2.

A typical SEFI waveform is shown in Figure 7. PG (red) indicates that the SEFI was approximately 13ms in duration. During the SEFI, V_{OUT} (black) fell after PG pulled low. V_{OUT} remained low while the device turned on again in a hiccup mode. After approximately 11ms, V_{OUT} underwent a spontaneous and full soft start, and it fully recovered around 13ms after the inception of the SEFI, coinciding with PG's recovery. The small spike in V_{OUT} at 15ms was a transient caused by the load current switching from 1.1A to 0A. All 44 SEFIs had waveforms similar to Figure 7.

SEFIs for the ISL73006SLH were caused by a standard fault response with hiccup and soft-start.

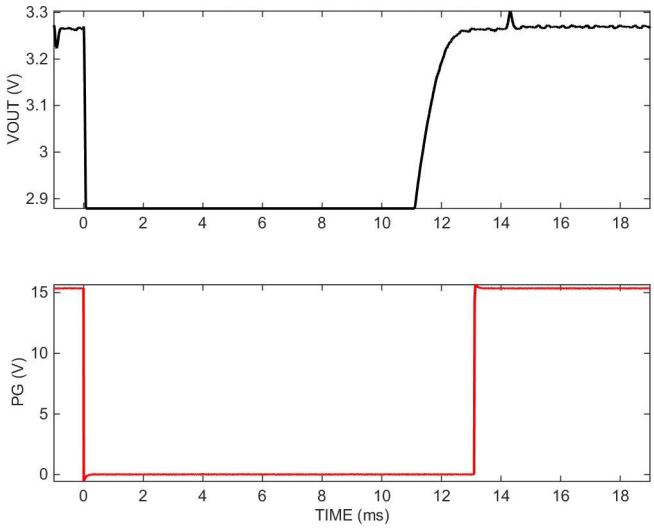

Figure 7. Typical SEFI Capture

3. Discussion and Conclusion

All SEE testing was performed with normal incidence gold for a LET of 86.3MeV·cm^2/mg at the surface of the device. The thickness of the metalization layers for the ISL73006SLH is 11.8µm, and the thickness of the active silicon layer is 10µm. The LET in the active silicon layer of the device ranged from 88.4MeV·cm^2/mg to 90.2MeV·cm^2/mg.

DSEE testing demonstrated operating the device with the following maximum parameter set to be robust against DSEE: PVIN = 16.5V and VCC = 6V.

Of the 18 captures by the ±2% trigger during SET testing, only 16 of the events were true SETs. Two of the events were double ion strike events. All the SETs resulted in positive deviations in V_{OUT}. The maximum V_{OUT} deviation was 2.33%. The longest amount of time it took for V_{OUT} to recover was 19.7µs. The largest cross-section for SETs on V_{OUT} was 17.5µm^2. Of the 16 SET events, only three had V_{OUT} deviations greater than 2.2% or recovery times longer than 15µs.

A total of 44 SEFIs were observed during testing. The total cross-section for SEFIs was 8.41µm^2. During SEFIs, PG was low for approximately 13ms. SEFIs recovered after allowing time for a hiccup and a full soft start. SEFIs for the ISL73006SLH were caused by a standard fault response with hiccup and soft-start.

A worst-case SEFI rate calculation can be performed in CRÈME96 using a step function with an onset value of 1MeV·cm^2/mg and a saturation cross-section of 8.41µm^2. A step function can be approximated using a Weibull curve with a width parameter of 0.1MeV·cm^2/mg and an exponent parameter of 10. The SEFI rate for the ISL73006SLH behind 100mils of aluminum shielding in a GEO orbit during solar minimum is 4.24E-3 SEFIs per year, which equates to an average of one SEFI every 236 years.

4. Revision History

Revision	Date	Description
1.01	Dec 18, 2023	Updated part number throughout.
1.00	Sep 19, 2023	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

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