

REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
	1.0	INITIAL RELEASE	2009-12-05	T. TRAN

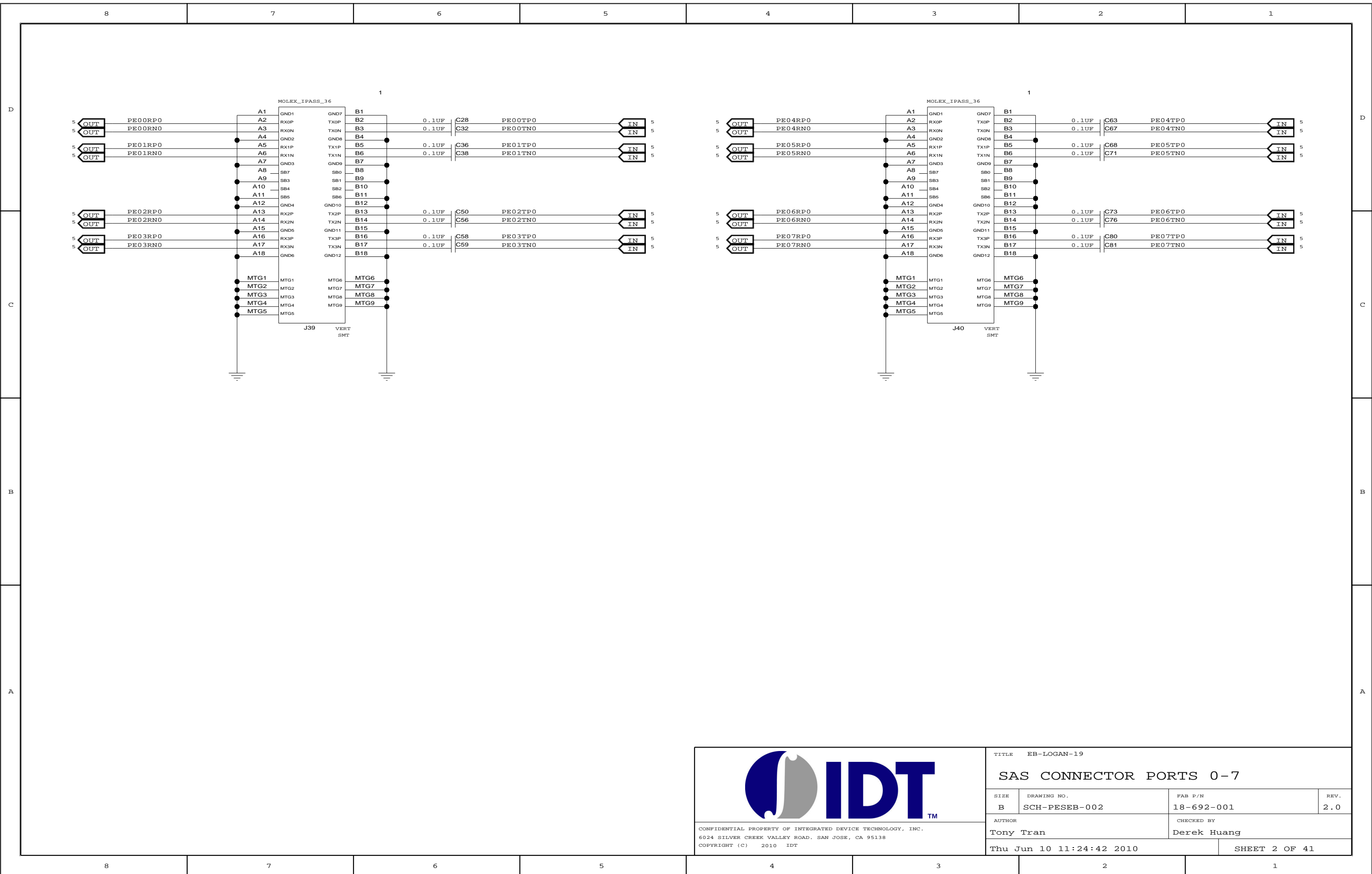
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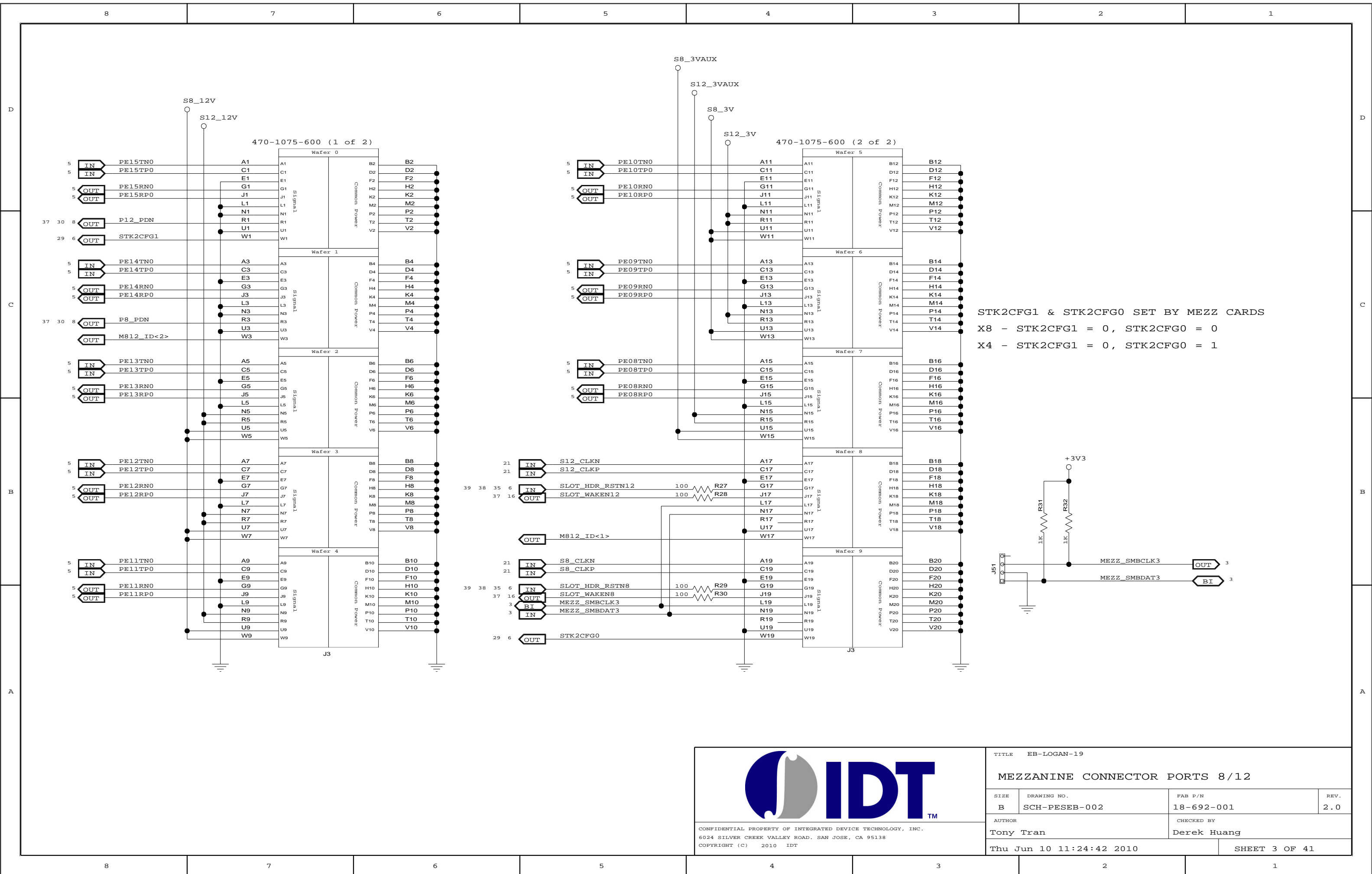
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TITLE EB-LOGAN-19			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:42 2010			SHEET 1 OF 41



		TITLE EB-LOGAN-19		
		SAS CONNECTOR PORTS 0-7		
SIZE	DRAWING NO.	FAB P/N	REV.	
B	SCH-PESEB-002	18-692-001	2.0	
AUTHOR		CHECKED BY		
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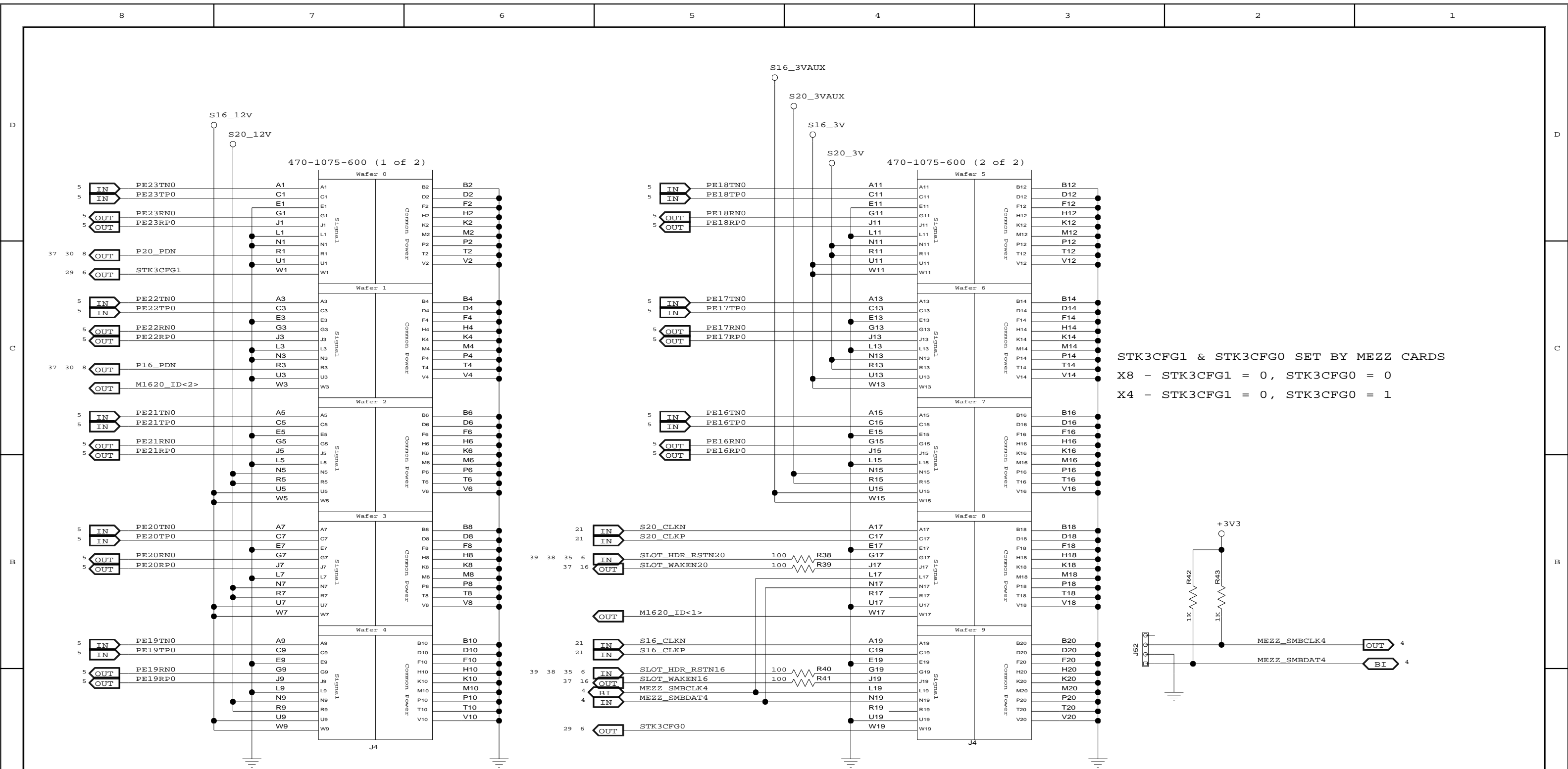


STK2CFG1 & STK2CFG0 SET BY MEZZ CARDS
 X8 - STK2CFG1 = 0, STK2CFG0 = 0
 X4 - STK2CFG1 = 0, STK2CFG0 = 1

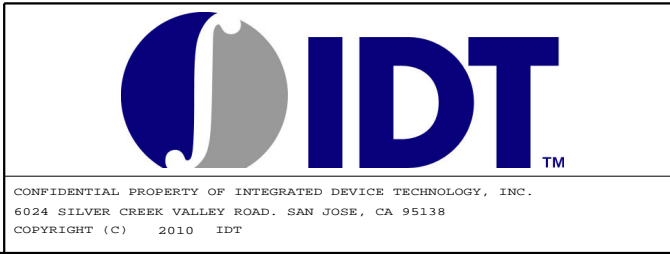


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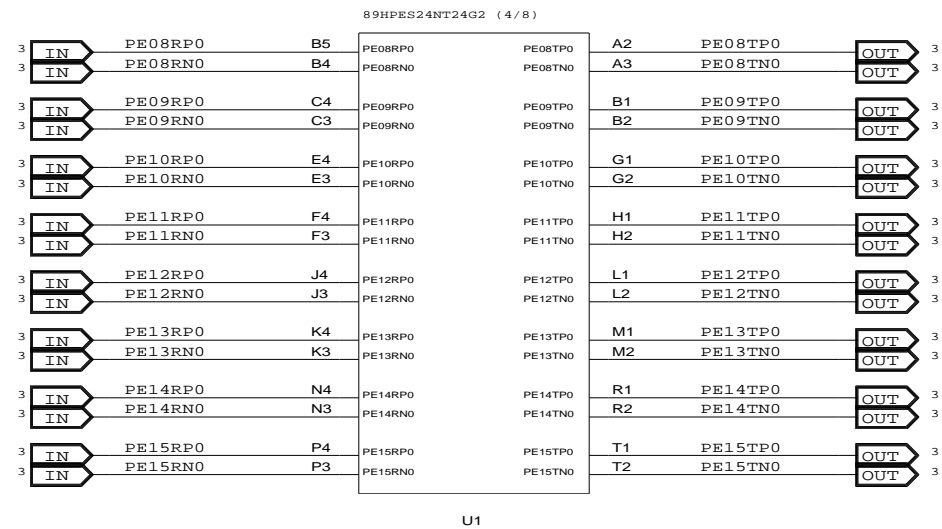
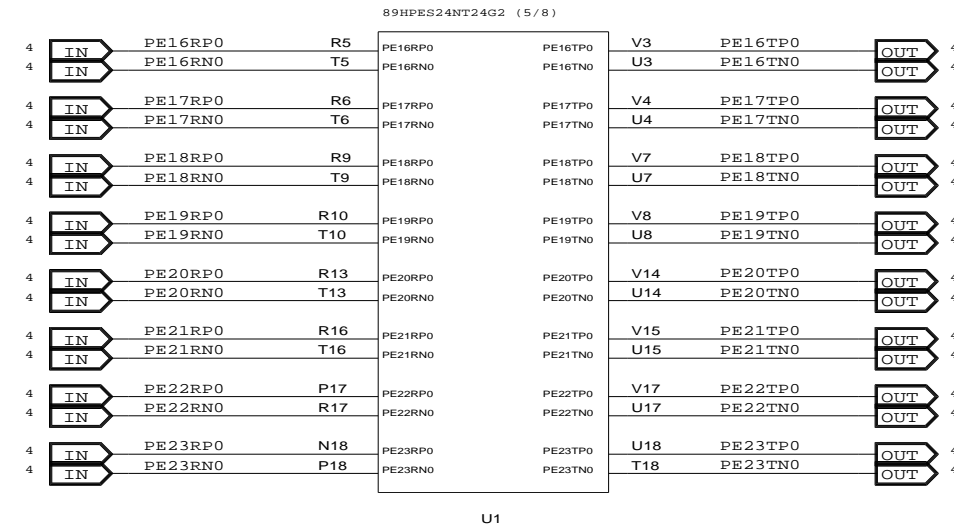
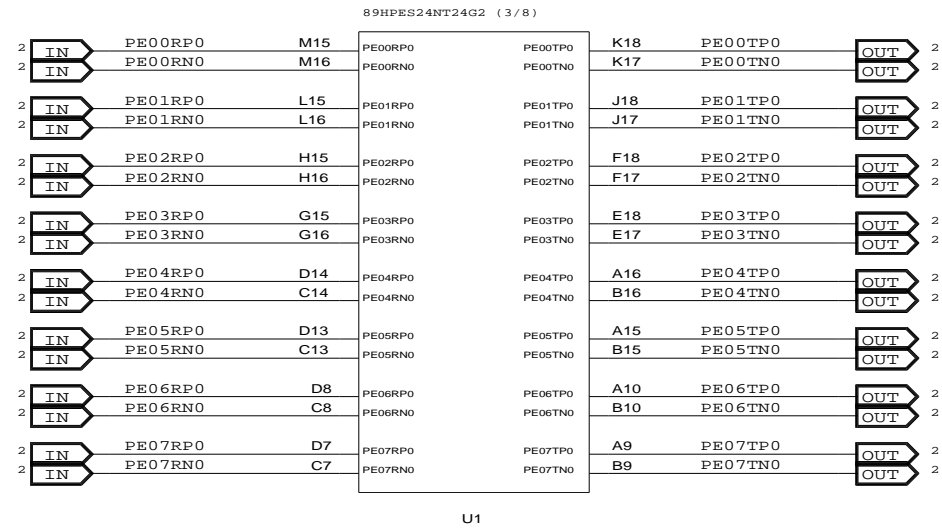
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MEZZANINE CONNECTOR PORTS 8/12			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:42 2010			SHEET 3 OF 41




STK3CFG1 & STK3CFG0 SET BY MEZZ CARDS
 X8 - STK3CFG1 = 0, STK3CFG0 = 0
 X4 - STK3CFG1 = 0, STK3CFG0 = 1

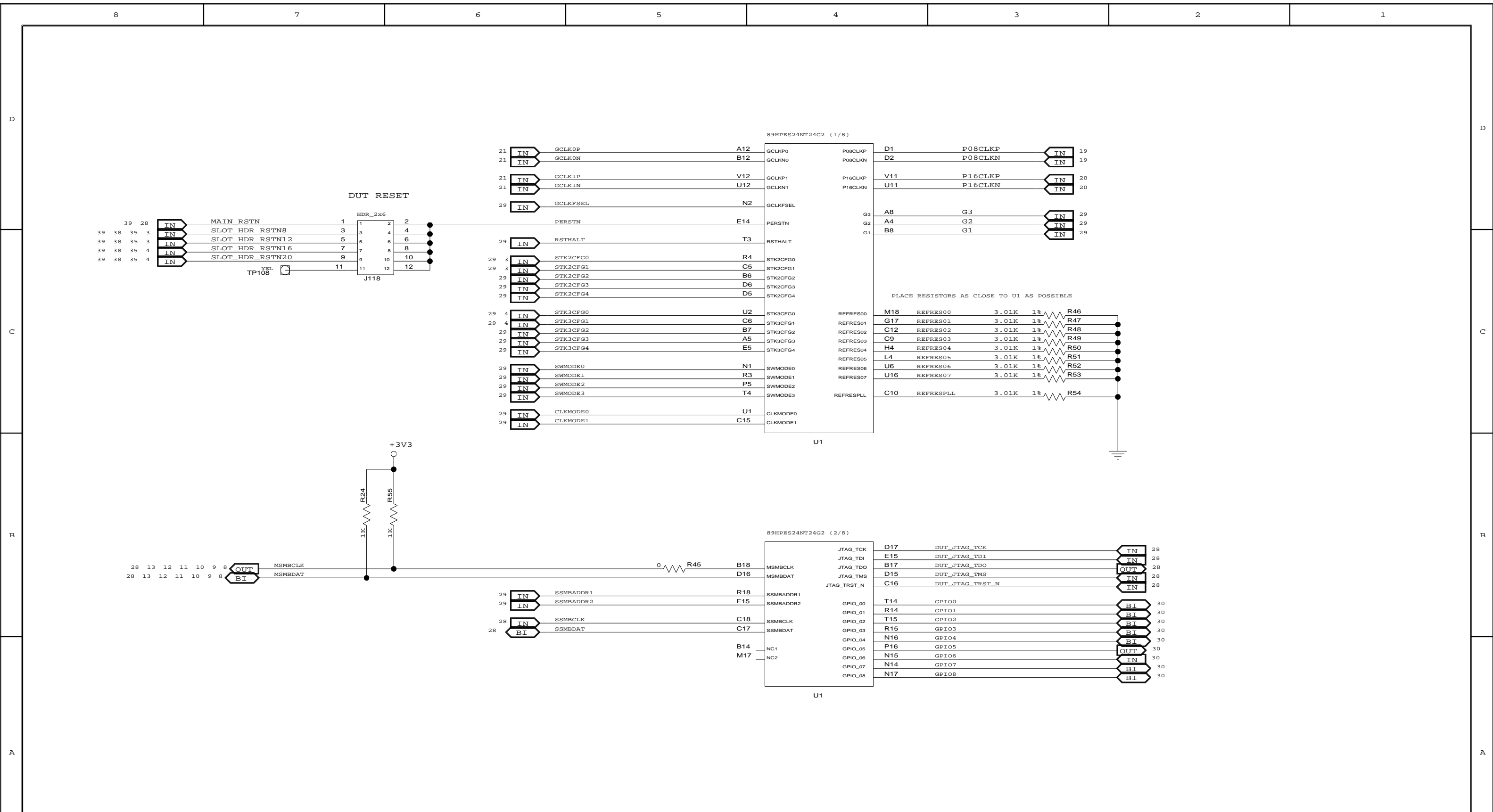


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MEZZANINE CONNECTOR PORTS 16/20			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
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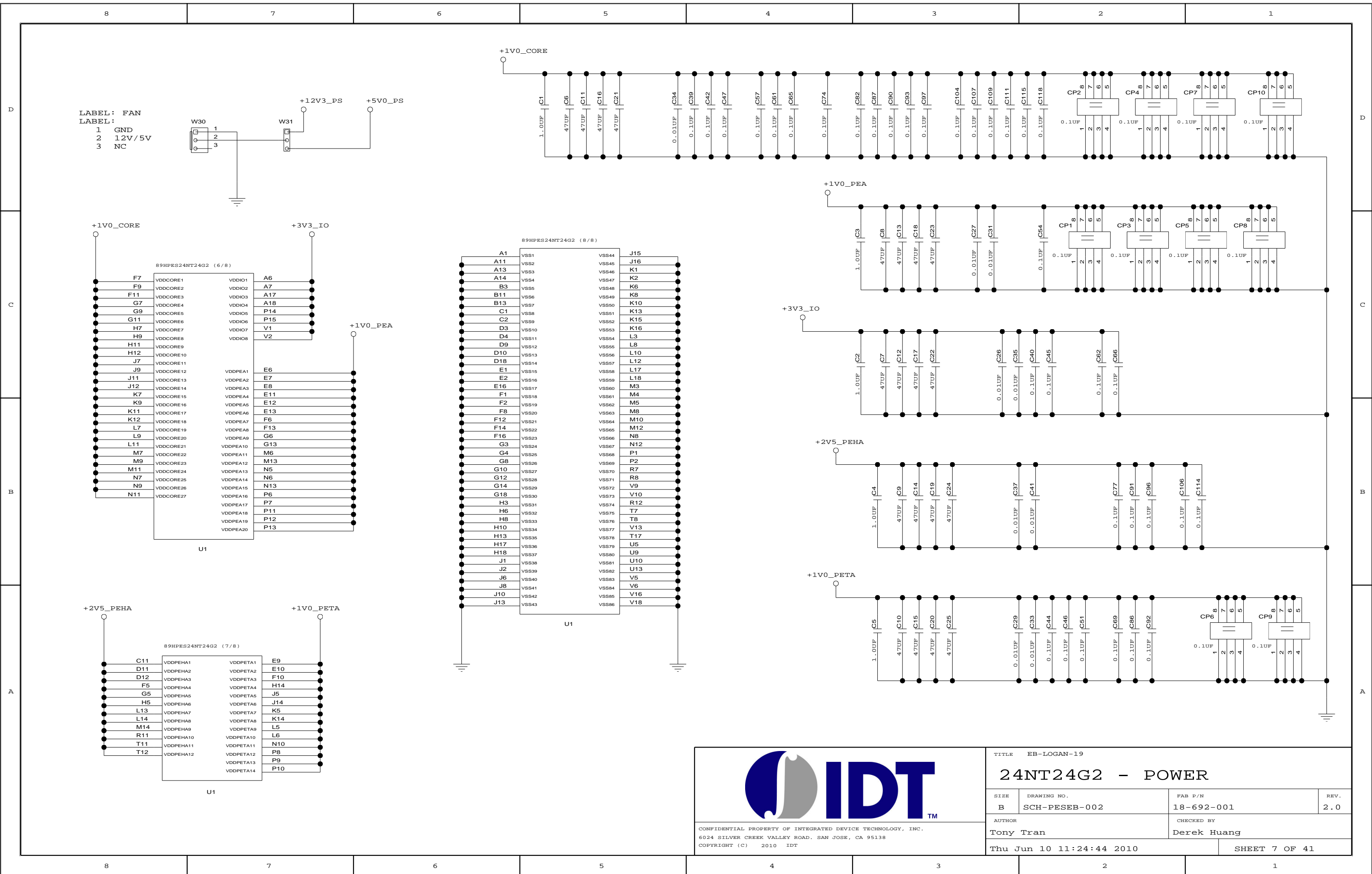
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SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
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TITLE EB-LOGAN-19			
24NT24G2 - CLK, CONFIG, GPIO			
SIZE	DRAWING NO.	FAB P/N	REV.
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LABEL: FAN
 LABEL:
 1 GND
 2 12V/5V
 3 NC



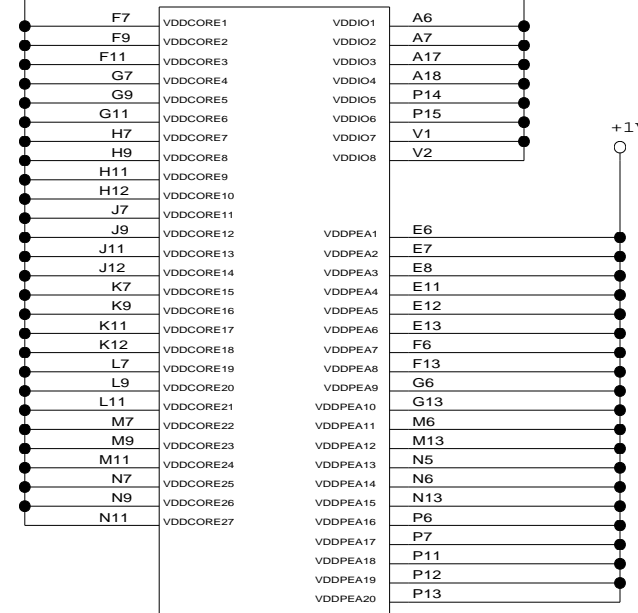
+12V3_PS
 +5V0_PS



+1V0_CORE

+3V3_IO

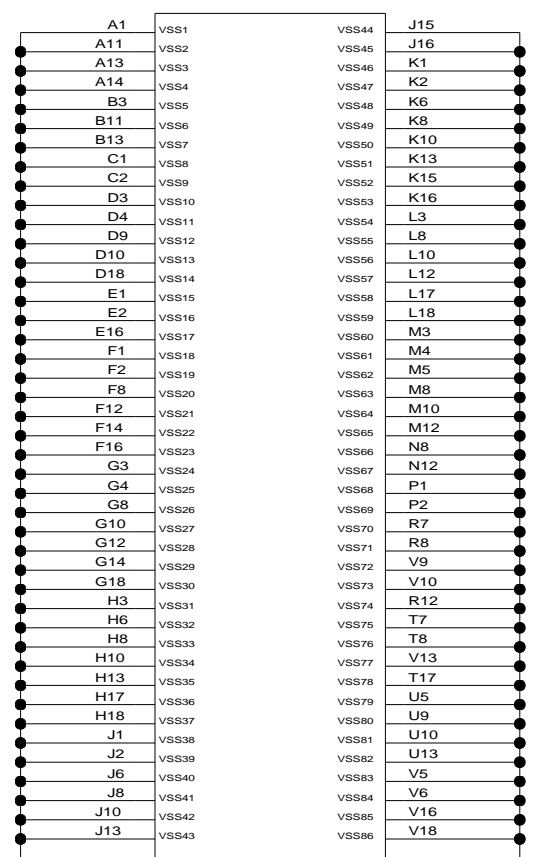
89HPES24NT24G2 (6/8)



U1

+1V0_PEA

89HPES24NT24G2 (8/8)

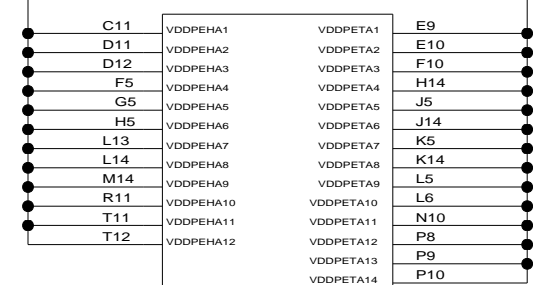


U1

+2V5_PEHA

+1V0_PETA

89HPES24NT24G2 (7/8)



U1

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24NT24G2 - POWER			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
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D

D

C

C

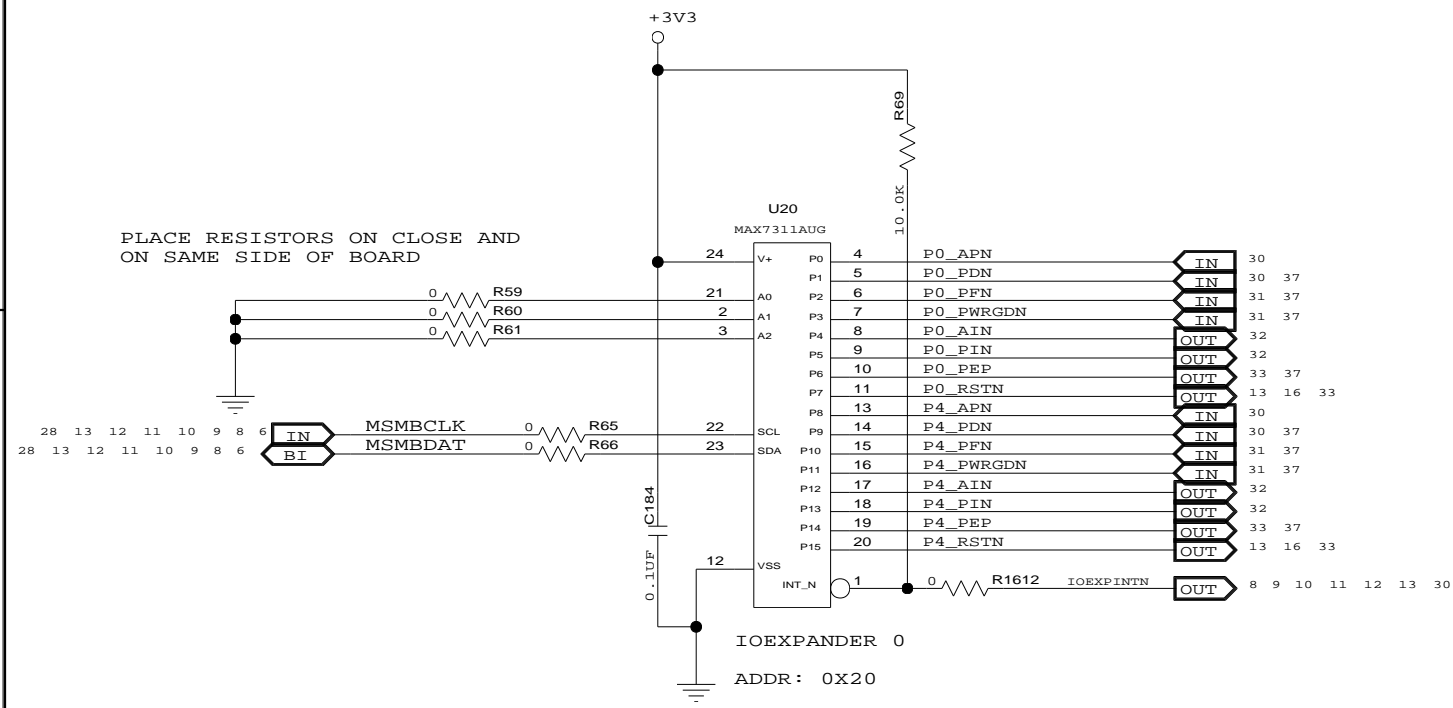
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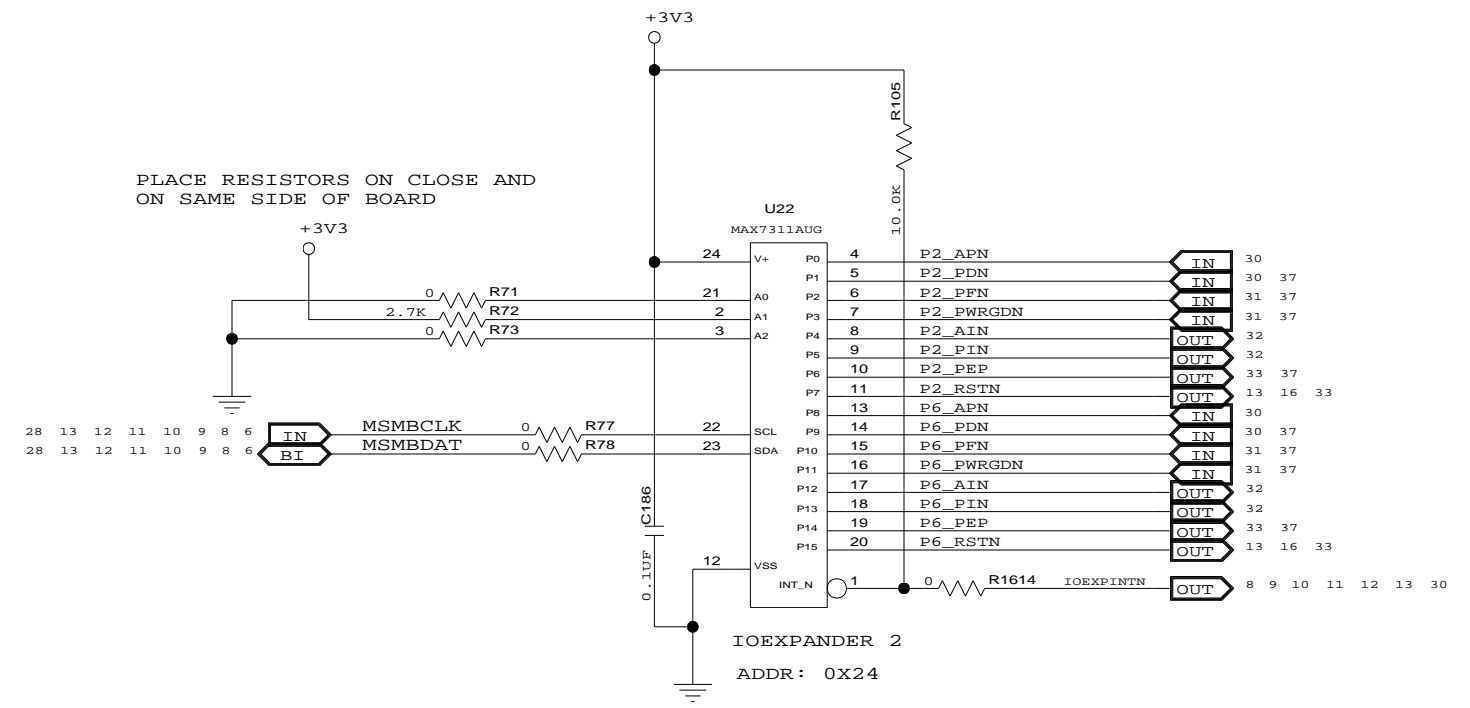
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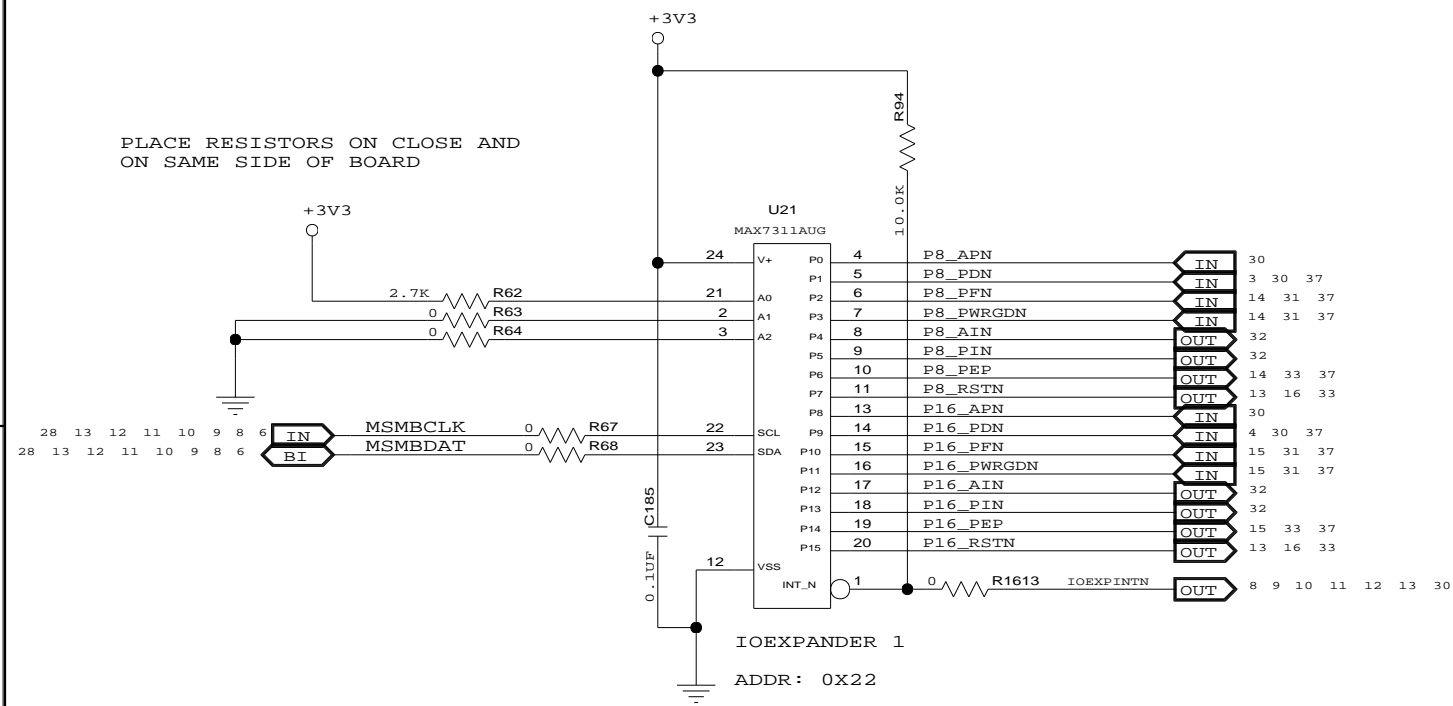
PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



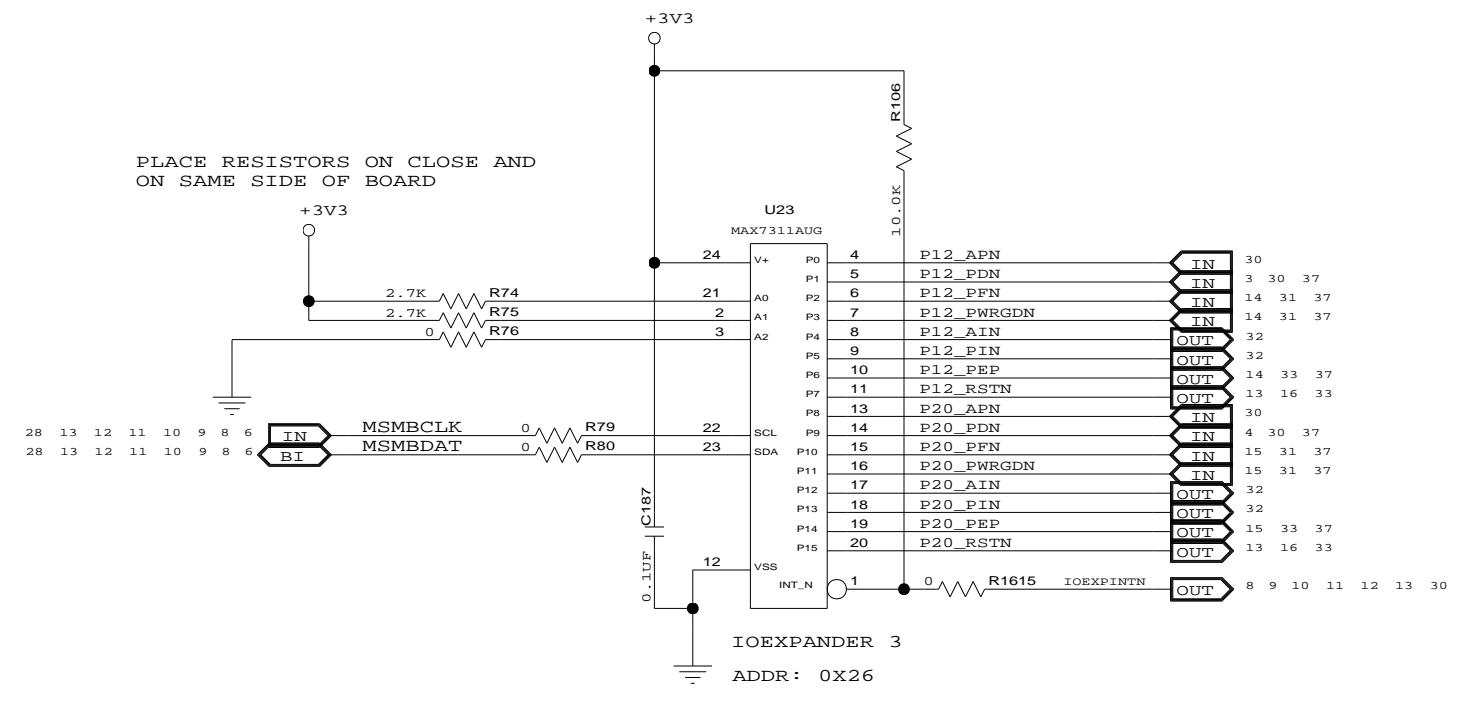
PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

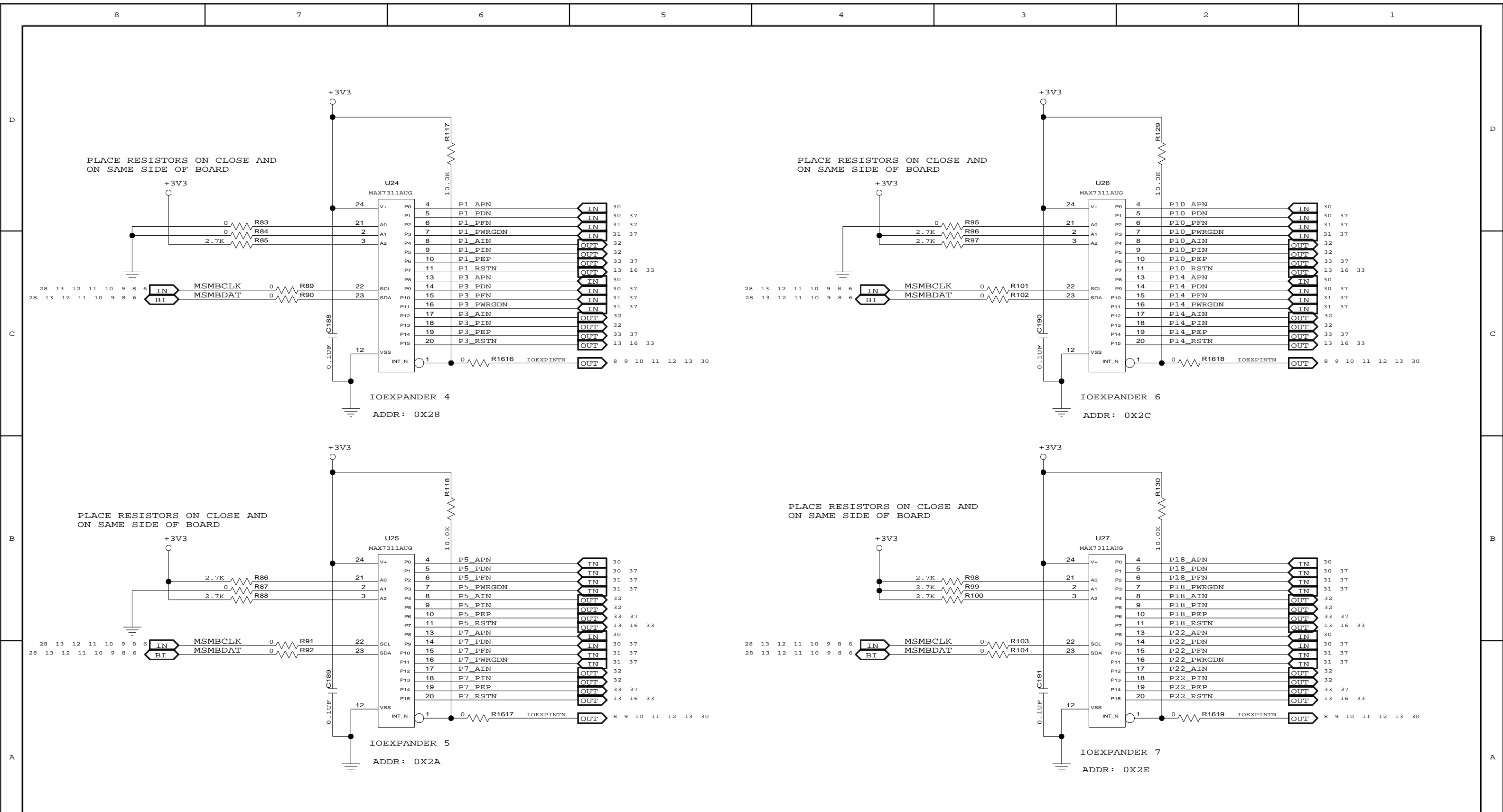



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TITLE EB-LOGAN-19

IOEXPANDER 0-3

SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
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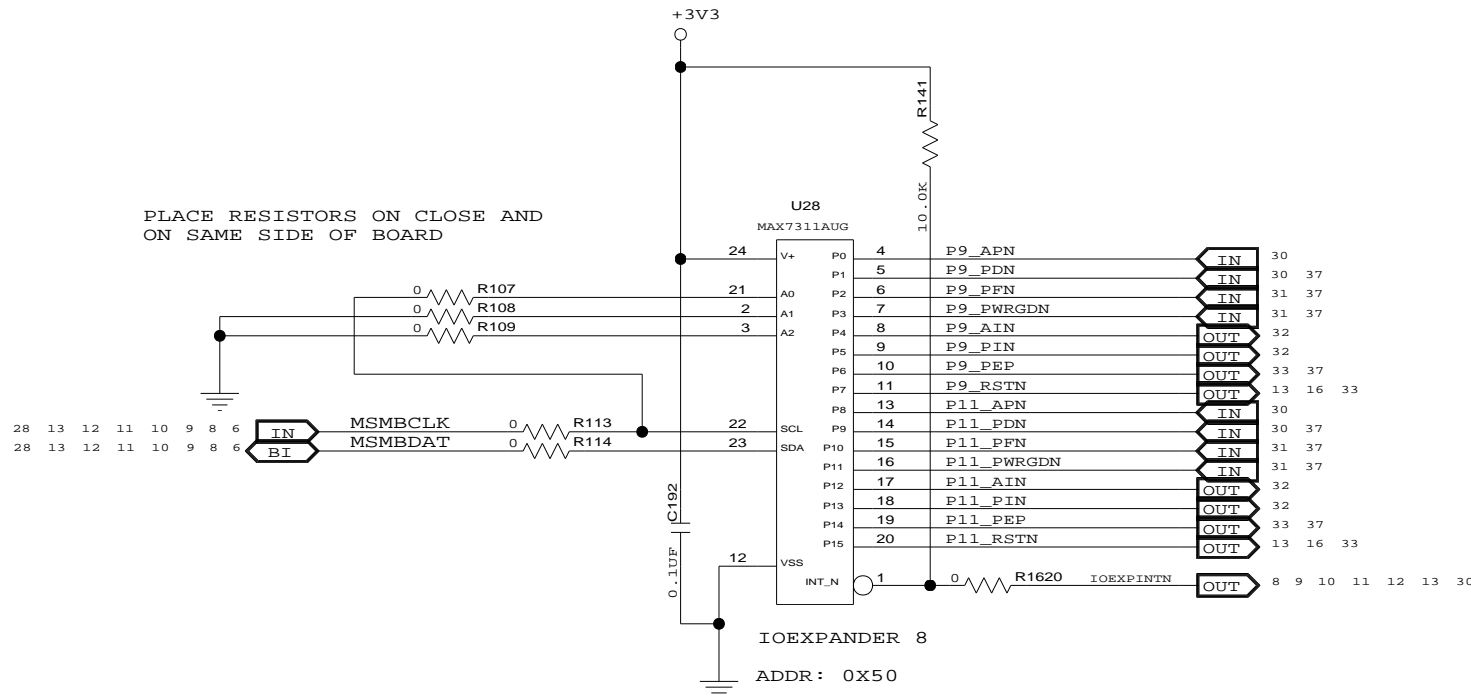
IOEXPANDER 4-7

SIZE	DRAWING NO.	FAB P/N	REV.
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AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:45 2010			SHEET 9 OF 41

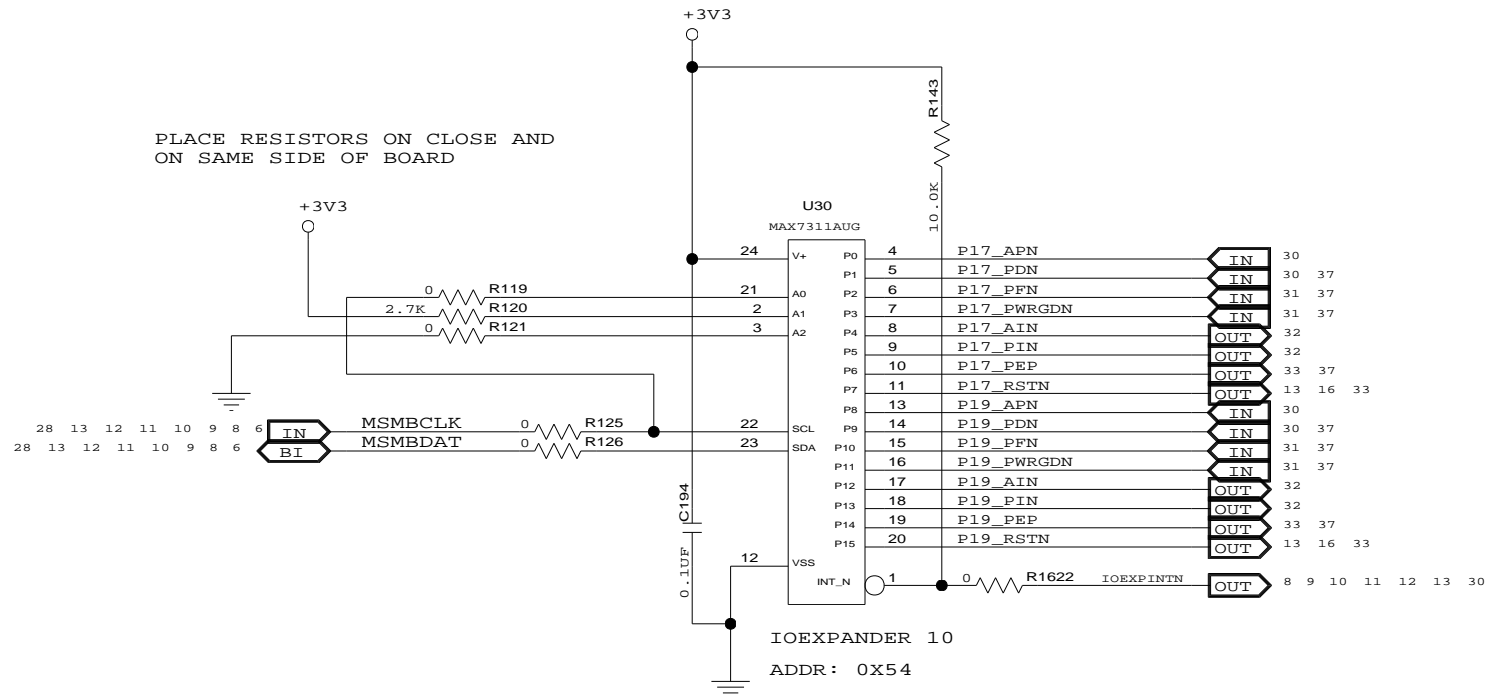
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PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



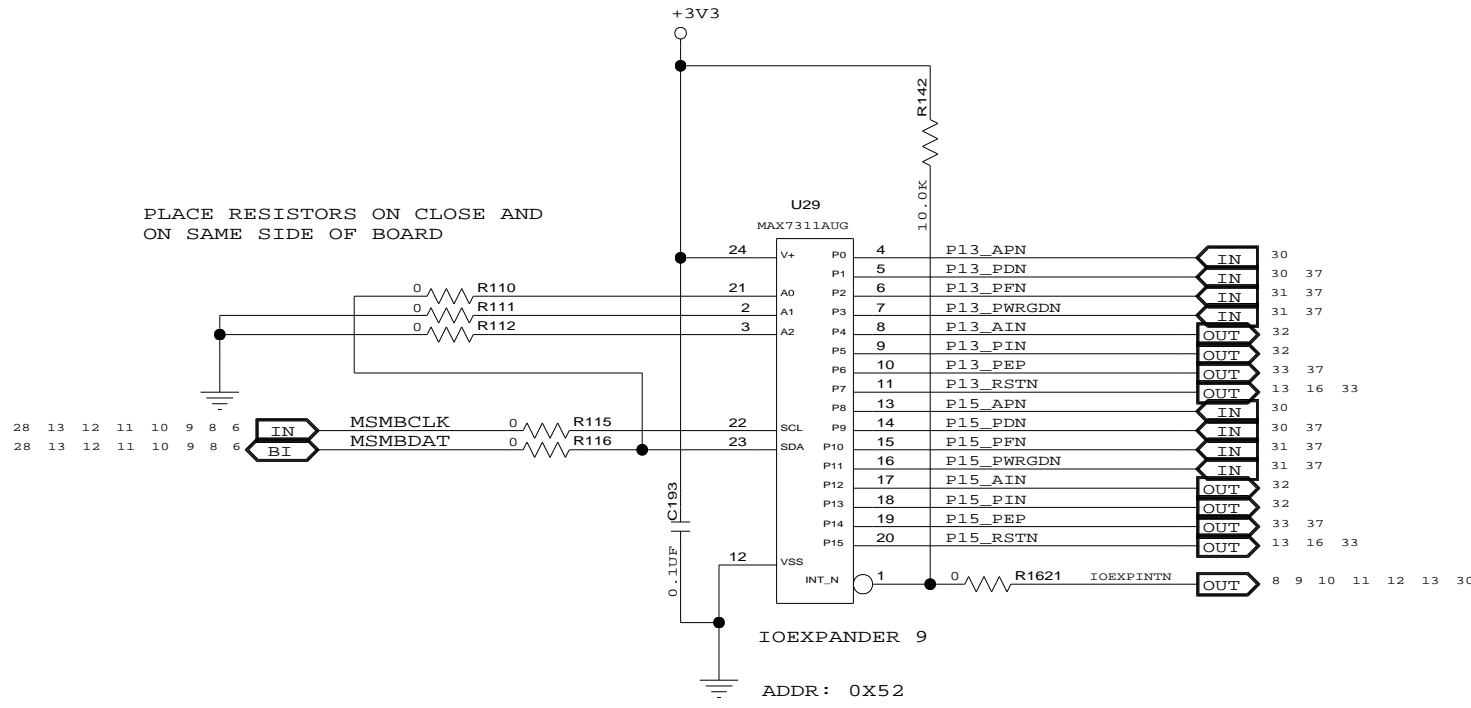
PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



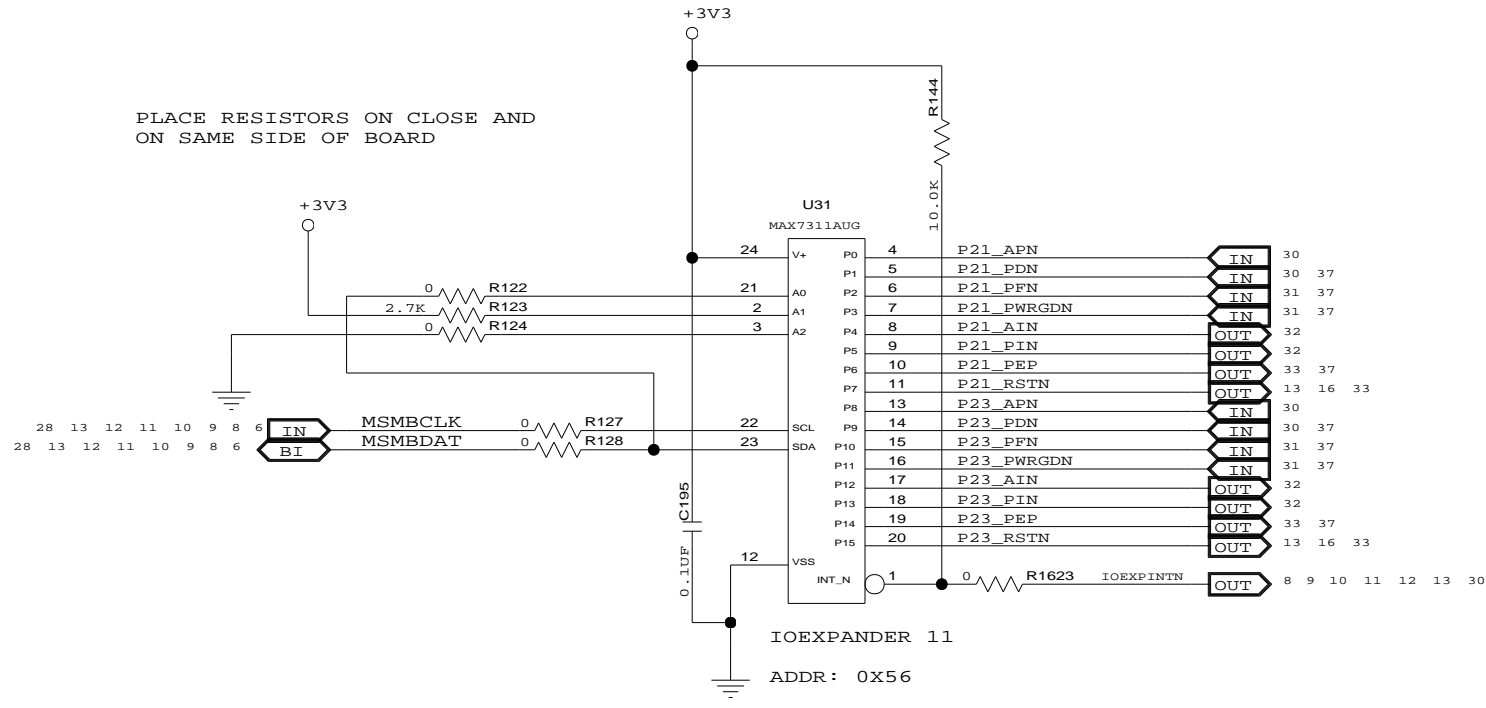
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C

PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



B

B

A

A



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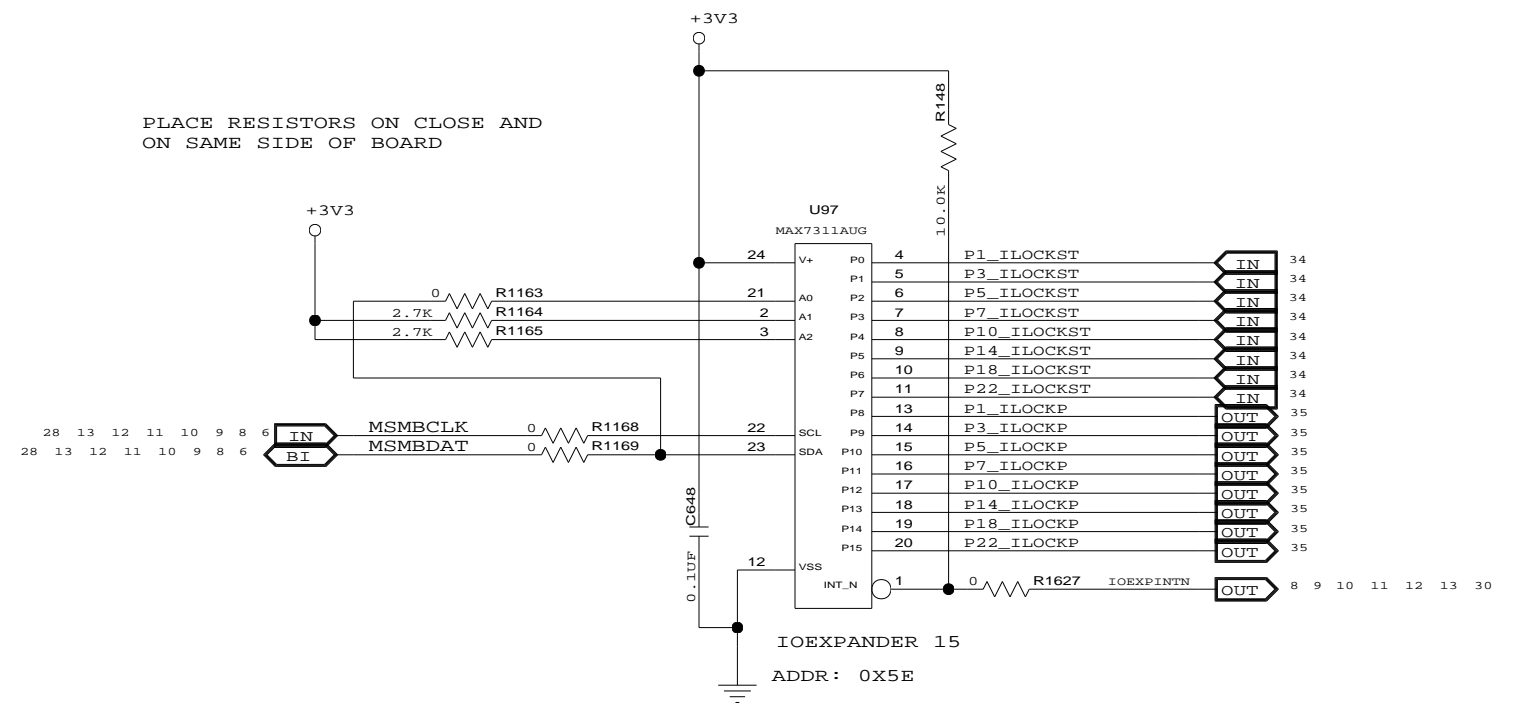
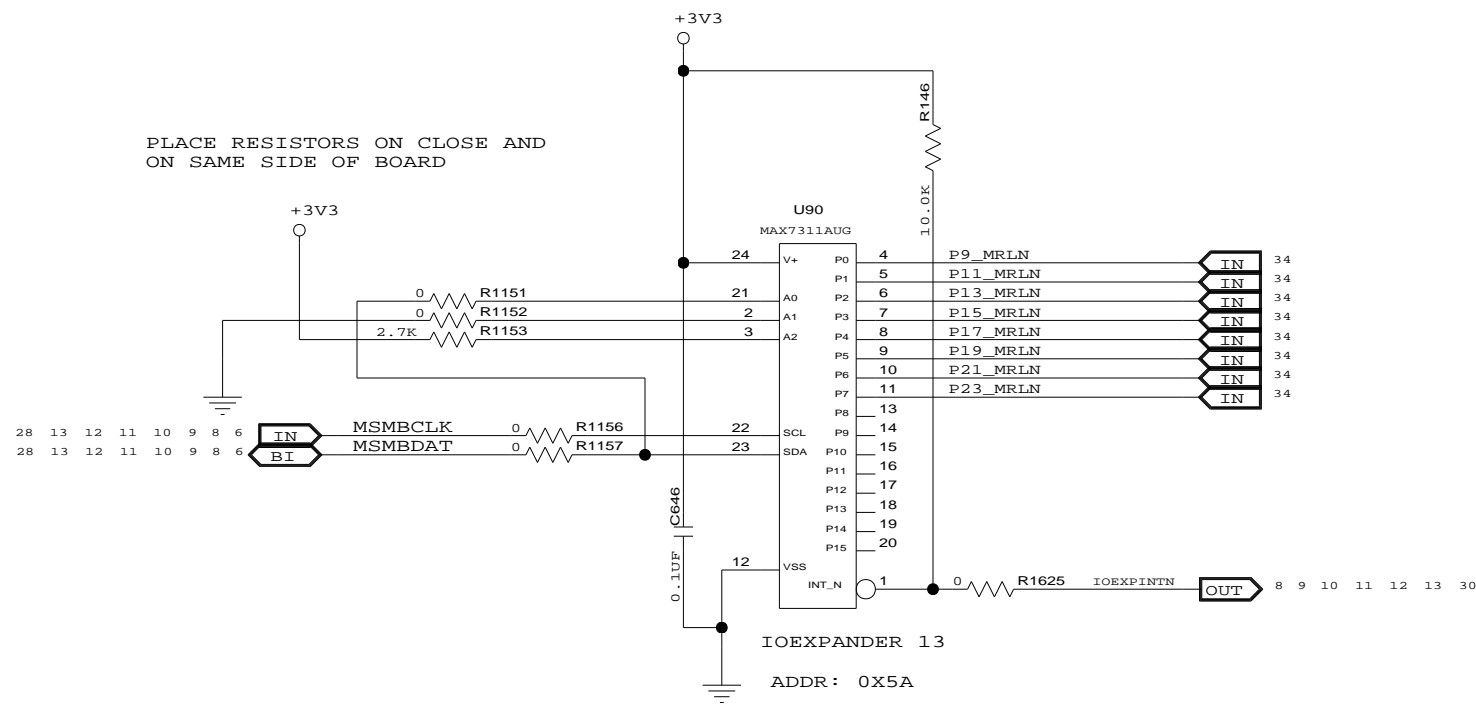
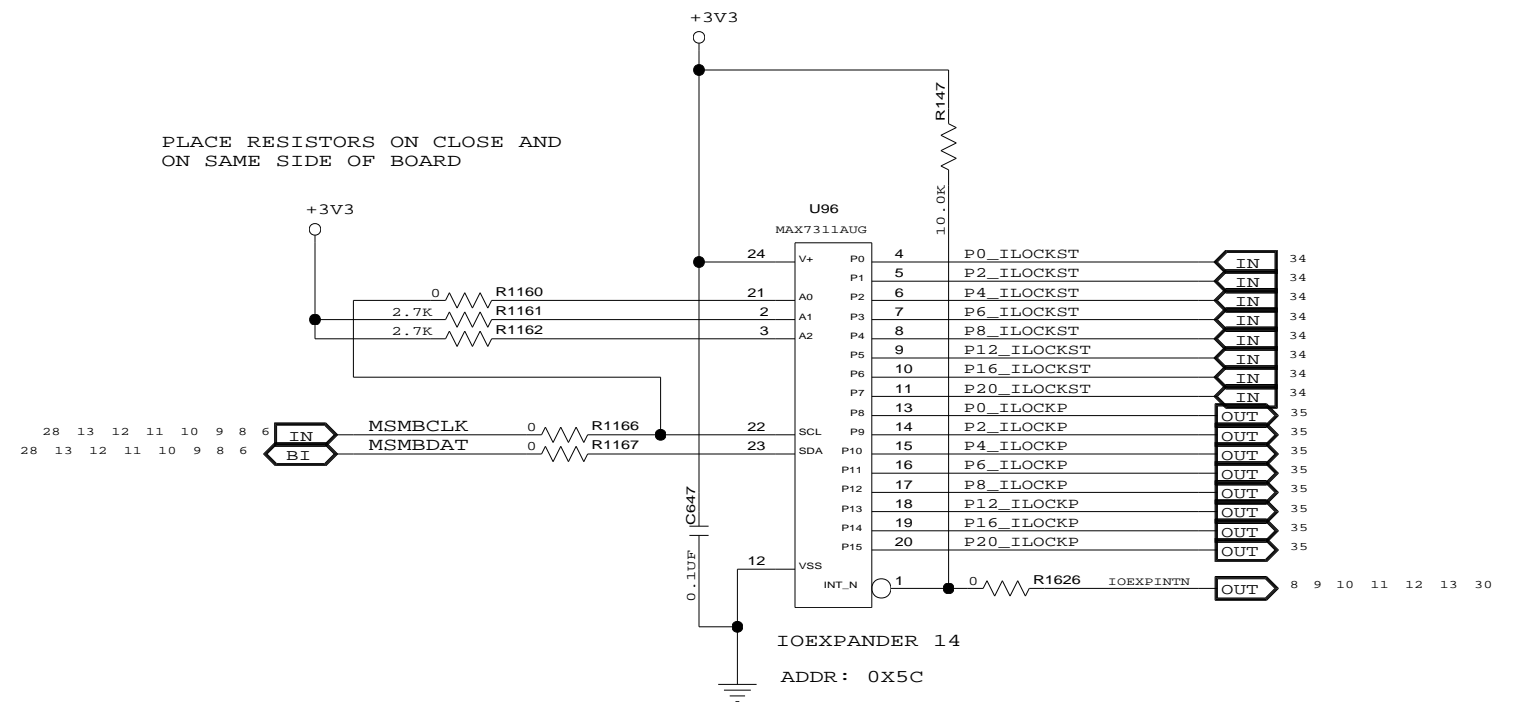
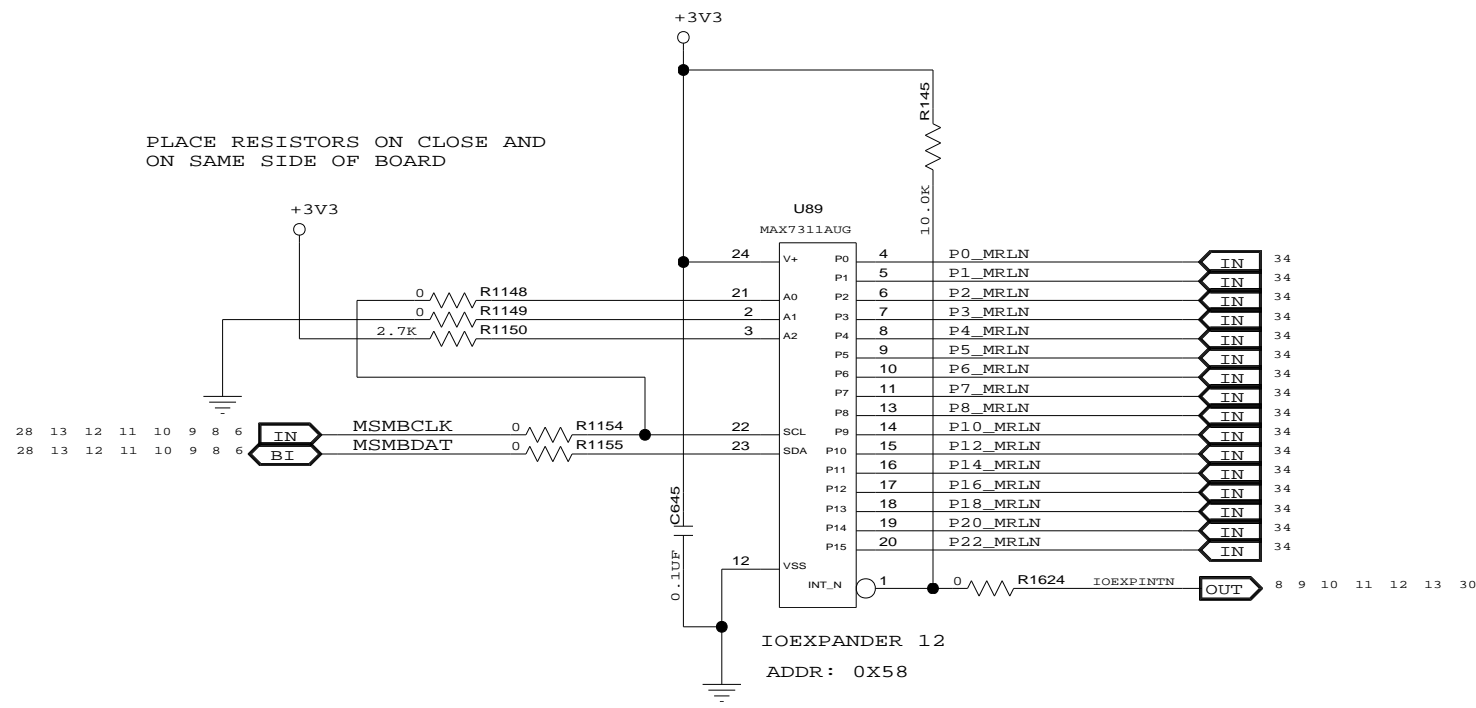
TITLE EB-LOGAN-19

IOEXPANDER 8-11

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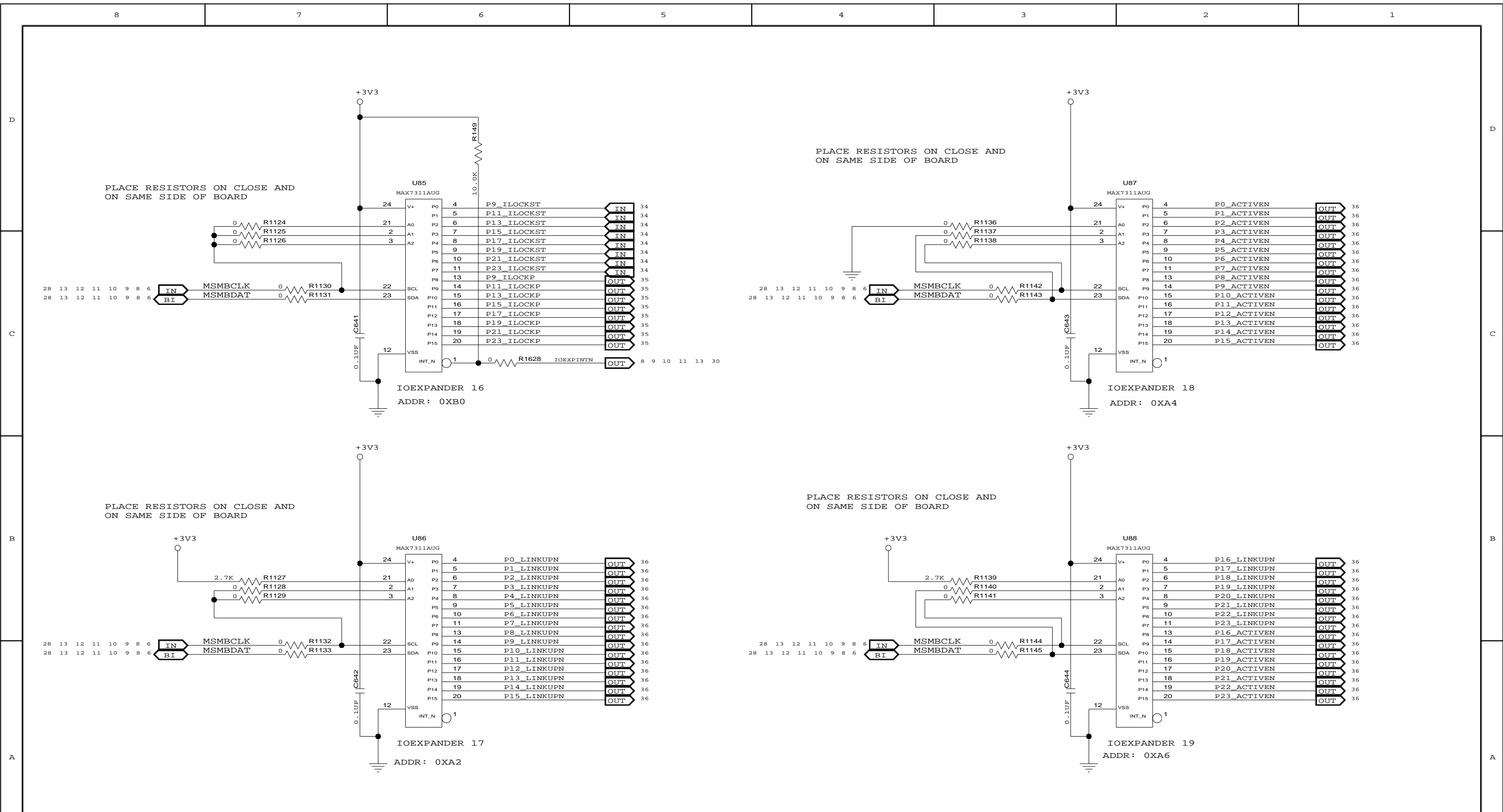
AUTHOR Tony Tran
CHECKED BY Derek Huang


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TITLE EB-LOGAN-19			
IOEXPANDER 12-15			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:45 2010			SHEET 11 OF 41



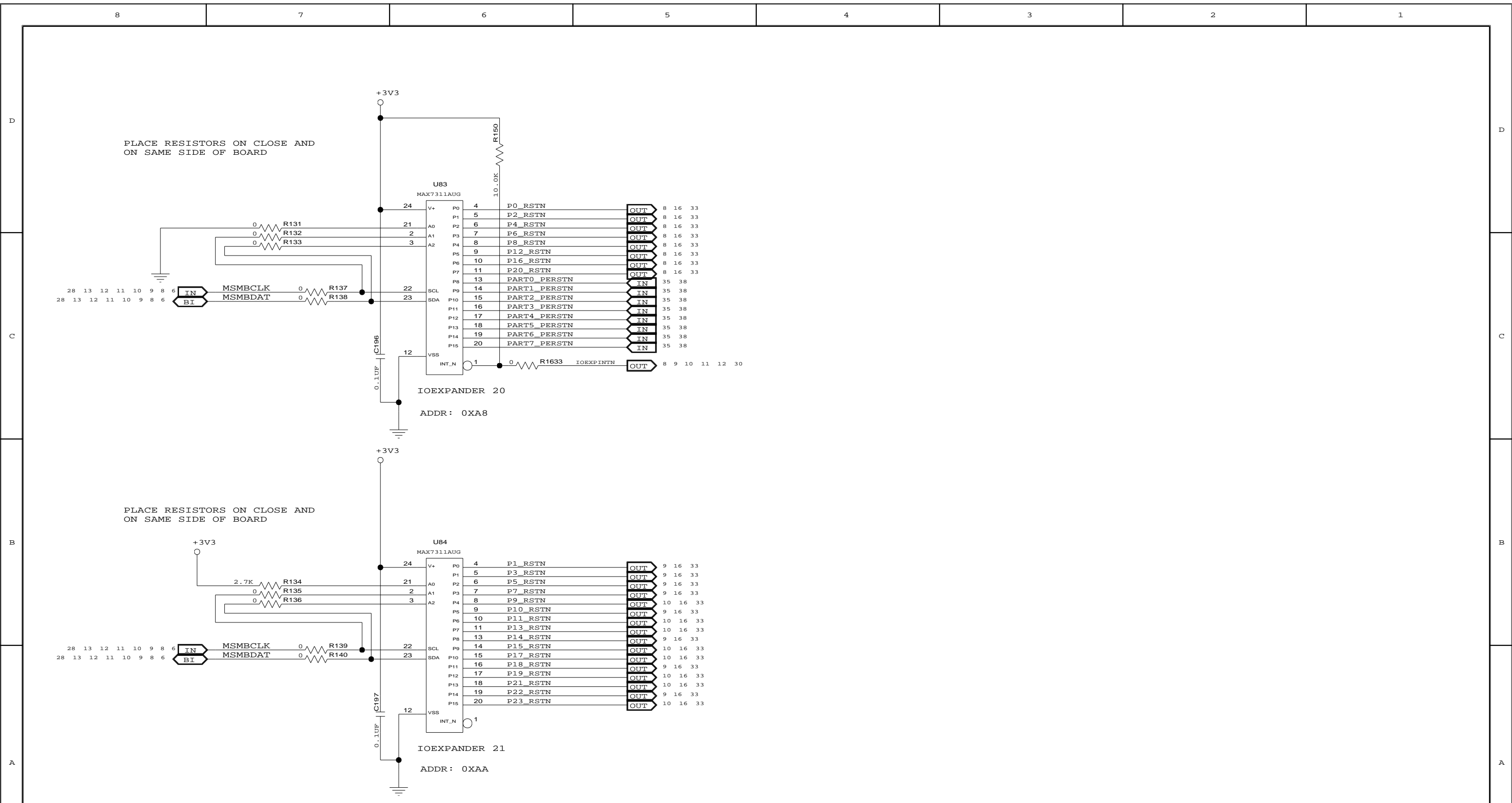


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TITLE EB-LOGAN-19

IOEXPANDER 16-19

SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:46 2010			SHEET 12 OF 41

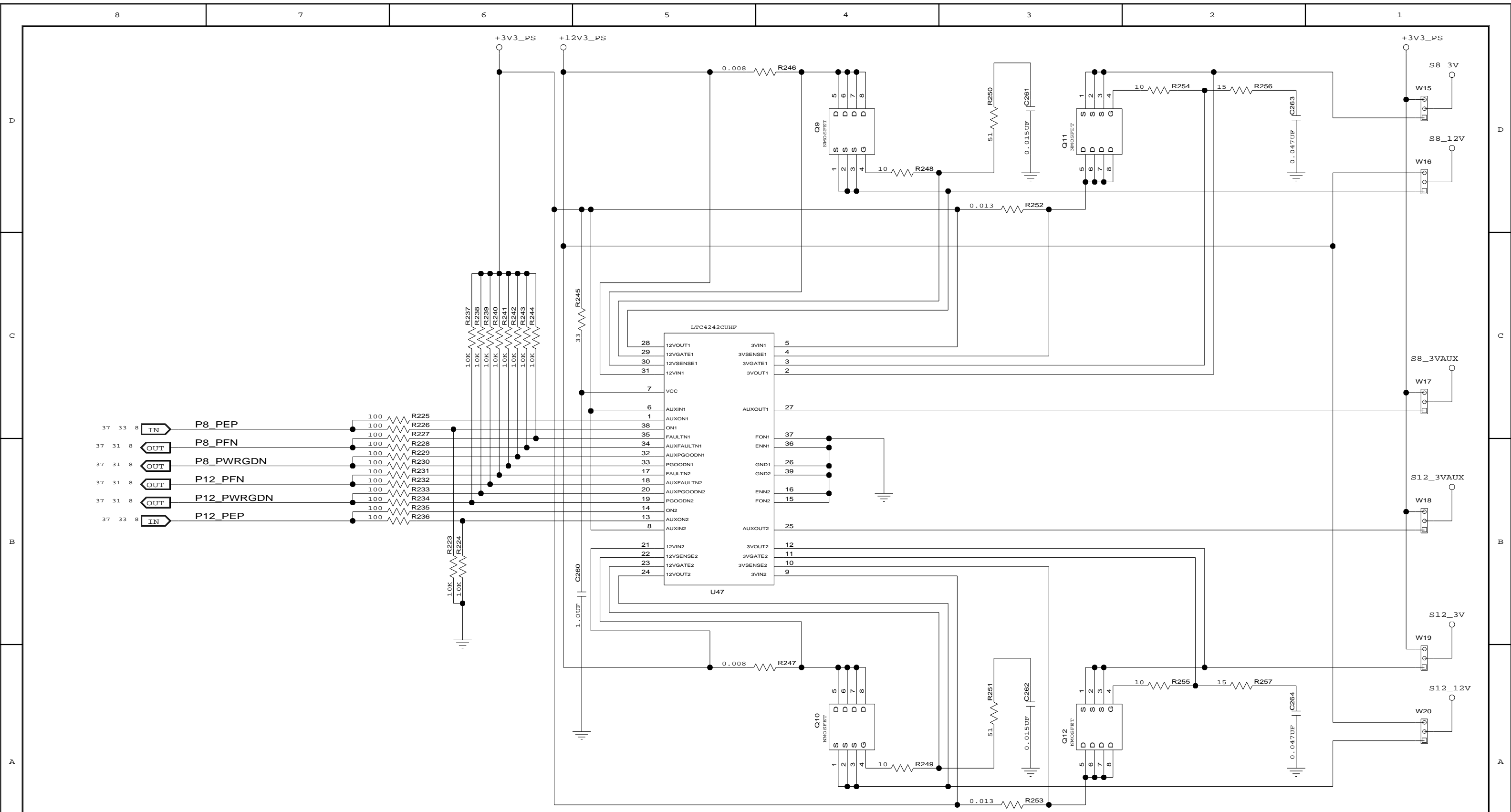



TITLE EB-LOGAN-19

IOEXPANDER 20-21

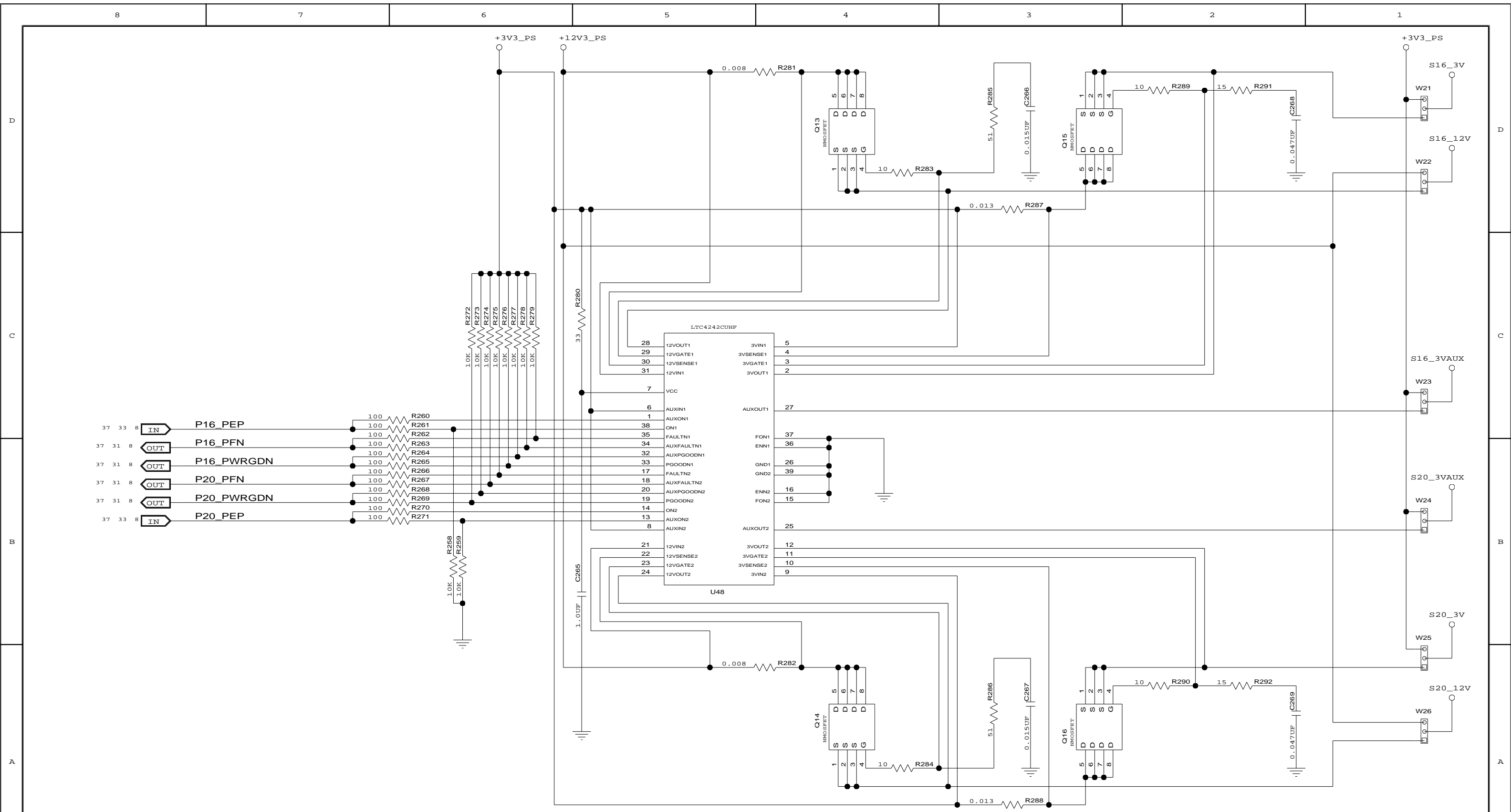

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
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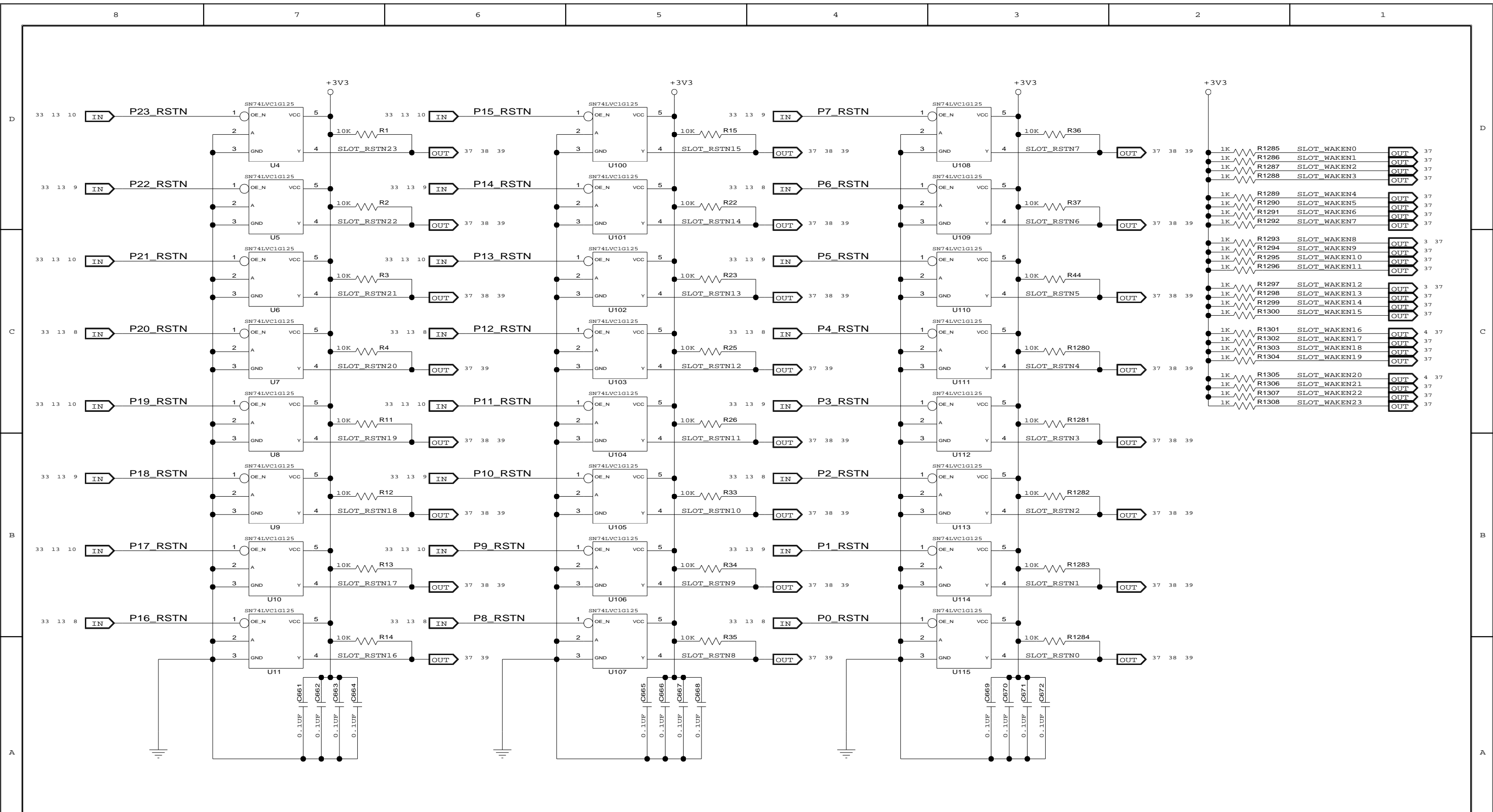
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TITLE EB-LOGAN-19			
HOT PLUG CONTROL PORTS 8-12			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
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TITLE EB-LOGAN-19			
HOT PLUG CONTROL PORTS 16-20			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:47 2010			SHEET 15 OF 41



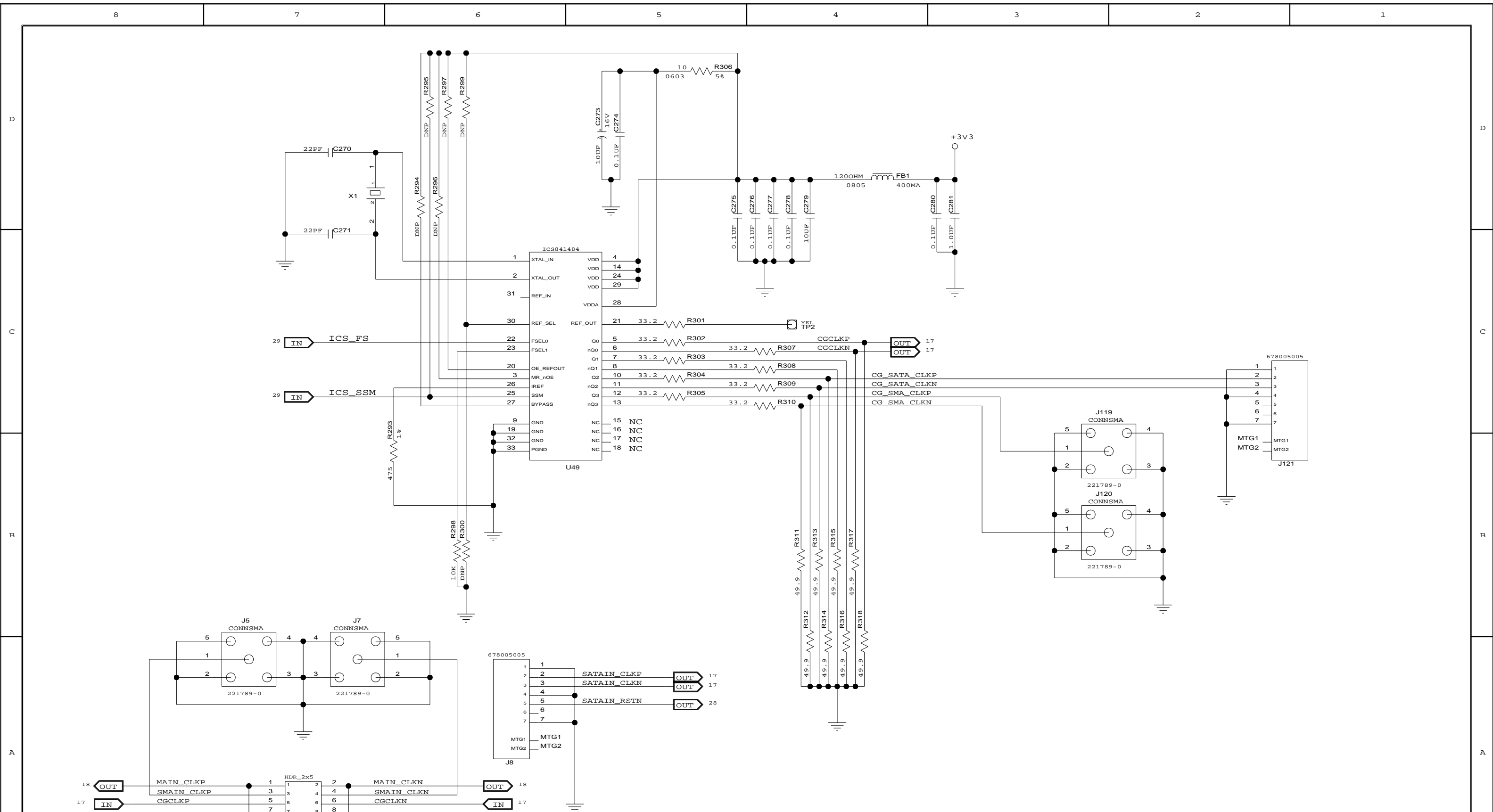



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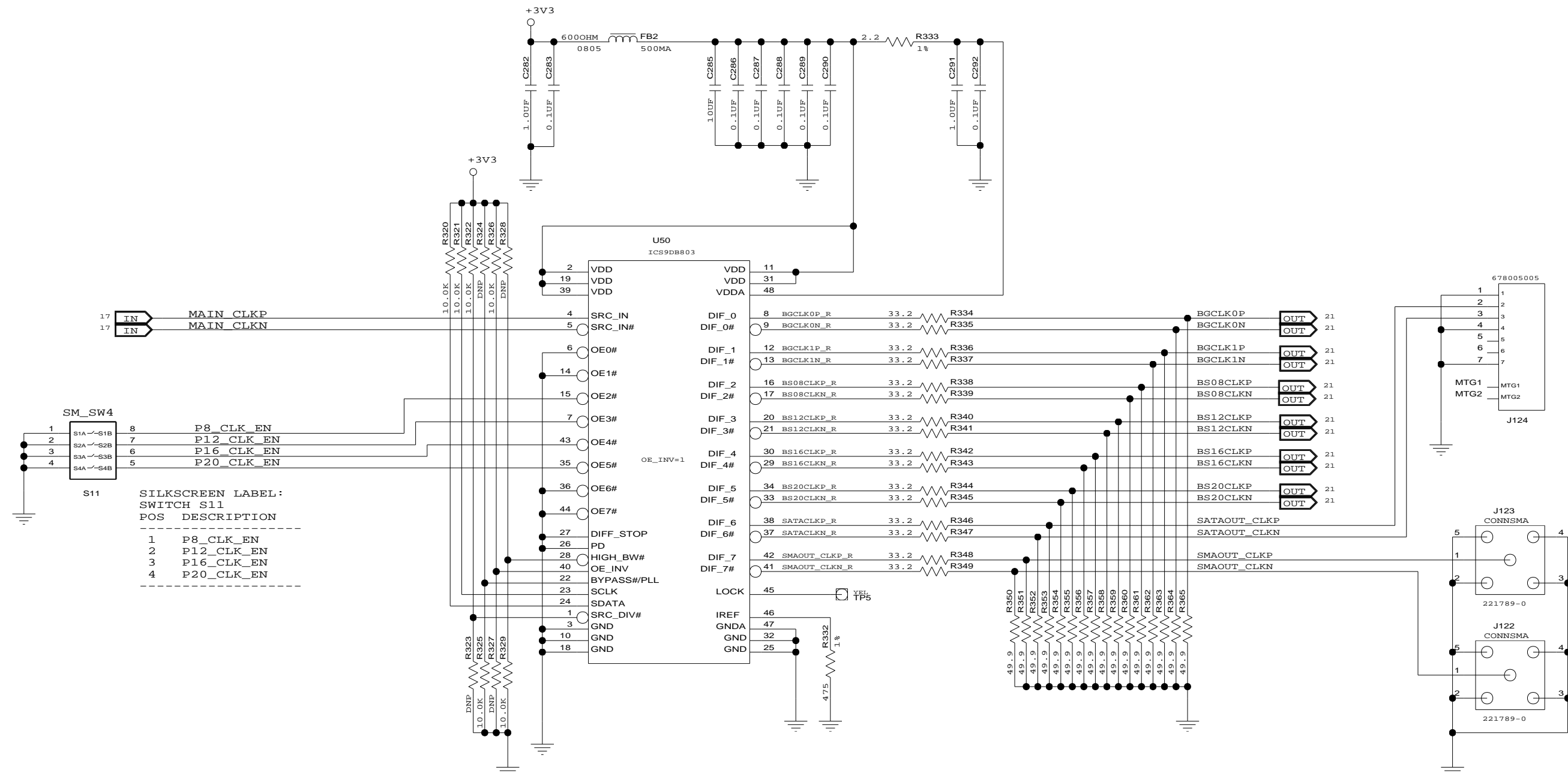
TITLE EB-LOGAN-19

SLOT RESETS AND WAKE PULL-UPS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
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Tony Tran		Derek Huang	
Thu Jun 10 11:24:47 2010			SHEET 16 OF 41




		TITLE EB-LOGAN-19	
		CLOCK	
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
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		SHEET 17 OF 41	



SILKSCREEN LABEL:
SWITCH S11
POS DESCRIPTION

POS	DESCRIPTION
1	P8_CLK_EN
2	P12_CLK_EN
3	P16_CLK_EN
4	P20_CLK_EN



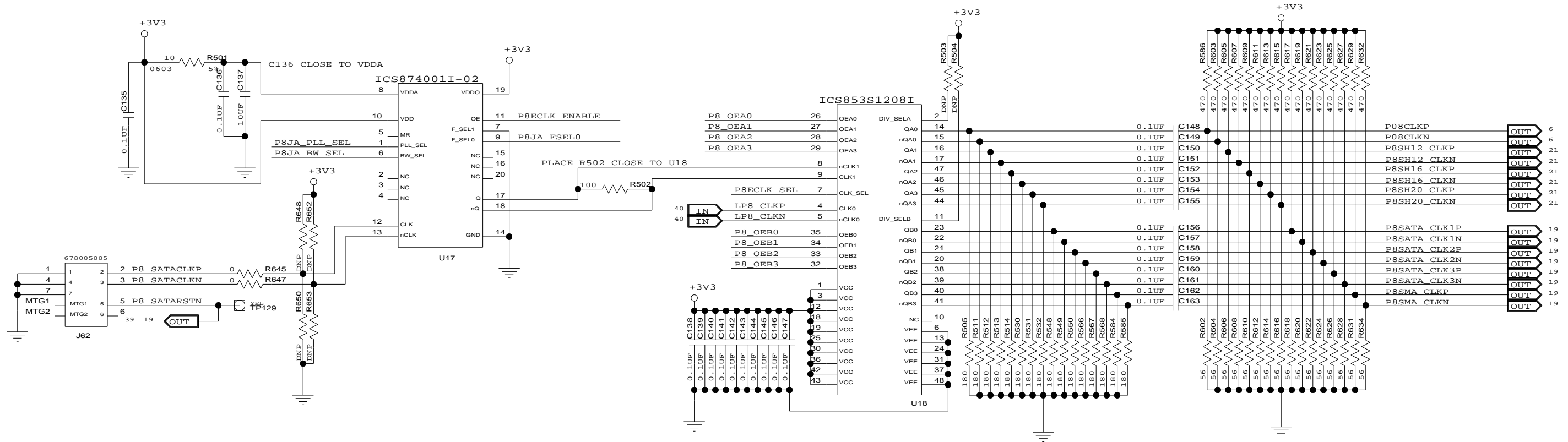
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TITLE EB-LOGAN-19

CLOCK BUFFER

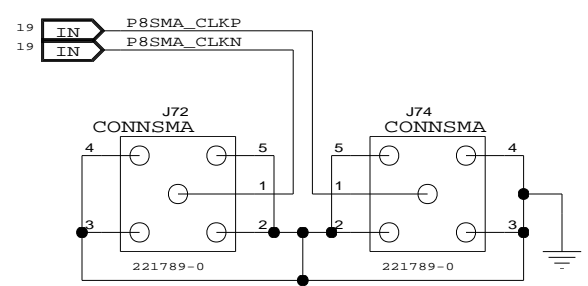
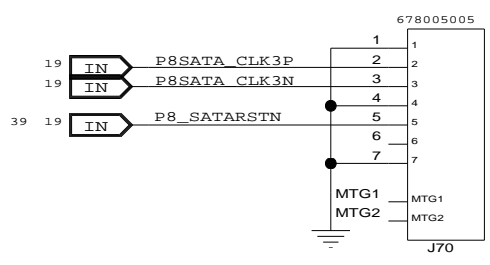
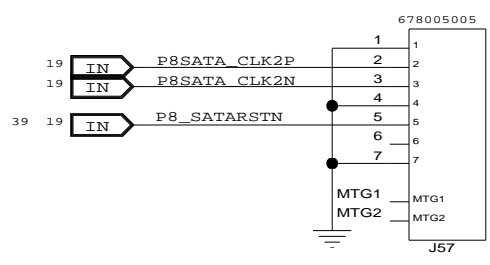
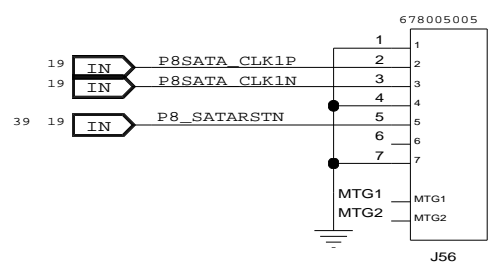
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:48 2010			SHEET 18 OF 41

P8CLK - DUT PORT 8 CLK
 LP8CLK - LOCAL CLOCK GEN. PORT 8 CLK
 P8SHXCLK - TO SLOT CLK HEADERS

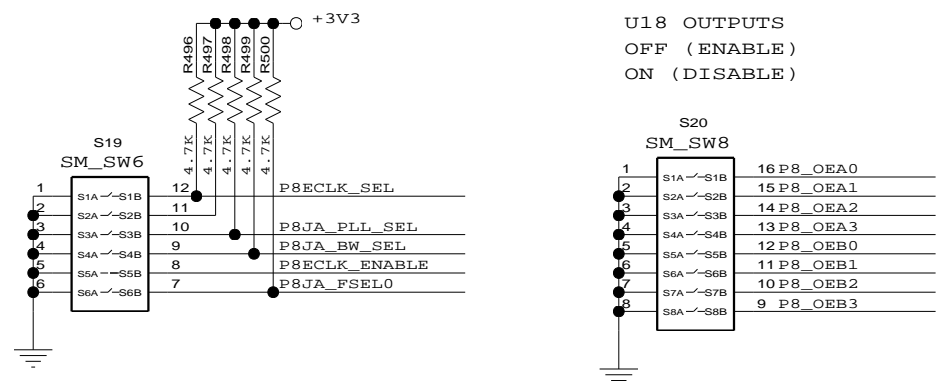


DEFAULT DIPSW SETTING

- S19:1 OFF (SATACLK)
- S19:3 OFF (PLL)
- S19:4 OFF (2.2MHZ)
- S19:5 OFF (U15 OUT ON)
- S19:6 ON (100MHZ)



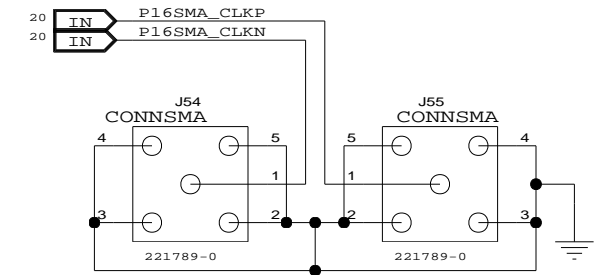
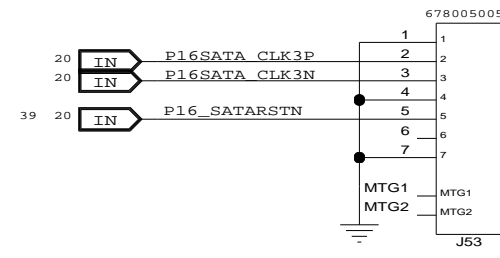
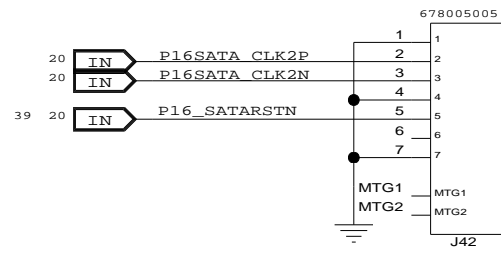
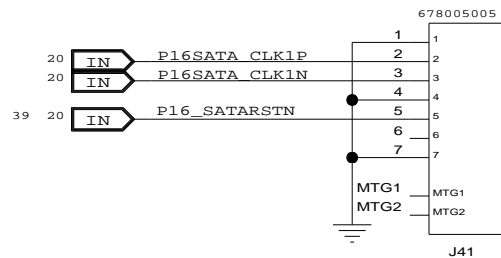
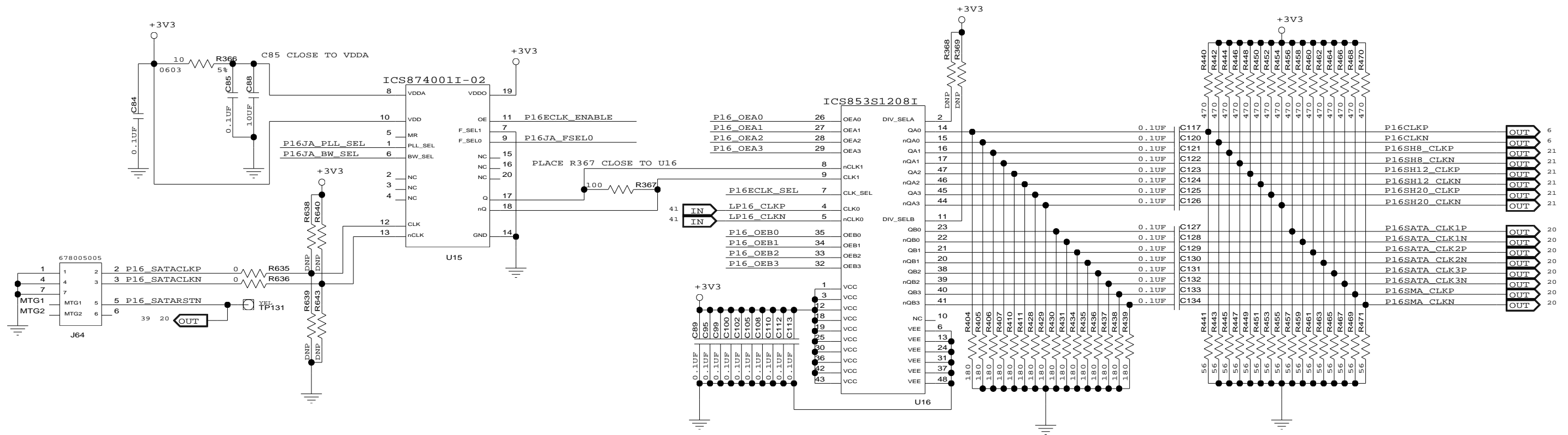
U18 OUTPUTS
 OFF (ENABLE)
 ON (DISABLE)



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TITLE EB-LOGAN-19			
CLOCK SELECTOR DUT PCLK 8			
SIZE	DRAWING NO.	FAB P/N	REV.
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AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:28:22 2010			SHEET 19 OF 41

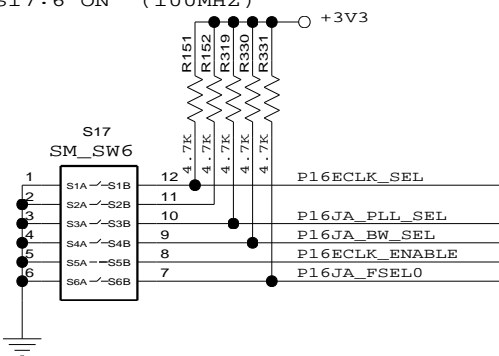
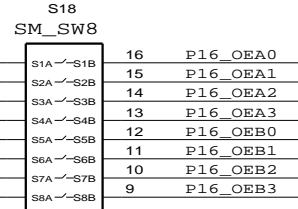
P16CLK - DUT PORT 16 CLK
 LP16CLK - LOCAL CLOCK GEN. PORT 16 CLK
 P16SHXCLK - TO SLOT CLK HEADERS



DEFAULT DIPSW SETTING

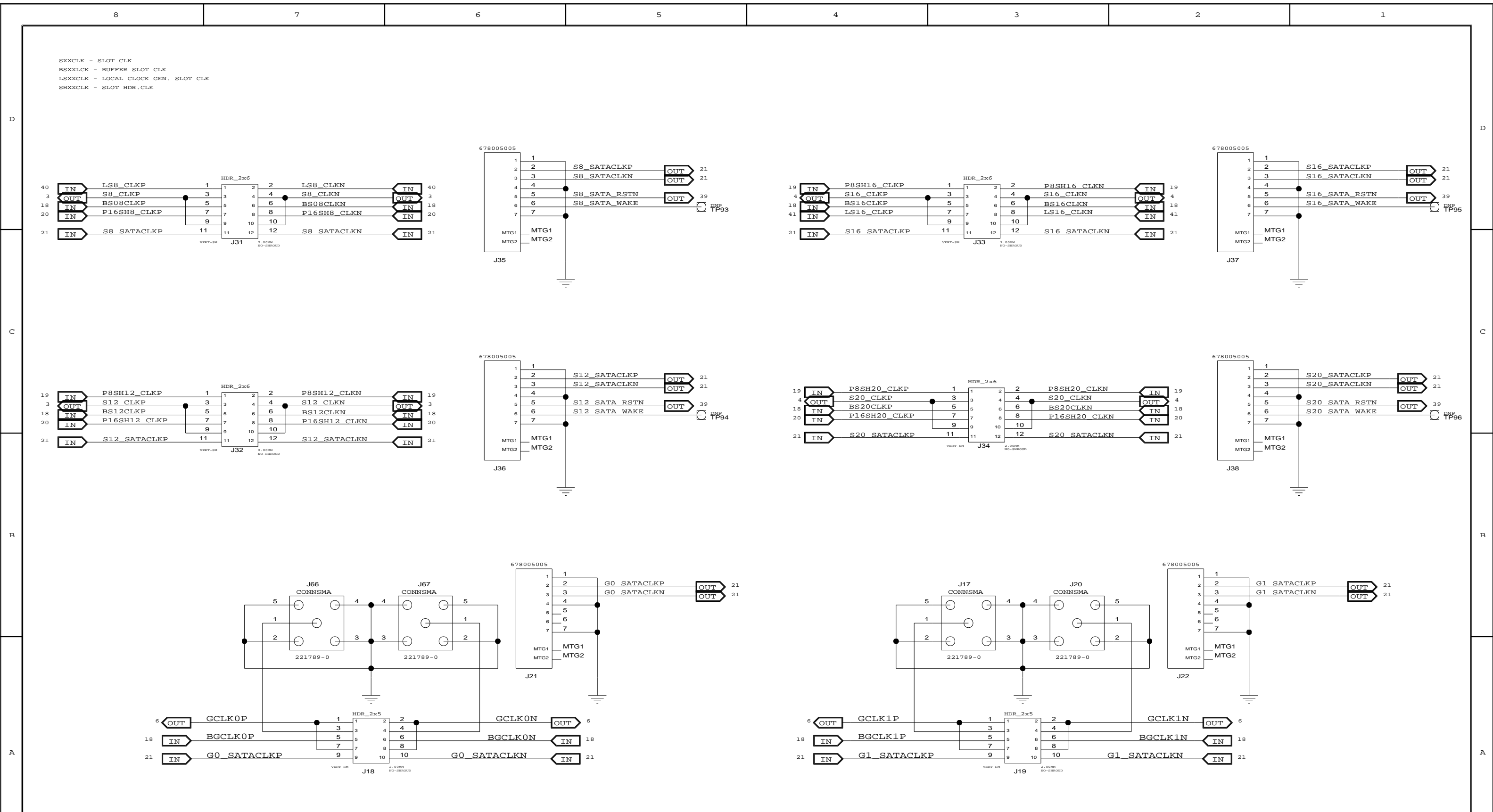
- S17:1 OFF (SATACLK)
- S17:3 OFF (PLL)
- S17:4 OFF (2.2MHZ)
- S17:5 OFF (U15 OUT ON)
- S17:6 ON (100MHZ)


U16 OUTPUTS
 OFF (ENABLE)
 ON (DISABLE)



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TITLE EB-LOGAN-19			
CLOCK SELECTOR DUT PCLK 16			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:28:19 2010			SHEET 20 OF 41





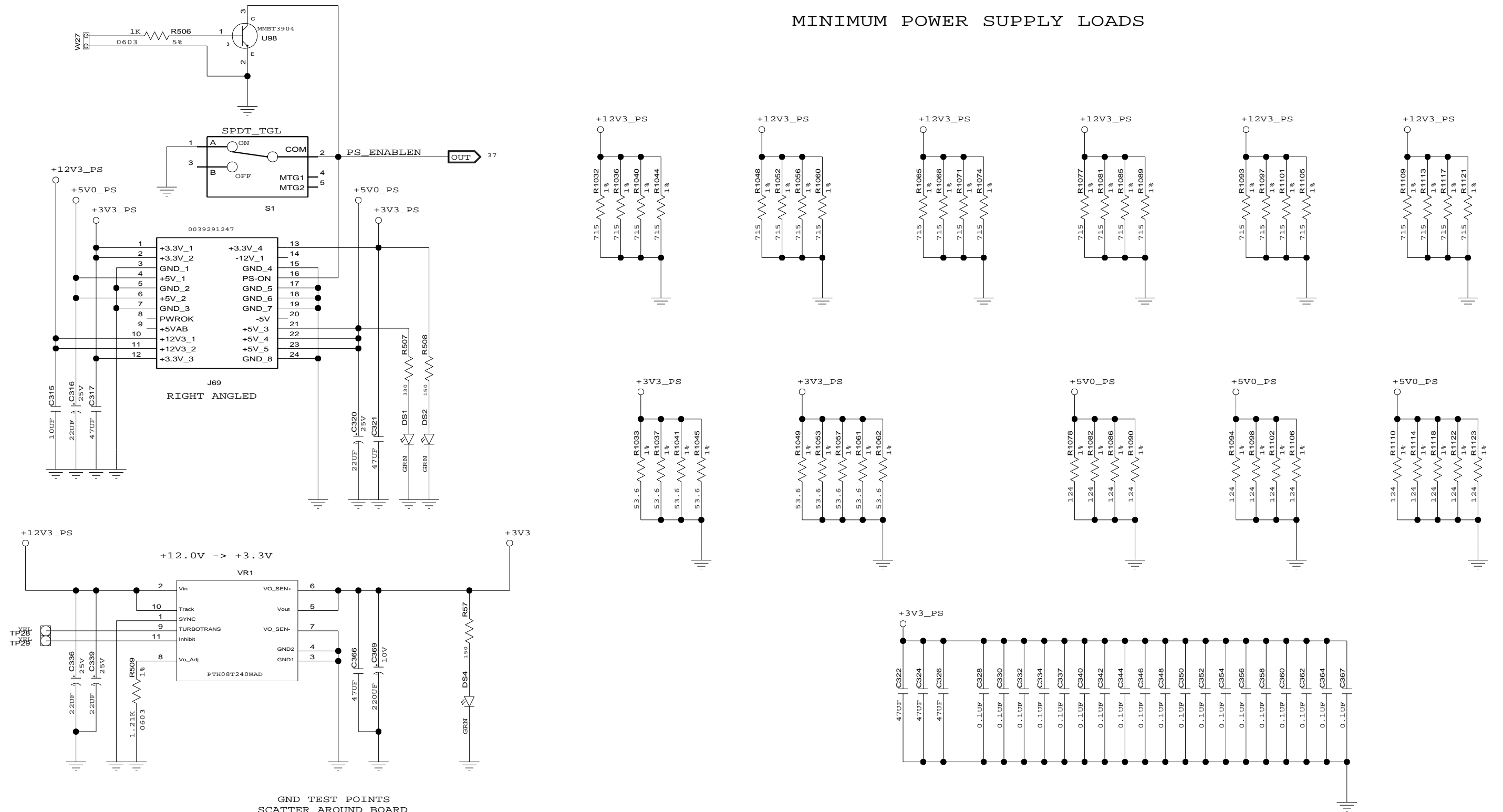
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TITLE EB-LOGAN-19

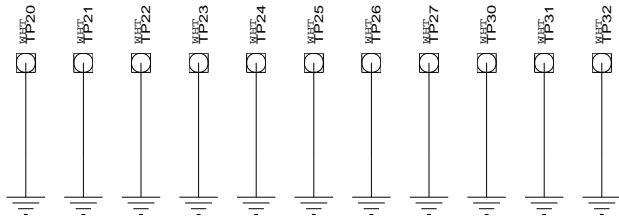
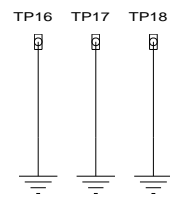
CLOCK SELECTOR SLOTS 8-20, GCLK

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:49 2010			SHEET 21 OF 41

MINIMUM POWER SUPPLY LOADS

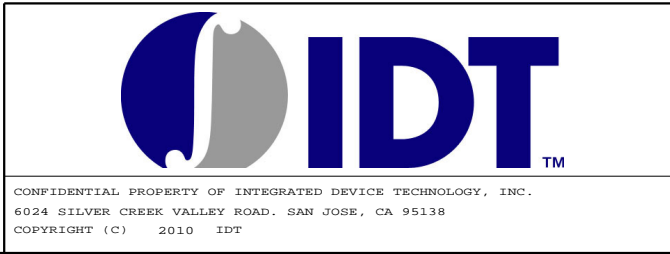
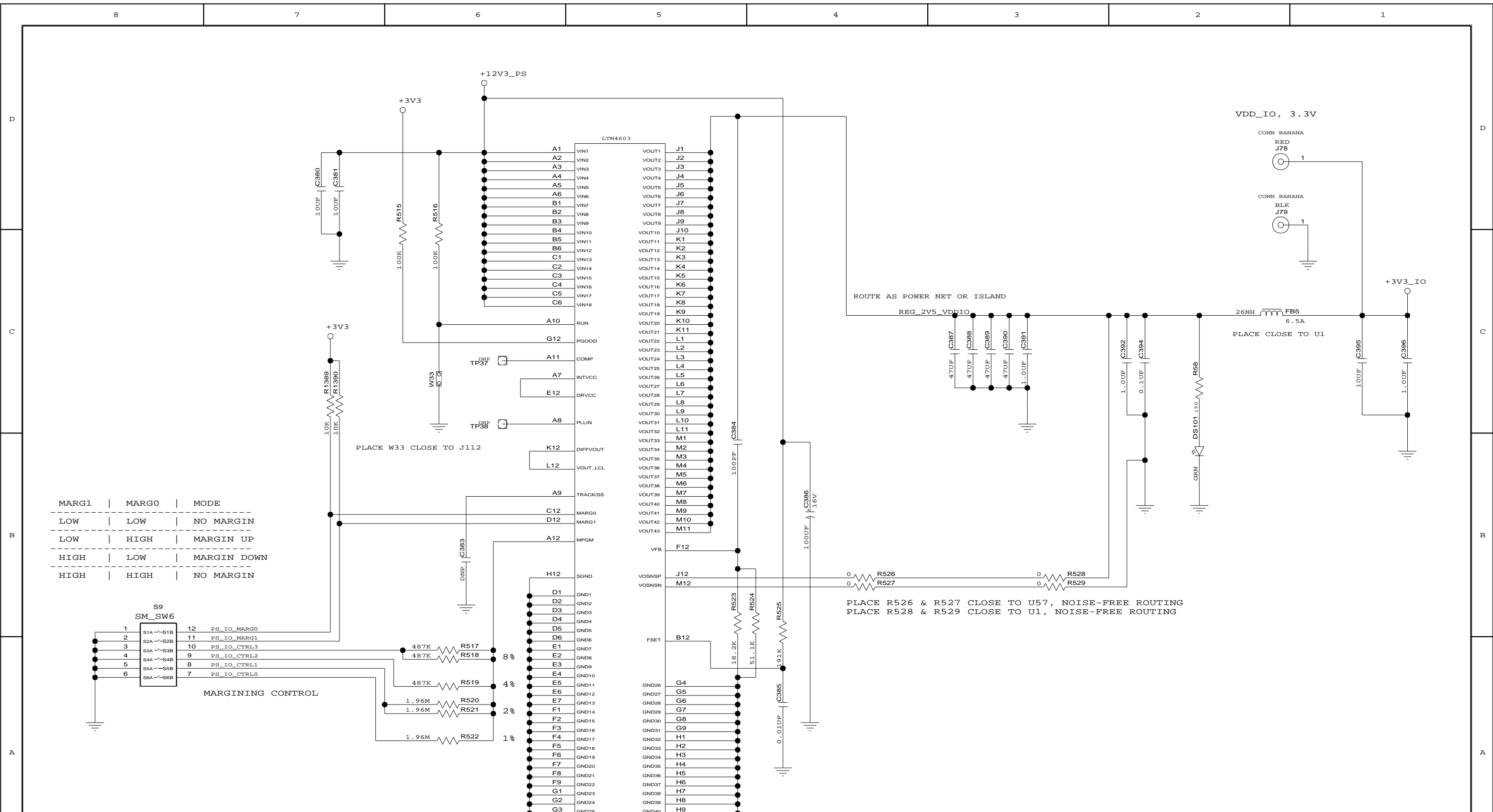


GND TEST POINTS
SCATTER AROUND BOARD

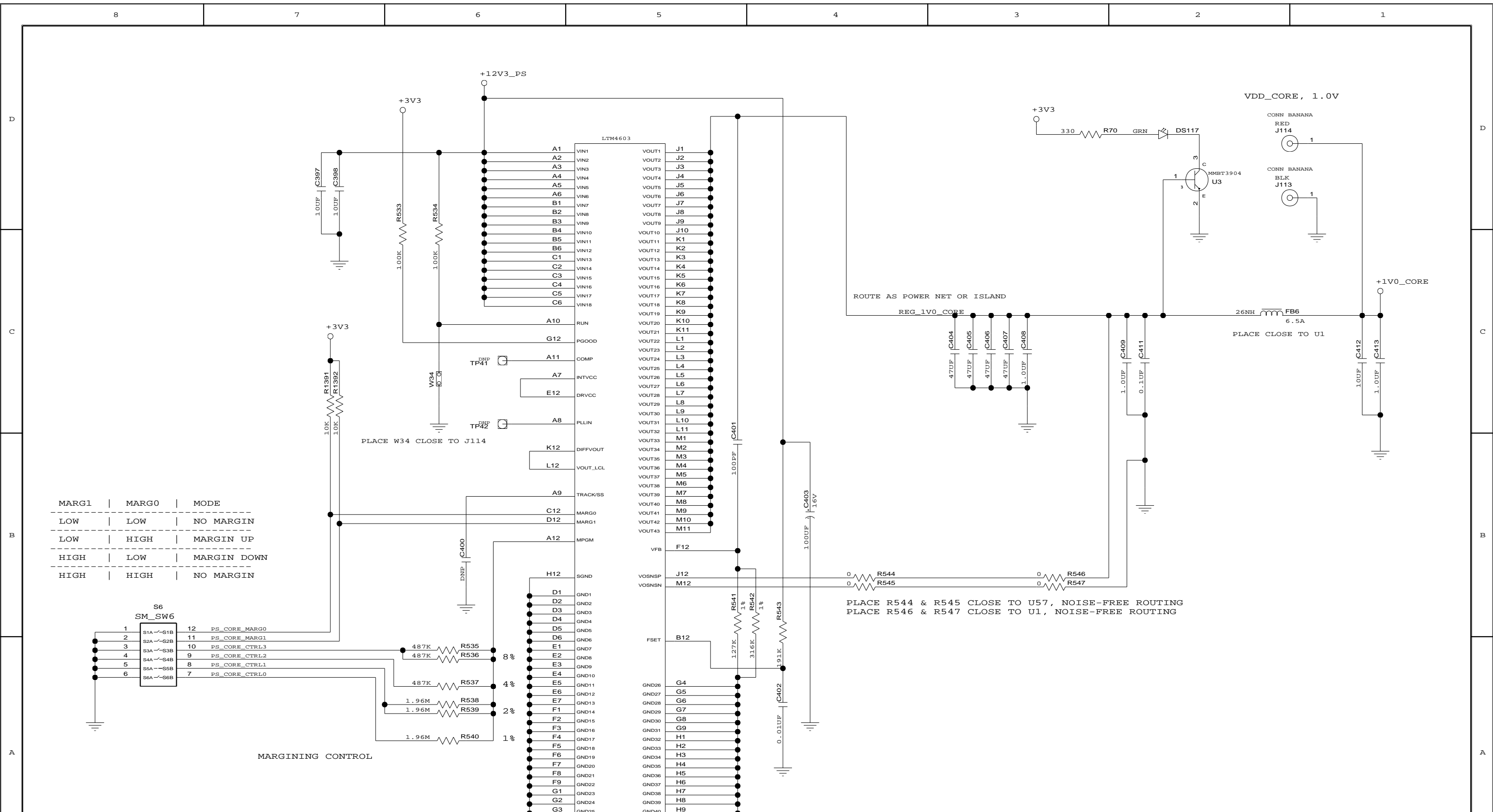


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TITLE EB-LOGAN-19			
POWER CONNECTORS, MIN LOAD RESISTORS			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:50 2010			SHEET 22 OF 41



TITLE EB-LOGAN-19			
POWER REGULATOR - VDDIO			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:50 2010			SHEET 23 OF 41



MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

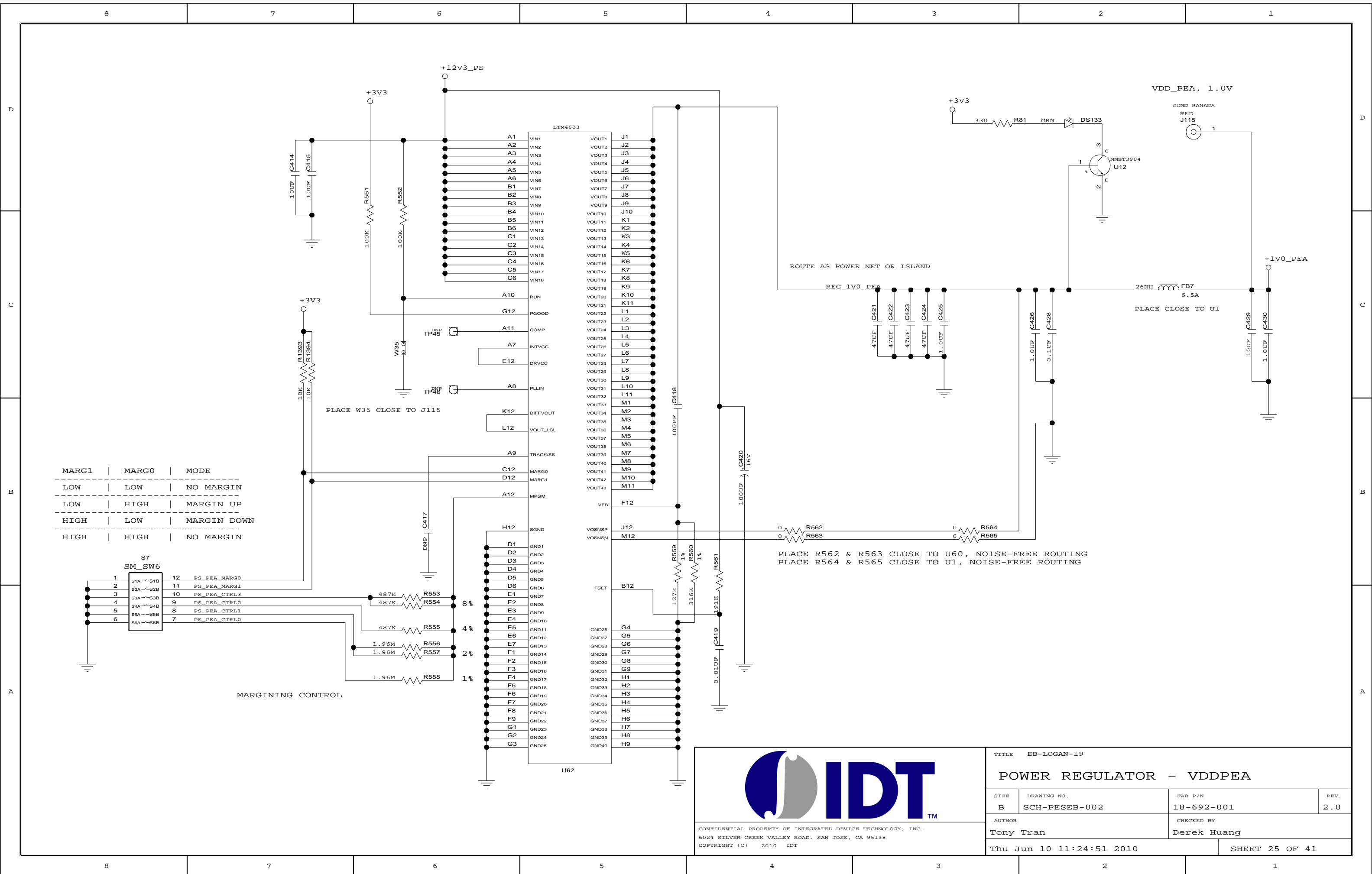
S6 SM_SW6	
1	S1A~S1B
2	S2A~S2B
3	S3A~S3B
4	S4A~S4B
5	S5A~S5B
6	S6A~S6B

MARGINING CONTROL

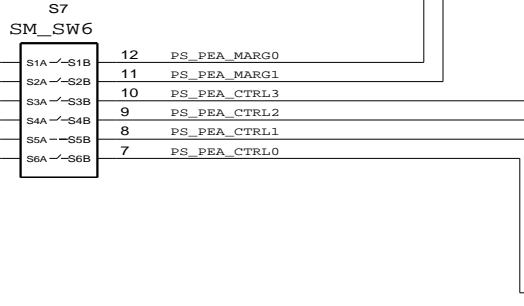
LTM4603	
A1	VIN1
A2	VIN2
A3	VIN3
A4	VIN4
A5	VIN5
A6	VIN6
B1	VIN7
B2	VIN8
B3	VIN9
B4	VIN10
B5	VIN11
B6	VIN12
C1	VIN13
C2	VIN14
C3	VIN15
C4	VIN16
C5	VIN17
C6	VIN18
A10	RUN
G12	PGOOD
A11	COMP
A7	INTVCC
E12	DRVCC
A8	PLLIN
K12	DIFFVOUT
L12	VOUT_LCL
A9	TRACK/SS
C12	MARG0
D12	MARG1
A12	MPGM
H12	SGND
D1	GND1
D2	GND2
D3	GND3
D4	GND4
D5	GND5
D6	GND6
E1	GND7
E2	GND8
E3	GND9
E4	GND10
E5	GND11
E6	GND12
E7	GND13
F1	GND14
F2	GND15
F3	GND16
F4	GND17
F5	GND18
F6	GND19
F7	GND20
F8	GND21
F9	GND22
G1	GND23
G2	GND24
G3	GND25

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TITLE EB-LOGAN-19			
POWER REGULATOR - VDDCORE			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:51 2010			SHEET 24 OF 41

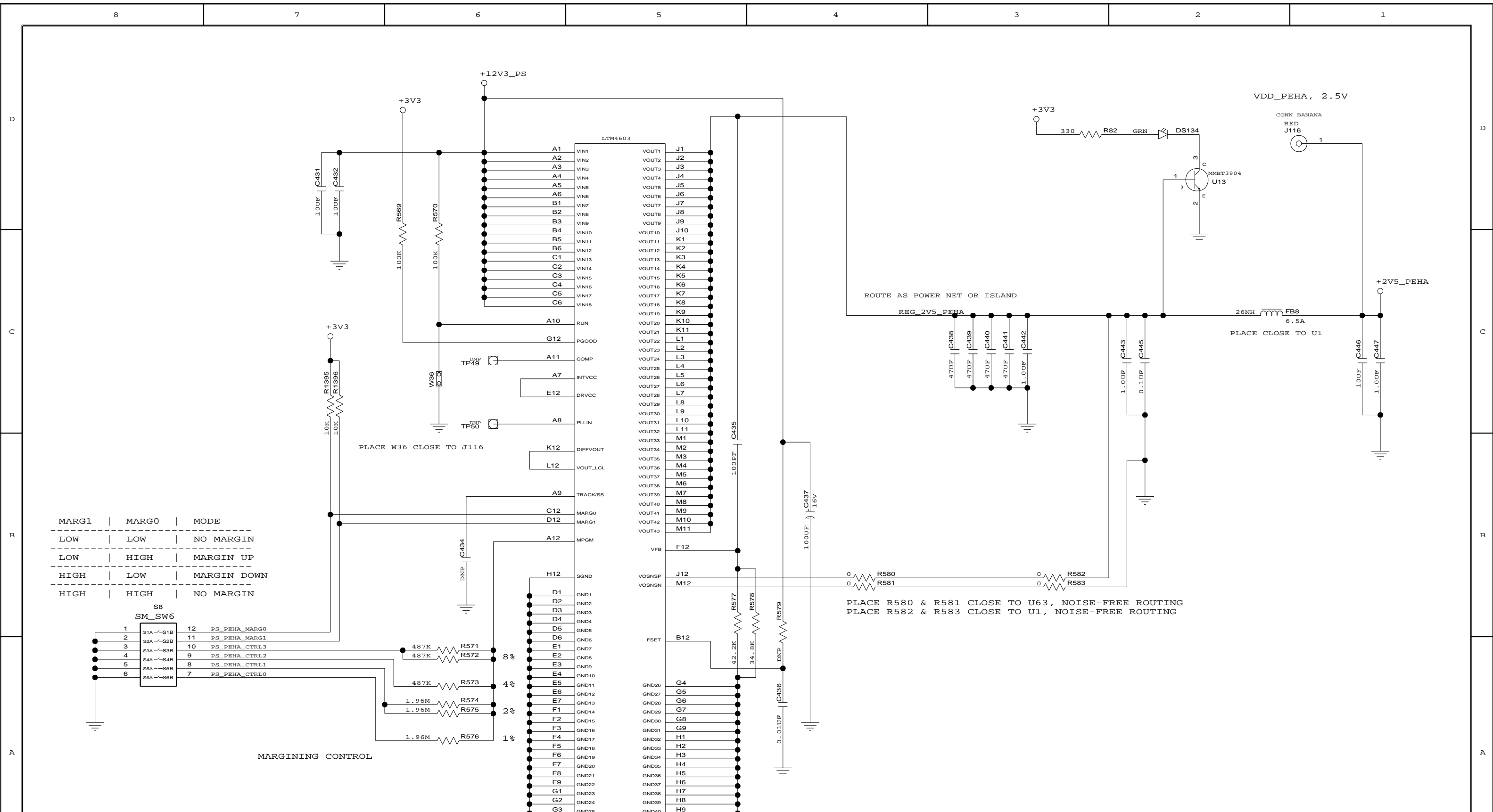


MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN



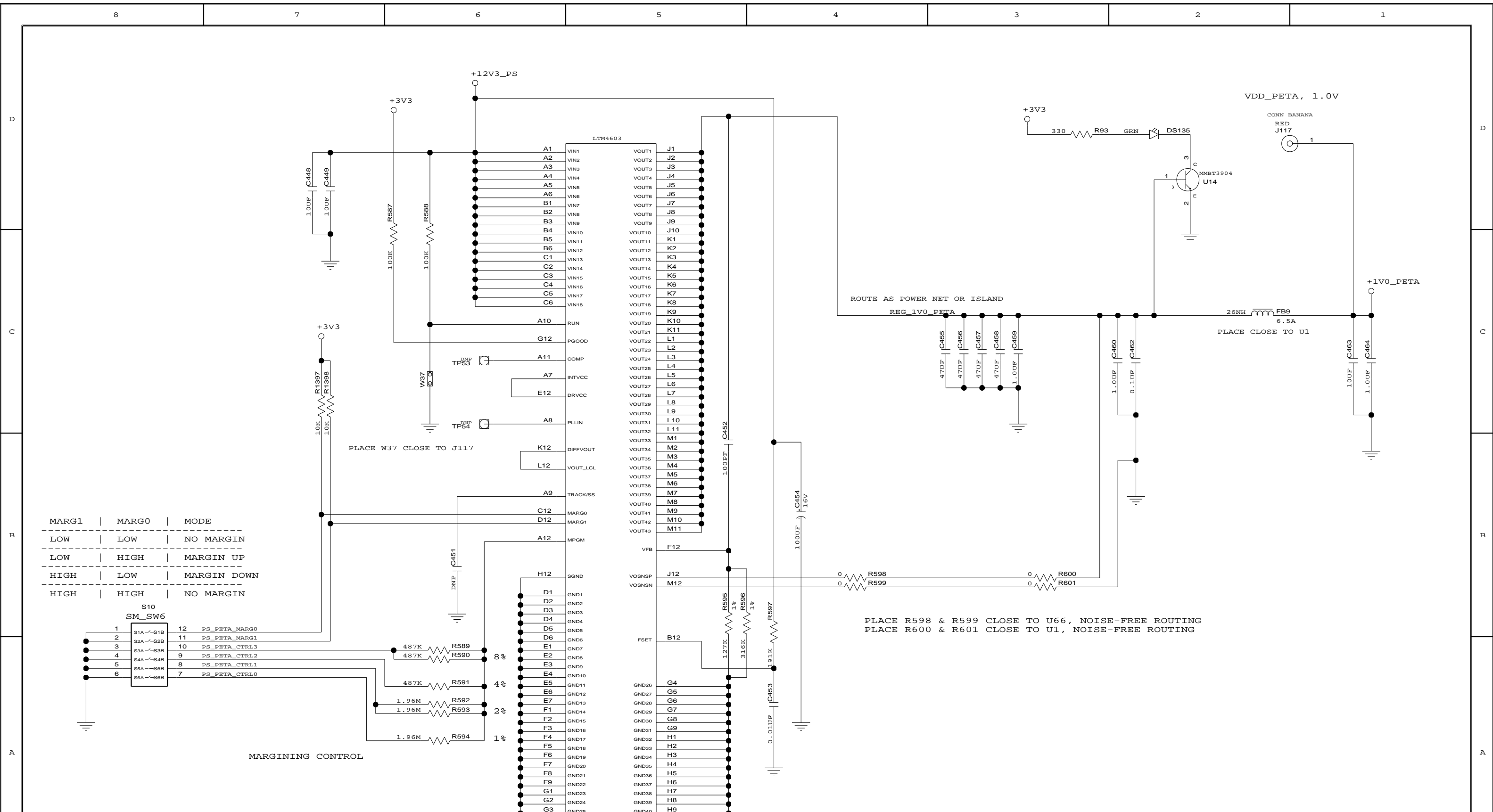
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TITLE EB-LOGAN-19			
POWER REGULATOR - VDDPEA			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:51 2010			SHEET 25 OF 41



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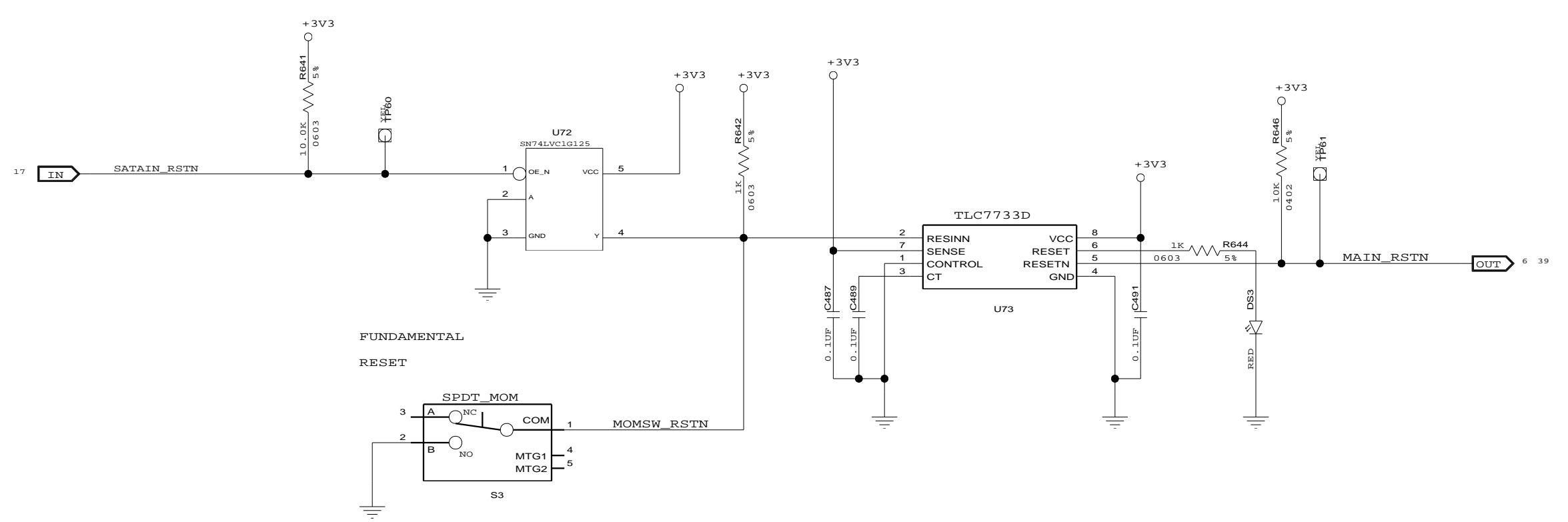
TITLE EB-LOGAN-19			
POWER REGULATOR - VDDPEHA			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:51 2010			SHEET 26 OF 41



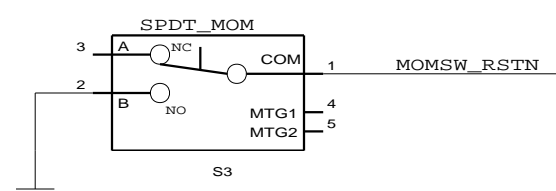


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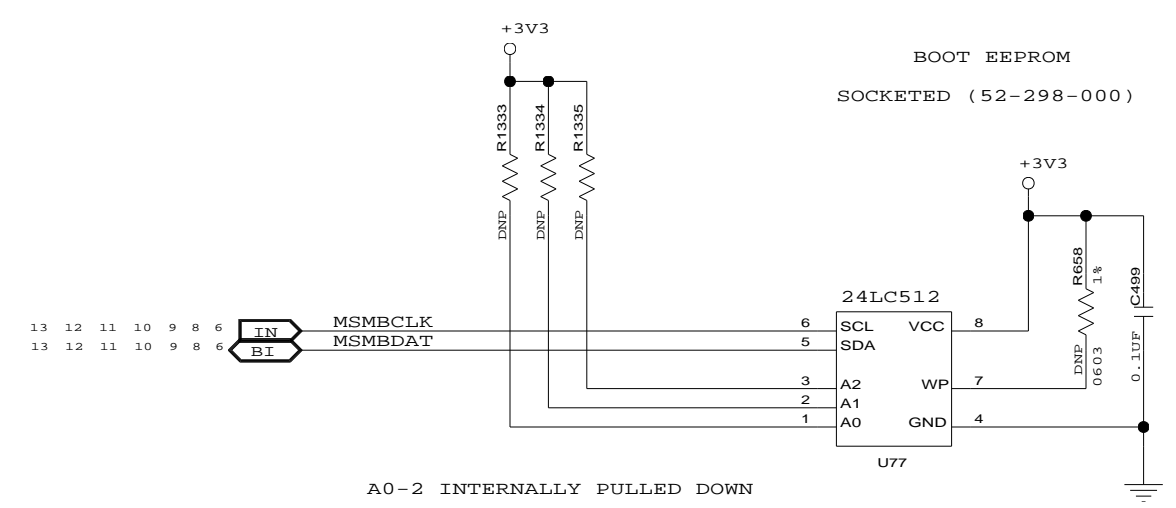
TITLE EB-LOGAN-19			
POWER REGULATOR - VDDPETA			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:52 2010			SHEET 27 OF 41



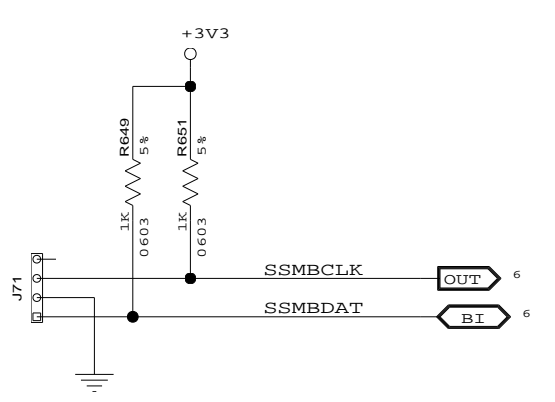
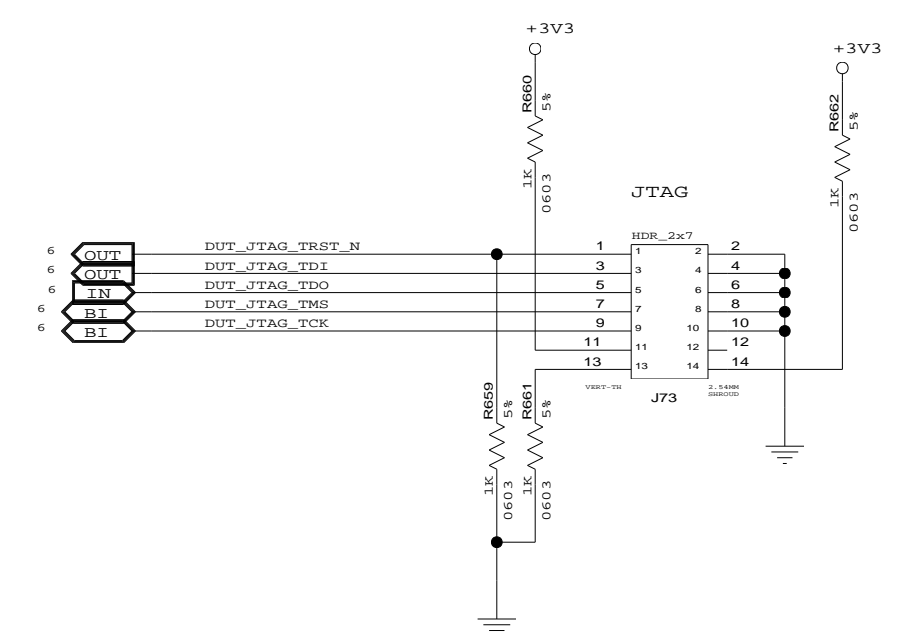
FUNDAMENTAL
RESET



BOOT EEPROM
SOCKETED (52-298-000)

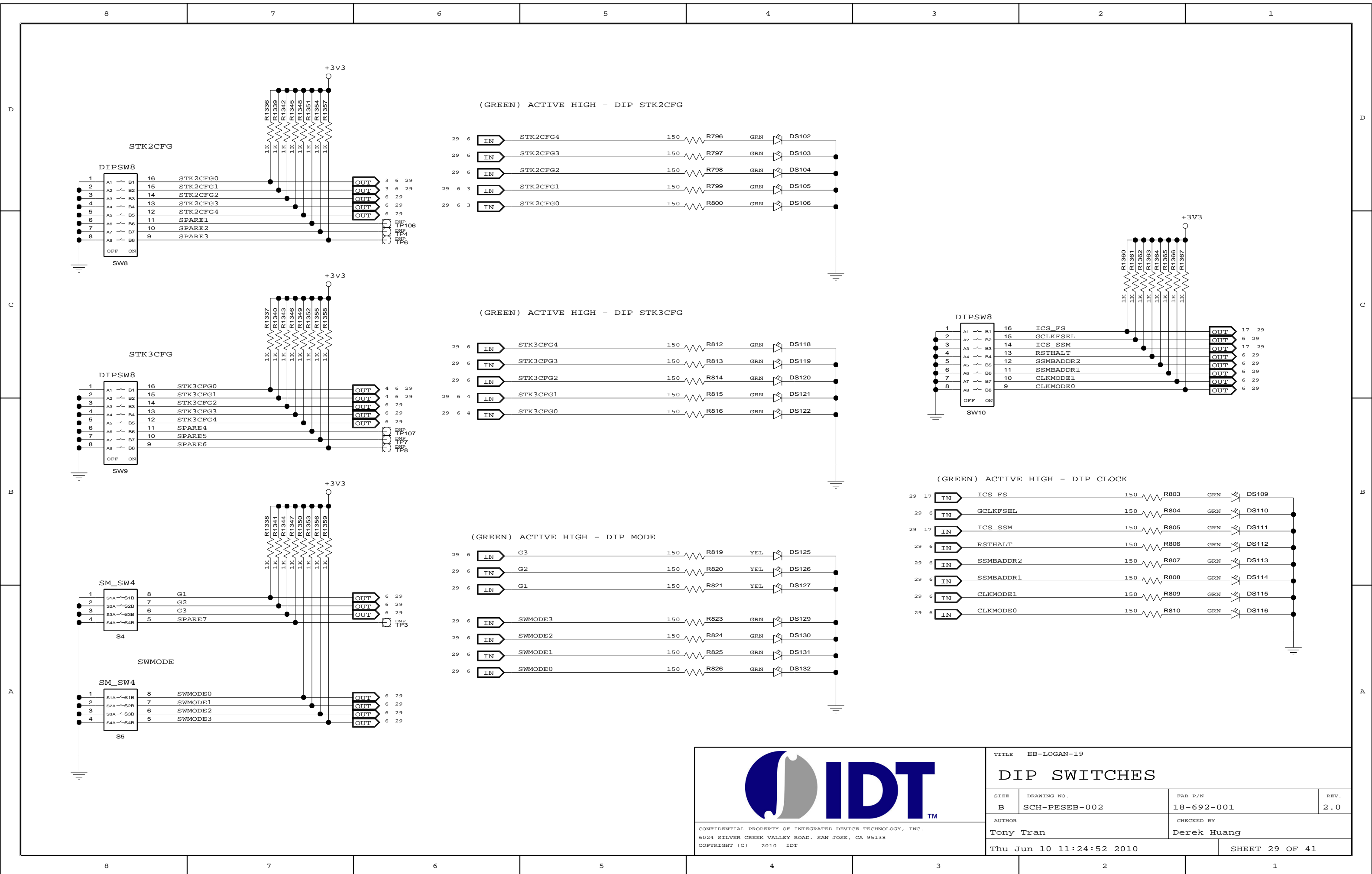



A0-2 INTERNALLY PULLED DOWN



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TITLE EB-LOGAN-19			
RESET, SMBUS, EEPROM, JTAG			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:52 2010			SHEET 28 OF 41



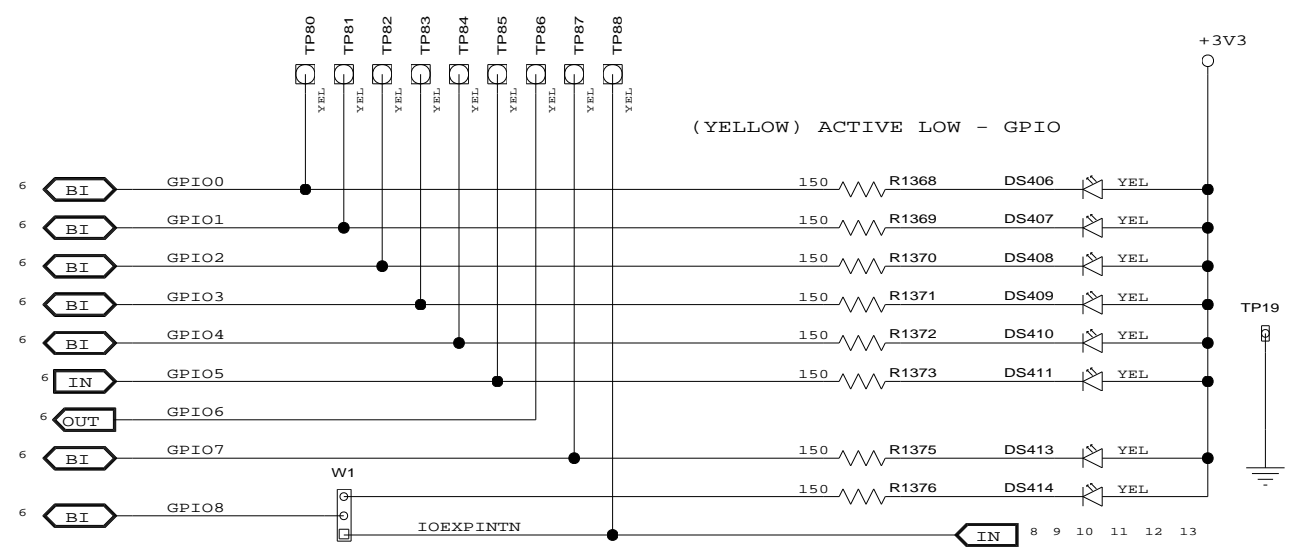


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TITLE EB-LOGAN-19

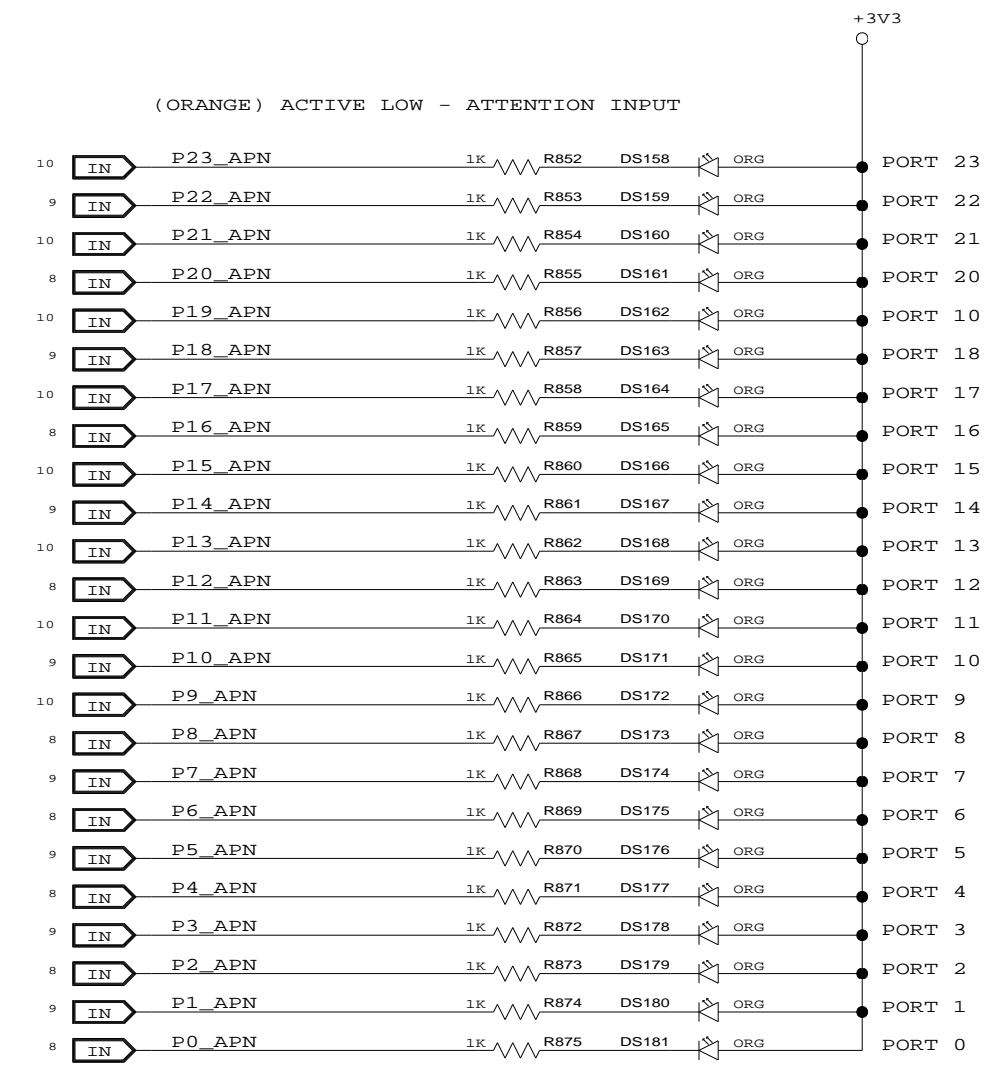
DIP SWITCHES

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:52 2010			SHEET 29 OF 41

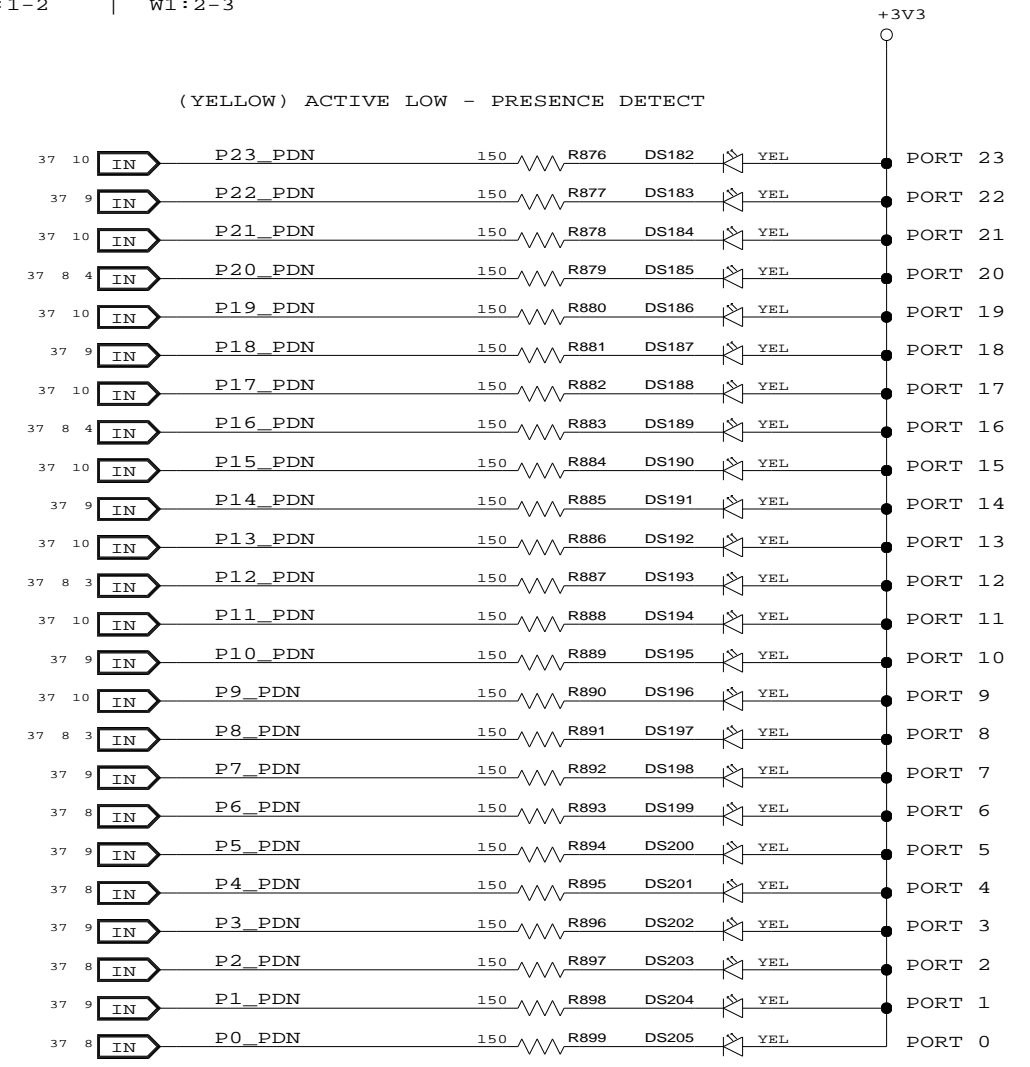


GPIO	ALT0	ALT1
0	PART0PERSTN	P16LINKUPN
1	PART1PERSTN	P16ACTIVEN
2	PART2PERSTN	P4LINKUPN
3	PART3PERSTN	P4ACTIVEN
4	FAILOVER0	P0LINKUPN
5	GPEN	P0ACTIVEN
6	FAILOVER1	FAILOVER3
7	FAILOVER2	P8LINKUPN
8	IOEXPINTN W1:1-2	P8ACTIVEN W1:2-3

(ORANGE) ACTIVE LOW - ATTENTION INPUT



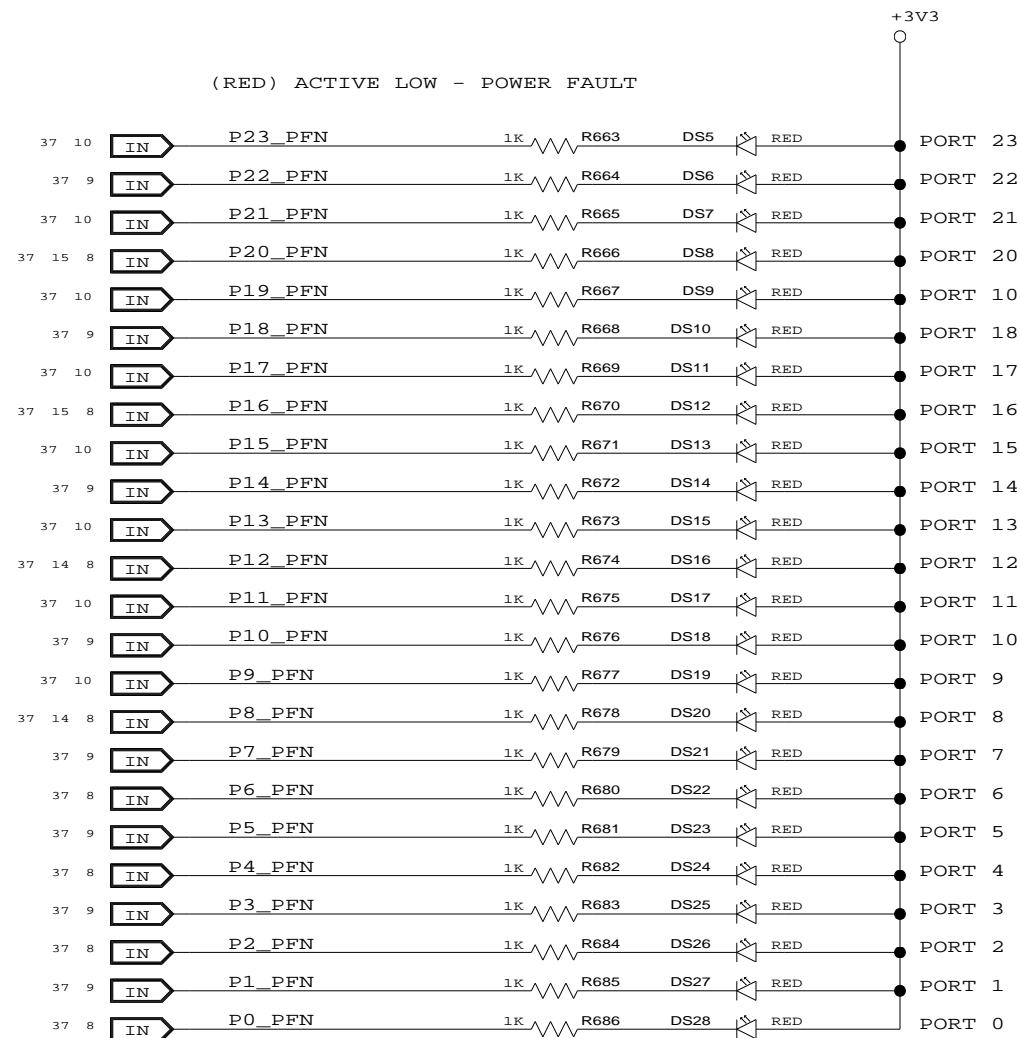
(YELLOW) ACTIVE LOW - PRESENCE DETECT



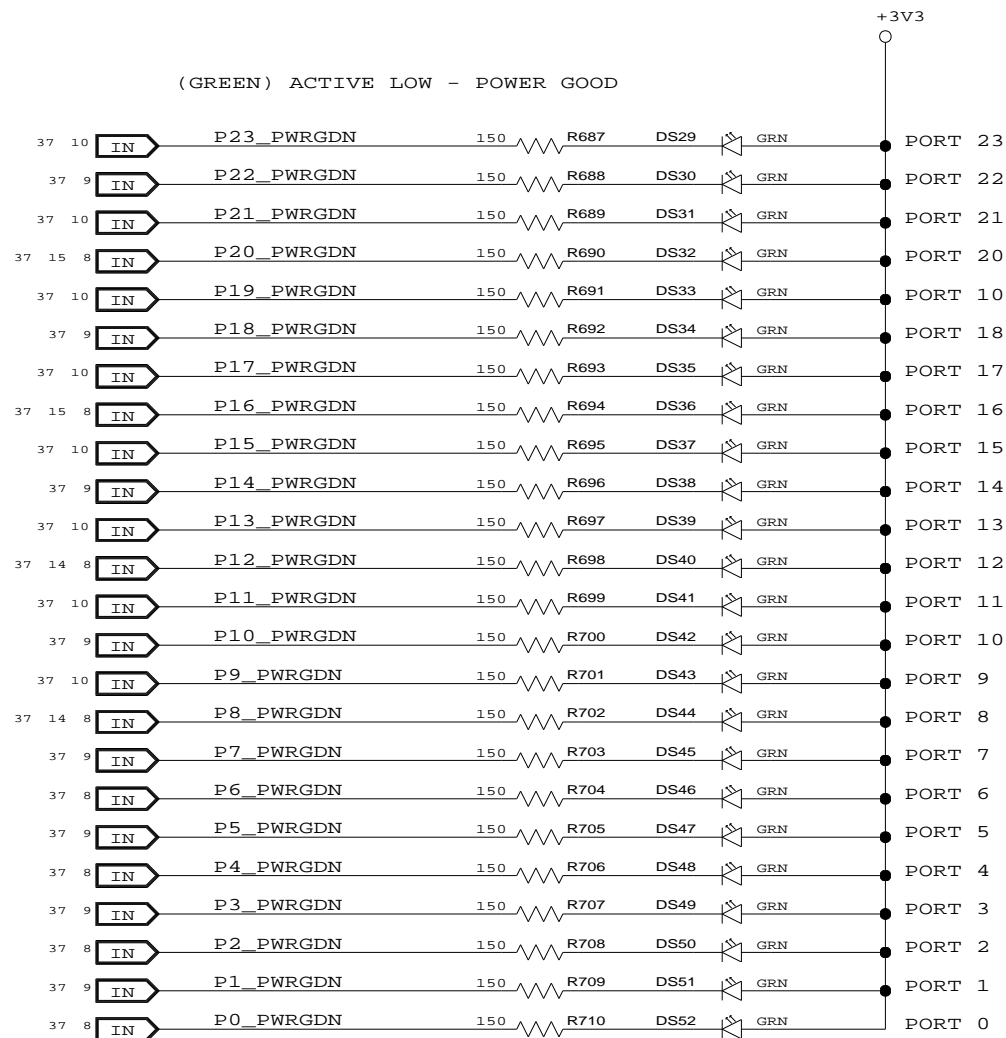
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TITLE EB-LOGAN-19			
LED - PORT STATUS (1 OF 7)			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:53 2010			SHEET 30 OF 41

(RED) ACTIVE LOW - POWER FAULT



(GREEN) ACTIVE LOW - POWER GOOD



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TITLE EB-LOGAN-19

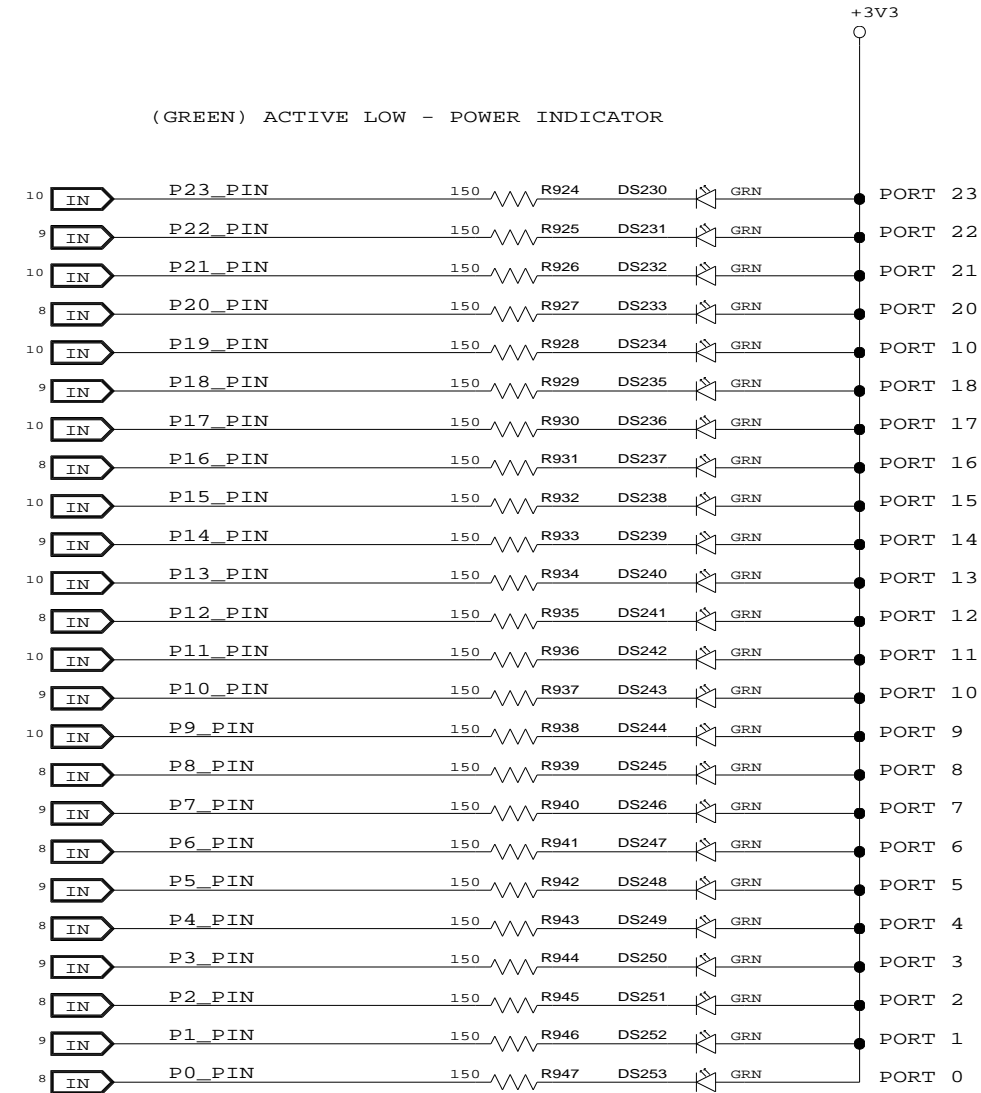
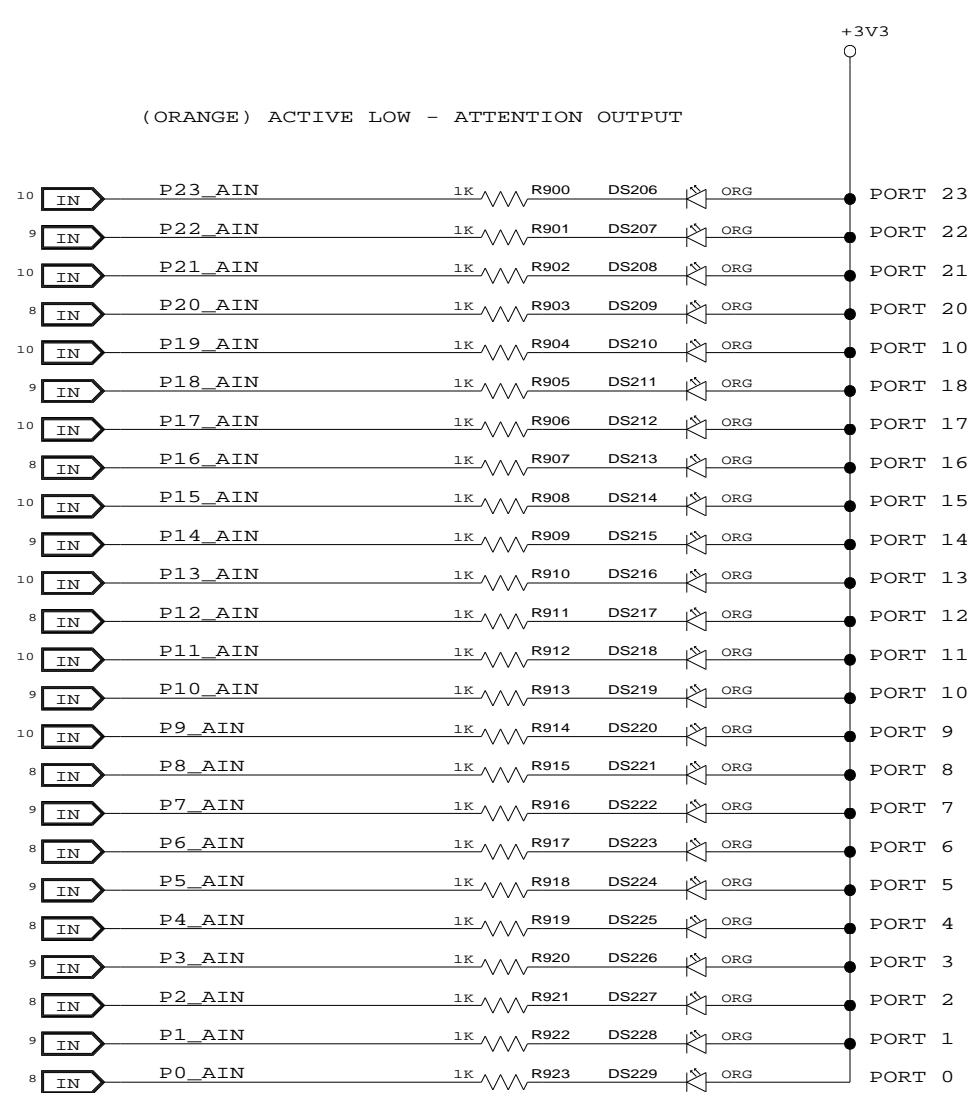
LED - PORT STATUS (2 OF 7)

SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
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AUTHOR Tony Tran	CHECKED BY Derek Huang
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Thu Jun 10 11:24:53 2010

SHEET 31 OF 41



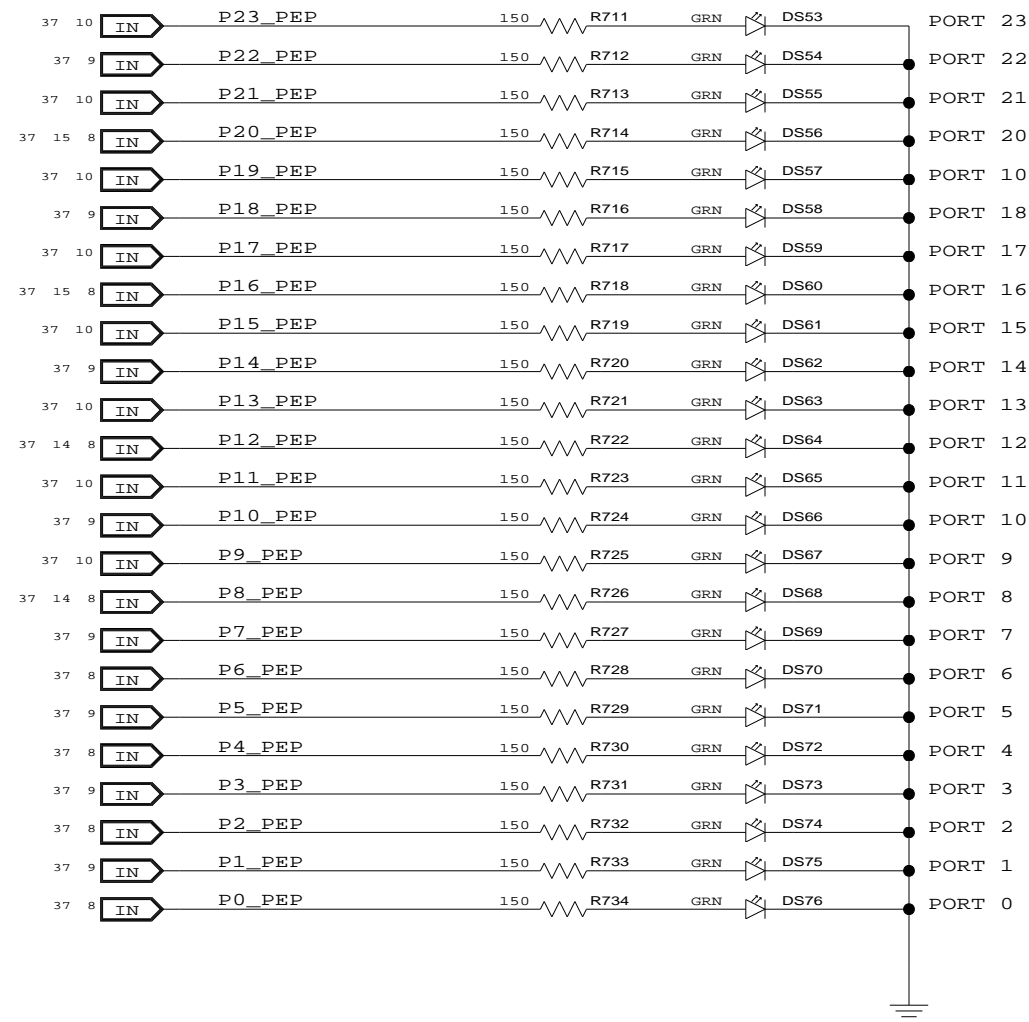
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TITLE EB-LOGAN-19

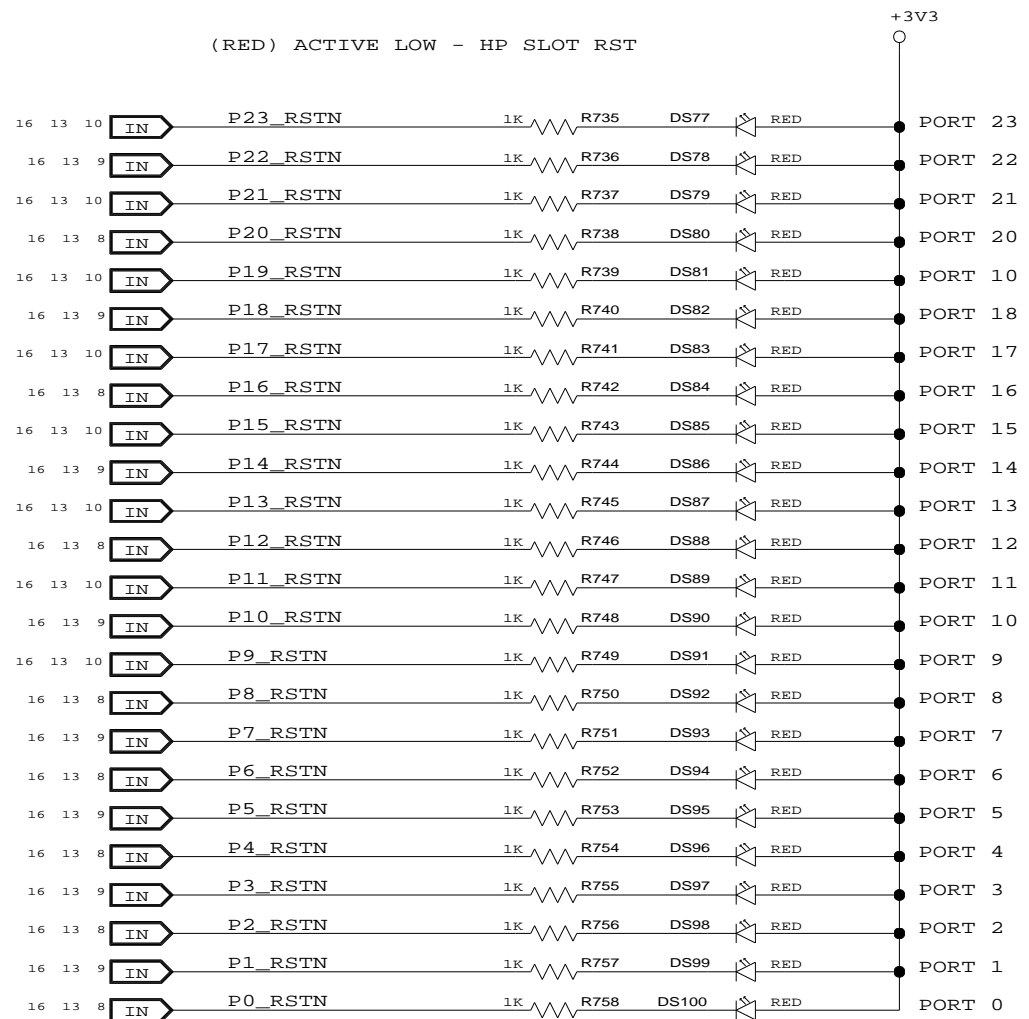
LED - PORT STATUS (3 OF 7)

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:53 2010			SHEET 32 OF 41

(GREEN) ACTIVE HIGH - POWER ENABLE



(RED) ACTIVE LOW - HP SLOT RST



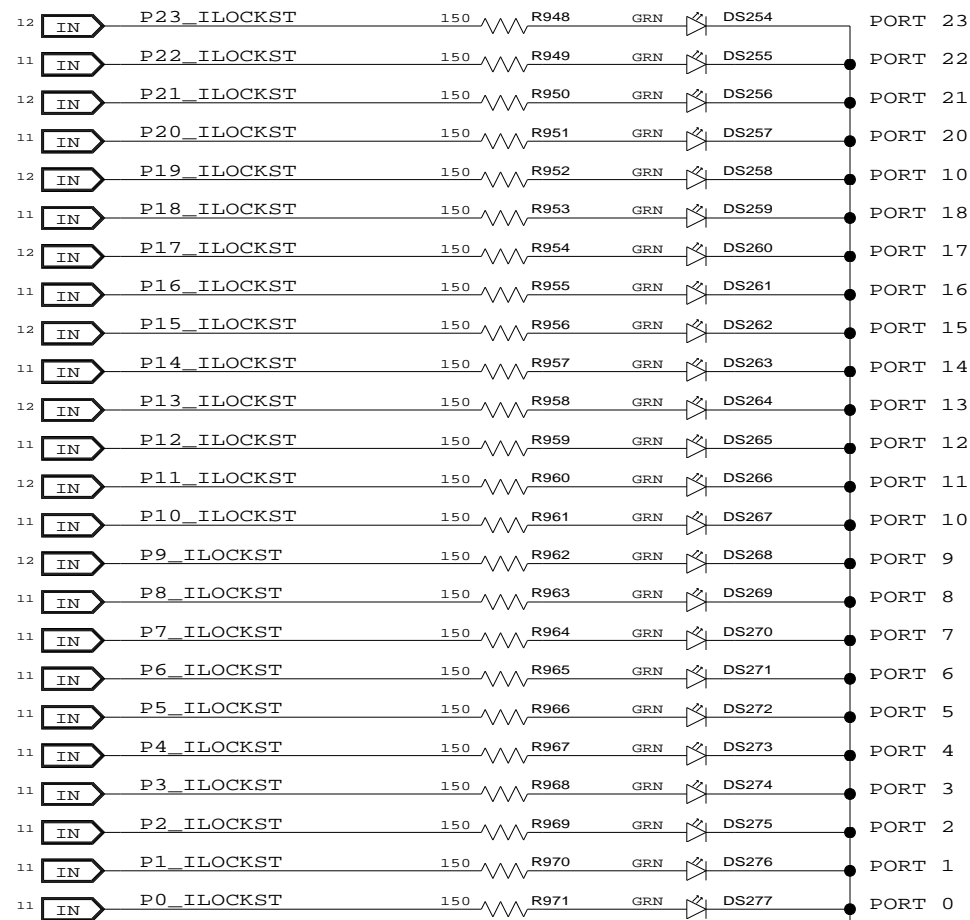
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TITLE EB-LOGAN-19

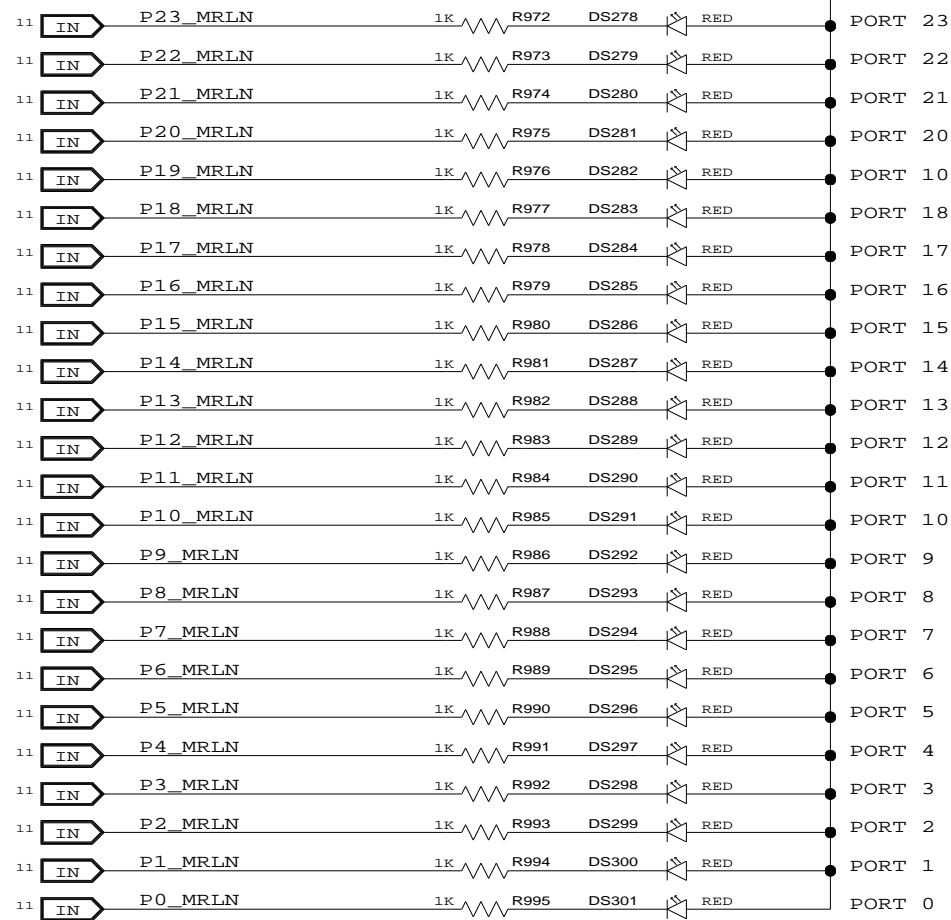
LED - PORT STATUS (4 OF 7)

SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:54 2010			SHEET 33 OF 41

(GREEN) ACTIVE HIGH - INTERLOCK INPUT



(RED) ACTIVE LOW - MRL



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TITLE EB-LOGAN-19

LED - PORT STATUS (5 OF 7)

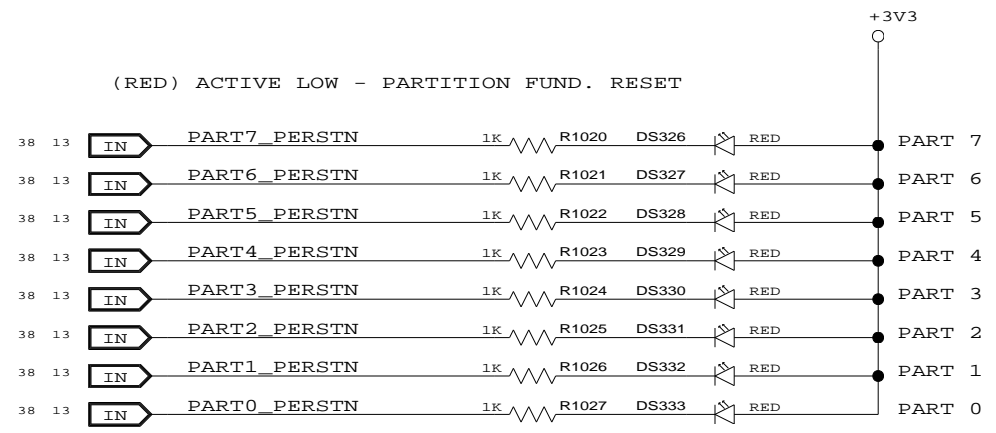
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
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AUTHOR Tony Tran	CHECKED BY Derek Huang
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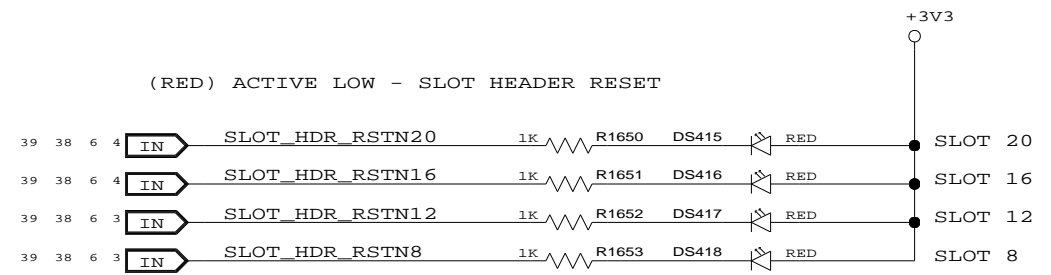
Thu Jun 10 11:24:54 2010

SHEET 34 OF 41

(RED) ACTIVE LOW - PARTITION FUND. RESET



(RED) ACTIVE LOW - SLOT HEADER RESET



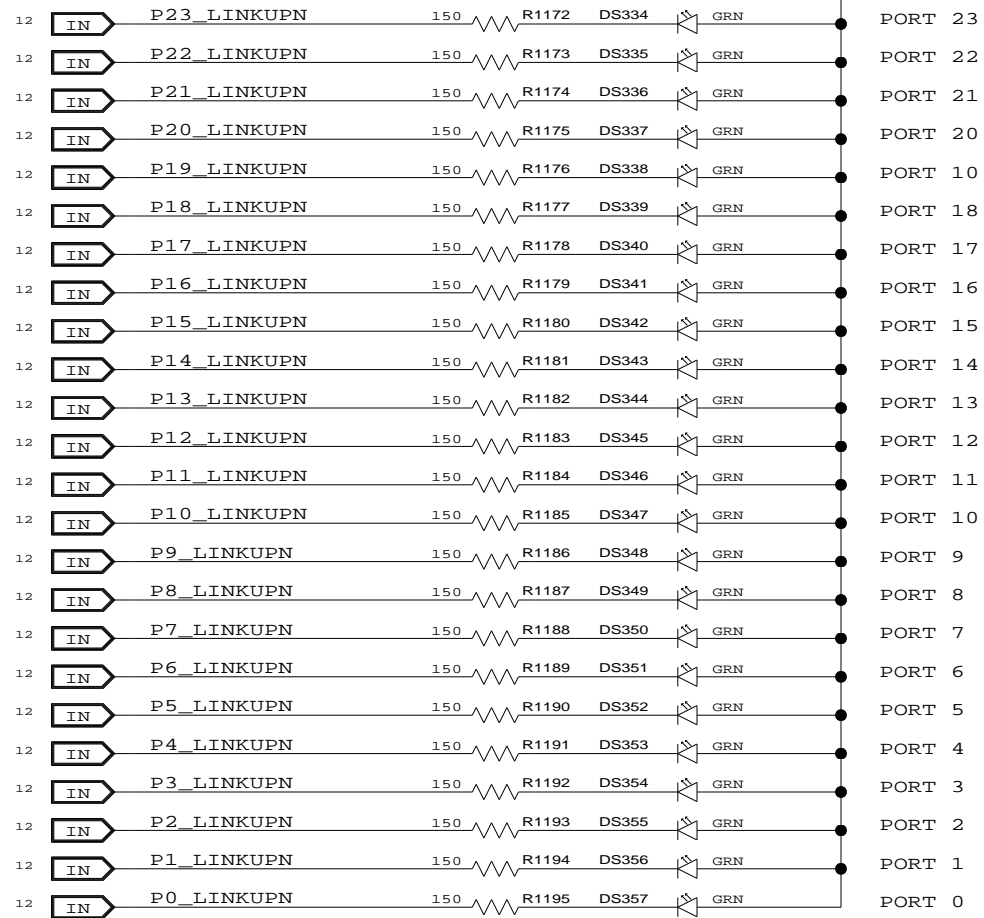
(GREEN) ACTIVE HIGH - INTERLOCK OUTPUT



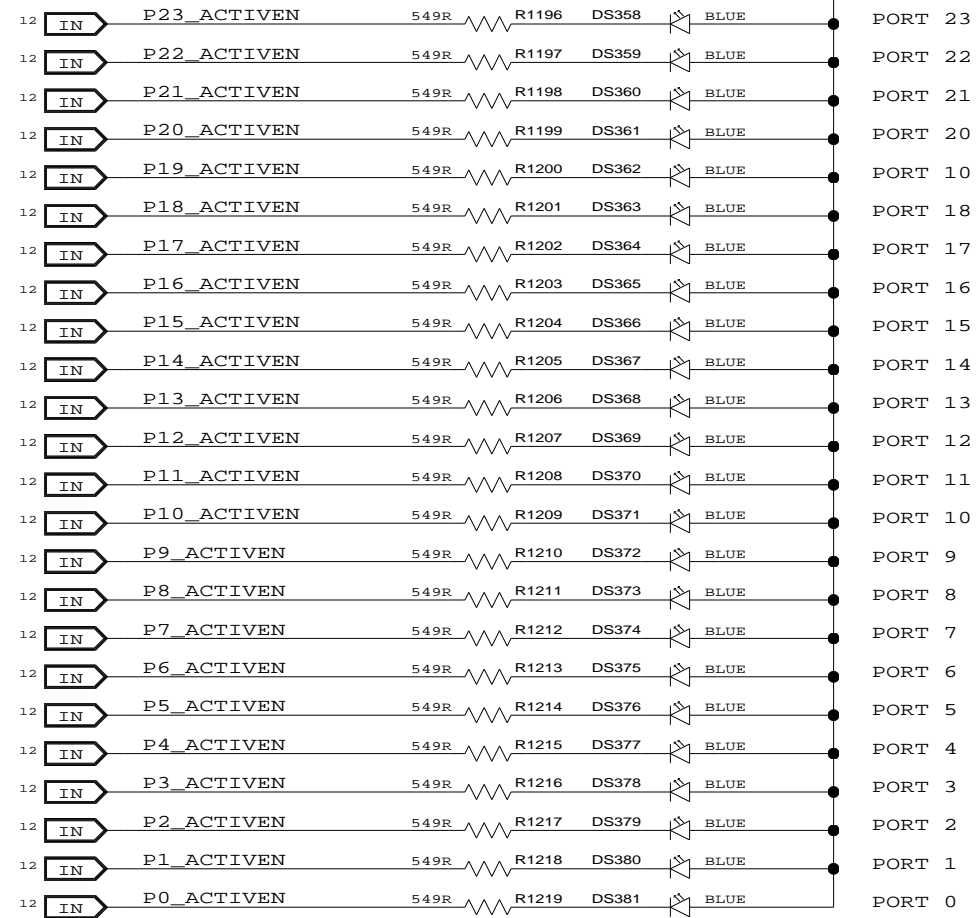
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TITLE EB-LOGAN-19			
LED - PORT STATUS (6 OF 7)			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:54 2010			SHEET 35 OF 41

(GREEN) ACTIVE LOW - LINK UP



(BLUE) ACTIVE LOW - LINK ACTIVITY



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TITLE EB-LOGAN-19

LED - PORT STATUS (7 OF 7)

SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
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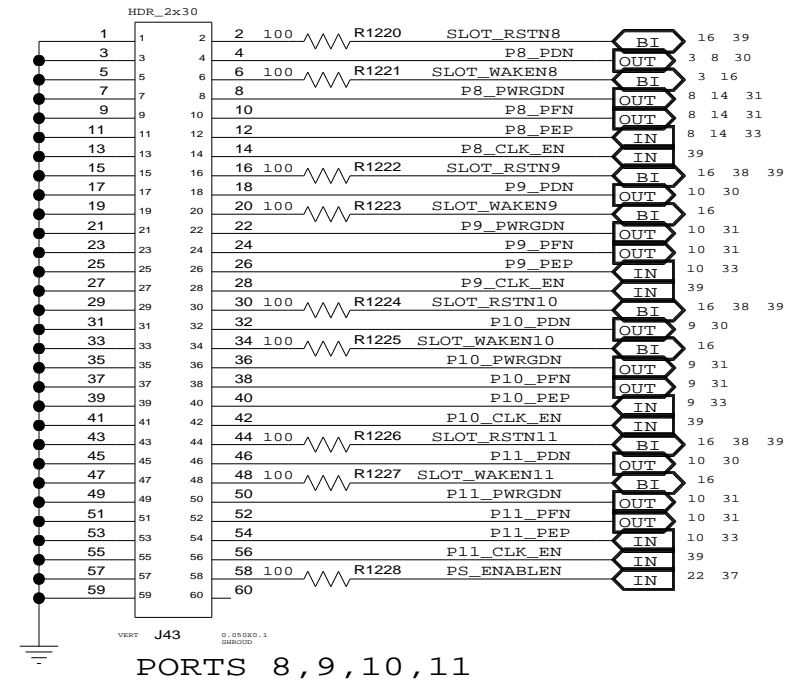
AUTHOR Tony Tran	CHECKED BY Derek Huang
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Thu Jun 10 11:24:55 2010

SHEET 36 OF 41

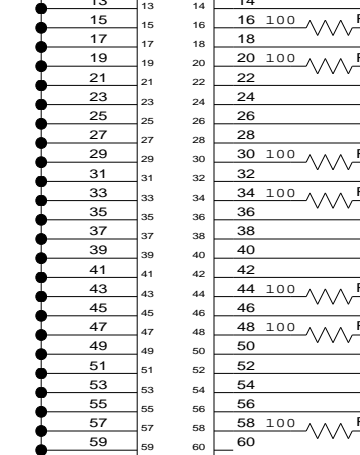
D

SLOT_RESETN
CARD_PRESENTN
WAKEN
POWERGOOD
PWR_FLTN
PWR_ENABLE
CLOCK_ENABLEN
PS_ENABLEN
CABLE SENSE



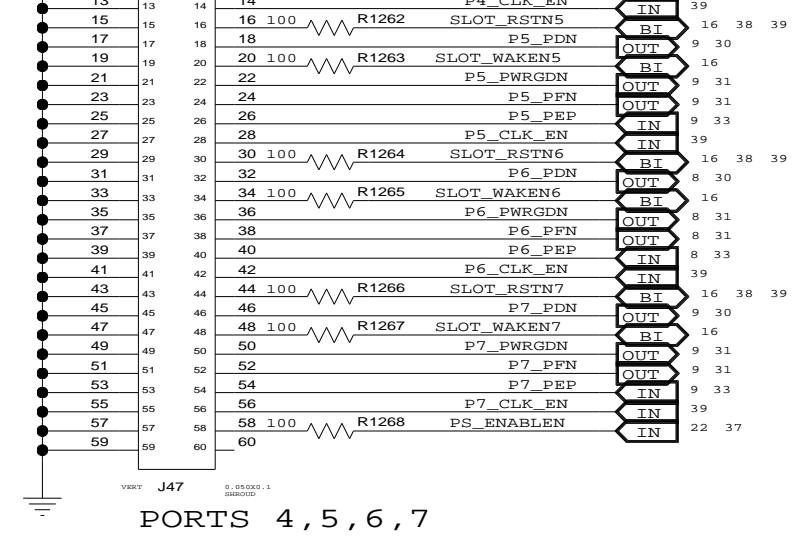
PORTS 8,9,10,11

D



PORTS 12,13,14,15

D

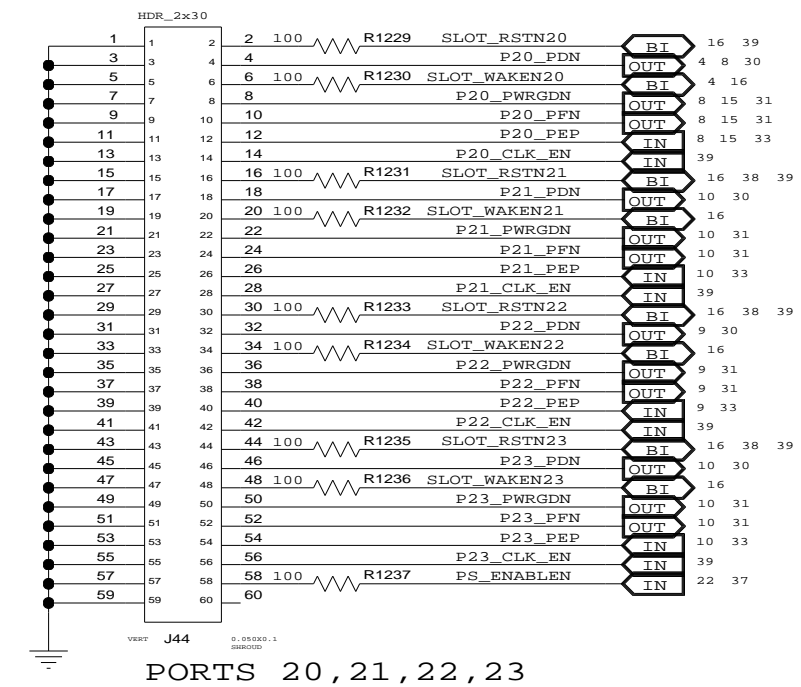


PORTS 4,5,6,7

C

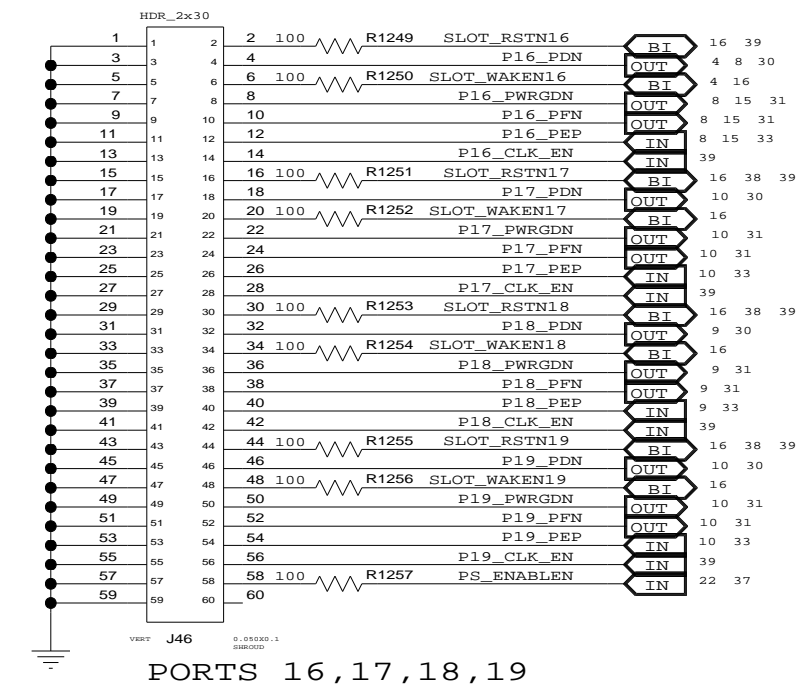
B

SLOT_RESETN
CARD_PRESENTN
WAKEN
POWERGOOD
PWR_FLTN
PWR_ENABLE
CLOCK_ENABLEN
PS_ENABLEN
CABLE SENSE



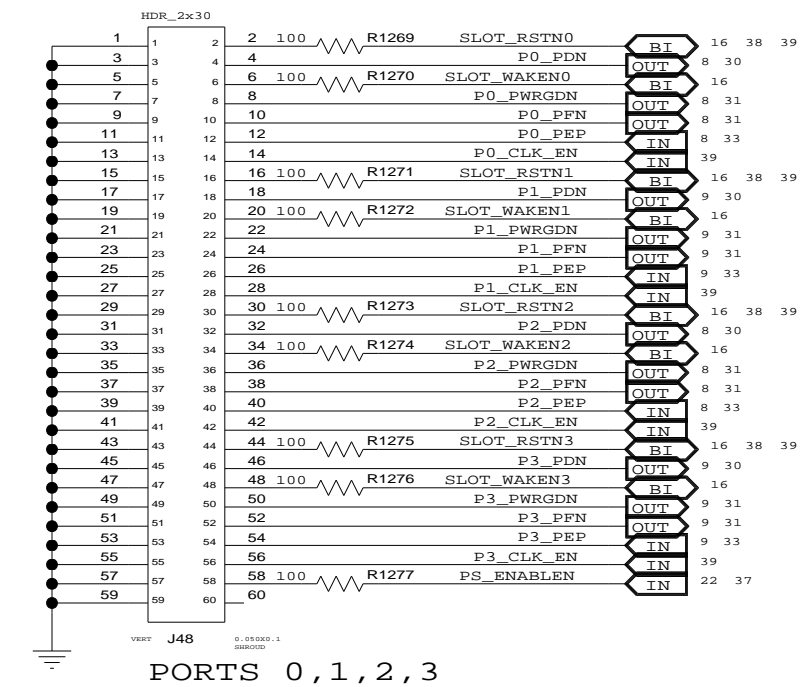
PORTS 20,21,22,23

B



PORTS 16,17,18,19

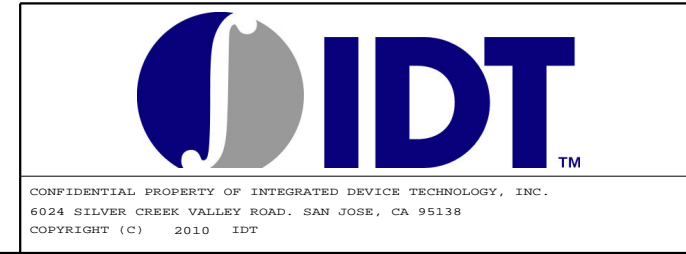
B



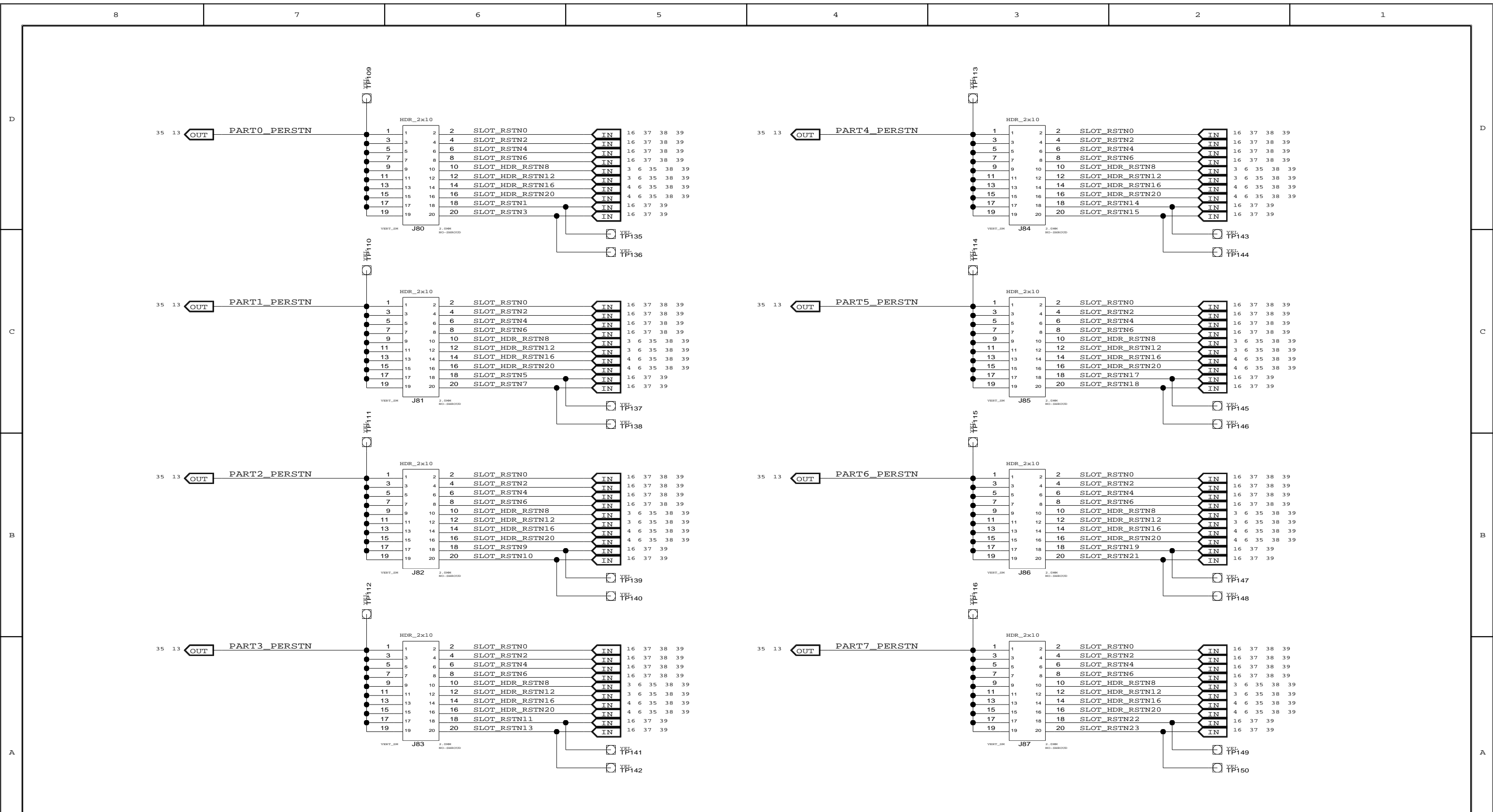
PORTS 0,1,2,3


A

A



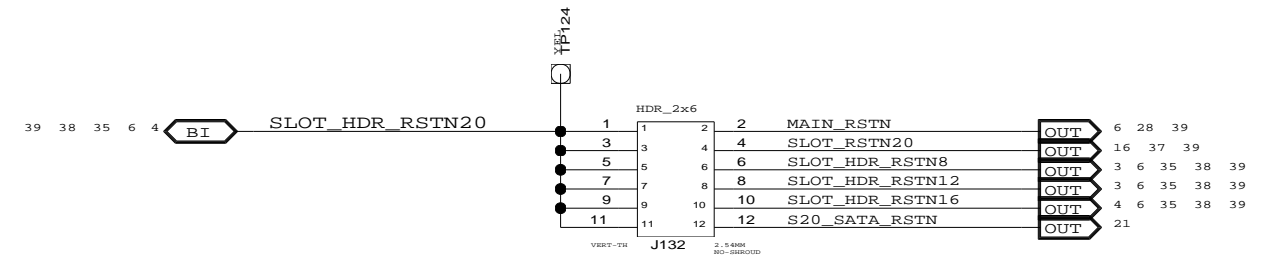
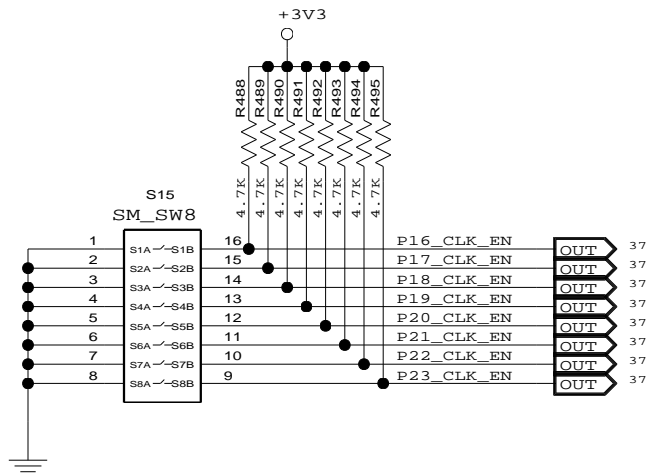
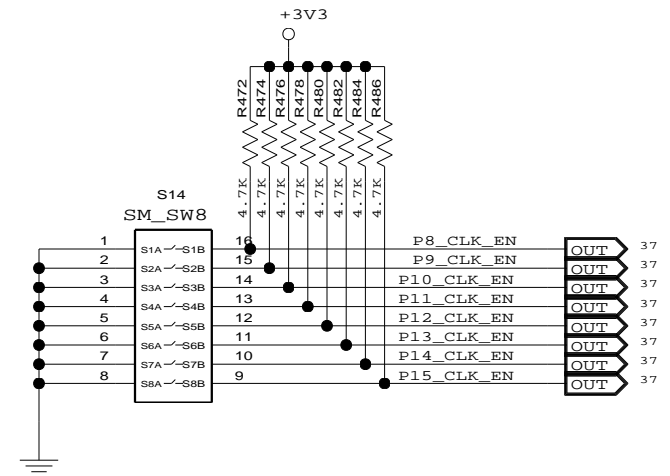
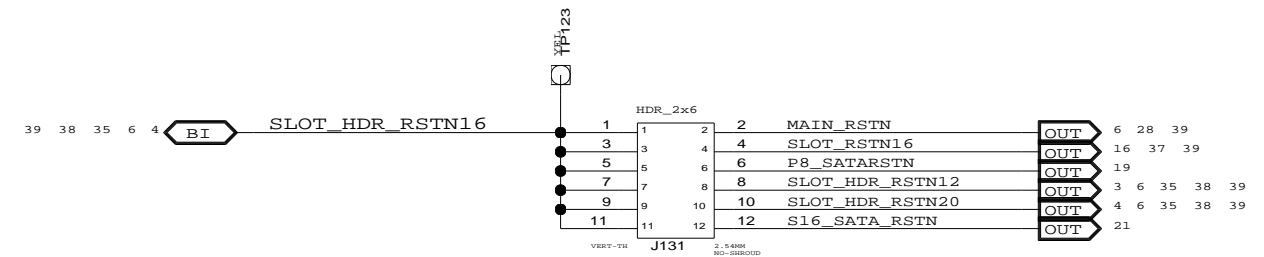
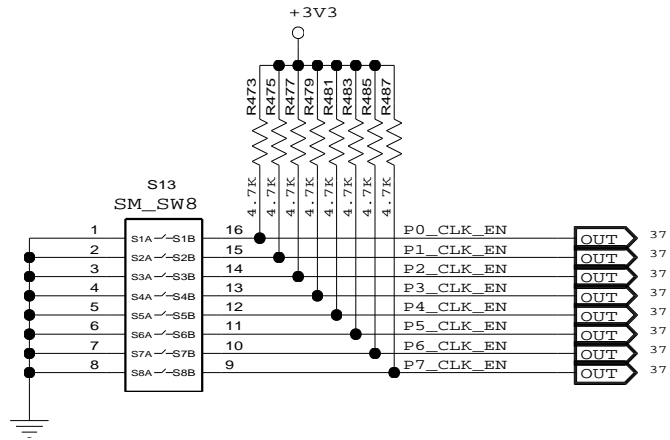
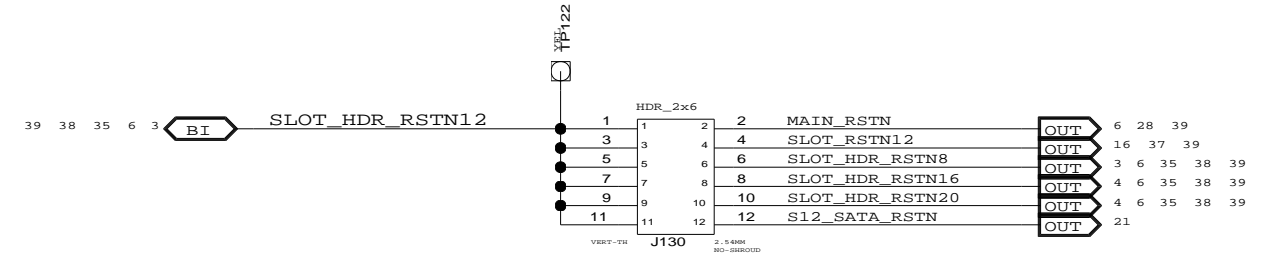
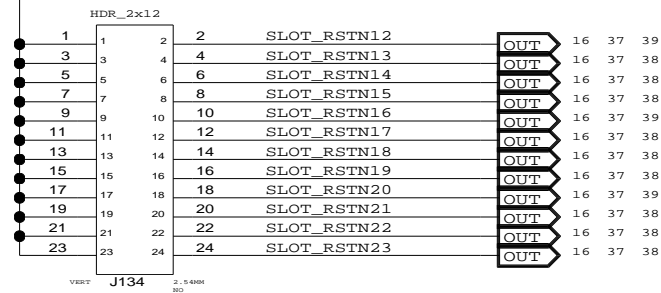
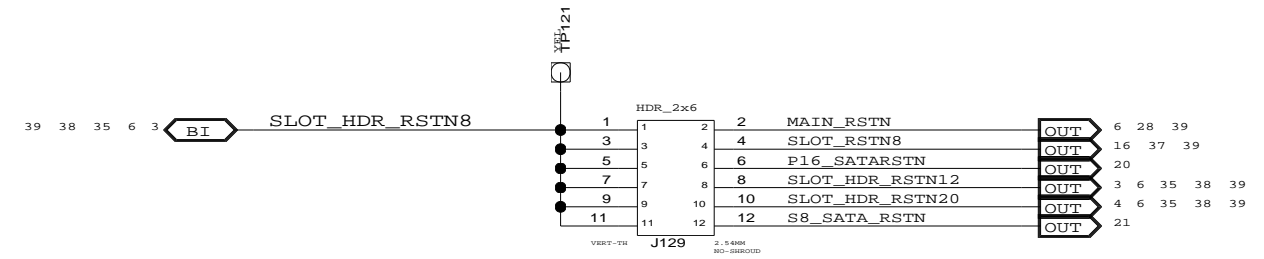
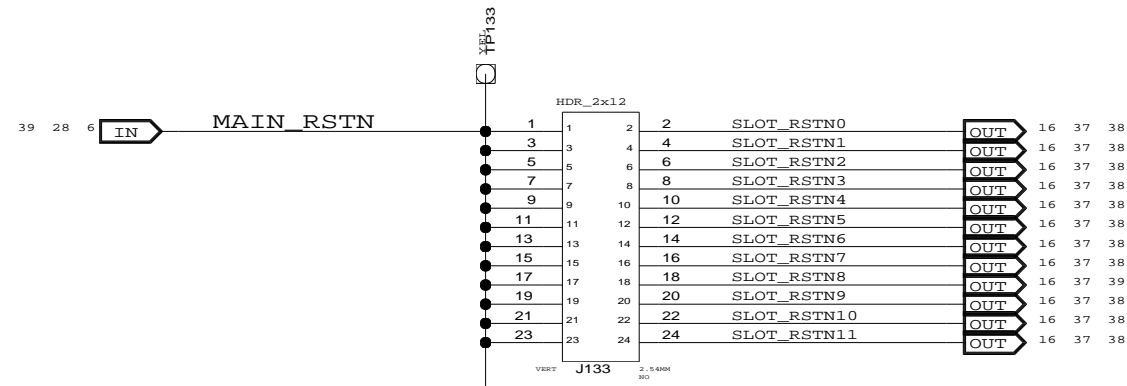
TITLE EB-LOGAN-19			
SIDEBAND CONNECTORS			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:55 2010			SHEET 37 OF 41



				TITLE EB-LOGAN-19			
				PARTITION RESET SELECT HEADERS			
SIZE	DRAWING NO.		FAB P/N		REV.		
B	SCH-PESEB-002		18-692-001		2.0		
AUTHOR			CHECKED BY				
Tony Tran			Derek Huang				
Thu Jun 10 11:24:56 2010				SHEET 38 OF 41			

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NOTE: DNP JUMPERS WHEN IOEXPANDER IS ENABLED



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TITLE EB-LOGAN-19

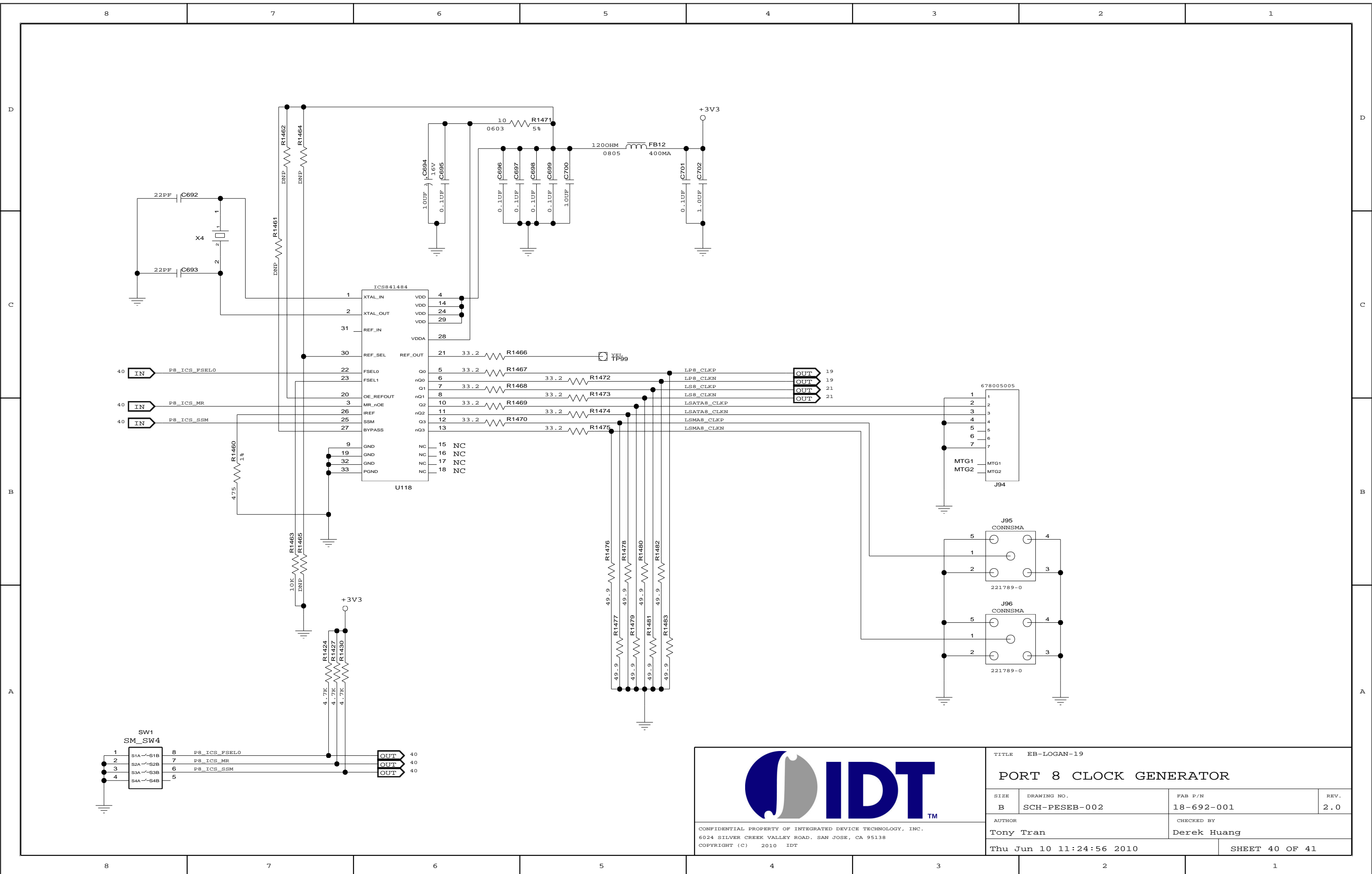
SLOT RESET SELECT HEADERS


SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

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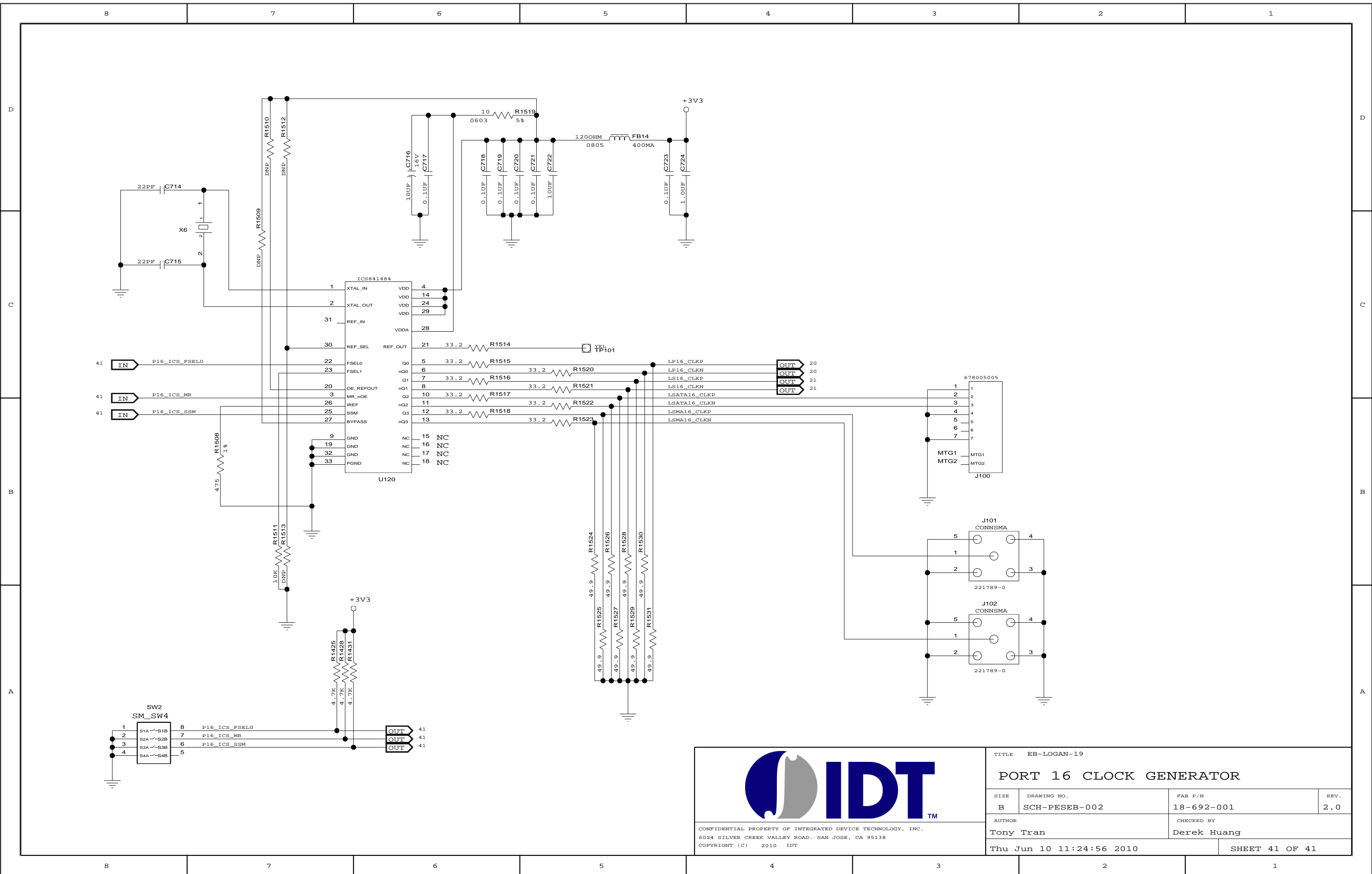



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PORT 8 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
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PORT 16 CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:56 2010			SHEET 41 OF 41