

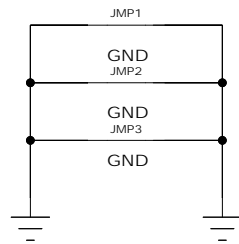
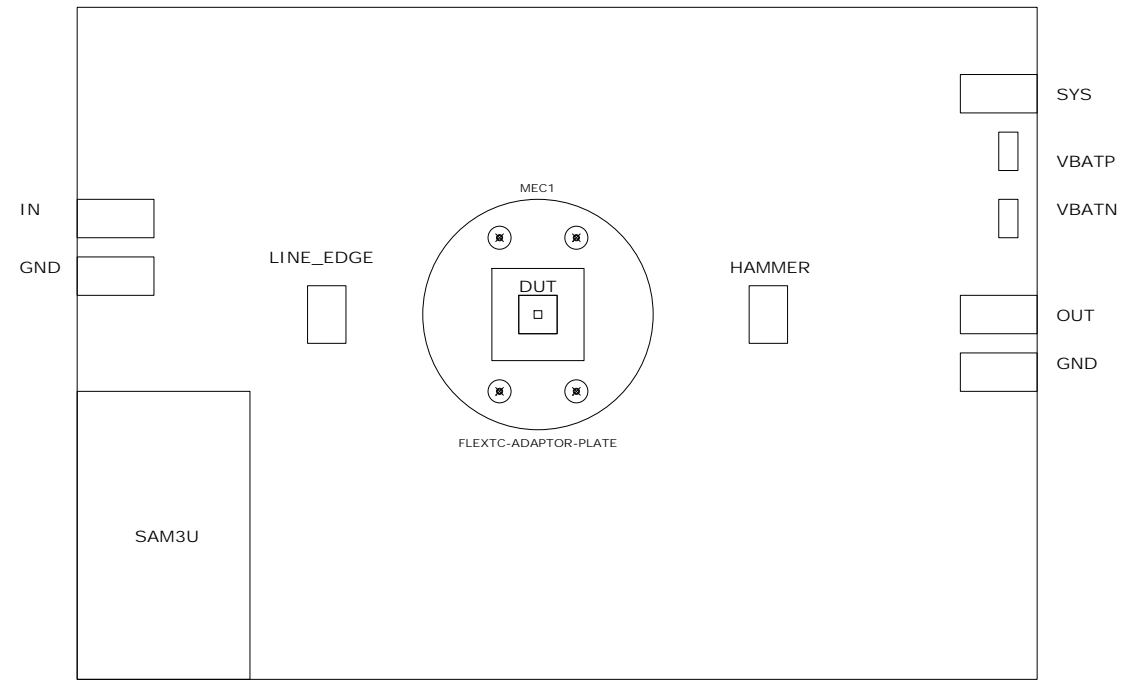
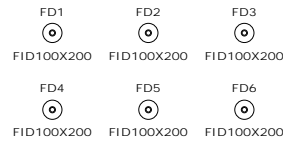
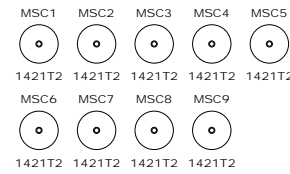
# REVISION TABLE

| REV. | DATE       | ENGINEER | NOTES  |
|------|------------|----------|--|
| A00  | 16/10/2016 | GF       | Initial version.   |
| A01  | 17/10/2016 | GC       | Some refdes changed to match board i will be using as my starting point. Silkscreen label at header J7 changed to OUT. Silkscreen label at header J3 changed to IN. Silkscreen labels added at RF connectors. Two single blue jumper links removed at headers J18 & J19 and replaced with one double black jumper link. Two single blue jumper links removed at header J22 and replaced with one double black jumper link. |
| A02  | 25/10/2016 | GC       | 1x2 header J7 removed. RF connectors J35, J52, J53 changed to Unpop. Resistors R46, R47, R60 changed to Unpop.   |
| A03  | 09/01/2017 | GF       | Added a clarifying note on page 1, explaining that C1M/C2M are used interchangeably with C1N/C2N.  |
|      |            |          |  |
|      |            |          |  |
|      |            |          |  |
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|      |            |          |  |
|      |            |          |  |
|      |            |          |  |
|      |            |          |  |
|      |            |          |  |

# MECHANICAL PARTS

NOTE: C1M = C1N  
C2M = C2N

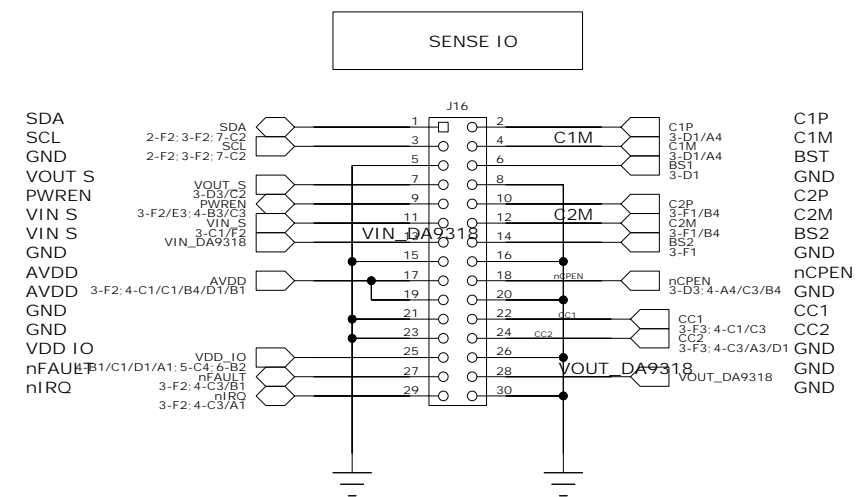
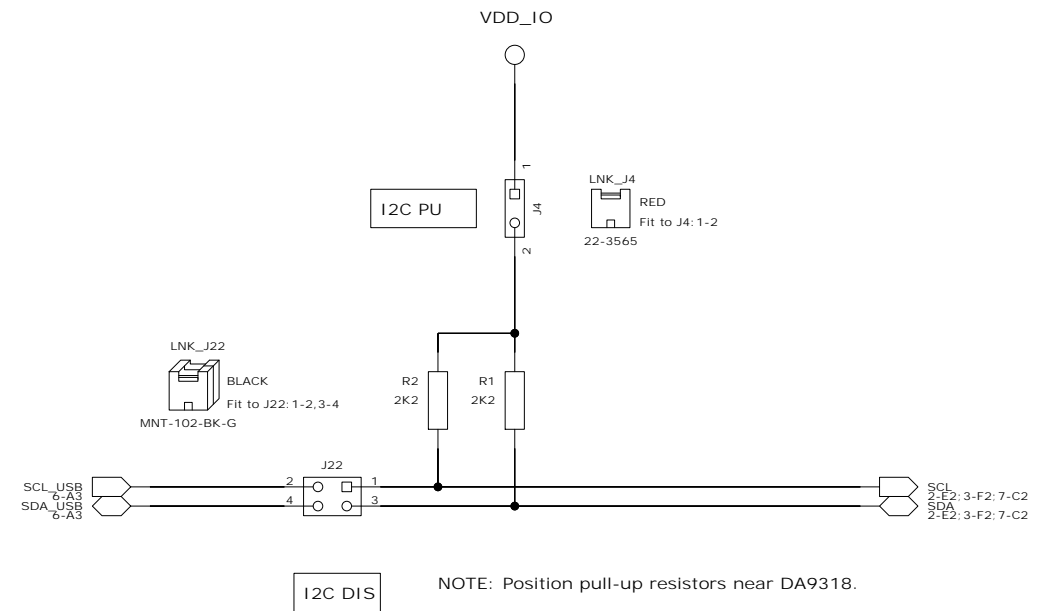
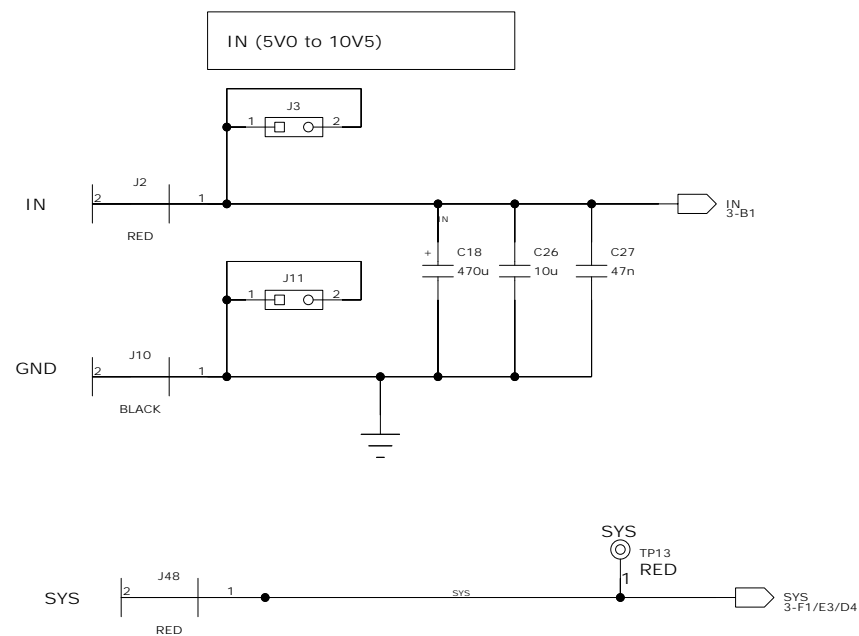
# MECHANICAL



LAYOUT NOTE: SPREAD GND LOOPS EVENLY AROUND THE BOARD.  
LAYOUT NOTE: REFER TO REDWOOD\_RECOMMENDED\_LAYOUT.PDF

|  |                             |                         |                             |  |
|--|-----------------------------|-------------------------|-----------------------------|--|
| SCHEMATIC TEMPLATE REV.xDxD_V3 (23-10-2015)<br>DESIGNED BY:<br>Greg Fattig<br><br>REVIEWED BY:<br>GF, GC | CONFIDENTIAL<br>INFORMATION | SIZE<br>A3L             | TITLE:<br>DA9318 EVB Solder |  |
|  | SAVED DATE:<br>25/02/2022   | DRAWING NO:<br>329-01-A | REV:<br>A01                 |  |
| REVIEWED DATE:<br>27/09/2016   | SHEET NAME:<br>REVISION     |                         | PAGE:<br>1 of 7             |  |

# POWER & IOs



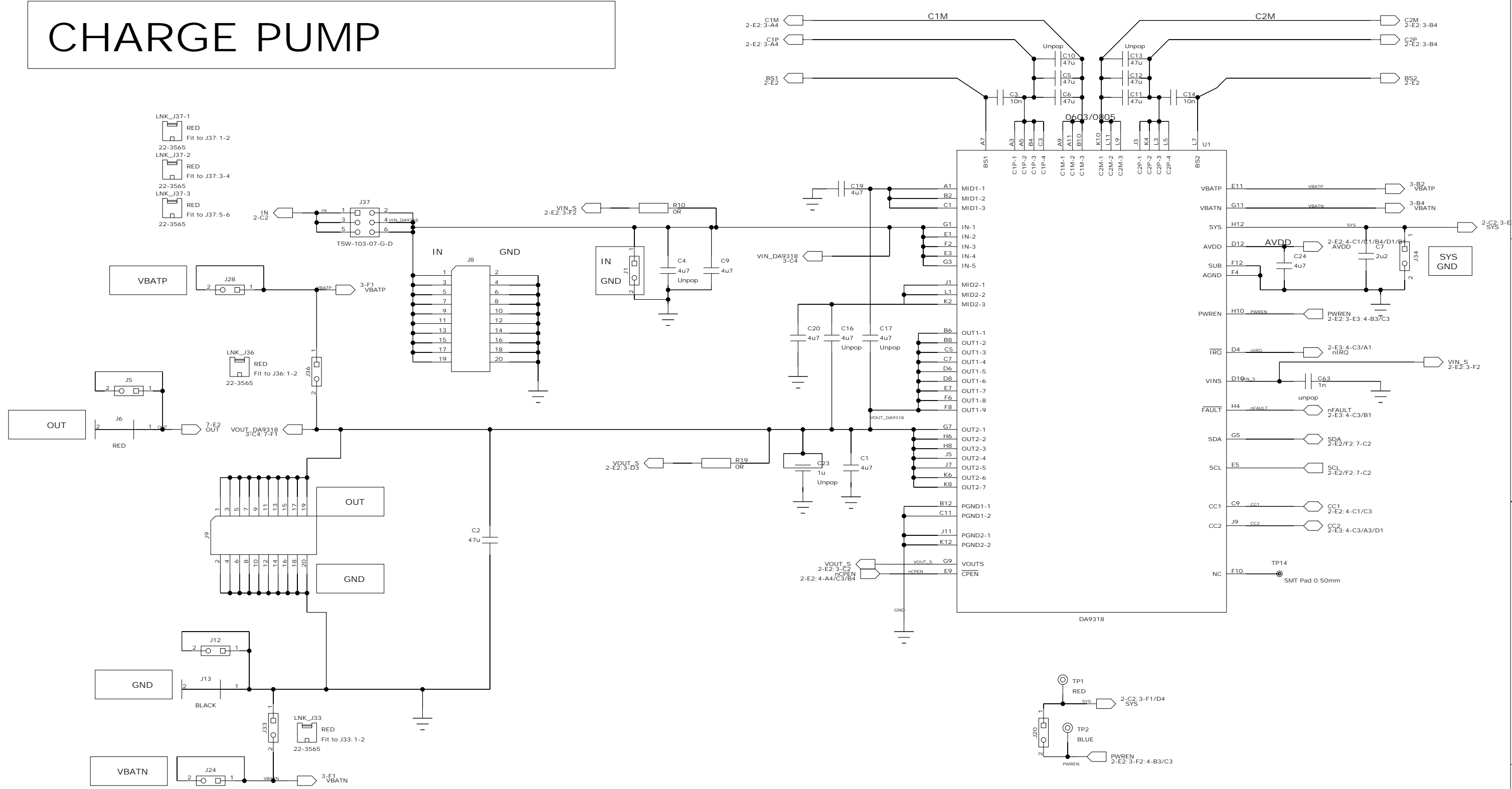
SCHEMATIC TEMPLATE REV. xDXD\_V3 (23-10-2015)

DESIGNED BY:  
Greg Fattig

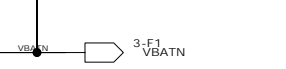
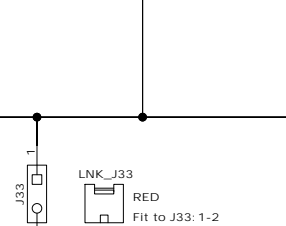
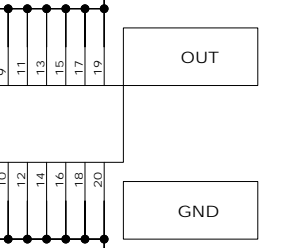
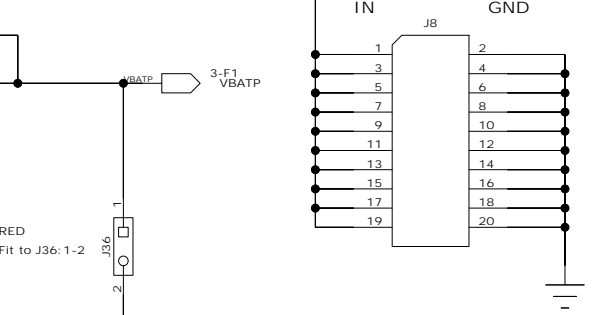
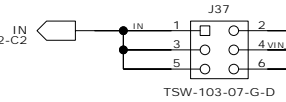
REVIEWED BY:  
GF, GC

|                              |                              |                             |  |
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| CONFIDENTIAL INFORMATION     | SIZE<br>A3L                  | TITLE:<br>DA9318 EVB Solder |  |
| SAVED DATE:<br>25/02/2022    | DRAWING NO:<br>329-01-A      | REV:<br>AO1                 |  |
| REVIEWED DATE:<br>27/09/2016 | SHEET NAME:<br>POWER_AND_IOs |                             |  |

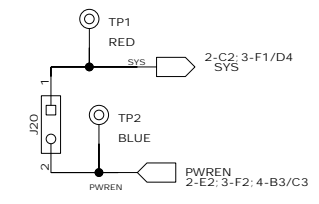
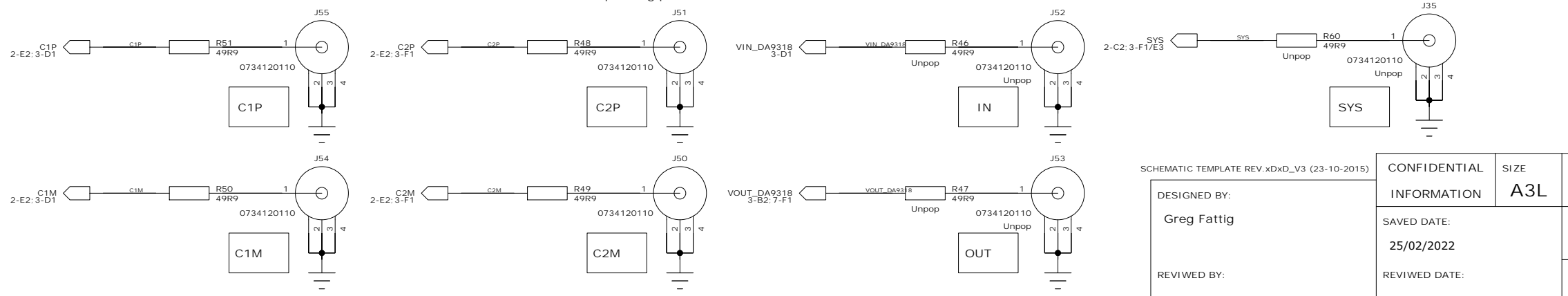
# CHARGE PUMP



- LNK\_J37-1 RED Fit to J37: 1-2
- 22-3565 LNK\_J37-2 RED Fit to J37: 3-4
- 22-3565 LNK\_J37-3 RED Fit to J37: 5-6



RF connectors should kelvin connect to corresponding pin on U1



SCHEMATIC TEMPLATE REV. xDxD\_V3 (23-10-2015)

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|                             |                           |                             |             |         |
|-----------------------------|---------------------------|-----------------------------|-------------|---------|
| CONFIDENTIAL<br>INFORMATION | SIZE<br>A3L               | TITLE:<br>DA9318 EVB Solder |             |         |
|                             | SAVED DATE:<br>25/02/2022 | DRAWING NO:<br>329-01-A     | REV:<br>A01 |         |
| REVIWED DATE:<br>27/09/2016 | SHEET NAME:<br>CP         |                             | PAGE:<br>3  | of<br>7 |

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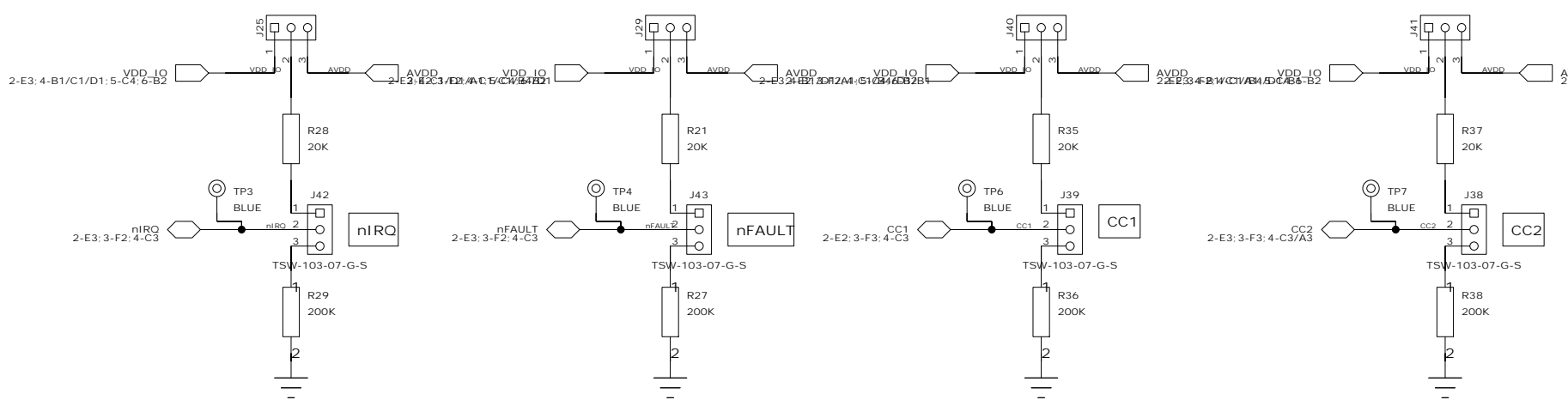
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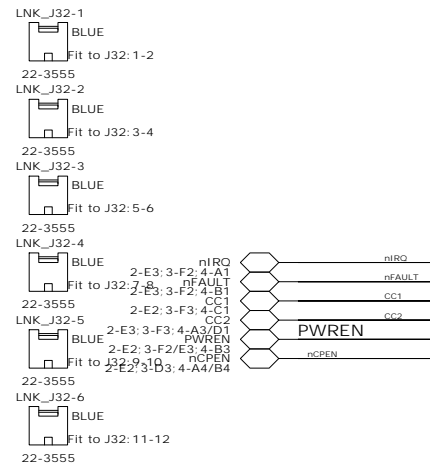
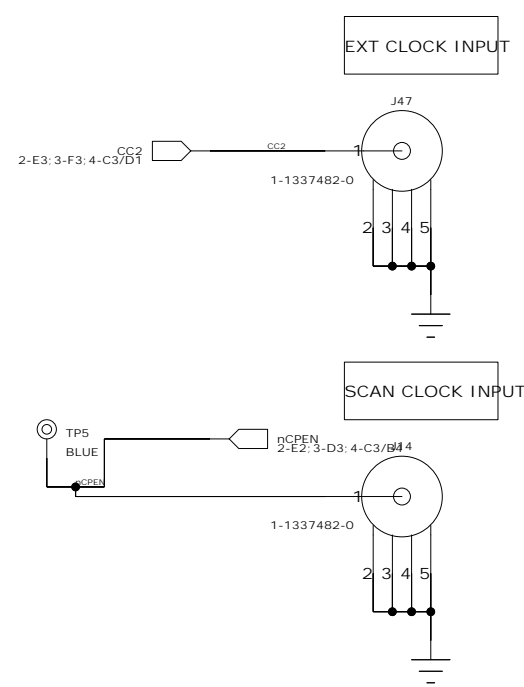
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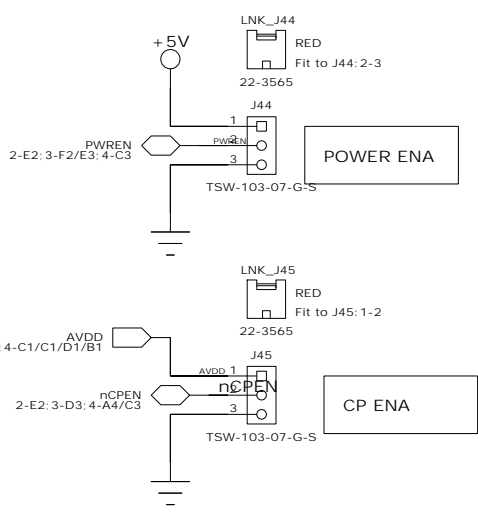
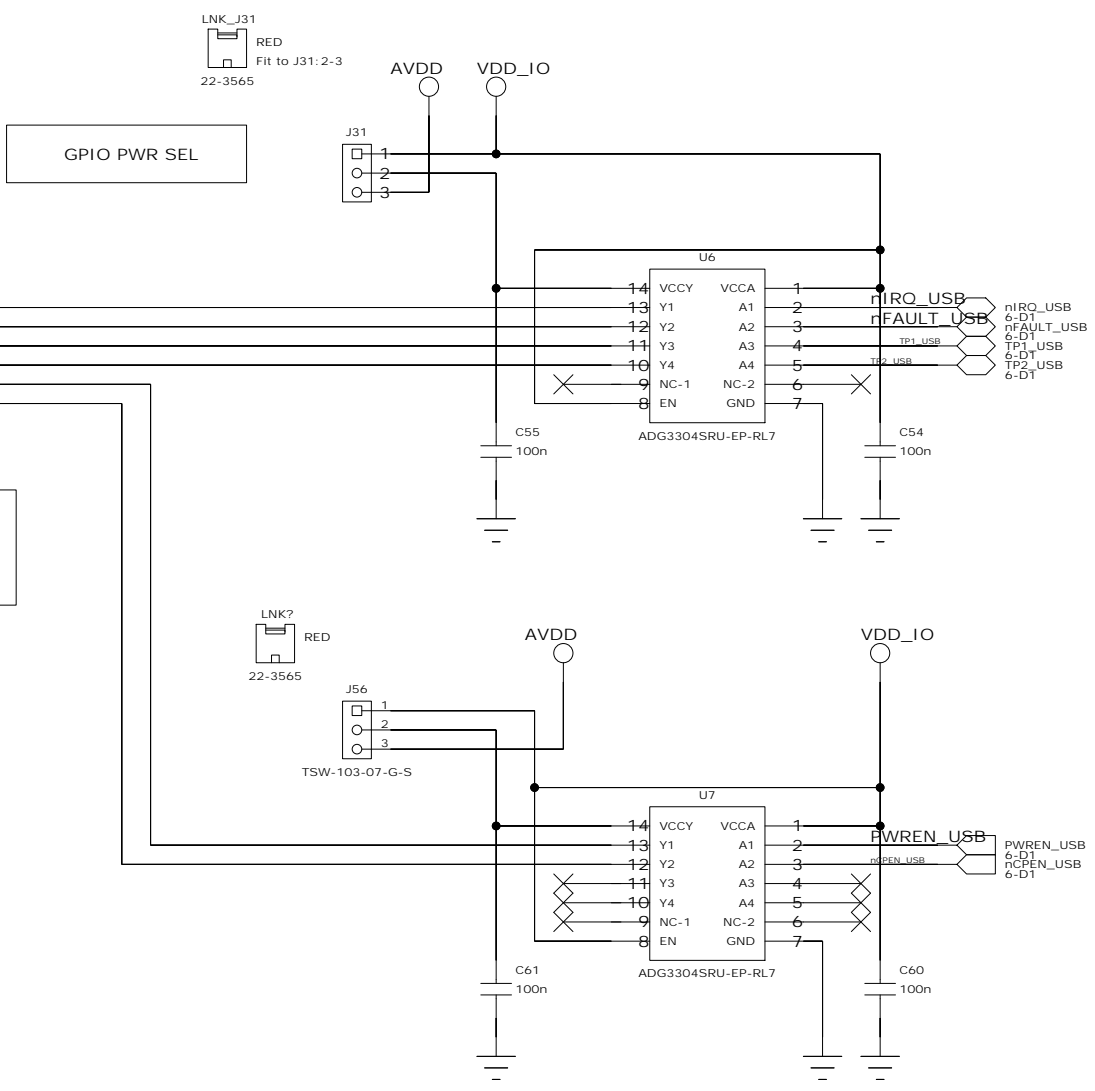


| J25, J29, J40, J41 | PU PWR SEL |
|--------------------|------------|
| 1-2                | VDD IO     |
| 2-3                | AVDD       |

| J38, J39, J42, J43 | PU or PD select |
|--------------------|-----------------|
| 1-2                | Pull Up         |
| 2-3                | Pull Down       |



SIGNALS:  
 nIRO  
 nFAULT  
 CC1  
 CC2  
 PWREN  
 nCPEN



# GPIOs

SCHEMATIC TEMPLATE REV. xDxD\_V3 (23-10-2015)

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Greg Fattig

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GF, GC

|                             |                         |                             |  |
|-----------------------------|-------------------------|-----------------------------|--|
| CONFIDENTIAL INFORMATION    | SIZE<br>A3L             | TITLE:<br>DA9318 EVB Solder |  |
| SAVED DATE:<br>25/02/2022   | DRAWING NO:<br>329-01-A | REV:<br>A01                 |  |
| REVIWED DATE:<br>27/09/2016 | SHEET NAME:<br>GPIOs    | PAGE:<br>4 of 7             |  |

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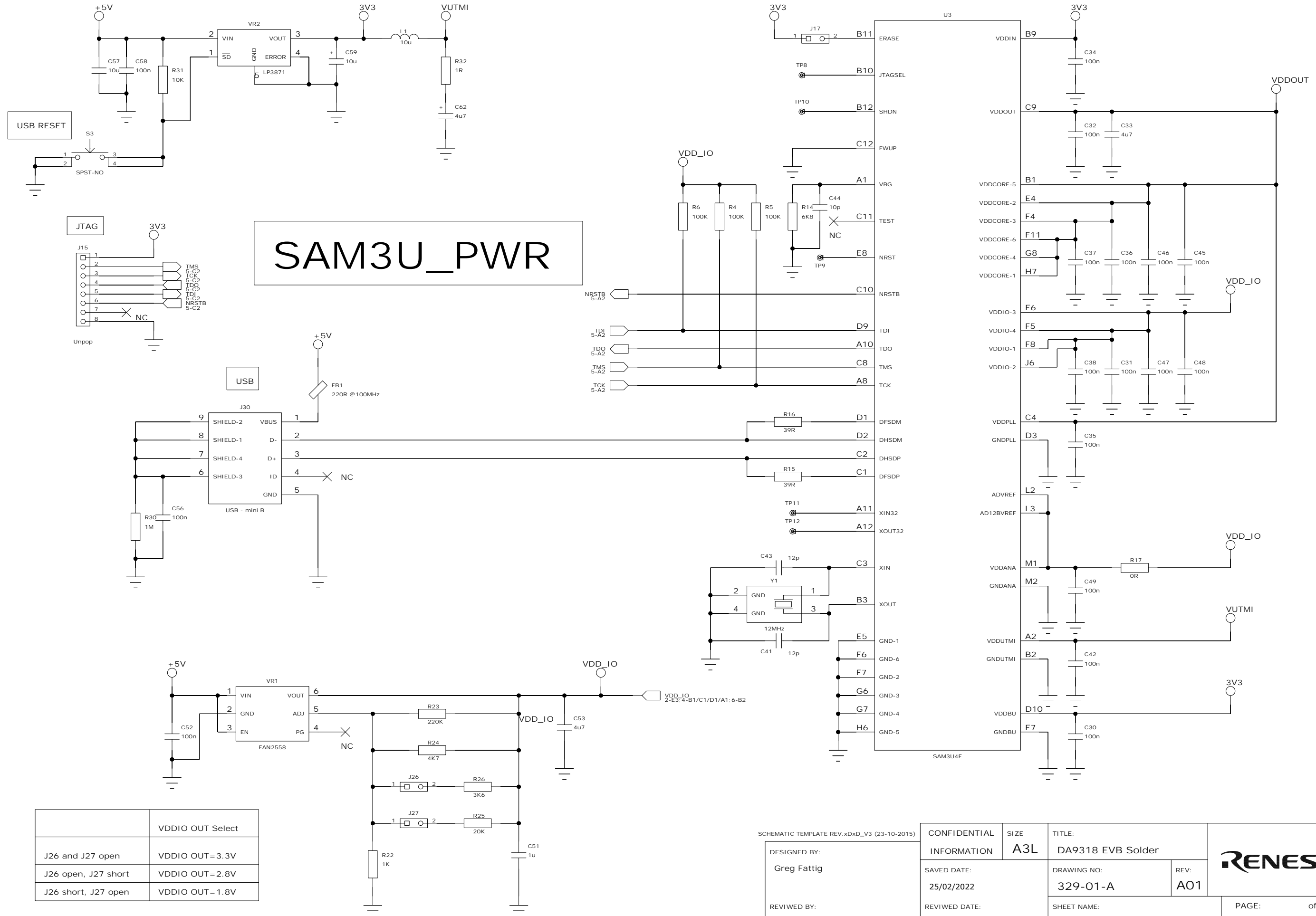
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# SAM3U\_PWR



|                     | VDDIO OUT Select |
|---------------------|------------------|
| J26 and J27 open    | VDDIO OUT=3.3V   |
| J26 open, J27 short | VDDIO OUT=2.8V   |
| J26 short, J27 open | VDDIO OUT=1.8V   |

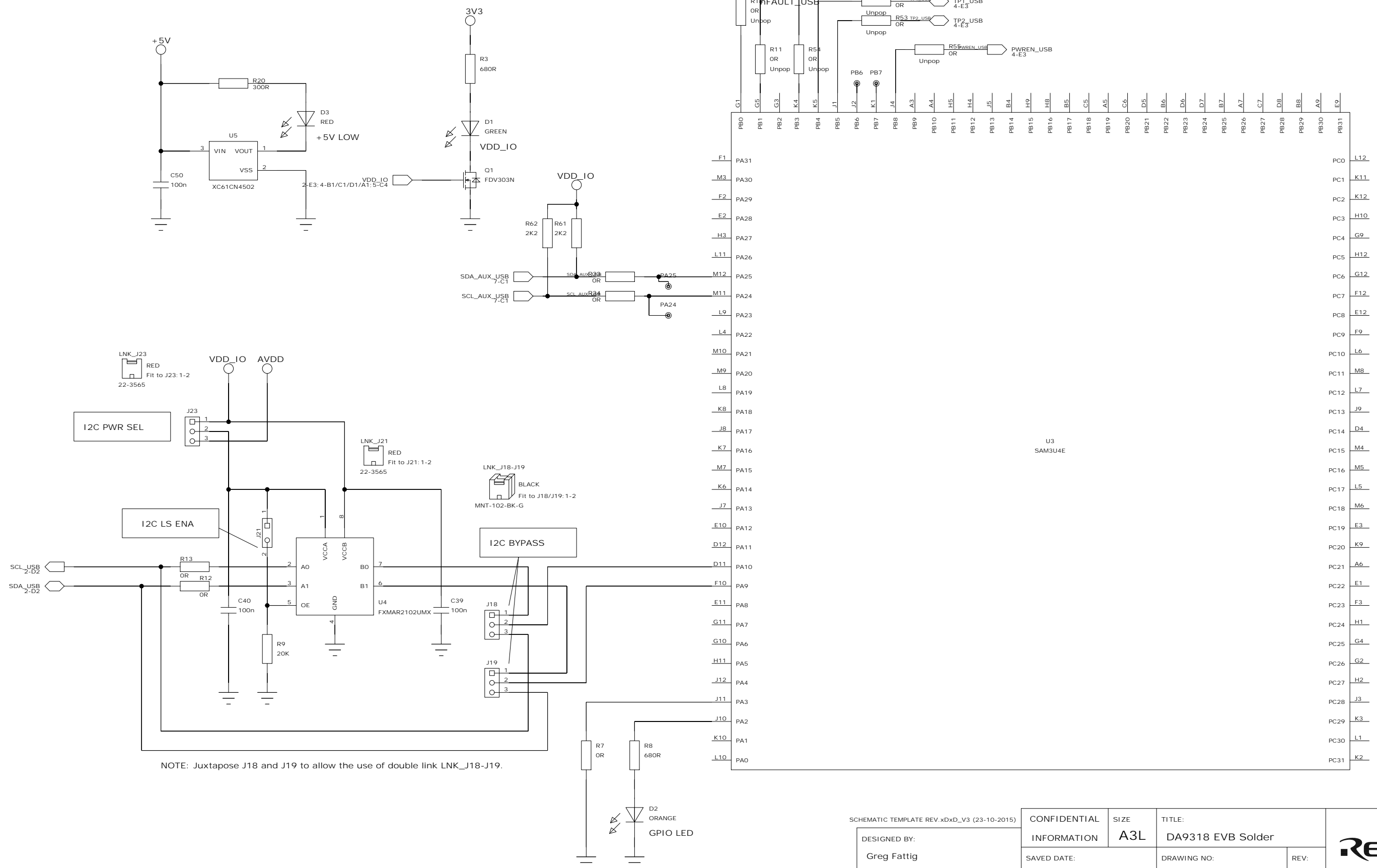
SCHEMATIC TEMPLATE REV. xDxD\_V3 (23-10-2015)

DESIGNED BY:  
Greg Fattig

REVIEWED BY:  
GF, GC

|                              |             |                             |             |
|------------------------------|-------------|-----------------------------|-------------|
| CONFIDENTIAL<br>INFORMATION  | SIZE<br>A3L | TITLE:<br>DA9318 EVB Solder |             |
| SAVED DATE:<br>25/02/2022    |             | DRAWING NO:<br>329-01-A     | REV:<br>A01 |
| REVIEWED DATE:<br>27/09/2016 |             | SHEET NAME:<br>USB_IF       |             |

# SAM3U\_IOs



NOTE: Juxtapose J18 and J19 to allow the use of double link LNK\_J18-J19.

SCHEMATIC TEMPLATE REV. xDxD\_V3 (23-10-2015)

DESIGNED BY:  
Greg Fattig

REVIEWED BY:  
GF, GC

CONFIDENTIAL  
INFORMATION

SAVED DATE:  
25/02/2022

REVIEWED DATE:  
27/09/2016

SIZE  
A3L

TITLE:  
DA9318 EVB Solder

DRAWING NO:  
329-01-A

SHEET NAME:  
USB\_LEVEL\_SHIFTER

REV:  
A01

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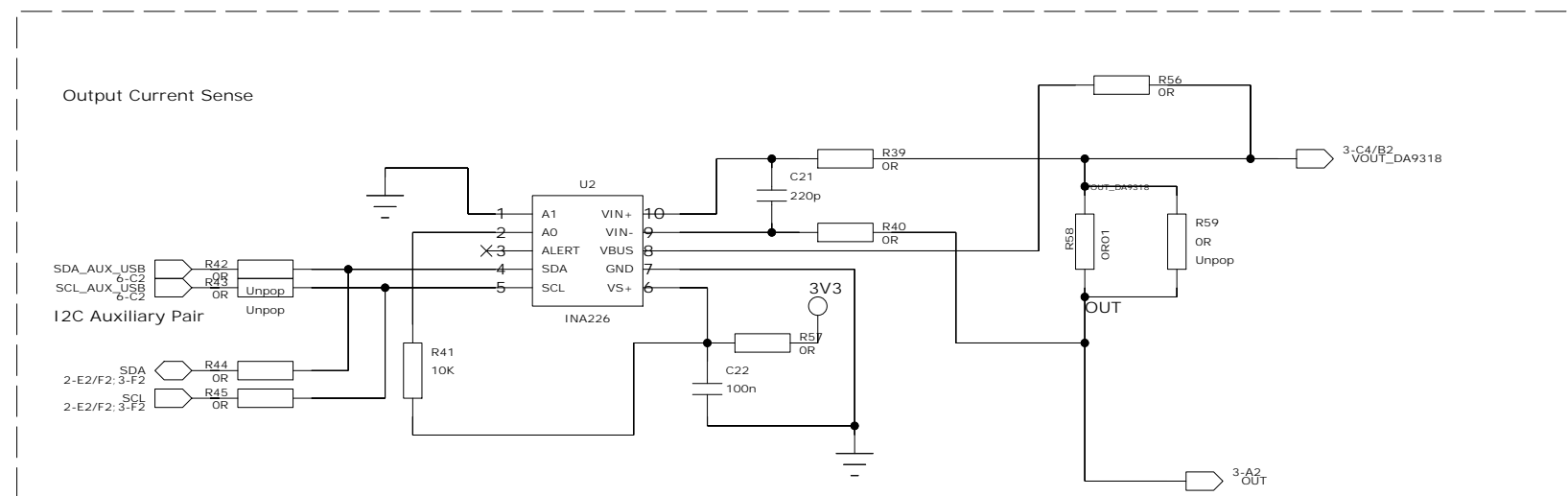
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SCHEMATIC TEMPLATE REV.xdxd\_V3 (23-10-2015)

DESIGNED BY:  
Greg Fattig

REVIWED BY:  
GF, GC

CONFIDENTIAL  
INFORMATION

SIZE  
A3L

TITLE:  
DA9318 EVB Solder

SAVED DATE:  
25/02/2022

REVIWED DATE:  
27/09/2016

DRAWING NO:  
329-01-A

SHEET NAME:  
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REV:  
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