

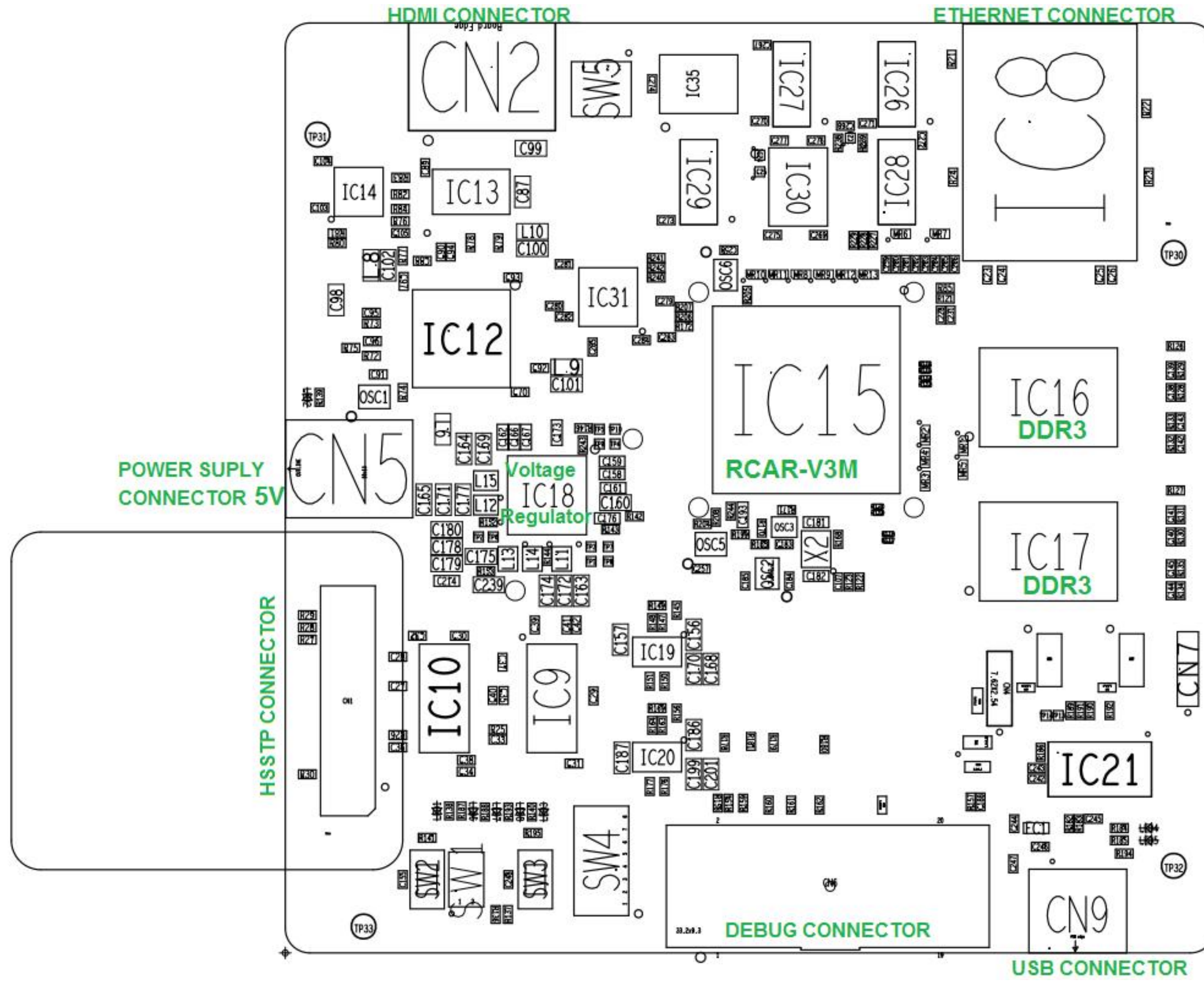
REV	COMMENT	DATE	DRAWN BY
1.00	Release	22/12/2016	M.Rafenne
2.00	Update V1.10 / V2.00 (mod1)	13th, Feb 2017	R.Romes

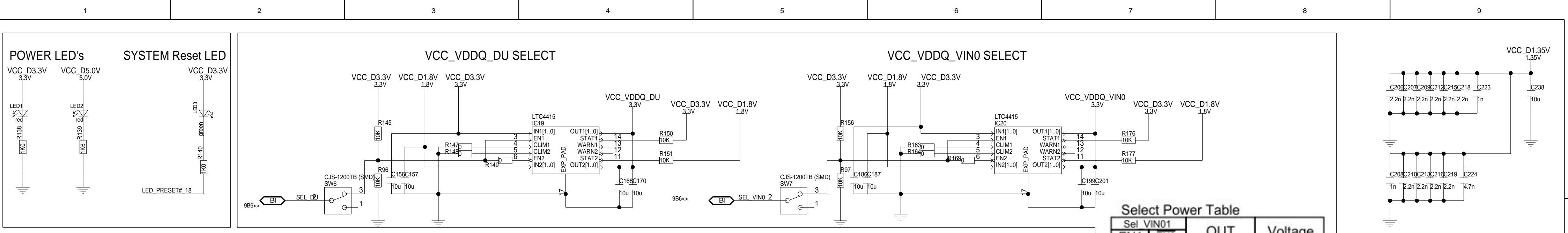
- P01: TITLE
- P02: Placement
- P03: R-CarV3M _POWER /Debug
- P04: R-CarV3M
- P05: R-CarV3M DDR3L
- P06: R-CarV3M HDMI
- P07: R-CarV3M ETHERNET
- P08: QSPI_Hyper_FLASH
- P09: MODE_SWITCH _ SCIF to USB/ HMI
- P10: R-CarV3M Connectors to Base Board

Preliminary

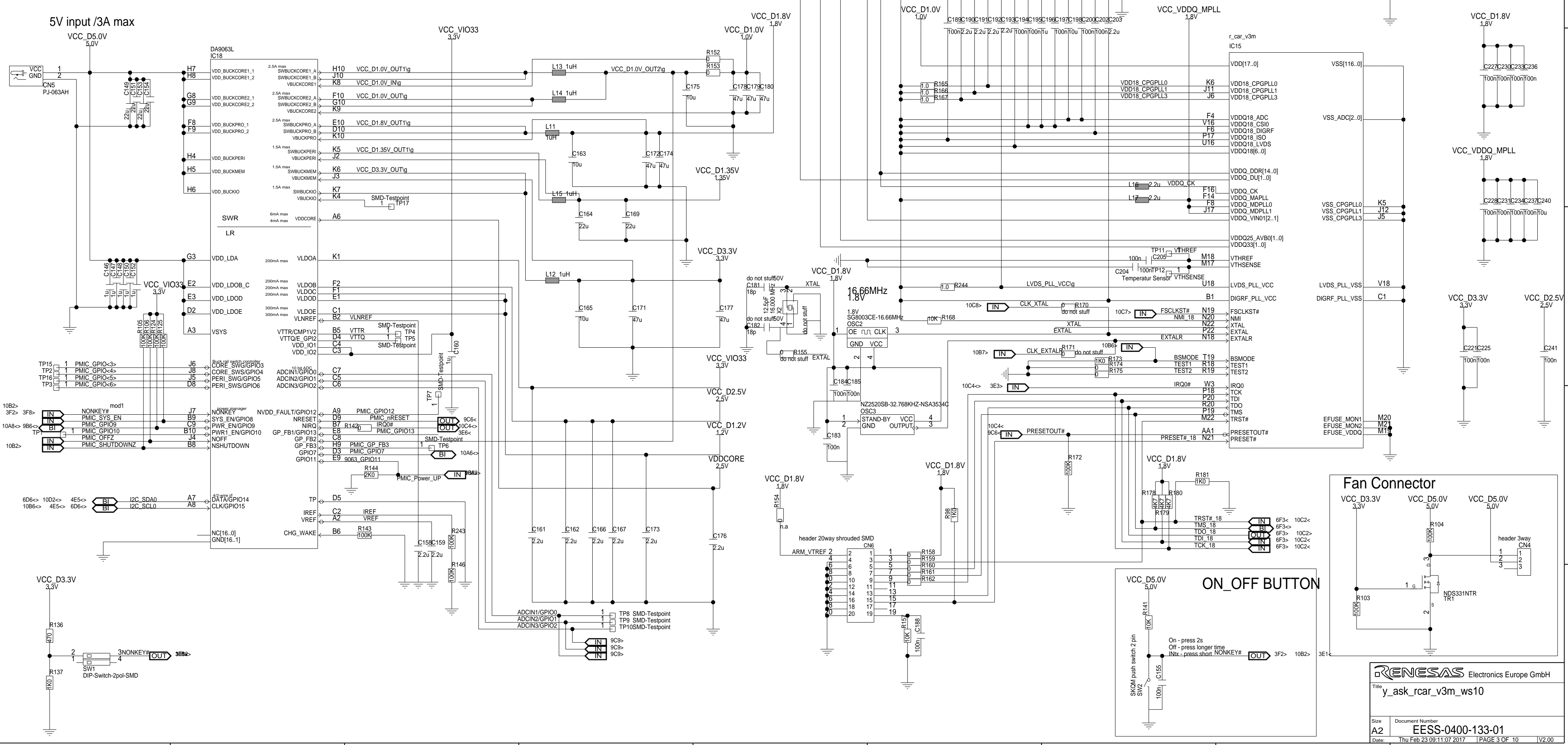
CONFIDENTIAL

P02: Placement

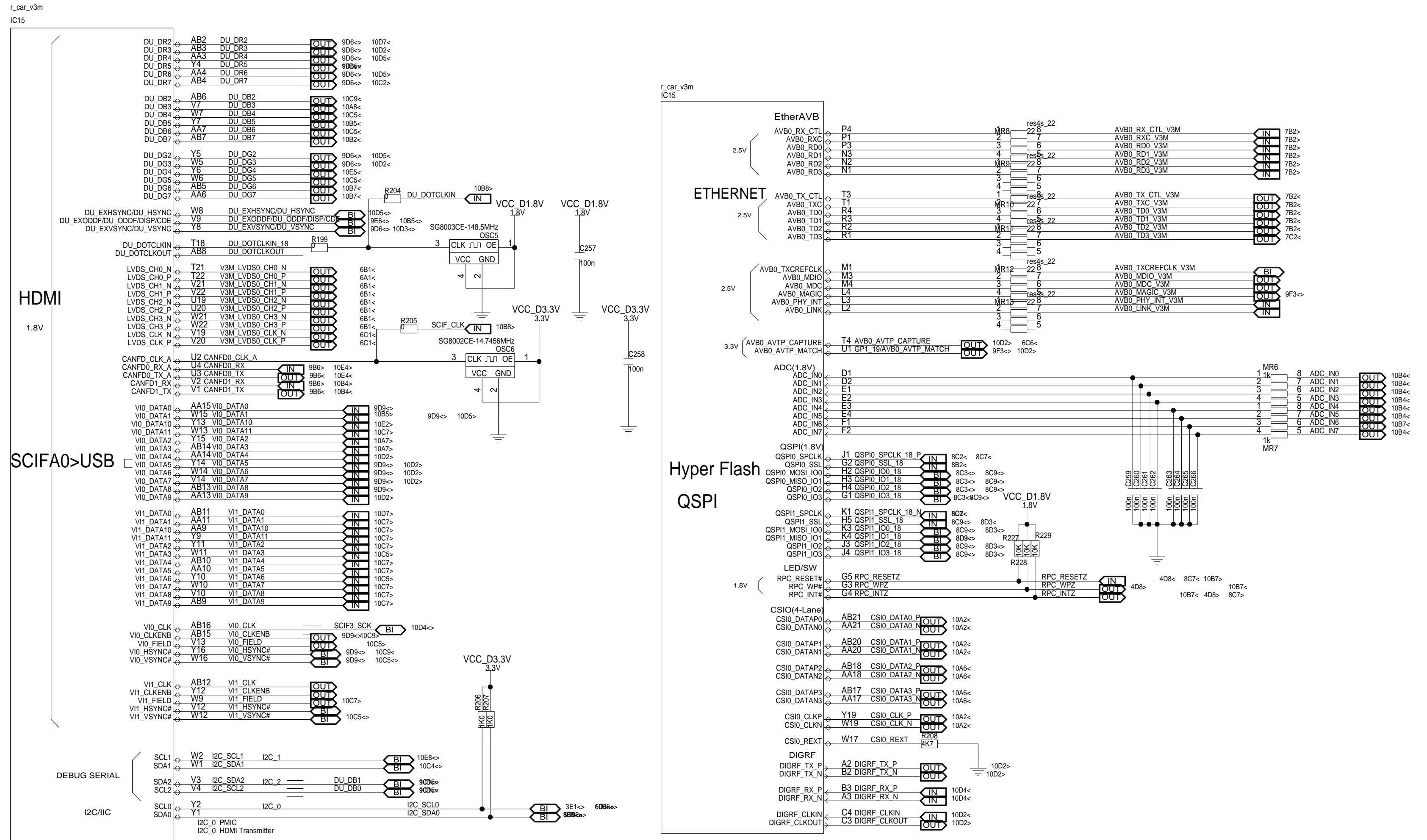




P03: R-CarV3M_POWER

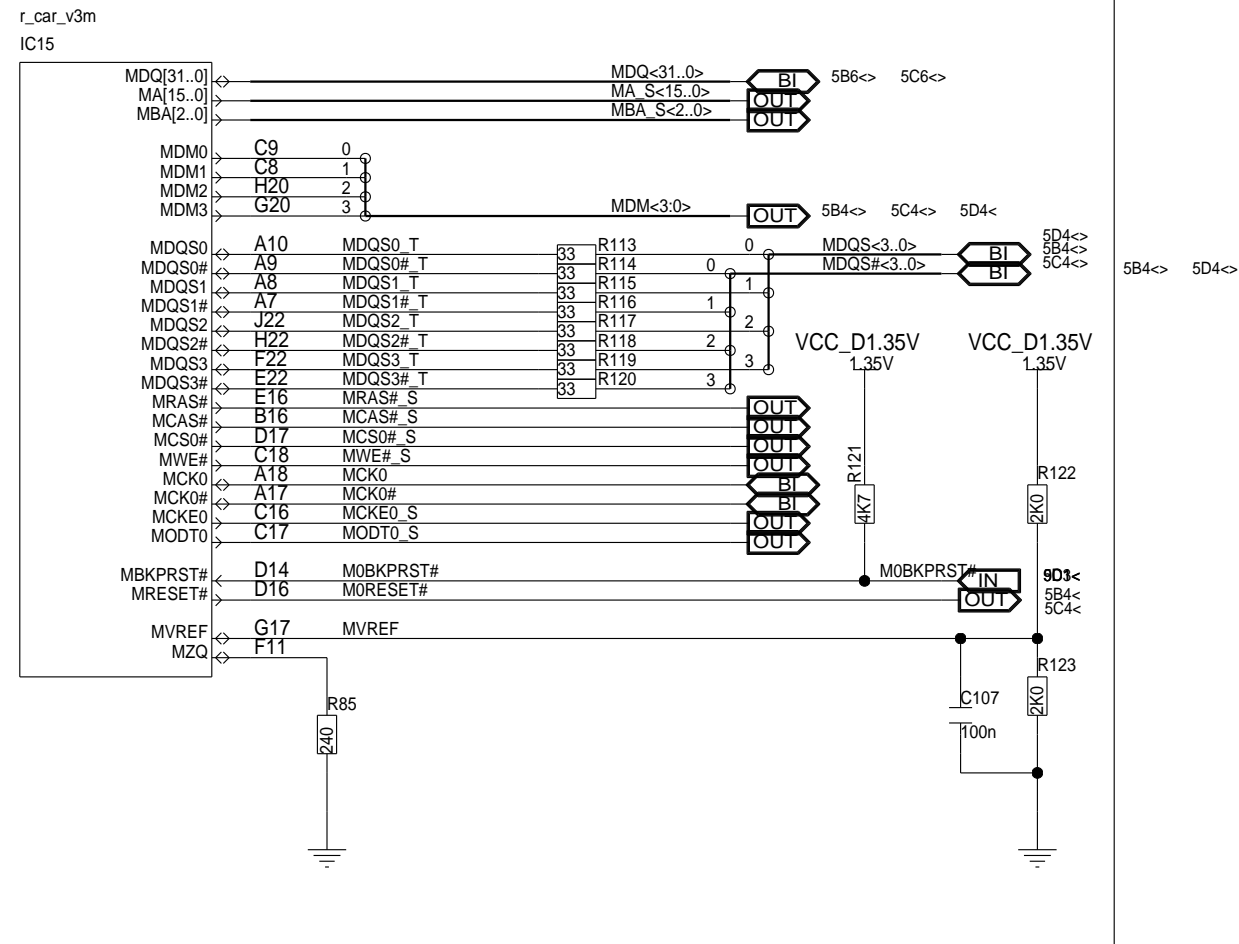


P04: R-CarV3M

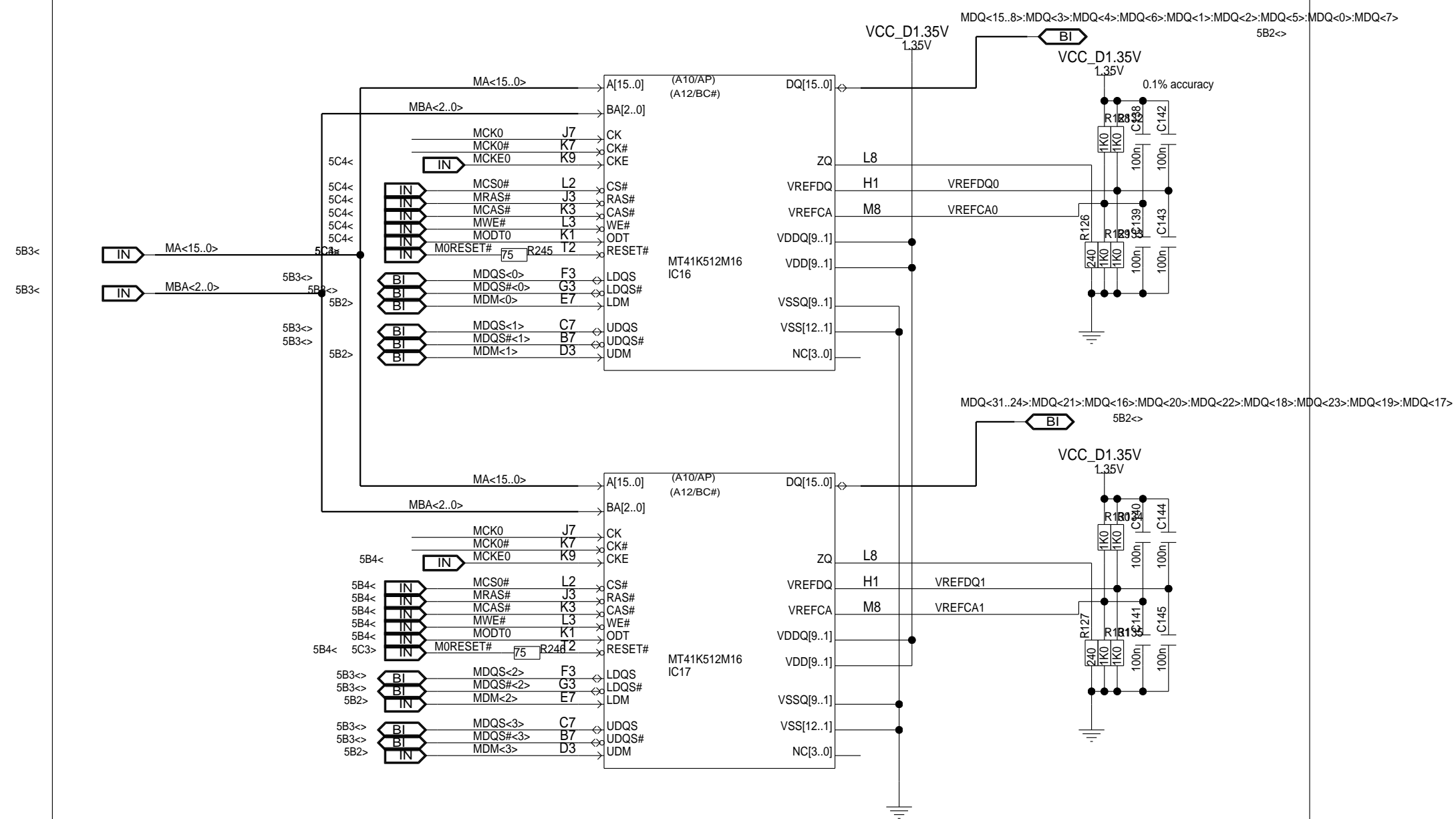


P05: R-CarV3M DDR3L

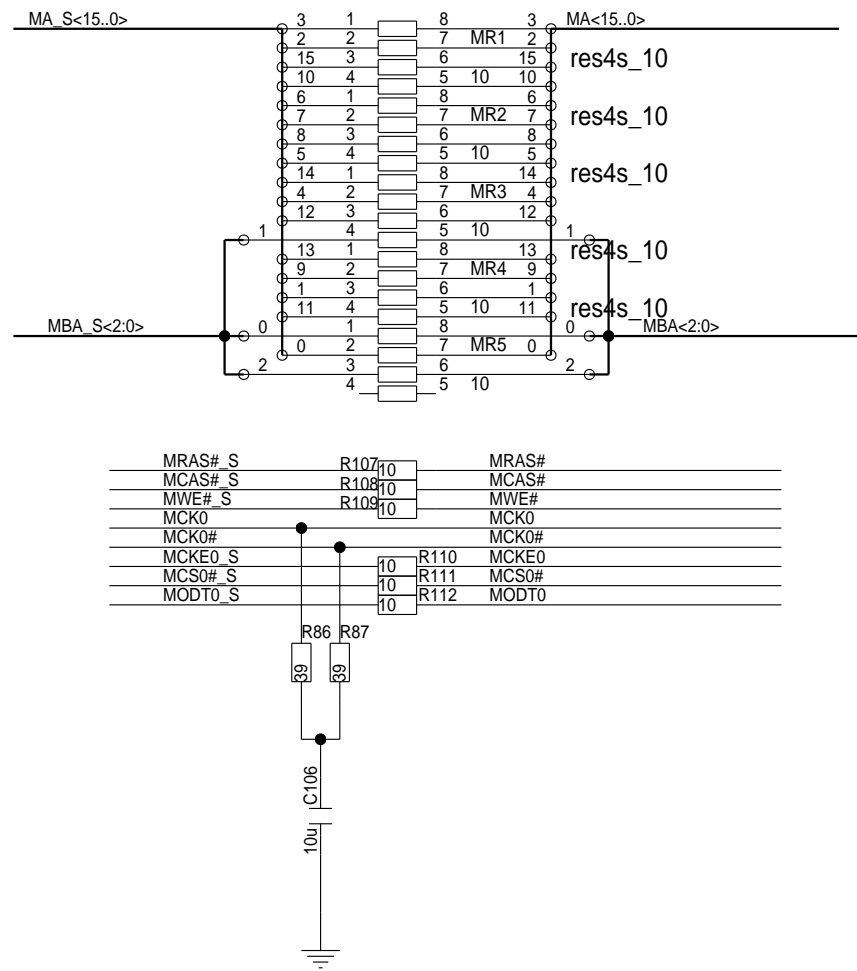
V3M DDR3L



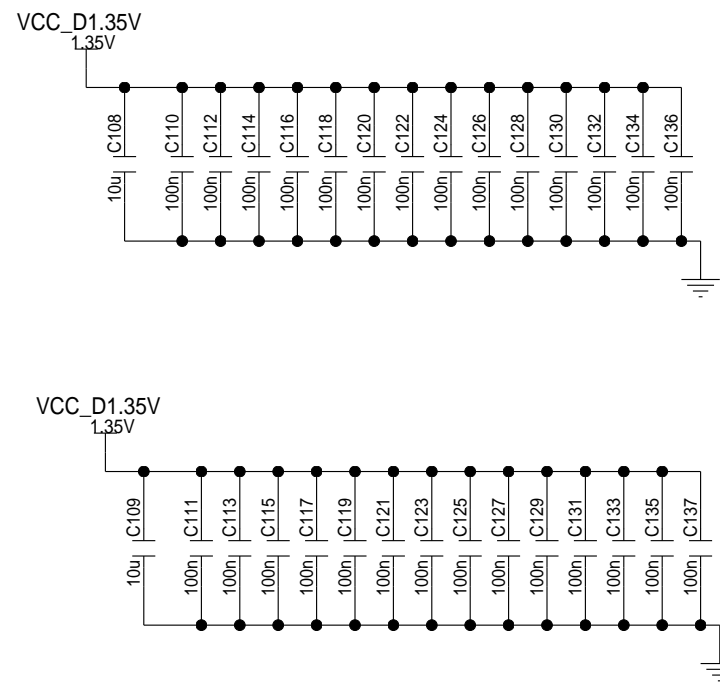
2 x DDR3 = 1Gbyte



Signals Termination



DDRs Decoupling



1GBx2 = 2GByte
Layout Note:

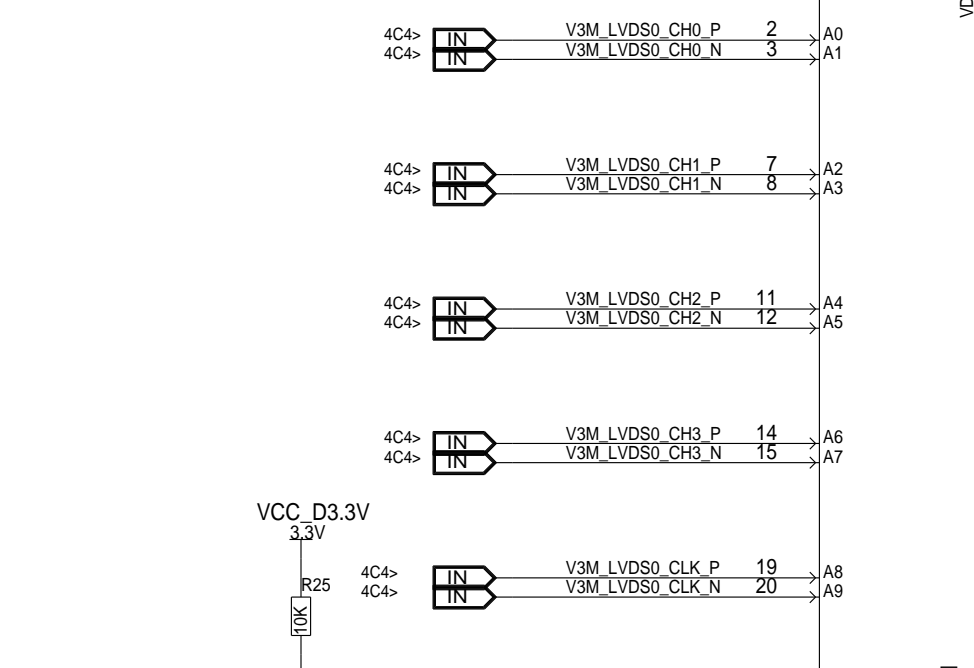
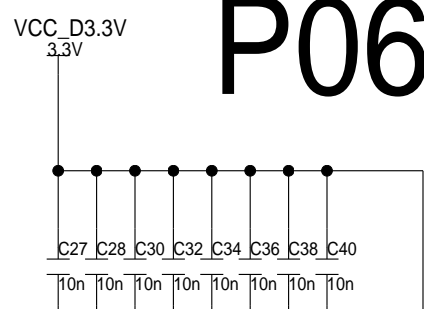
Following signals need Ground guard.
MCK0, MCK0#

P06: R-CarV3M HDMI

REV	COMMENT	DATE	DRAWN BY
1.00	Release	22/12/2016	M.Rafenne

LAYOUT!
LVDS(V3M, LVDS_CLK, V3M, LVDS[3:0])
(1) Matched trace length from V3M until IC9 (LVDS Receiver) and HSSTP Connector
(2) Differential Impedance= 100 ohm

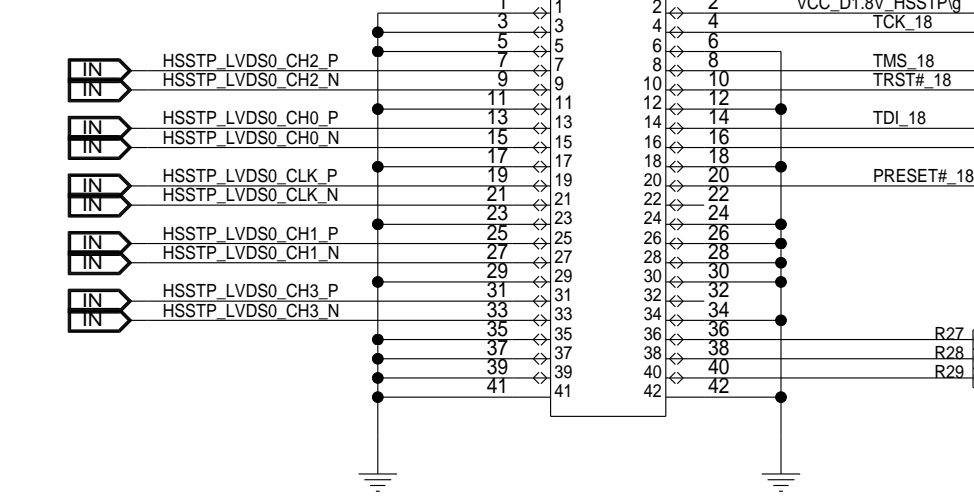
HDMI



[Design Note]
LVDS_SEL_SK- ON: Selects HDMI output side.
LVDS_SEL_SK- OFF: Selects HSSTP Connector side.

#[HSSTP 40pin] HSSTP Connector

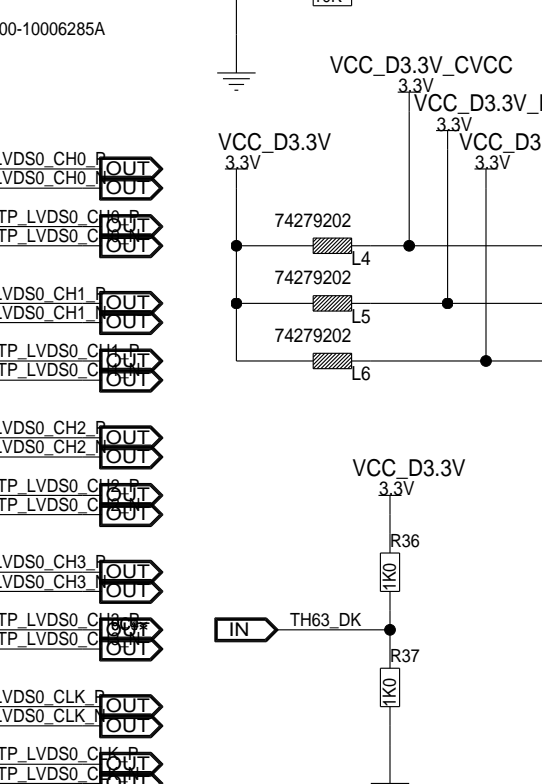
LAYOUT!
LVDS(HSSTP, LVDS, CLK, HSSTP, LVDS[3:0])
(1) Matched trace length from IC10 until IC11 (LVDS Receiver)
(2) Differential Impedance= 100 ohm



LAYOUT!
LVDS(SK, LVDS, CLK, SK, LVDS[3:0])
(1) Matched trace length from IC9 until comexpress connector
(2) Differential Impedance= 100 ohm



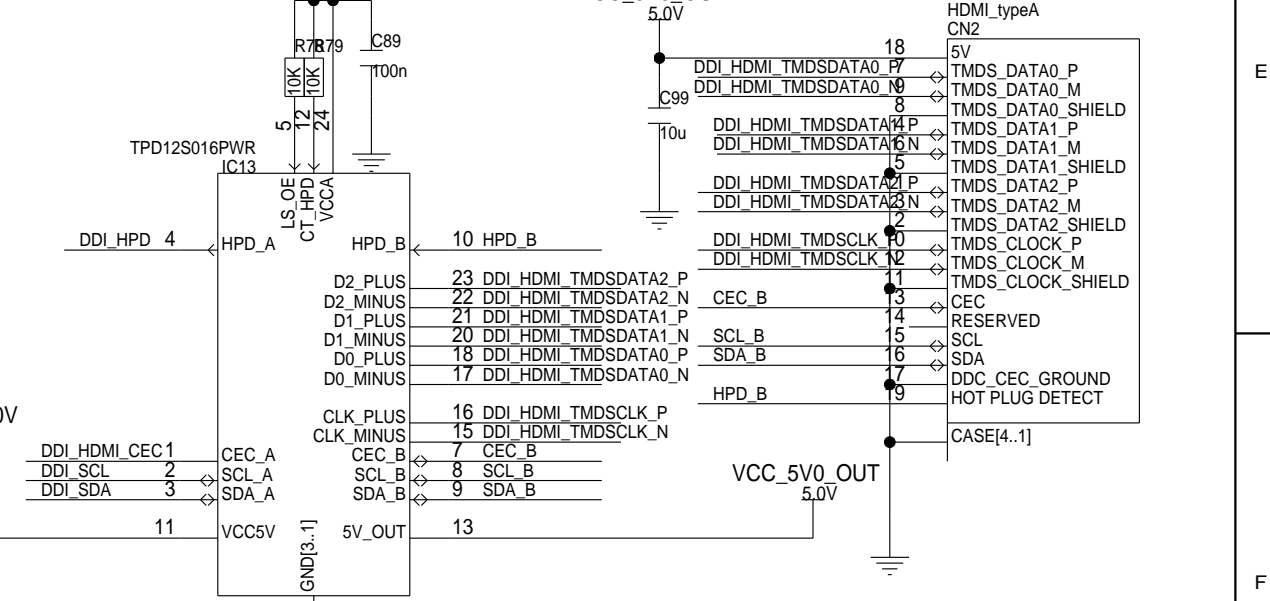
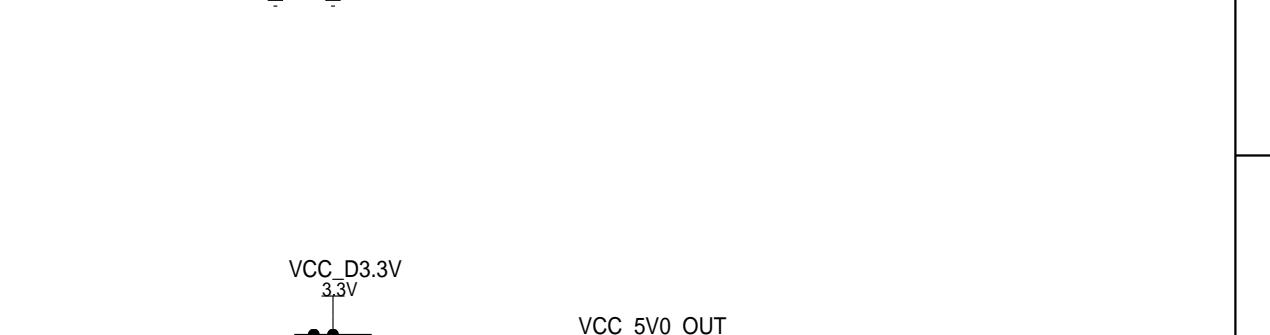
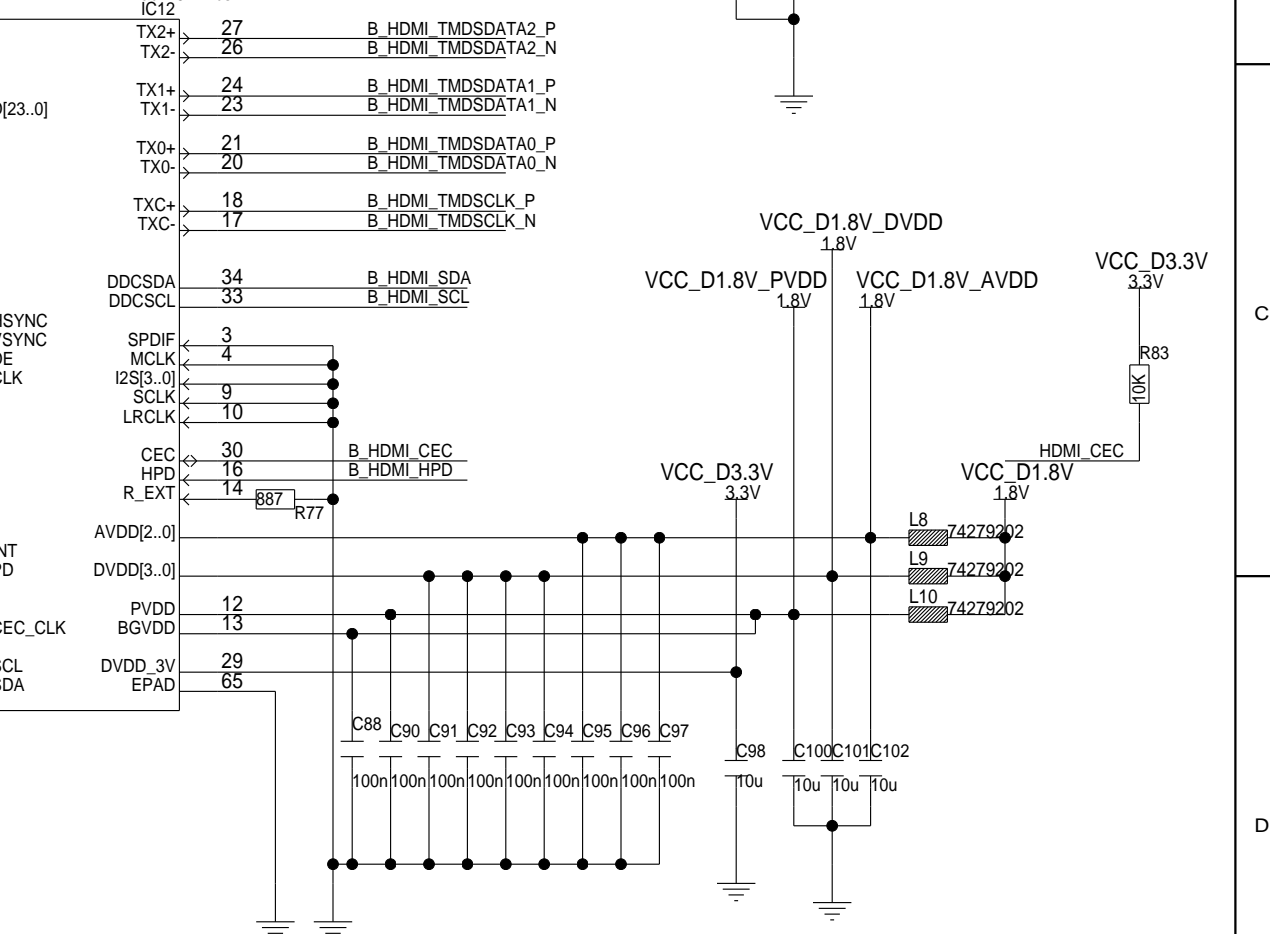
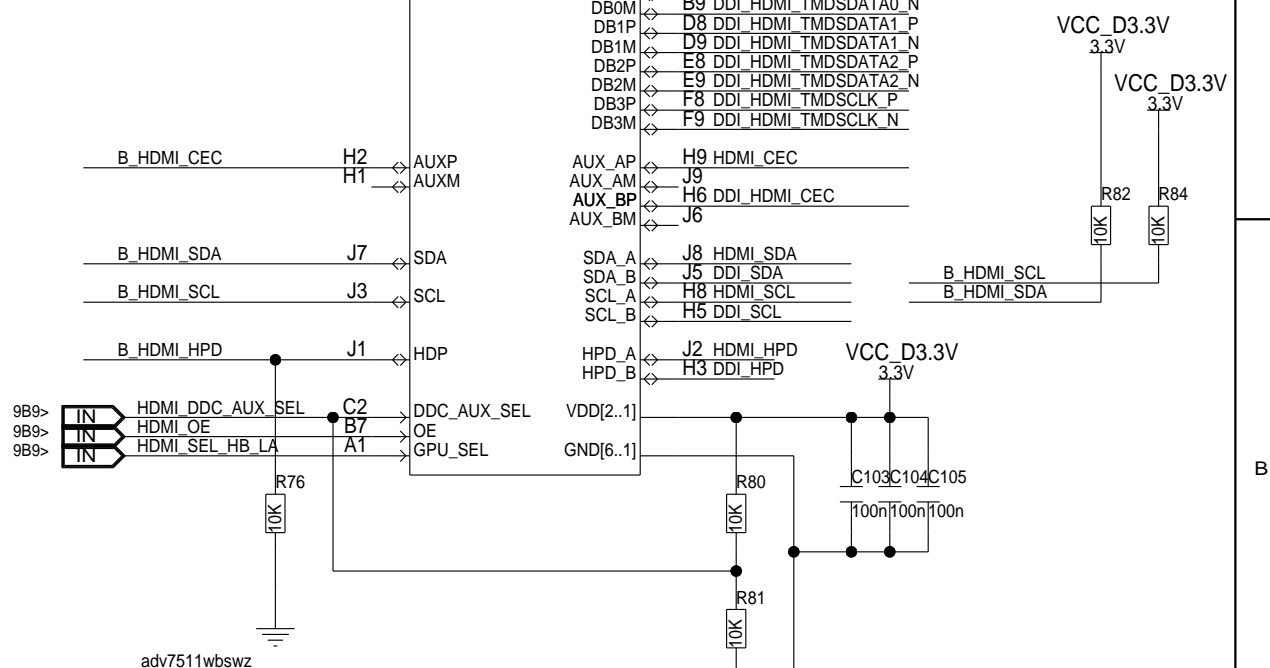
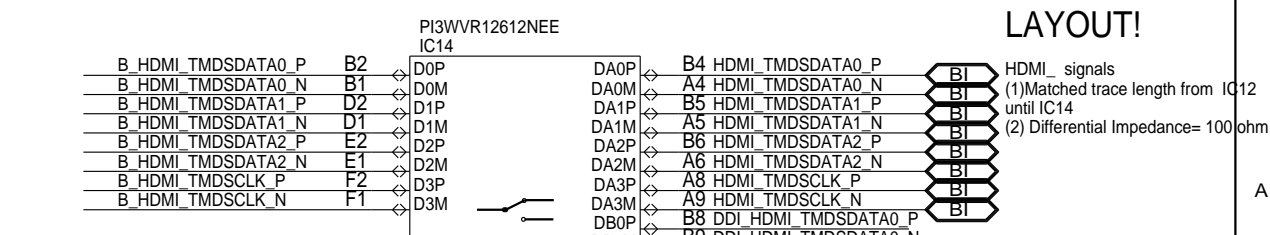
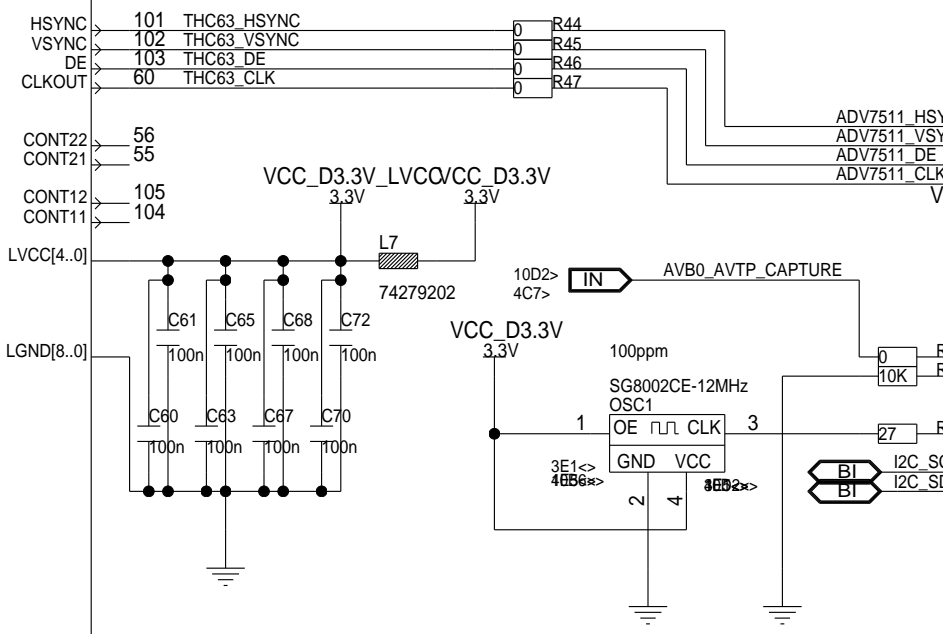
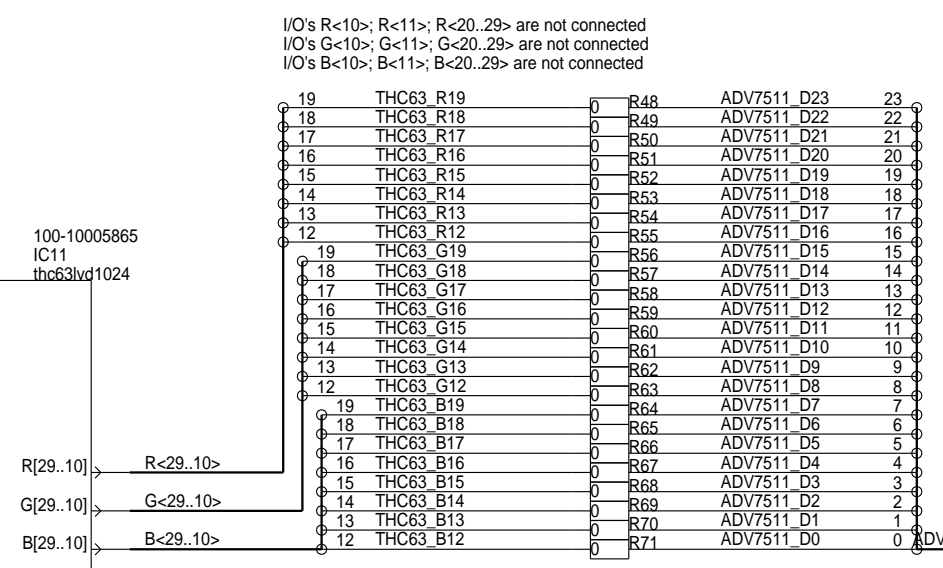
LAYOUT!
LVDS(TH63, LVDS, CLK, TH63, LVDS[3:0])
(1) Matched trace length from IC10 until IC11 (LVDS Receiver)
(2) Differential Impedance= 100 ohm



TH63_DK level can be HI or LOW !?

LAYOUT!

B HDMI signals
(1) Matched trace length from IC12 until IC14
(2) Differential Impedance= 100 ohm



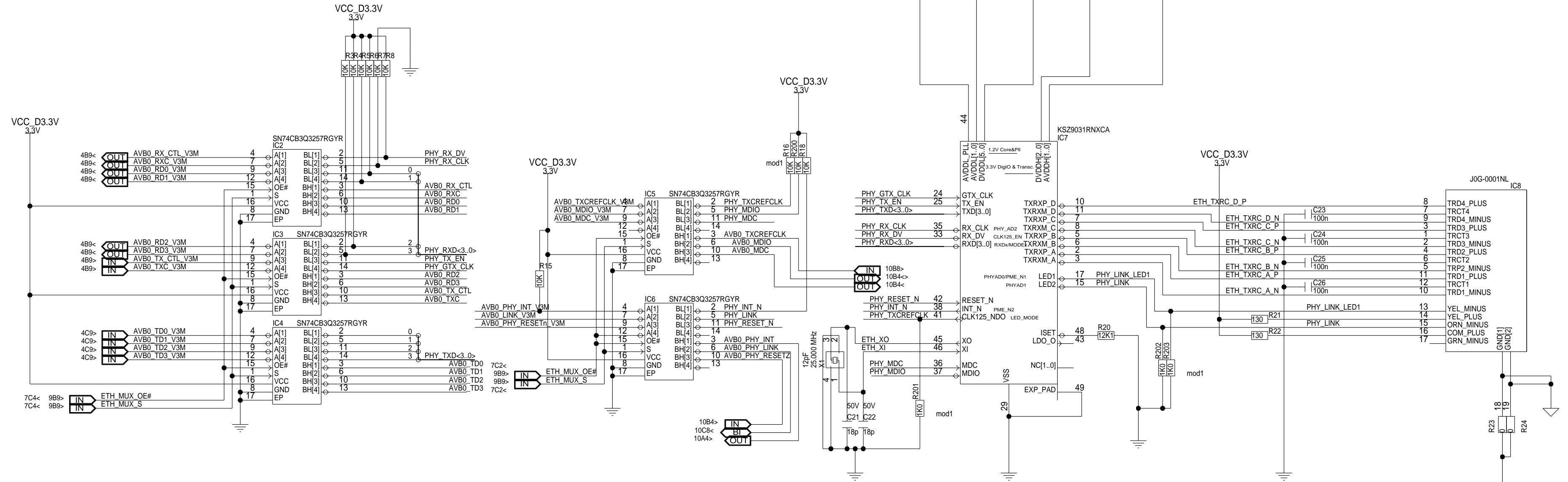
RENESAS Electronics Europe GmbH
Title: y_ask_rcar_v3m_ws10
DU (YCbCr3/LVDS), SDx, USBx...
Size: A2
Document Number: EESS-0400-133-01
Date: Thu Feb 23 09:11:08 2017 PAGE 6 OF 10 V2.00

P07: R-CarV3M ETHERNET

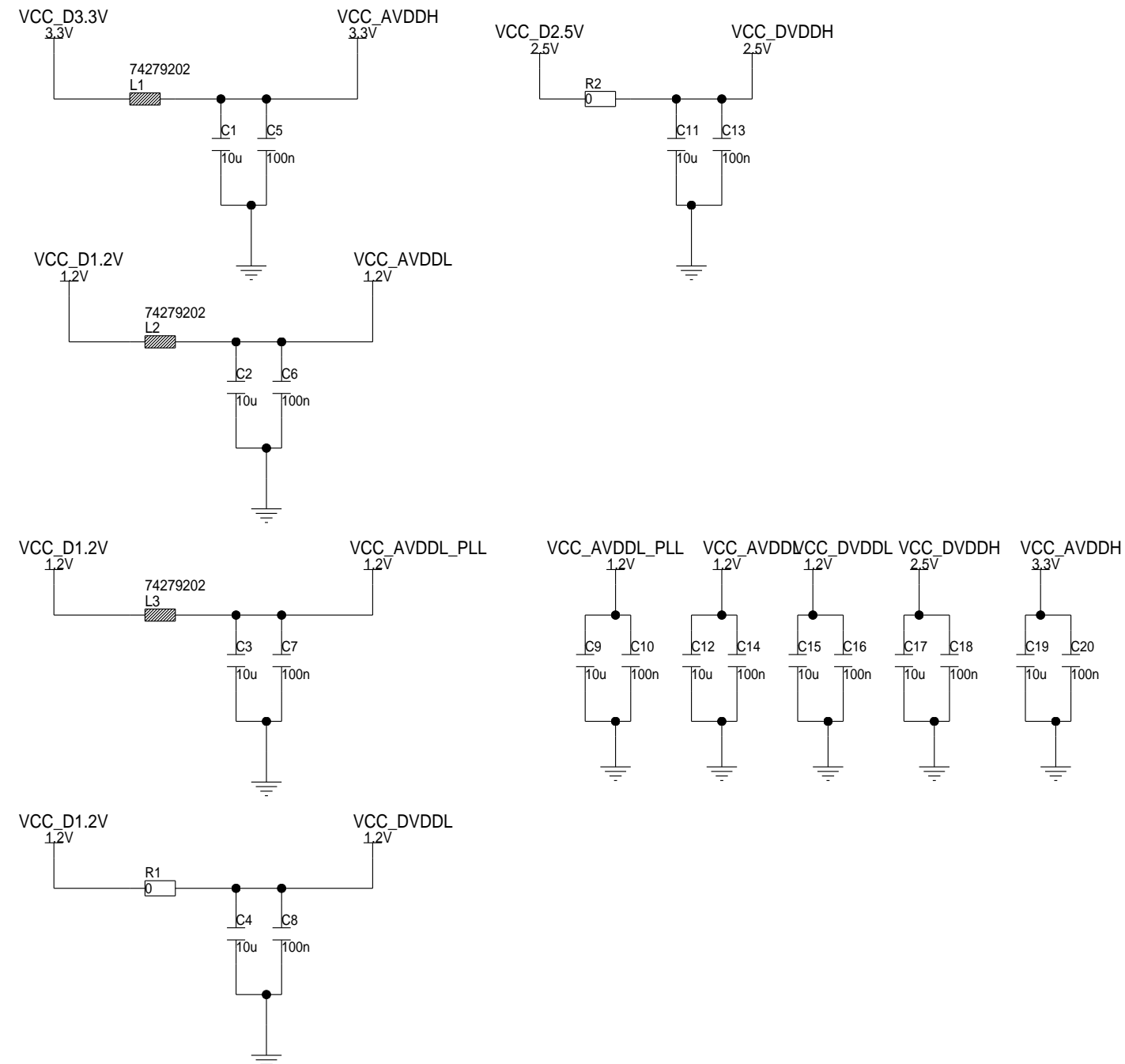
- Group 1
 AVB_TXC_V3M
 AVB_TX_CTL_V3M
 AVB_TD[3:0]_V3M
- Group 2
 AVB_RXC_V3M
 AVB_RX_CTL_V3M
 AVB_RD[3:0]_V3M
- Layout Note:
 Matched Trace Length from R-CarV3M to KS29031.
 (max 250Mbps/pin)

CPLD configuratrion

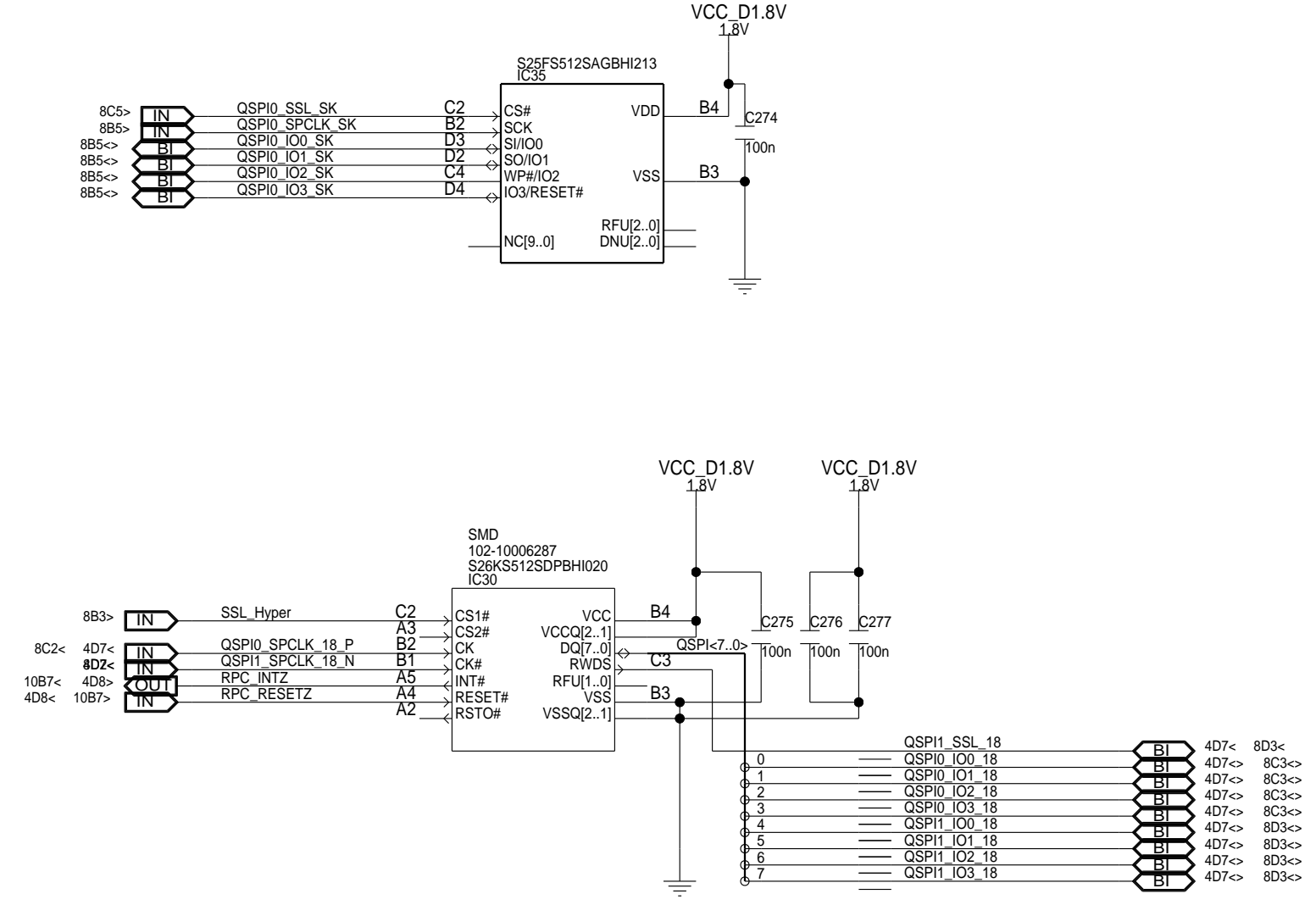
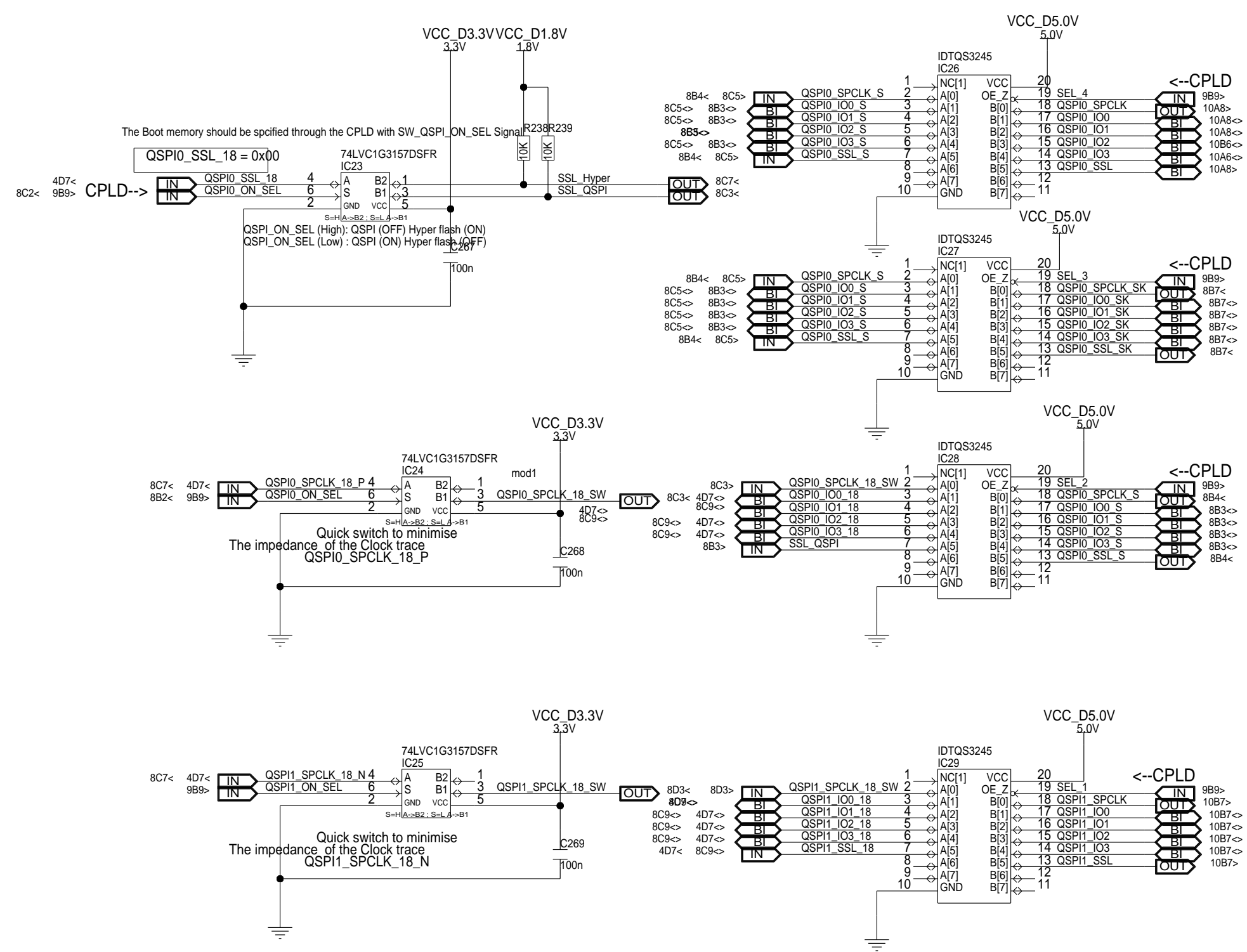
IF	and	Then
AVB0_MAGIC_V3M	PRESETOUT#	AVB0_PHY_PRESETn_V3M
0	0	0
0	1	0
1	0	0
1	1	1



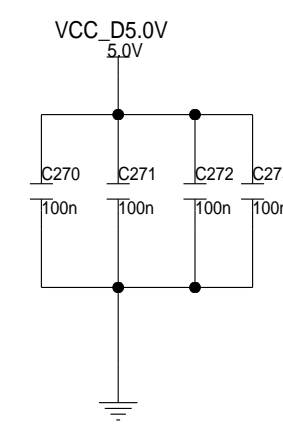
INPUTS		INPUT/OUTPUT	FUNCTION
OE	S		
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect



P08: QSPI_Hyper_FLASH

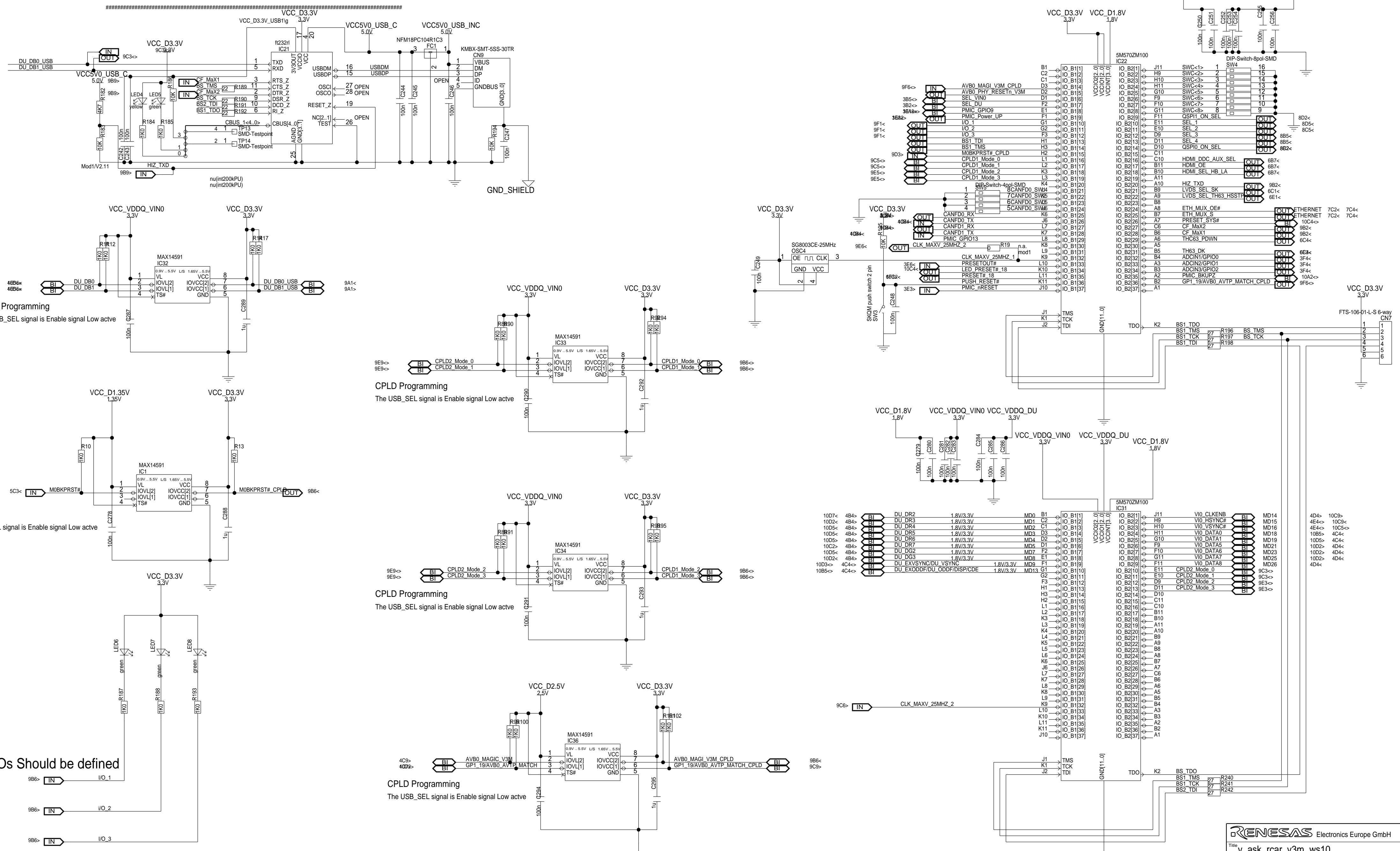


CPLD signals configuration	QSPI0_ON_SEL	QSPI1_ON_SEL	SEL_1	SEL_2	SEL_3	SEL_4
Hyper_Flash	1	1	1	1	1	1
QSPI0_on_board	1	0	1	0	0	1
QSPI0_Base	0	0	1	0	1	0
QSPI1_Base	0	0	0	1	1	1



P09: MODE_SWITCH / SCIF to USB/ HMI SCIF0>USB

Mode Pin setting via CPLD After RESET# release High Z



CPLD Programming
The USB_SEL signal is Enable signal Low active

CPLD Programming
The USB_SEL signal is Enable signal Low active

CPLD Programming
The USB_SEL signal is Enable signal Low active

CPLD Programming
The USB_SEL signal is Enable signal Low active

HMI OUTPUT/INPUT

P10: R-CarV3M Connectors to Base Board

