

5RCD0148HC3

DDR5 Register Command Address up to 4800MT/s

The 5RCD0148HC3 (RCD) is a registering clock driver used on DDR5 RDIMMs, LRDIMMs, and NVDIMMs. Its primary function is to buffer the Command Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus to control the data buffers for LRDIMMs.

The 5RCD0148HC3 contains two separate channels with some common logic such as clocking, but otherwise operate independently of each other. Each channel has a 7-bit double data rate CA bus input, a single parity input, two chip-select inputs, produces two copies of 14-bit single data rate CA bus outputs and two copies of the chip select outputs. The 5RCD0148HC3 has a common clock input and PLL, but produces separate clock outputs to the DRAM channels.

The following block diagram show the 5RCD0148HC3 in RDIMM and LRDIMM configurations.

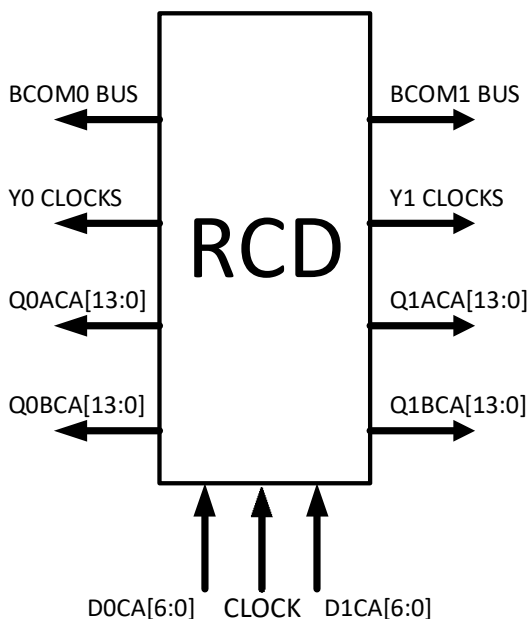
Typical Applications

- RDIMM, LRDIMM, NVDIMM modules for Enterprise Servers
- RDIMM modules for Telecom

Features

- Pinout optimized DDR5 RDIMM PCB layout
- DDR5 server speeds up to 4800MT/s
- Supports power-down modes to conserve server power
- Supports 1-rank/2-rank DIMM configurations
- Supports SDP, DDP, 3DS DRAM types
- Supports up to 16Gb DRAM die
- Provides access to internal control words for configuring device features and adapting to different RDIMM and system applications
- I3C sideband access for asynchronous register access control
- BCOM SidebandBus for LRDIMM data buffer control
- Loopback and pass-through modes
- Package: 8.7 × 13.5 mm, 240-FCBGA
- Available in commercial temp. range (0°C to 70°C) and industrial temp. range (-40°C to 105°C)

Block Diagram



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