ISL78365

Automotive High-Speed Quad Laser Diode Driver

FN8831
Rev 2.00
October 20, 2016

The ISL78365 high-speed, quadruple output Laser Diode Driver (LDD) is designed to support high speed RGB/RGGB laser scanning projection systems.

Each output driver channel consists of independent threshold and color DACs for greater laser control and flexibility. Separate scale DACs allow independent scaling of both threshold and color DAC output values to control the projector brightness or provide simple Automatic Power Calibration (APC) for laser based systems. Pixel data information is transferred through the LDD's high speed 10-bit parallel video interface. There are two parallel interface modes to allow three or four color pixel data to be entered efficiently. Pixel data employs a double data rate scheme, allowing video data to be transferred using both edges of the clock.

Applications

- RGB scanning laser projection system
- Laser-based projectors
- Generic laser-based applications requiring multiple independently controlled lasers or a single high current driver

Features

- High-speed quadruple output laser diode driver supporting up to 150MHz maximum output pixel clock
- Up to 750mA of peak current output per channel
- Fast output switching speeds with pulse rise/fall times of 1.5ns for crisp pixels
- Intersil laser voltage sampler function with integrated dynamic power optimization controller to dramatically minimize system power
- Flexible data order supports different RGB LD opto-mechanical placement
- Blanking time power reduction to reduce LDD current consumption
- Programmable multi-pulse Return to Zero (RTZ) function to provide maximum flexibility
- Single 3.3V supply and 1.8V video interface compatible for low power systems
- 3-wire SPI interface
- Operating temperature range: -40°C to +125°C
- AEC-Q100 qualified

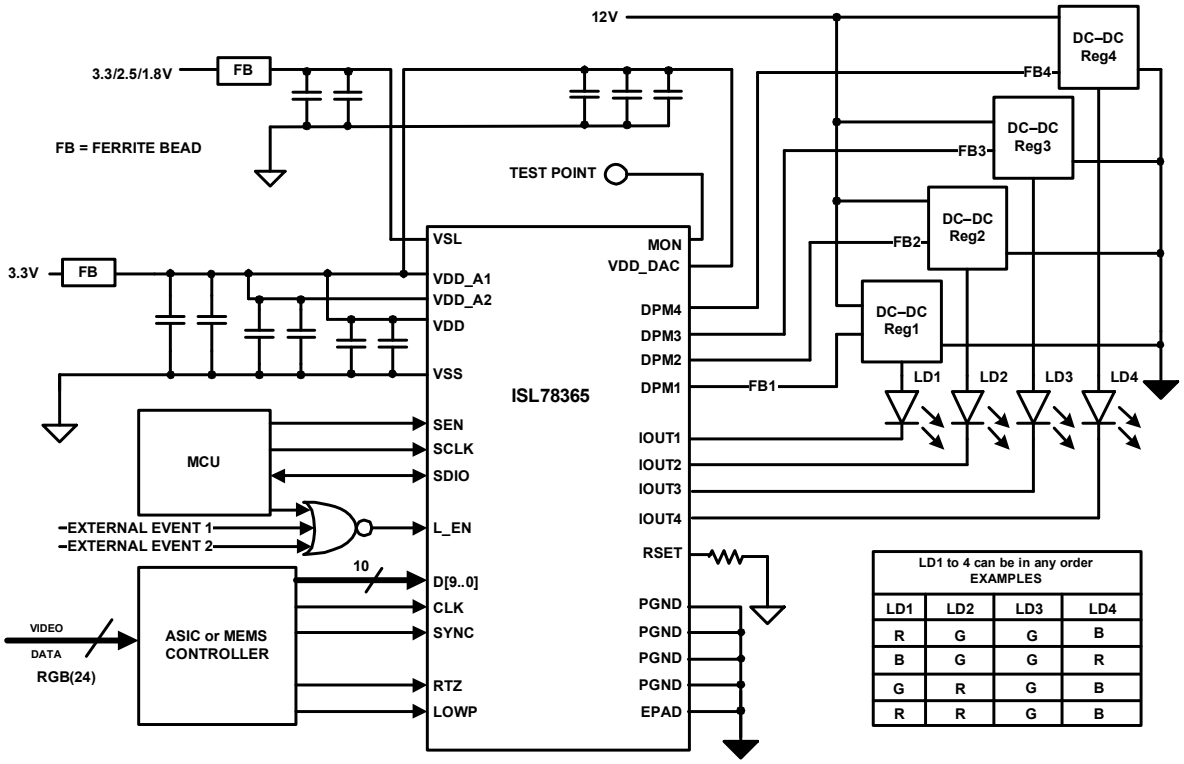


FIGURE 1. TYPICAL APPLICATION DIAGRAM

Functional Block Diagram

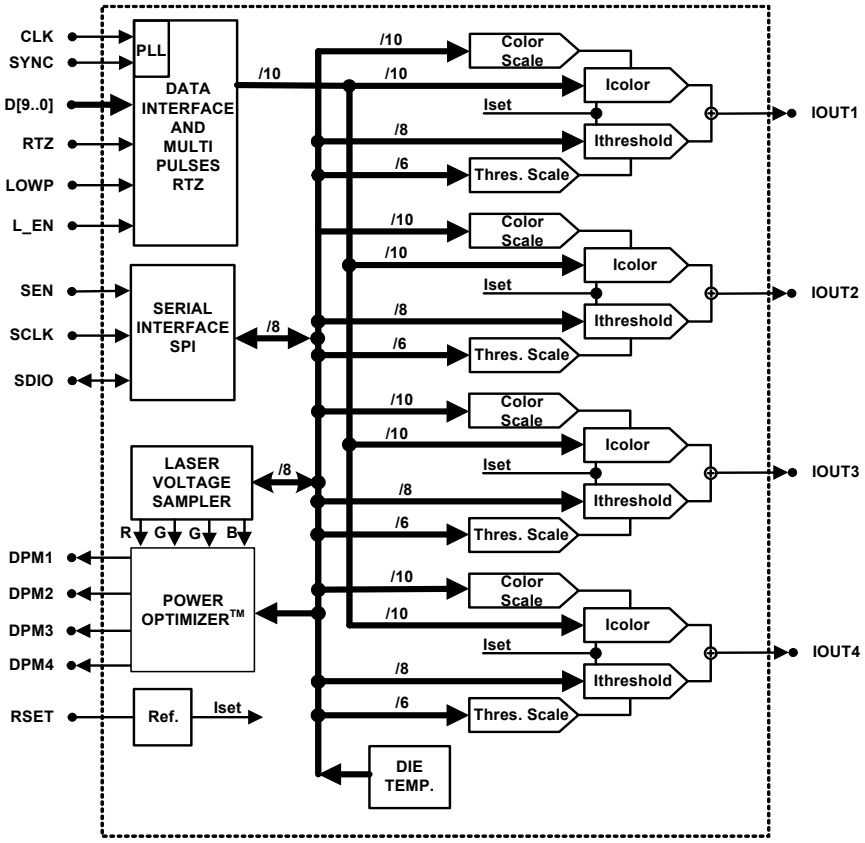


FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

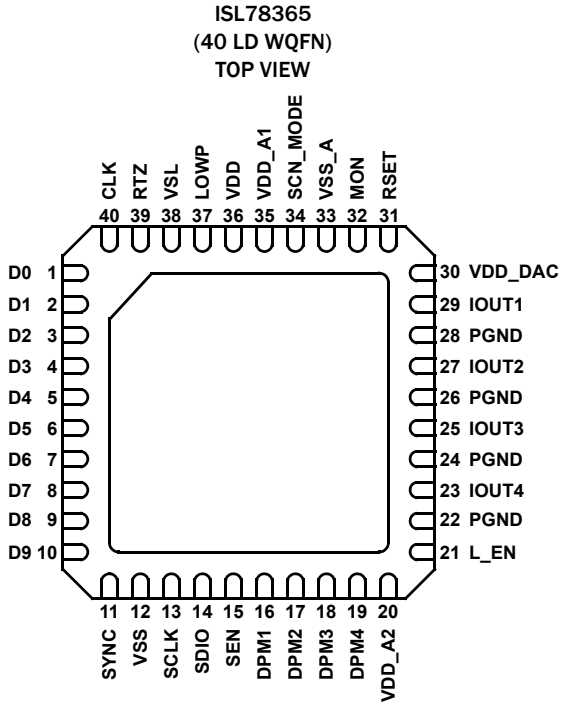
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL78365ARZ	78365 ARZ	-40 to +125	40 Ld WQFN	L40.6x6C
ISL78365EVAL1Z	Evaluation Board			

NOTES:

1. Add “-T” suffix for 4k unit or “-T7A” suffix for 250 unit Tape and Reel options. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see product information page for ISL78365. For more information on MSL, see techbrief TB363.

Pin Configuration



Pin Descriptions

PIN NAME	PIN NUMBER	I/O	PIN TYPE	PIN DESCRIPTION
D0	1	Input	Digital	D0 to D9 form the parallel interface data bus. These 10 pins (bits) form each I_{OUT} DAC's data. There are two modes on latching the data into the device These 10 signals can be operated at 1.8V, 2.5V, or 3.3V CMOS logic levels. The VSL pin configures this setting (see VSL pin for description). By default, it is 1.8V.
D1	2			
D2	3			
D3	4			
D4	5			
D5	6			
D6	7			
D7	8			
D8	9			
D9	10			
SYNC	11	Input	Digital	This pulse aligned with the CLK edge indicates the data on that edge is the final word of the sequence. The SYNC signal can be operated at 1.8V, 2.5V, or 3.3V CMOS logic levels. The VSL pin configures this setting (see VSL pin for description). By default, it is 1.8V.
SCLK	13	Input	Digital	The SCLK is the serial interface clock signal. It can be operated at 1.8V, 2.5V, or 3.3V CMOS logic level. The VSL pin configures this setting (see VSL pin for description). By default, it is 1.8V.
SDIO	14	Bi-Dir	Digital	The SDIO is the serial interface data signal. It can be operated at 1.8V, 2.5V, or 3.3V CMOS logic level. The VSL pin configures this setting (see VSL pin for description). By default, it is 1.8V.
SEN	15	Input	Digital	The SEN is the serial interface select enable signal. It can be operated at 1.8V, 2.5V, or 3.3V CMOS logic level. The VSL pin configures this setting (see VSL pin for description). By default, it is 1.8V.

Pin Descriptions (Continued)

PIN NAME	PIN NUMBER	I/O	PIN TYPE	PIN DESCRIPTION
DPM1	16	Output	Analog	Dynamic power management to control the voltage headroom at I_{OUT1}. This is current output and the current is sunk from this pin to ground. If DPM function is not implemented, this pin should be left open.
DPM2	17	Output	Analog	Dynamic power management to control the voltage headroom at I_{OUT2}. This is current output and the current is sunk from this pin to ground. If DPM function is not implemented, this pin should be left open.
DPM3	18	Output	Analog	Dynamic power management to control the voltage headroom at I_{OUT3}. This is current output and the current is sunk from this pin to ground. If DPM function is not implemented, this pin should be left open.
DPM4	19	Output	Analog	Dynamic power management to control the voltage headroom at I_{OUT4}. This is current output and the current is sunk from this pin to ground. If DPM function is not implemented, this pin should be left open.
L_EN	21	Input	Digital	The L_EN signal is an active high input with 1.8V logic threshold and it is 3.3V tolerance. It has a programmable current pull-up to VDD_A (3.3V) supply.
IOUT4	23	Output	Analog	Current output for the I_{OUT4} laser. Current is sunk from the laser cathode to ground. I_{OUT1}, I_{OUT2}, I_{OUT3}, I_{OUT4} have similar performance capability.
IOUT3	25	Output	Analog	Current output for the I_{OUT3} laser. Current is sunk from the laser cathode to ground. I_{OUT1}, I_{OUT2}, I_{OUT3}, I_{OUT4} have similar performance capability.
IOUT2	27	Output	Analog	Current output for the I_{OUT2} laser. Current is sunk from the laser cathode to ground. I_{OUT1}, I_{OUT2}, I_{OUT3}, I_{OUT4} have similar performance capability.
IOUT1	29	Output	Analog	Current output for the I_{OUT1} laser. Current is sunk from the laser cathode to ground. I_{OUT1}, I_{OUT2}, I_{OUT3}, I_{OUT4} have similar performance capability.
RSET	31	Output	Analog	The RSET pin connects to a resistor to ground the device to set the bias current for the device. A 13kΩ, 1% tolerance resistor is recommended value. The placement of the R_{SET} resistor must be as close as possible to the pin.
MON	32	Output	Test	This pin is reserved for factory testing. It must be left floating. Do not tie to ground.
SCN_ MODE	34	Input	Test	This pin is reserved for factory testing. This pin must tie to ground for normal operation.
LOWP	37	Input	Digital	LOWP is an active high input signal. When asserted, the device goes into the low power mode. The operating voltage is based on the VSL input voltage (see VSL pin description). A high resistance to ground resistor can be used to bias the pin to ground.
RTZ	39	Input	Digital	RTZ is an active high input signal. The operating voltage depends on the VSL input voltage and register 0x08[7:6] setting (see VSL pin description). When asserted, it causes the RTZ function to be driven on to the I_{OUTx}. If the RTZ function is not implemented, this pin should be tied to ground.
CLK	40	Input	Digital	CLK is the input data clock that latches the data D[0:9] into the parallel data interface. Data is latched on each edge of the CLK, thus its signal integrity is critical to correctly latching data into the device. If interface method chosen to use PLL only, the CLK pin should be tied to ground. The CLK can be operated with different voltage level and it is configured by the VSL pin (see VSL pin for description).
VDD_DAC	30	-	Power	VDD_DAC is the 3.3V supply pin for the output DACs. Due to large current changes during switching of these DACs, a good size decoupling capacitor pairs should be tied to this pin. We recommend the use of 10µF and 0.1µF capacitor pair with the smallest value capacitor placed closest to the pin.
VDD_A1	35	-	Power	VDD_A1 is the 3.3V supply pin for the DPM and other DACs. A decoupling capacitor pair of 0.1µF and 4.7µF should be tied to this pin with the smallest value placed closest to the pin.
VDD_A2	20	-	Power	VDD_A2 is the 3.3V supply pin for the DPM circuits. A decoupling capacitor pair of 0.1µF and 1.0µF should be tied to this pin with the smallest value placed closest to the pin.
VDD	36	-	Power	VDD is the 3.3V supply pin for the analog and digital block. A decoupling capacitor pair of 0.1µF and 1.0µF should be tied to this pin with the smallest value placed closest to the pin.

Pin Descriptions (Continued)

PIN NAME	PIN NUMBER	I/O	PIN TYPE	PIN DESCRIPTION
VSL	38	-	Power	VSL is the digital I/O pin supply rail. An 1.8V, 2.5V and 3.3V can be applied to this pin. The register 0x08 Bits[7:6] must be set to the applied voltage to correctly configure the I/O pin voltage threshold. This pin should be decoupled using an 0.01µF and 1.0µF capacitor pair to ground. The smallest value capacitor should be placed closest to the VSL pin. This pin sets the I/O voltage threshold for the following signals: CLK, D[0:9], SYNC, LOWP, RTZ, SCLK, SDIO, and SEN.
VSS_A	33	-	Power	VSS_A is ground return for VDD_A1 and VDD_A2. GND connections should be made on the PCB to all GND pins. Decoupling capacitors for VDD_A1 and VDD_A2 returns should be placed as close as possible to this pin.
PGND	22, 24, 26, 28	-	Power	These four pins are the ground returns for the I_{OUT} DAC.
VSS	12	-	Power	GND connections should be made on the PCB to all GND pins.
EPAD	PAD	-		This is the thermal pad of the device and can be connected to ground. It is important to remove as much of the thermal heat away from the device as possible. We recommend placing a thermal pad under the EPAD using our guideline given in the “General PowerPAD Design Considerations”.

NOTE: Pins with the same name are internally connected together.