P8620

Programmable Multi-Channel PMIC Solution for Intel Industrial SOCs

The P8620 is a Cortex™ M0 based multiple channel Power Management Integrated Circuit (PMIC) designed to meet high-performance requirements as well as to provide a high level of integration to minimize system board area and BOM.

The PMIC includes sub-systems for voltage regulation, power sequencing management, A/D conversion, I2C/SPI and SVID communication, and programmable GPIOs, to meet the Intel VR 13.0 specification.

The P8620 incorporates five independent Distributed Power Unit (DPU) controllers that can support up to four P8610 DPUs (allowing up to 29A of pulsed load current) per rail. Four internal Buck regulators provide additional rails. A proprietary multi-protocol single-wire digital bus connects the host PMIC to the DPUs to provide control and exchange status information. The DPUs seamlessly integrate into the PMIC eco-system and are transparent from a user point of view.

The P8620 PMIC integrates many advanced features that are user-programmable to allow the attached DPUs to be optimized either for efficiency, transient response and/or standby power. The PMIC also supports output current measurement of the DC/DC rails and includes safety and diagnostic functions to allow easy debug of a prototype system.

The P8620 has firmware developed for the Intel Tiger Lake UP3/ Corner Stone Ridge customer reference board (CRB) and the Intel Tiger Lake H/Whale Mountain CRB.

The device is available in a thermally enhanced 9 × 9 mm 64-QFN package.

Note: The functionality of this PMIC is defined by its firmware code running on the internal Cortex M0. The functional description and pin mapping documented in this document may change based on the specific platform implementation. For every firmware option, there will be a detailed implementation document.

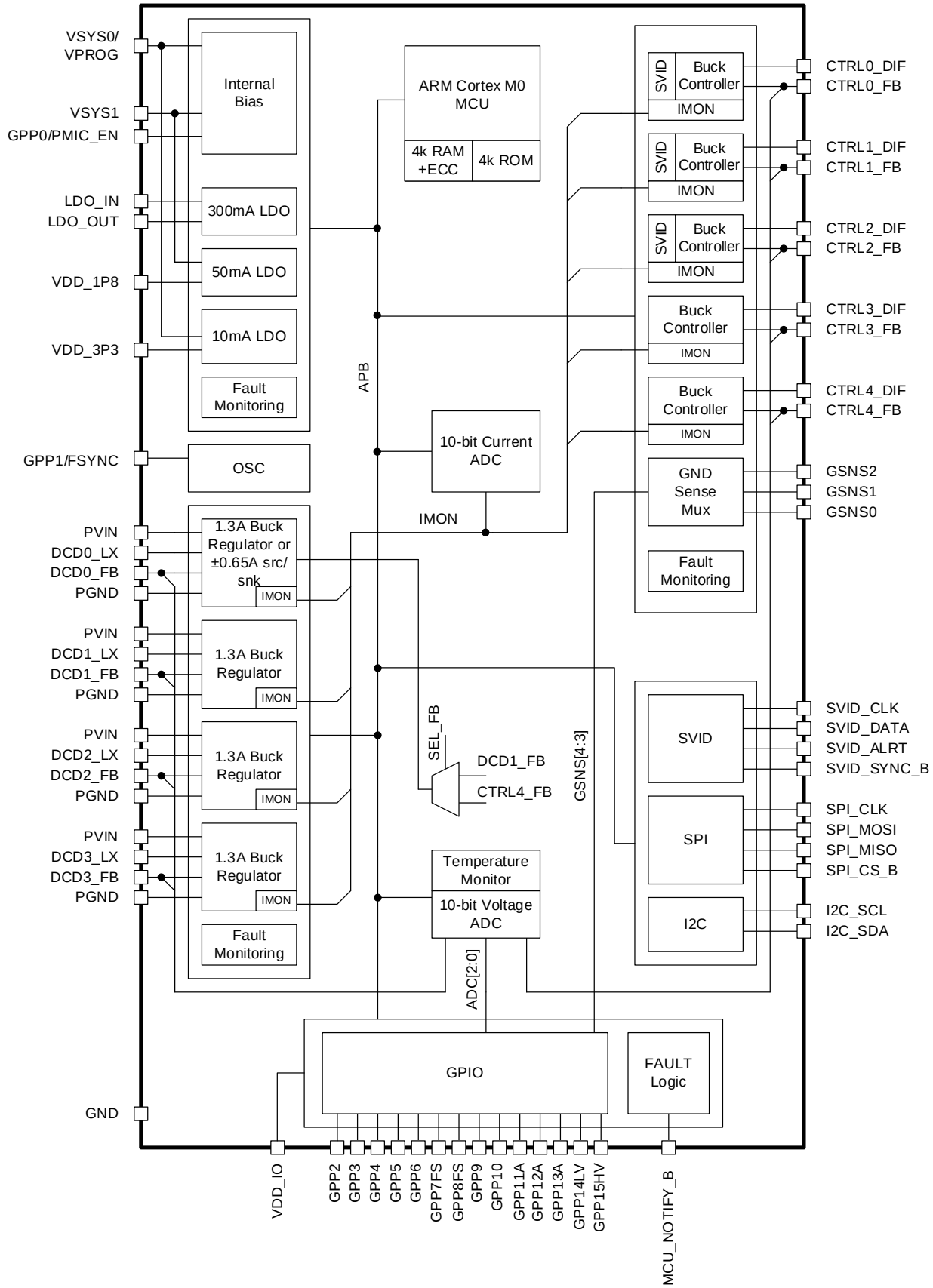
Features

- Operates from 4.2V to 5.5V supply
- Four Buck Regulators with internal FETs, one configurable for source/sink capability
- Five Buck Controllers (for external DPUs)
- Individually configurable output voltage for each rail
- Individually configurable sequence for each rail
- Intel VR 13.0 compliant
- Three LDOs
- Two 10-bit ADCs
- Monitors internal and external voltages, die temperature and rail currents
- High-speed SPI Master/Slave interface (up to 8MHz)
- High-speed I^2C Slave interface (up to 3.4Mbps)
- Failure analysis and reporting
- Usage monitoring and reporting
- Interrupt controller alert to SOC
- 16 programmable GPIOs
- One high-voltage capable GPIO for driving external OVP switch
- -40°C to +85°C ambient operating temperature range
- 64-QFN, 0.5mm pitch, 9 × 9 mm package with 7.7 × 7.7 mm Epad

Applications

- SOC power management

1. Block Diagram



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