RENESAS

RAA225019

Configurable, 6-Phase, 3 Output Client Computing PMIC for IMVP9.2 Applications

The RAA225019 is a highly configurable PMIC for Intel IMVP9.2 Lunar Lake applications. It features fully integrated power MOSFETs and current-sensing circuitry, which when coupled with high switching frequencies makes it well suited to small form factor applications without compromising efficiency.

Six phases can be distributed across three outputs (two SVID rails and one auxiliary rail). The SVID1 rail operates from a max phase count of 2 to 6 while the SVID2 and BUCK3 rails can run either a 1 or 2 phase configuration. Additionally, the device contains an integrated LDO with Power Gate bypass option.

The PMIC uses the Renesas Robust Ripple Regulator technology with its many advantages as compared to traditional modulation schemes. Output capacitance requirements are minimized because of fast transient settling time and a variable switching frequency in response to load transients. Light load efficiency is boosted in DCM because of natural period stretching at low load currents.

Input voltage, output current, temperature, and PSYS telemetry is available through the addition of an I^2C bus. This bus also allows for integrated compensation to further reduce BOM cost and PCB area.

Features

- WLCSP package of 12×9 ball array in 0.4mm pitch, approximately 5.04mm×3.74mm in size
 - Total height of 0.525mm including solder balls supporting ultra low profile design
- Input voltage range from 2.7V to 4.5V
- Integrated FETs and current sensing for small form factor designs
- 6 phases configurable over 3 outputs 2 SVID rails and 1 auxiliary rail
- Integrated LDO with a power gate bypass option
- Switching Frequency of 2MHz across rails, supporting small form factor chip inductor
- Cycle-by-cycle current limiting feature supports
 Fast V-Mode (FVM) operation
- Automatic phase add/drop for optimal efficiency over the entire load current range.
- Output current, temperature, and PSYS telemetry available through SVID and I²C Bus

Applications

- Low power mobile devices



Figure 1. Simplified System Diagram





Figure 2. Block Diagram



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