ISL70002SEH

High Power, High Temperature Operating Life (HTOL) at High Currents

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Abstract

The ISL70002SEH device was recently recommended for use at increased current levels up to 22A. This new recommendation comes with caveats outlined in this and other supporting documentation. In the course of production, all ISL70002SEH devices are exposed to high temperature burn-ins totaling 288hrs at +135°C, as part of production screening focused on voltage stress induced infant failures. That burn-in stress, however, does not include a high power operational condition where the IC is subjected to a high power dissipating condition. This technical brief will demonstrate that the ISL70002SEH output power structure is robust to power excesses beyond that of the newly recommended operating conditions.

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Related Literature

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- ISL70002SEH product page

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1. Introduction

Four ISL70002SEH devices were subjected to a high power test for 2000hrs at T_A = +125°C, each biased with an input voltage of 5V, an output voltage (nominally 2V) adjusted to keep an output current of 22A minimum equivalent with the switching frequency set to 500kHz.

On each device, only three (2, 6, 9) of the ten power blocks were used (the other seven LX pins were lifted) and biased with a minimum output current of 6.6A to a maximum of 7.8A to equate to the current density in each power block of a 22A to 26A current load with all ten power blocks in use. This was done to reduce the die temperature to a level that was non-destructive, yet run at an excessive power block current density, and have enough power blocks being stressed on each device.

2. Test Information and Procedure

Measuring the die temperature was done in the proposed 5V input to 2V output at 500kHz to characterize die temperature over output current. Table 1 details the measured die temperature with all ten power blocks in use. Decreasing the number of power blocks allowed for the higher current density to be achieved without destruction due to excessive Si temperature. Die temperature was measured with a thermocouple affixed to the die surface.

Table 1. Measured Die Temperature at 5V input to 2V Output at Room Ambient Temperature (Ten Power Blocks).

Output Current (A)	Temperature (°C)
0	29
5	39
10	67
15	122
20	186

This data was taken on the package option that does not have the heat spreader underneath and the four parts used in the excessive current testing were also of the non heat spreader variant providing a worst case thermal characteristic in the stress test. The package with the heat spreader is the only recommended package variant when using the newly extended output current operation. This data also highlights the need for implementing effective die thermal management. During the stress test, the top of the four packages were occasionally monitored and the four devices ranged from +150°C to +200°C. This wide range was a result of passive component changes that caused lower currents from the initial ~8A setting and higher output voltages over the initial 2V setting. Current loading and output voltage adjustments were made to maintain the intended stress conditions.

With four parts mounted on ISL70002SEHEVAL1Z evaluation boards, the input voltage was set to deliver 5.1V on each board with the output voltage initially set to 2V across a 0.25Ω, 50W resistor to ensure the ~8A desired current load. This current level was, in addition to the previously mentioned reasons, chosen to ensure the die temperature was below the temperature at which the internal SYNC signal frequency is perturbed and shown to be drifting at the in-oven temperature of +125°C.

On a separate device operating at the initial test conditions, the die temperature was measured at ~+166°C with a thermocouple affixed to the die surface and the lid taped to reduce moving air effects, mimicking the DUTs as much as possible.

The stress test with a die temperature range of +150°C to +170°C provides an aging acceleration of three to eight times at an operating die temperature of +125°C with an activation energy of 0.7eV.

The purpose of this stress test was to monitor for any resulting deleterious effects on device performance, particularly efficiency. The reference voltage and efficiency data were taken at 0hr and at the 2000hrs downpoint for comparison.

3. Test Results

With the four parts mounted on the ISL70002SEHEVAL1Z evaluation boards used in the stress test, the reference voltage and efficiency comparisons are provided below.

Table 2 details the 0.6V reference voltage over the 2000hrs of the stress test.

Table 2. V_{REF} (mV) PRE and POST High Power Stress

Part Id	0hr	2000hr
1	599	598
2	598	598
3	600	600
4	599	599

As expected, there was no change in the reference voltage.

The following graphs illustrate the change in efficiency over the 2000hrs excessive current stress testing.

Having experienced passive component changes, leakage, and failure during the stress test it was decided to remount Parts 1 and 2 onto unstressed boards for retesting, Parts 3 and 4 were not.

Figure 1 displays the efficiency curves for the Number 1 device pre and post on an unstressed board after the 2000hr high power stress. There is minimal difference between the two test points.

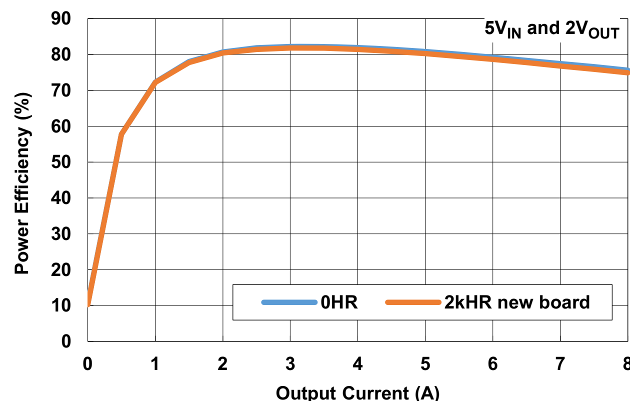

Figure 1. Number 1 Pre and Post (Unstressed Board) High Power Test Efficiency Curves

Figure 2 displays the efficiency curves for the Number 2 device pre and post on an unstressed board after the 2000hr high power stress. There is a significantly higher efficiency seen post test than at 0hr. Comparing this data to the post test for the other three devices provides the very likely explanation that the 0hr efficiency data was faulty and incorrectly low.

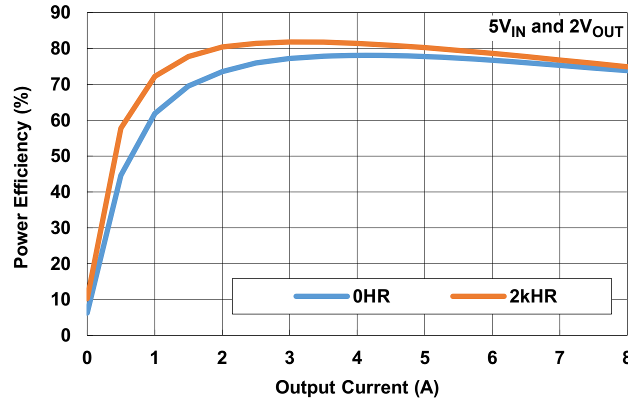

Figure 2. Number 2 Pre and Post (Unstressed Board) High Power Test Efficiency Curves

Figure 3 displays the efficiency curves for the Number 3 device pre and post 2000hr high power stress test. There is a slight difference over time.

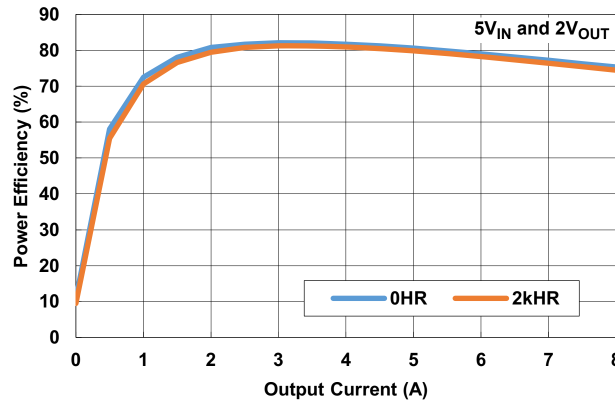

Figure 3. Number 3 Pre and Post High Power Test Efficiency Curves

Figure 4 displays the efficiency curves for the Number 4 device pre and post 2000hr high power stress test. There is little difference over test time.

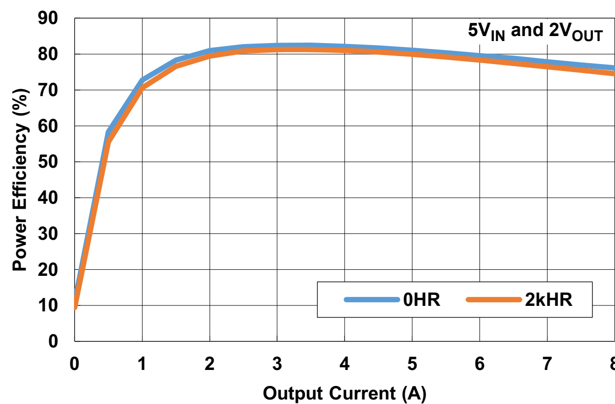

Figure 4. Number 4 Pre and Post High Power Test Efficiency Curves

Figure 5 displays the efficiency curves showing no significant difference in efficiency post test across the four ISL70002SEH devices.

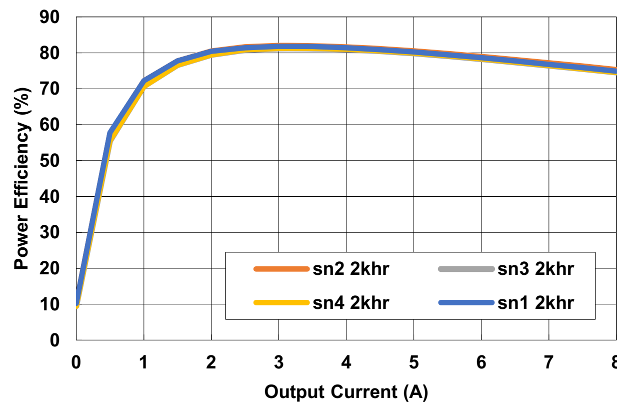

Figure 5. Comparison of All Four Devices Post High Power Stress Efficiency Curves

4. Extended Output Current Usage Constraints

The constraints under which the newly revised output current recommendations are provided:

- Maximum output current for a single device
  - PVIN ≤ 5.5V; 18A to 22A at T_J = +125°C with Schottky clamp diode LX to GND
  - PVIN ≤ 5.5V; up to 18A at T_J = +125°C without Schottky clamp diode
  - PVIN ≤ 6.2V; up to 14A at T_J = +125°C, 12A at T_J = +150°C without Schottky clamp diode
- Maximum output current for two current sharing devices based on 27% worst case current share mismatch
  - PVIN ≤ 5.5V; 28A to 38A at T_J = +125°C with Schottky clamp diode LX to GND
  - PVIN ≤ 5.5V; up to 28A at T_J = +125°C without Schottky clamp diode
  - PVIN ≤ 6.2V; up to 22A at T_J = +125°C, 19A at +150°C without Schottky clamp diode

The electrical constraints noted above are not the only bindings, the other is the maximum die temperature of +150°C thermal constraint.

Taking into account the input and output voltages, the output current, using the datasheet values for the thermal impedances of the junction to case (θ_{JC}) and case to ambient (θ_{CA}) along with the on resistance values for the high-side and low-side power devices, several calculations must be made to understand the IC power dissipation and temperature.

Working an example for an input voltage of 5V, an output voltage of 3.3V with an output current of 20A.

Duty cycle = 3.3 / 5 = 66%

From the SMD spec table the $r_{DS(ON)}$ of the output devices are highest at high temp, 40mΩ and 30mΩ of $r_{DS(ON)}$ respectively for the upper and lower power devices.

The total IC power dissipation (Pd) can be calculated as; Pd = $((0.04 \times 20^2)0.66)+((0.03 \times 20^2)0.33 = 14.5W$

From the datasheet, the junction to case (θ_{JC}) = 0.7°C/W, applying the thermal resistance to the power dissipation results in a temperature rise of 10.2°C

Thus, in this example the case temperature must be held at +115°C maximum to keep a maximum die temperature of ~+125°C with the stated electrical conditions.

Thermal design in the final system must provide adequate heat sinking to achieve the die temperature.

Figure 6 illustrates the ISL70002 case temperature and power dissipation over output current for a 5V input voltage and 3.3V output voltage while maintaining a maximum die temperature of +125°C.

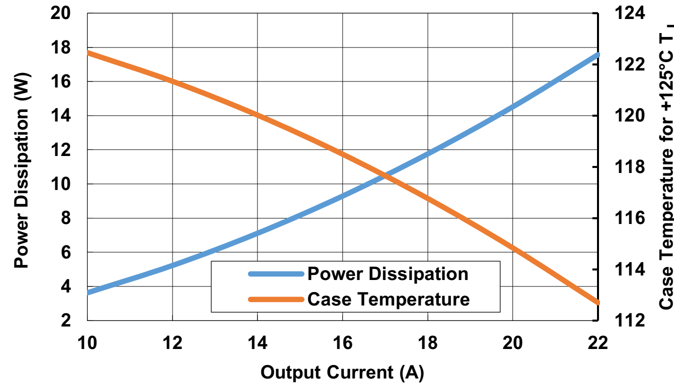

Figure 6. Output Current vs. Case Temperature and Power Dissipation

5. Conclusion

In conclusion, the ISL70002SEH output structure was subjected to currents and die temperatures beyond the newly established 22A and +125ºC absolute maximums for a duration of 2000hours. This stress test demonstrated that there is insignificant impact over time to device integrity and performance by current loading conditions that are presented here.

Working within the newly recommended input voltage, output current, die temperature constraints the ISL70002SEH is not compromised.

6. Revision History

Rev.	Date	Description
0.00	Jun 4, 2018	Initial release

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