SLG46625-A Errata Note

This document contains the known errata for SLG46625-A and the recommended workarounds.

1. Information

Package(s)	20-pin TQFN: 3.5 mm x 3.5 mm x 0.75 mm, 0.5 mm pitch

2. Errata Summary

Issue #	Issue Title
1	ACMP IN- Leakage Current when Powered Down
2	ACMP Output Glitch due to Ring OSC Operation
3	Long Ring OSC Settling Time
4	PGA Has an Offset when Loaded
5	Incorrect Counter Operation after the Reset
6	DCMP OUT+ Output Glitch

3. Errata Details

3.1 ACMP IN- Leakage Current when Powered Down

3.1.1. Effect

ACMPs

3.1.2. Conditions

ACMP uses EXT Vref and it is powered down.

3.1.3. Technical Description

There is a leakage current from the EXT Vref pin when ACMP uses EXT Vref and the ACMP is powered down.

3.1.4. Workaround

Currently there is no workaround. The only alternative is to turn off the IN- external Vref source.

3.2 ACMP Output Glitch due to Ring OSC Operation

3.2.1. Effect

W/S Control, ACMP

3.2.2. Conditions

WS Controller uses RING OSC for ACMP.

3.2.3. Technical Description

The output of the ACMP incorrectly goes low even when IN+ is greater than IN- if the RING OSC is active when the WS signal rises.

Channel 1 – ACMP out

Channel 2 – WS_OUT

Figure 1. ACMP Output Glitch

3.2.4. Workaround

Avoid using the RING OSC with the WS Controller or add a filtering block on the ACMP output to filter out the glitch.

3.3 Long Ring OSC Settling Time

3.3.1. Effect

Ring OSC, Delay, Counter

3.3.2. Conditions

Ring OSC is set to Auto Power On.

3.3.3. Technical Description

The Ring OSC has a longer settling time when configured as Auto Power On in the designs that have very short Ring OSC disable time. An example of this issue is shown in the following configuration:

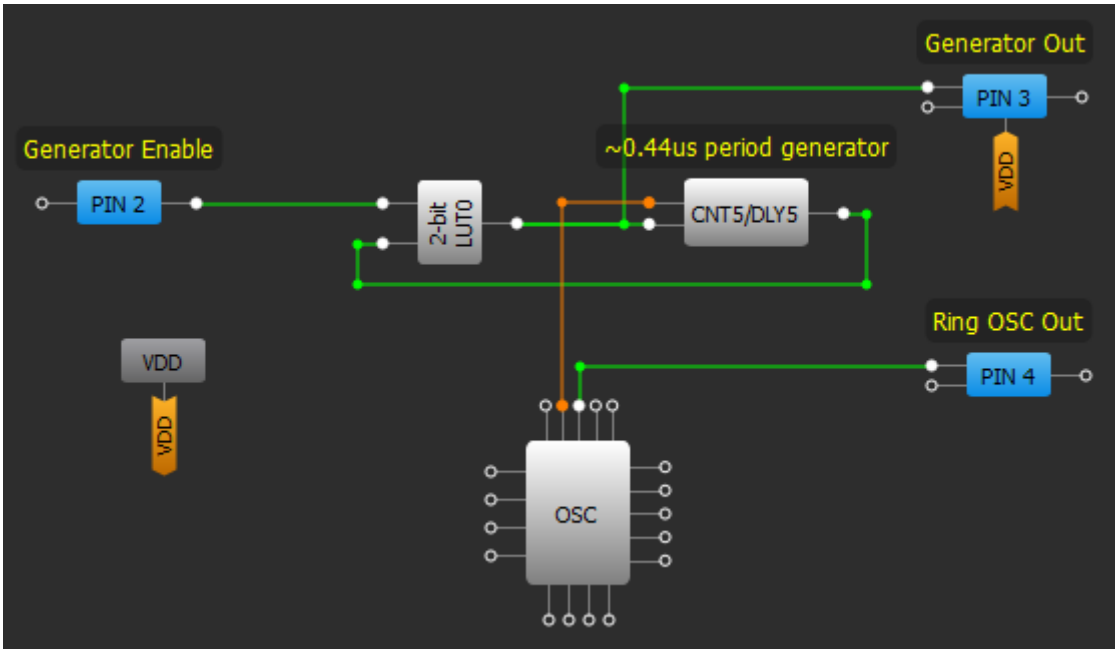

Figure 2. Ring OSC Test Design

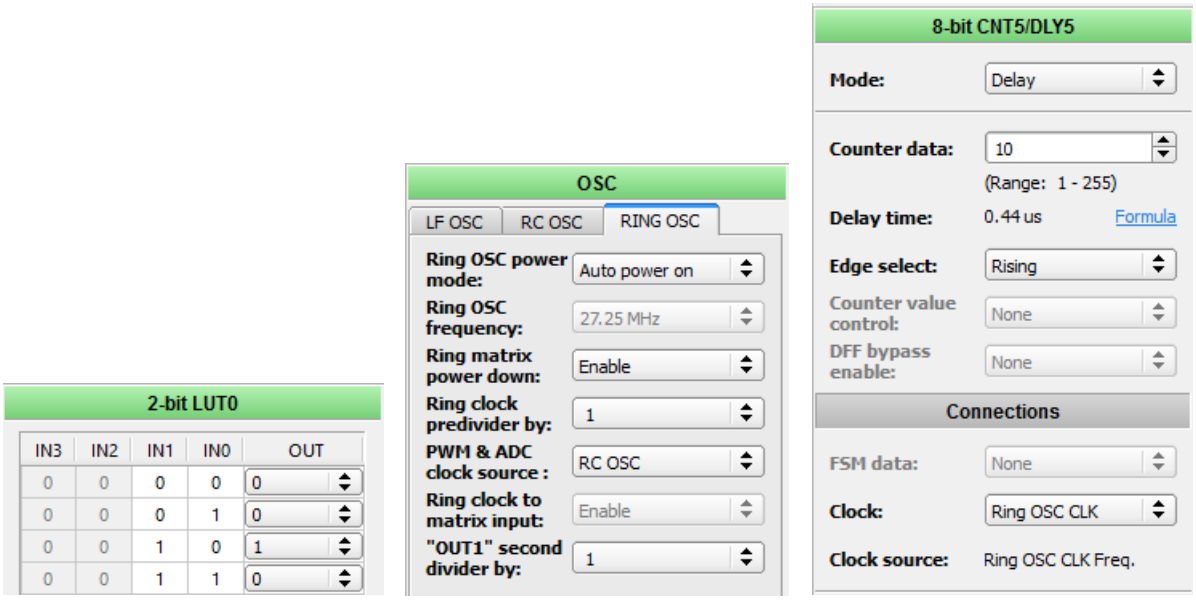

Figure 3. Blocks Properties

The configuration shown above generates a periodical signal with a frequency defined by the Delay cell and started by a high signal on PIN2. The issue becomes apparent in a longer settling time when the scheme generates short pulses (Delay is configured as a rising edge delay only). See the waveform in Figure 4.

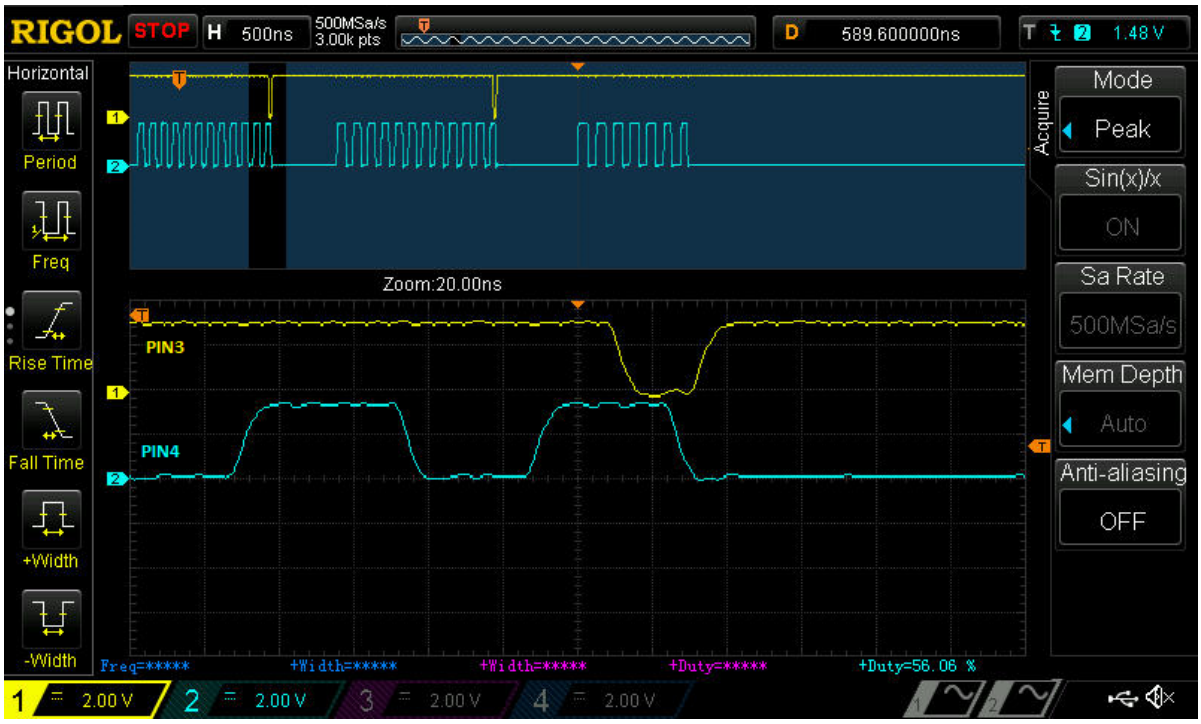

Figure 4. Ring OSC Output

Channel 1 – 2-bit LUT0 output

Channel 2 – Ring OSC output

Such behavior will lead to substantial error in period calculations if the delay time is relatively small.

A similar situation can occur while using two connected delays (all edge detect types except for a pair “Rising edge DLY – Falling edge DLY”).

In Figure 5, Delay5 and Delay6 are configured in the same way. However, Delay5 time is 11.4 us instead of expected 0.4 us (Delay5 time).

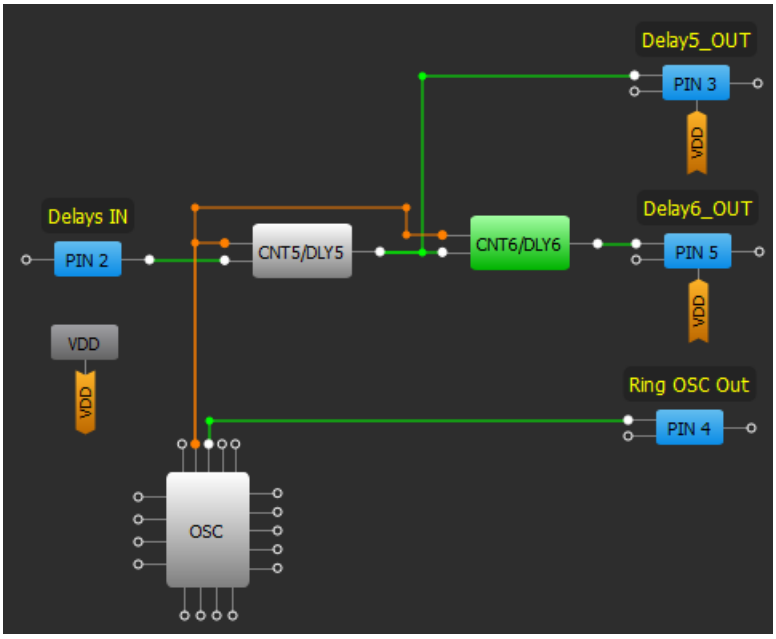

Figure 5. Ring OSC with DLY5, DLY6 Test Design

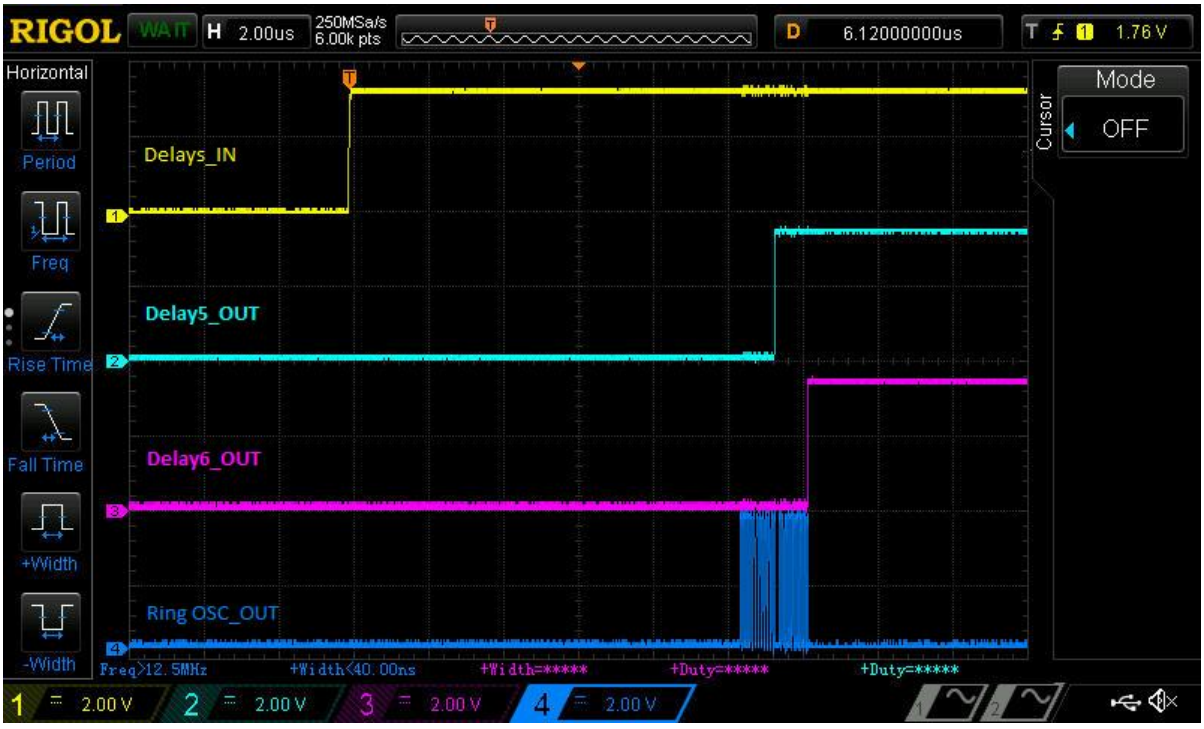

Figure 6. Ring OSC, DLY5 and DLY6 Waveform

3.3.4. Workaround

Set Ring OSC power mode to “Force Power On” or Set Turn on by register option in BG (Band Gap) block as “Enable”.

3.4 PGA Has an Offset when Loaded

3.4.1. Effect

PGA, Vref

3.4.2. Conditions

PGA load higher than 10 mA.

3.4.3. Technical Description

The PGA block has an offset when its output through the VREF is loaded. For reference, Table 1 shows the load vs PGA 4x gain.

Table 1. PGA Gain vs Load

Load, mA	Gain (Ideal = 4x)
0	3.87
1	3.84
5	3.78
10	3.71
20	3.5
40	3
80	2.2
160	1.4

When the load current is higher than 10 mA the output offset is large and may influence the design operation significantly.

3.4.4. Workaround

Use an external buffer to support high load.

3.5 Incorrect Counter Operation after the Reset

3.5.1. Effect

Counter

3.5.2. Conditions

Counter Reset at very high CLK frequencies.

3.5.3. Technical Description

If the Counter Reset occurs at a time very close to a rising edge of the clock signal during clock signal generation (for example OSC operation), there is a possibility that the Counter Data of the Counter is reset incorrectly and the counter end signal (HIGH pulse) may appear faster than expected. This phenomena appears more frequently the higher the clock frequency is.

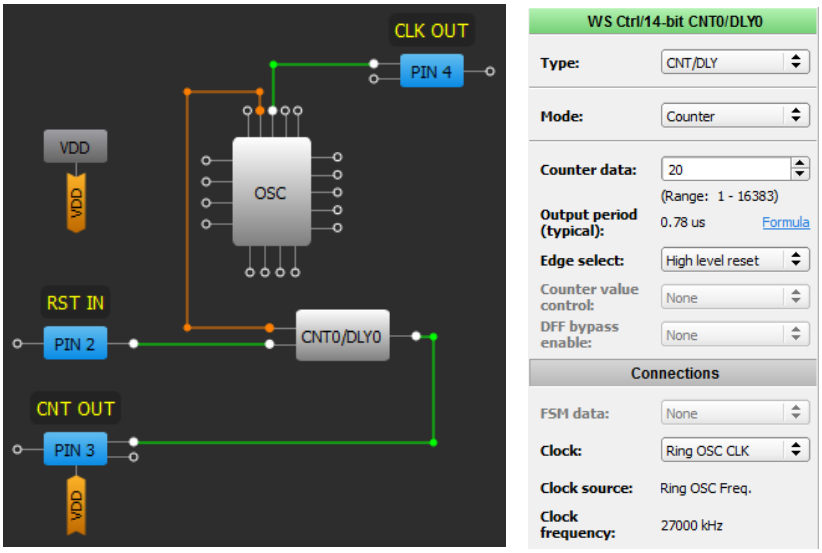

Figure 7. CNT Test Design

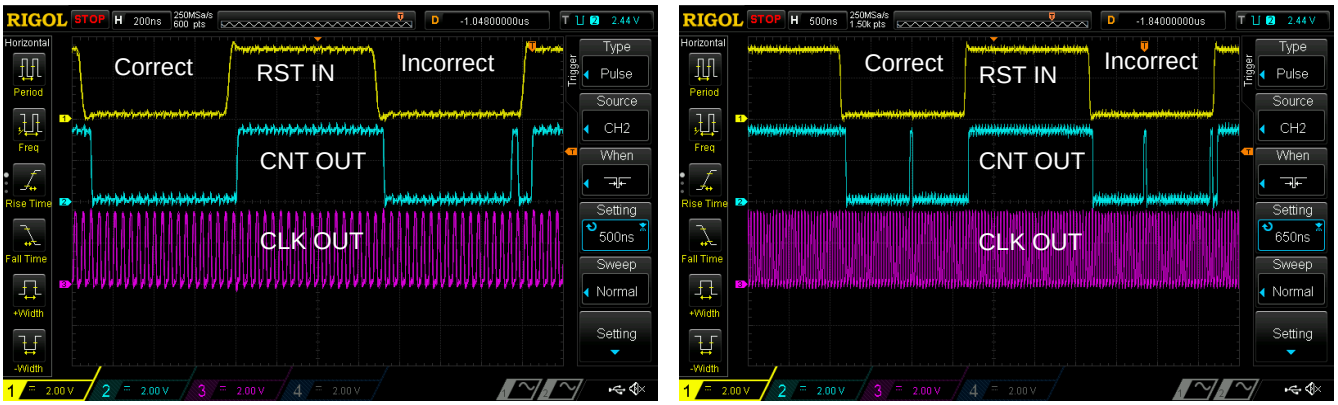

Figure 8. CNT Incorrect Operation

3.5.4. Workaround

Synchronize RESET input of the Counter with its CLK using 2 DFF cells as shown in Figure 9.

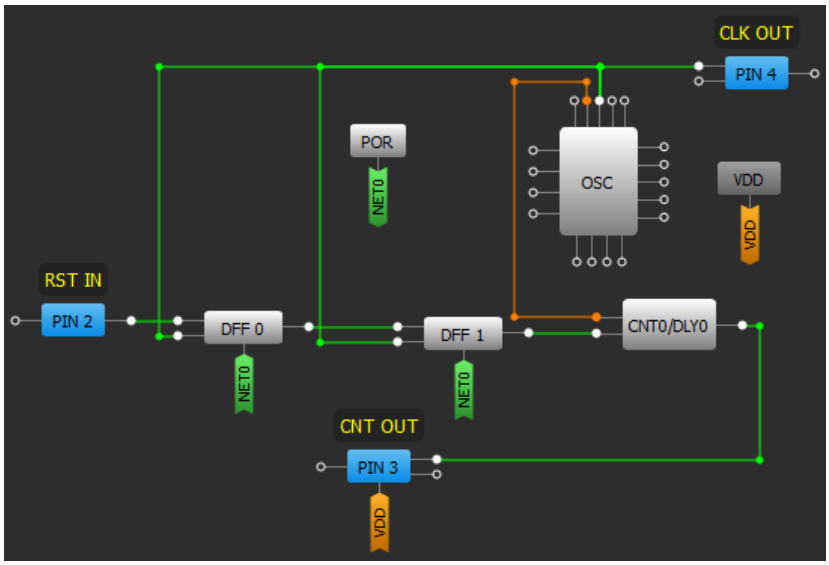

Figure 9. CNT with Sync Reset

3.6 DCMP OUT+ Output Glitch

3.6.1. Effect

DCMPs

3.6.2. Conditions

DCMP at very high CLK frequencies.

3.6.3. Technical Description

DCMP's OUT+ output may have a glitch when the input data is changed. This issue appears more frequently the higher DCMP clock is.

For example, DCMP IN+ sources from FSM0 and IN- from Register0. DCMP is clocked from the Ring OSC.

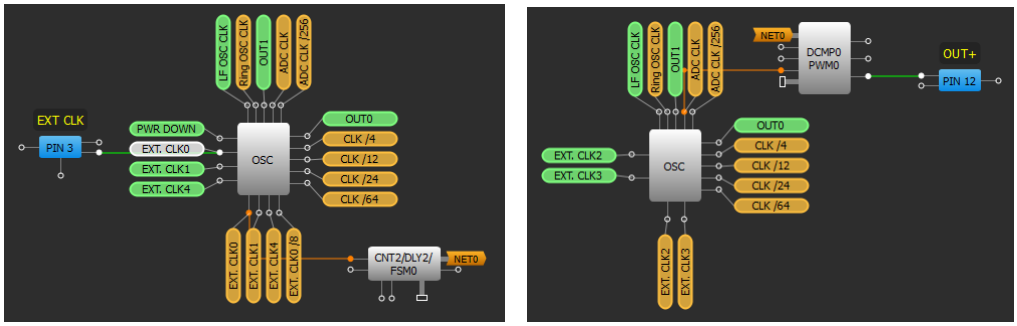

Figure 10. DCMP Test Design

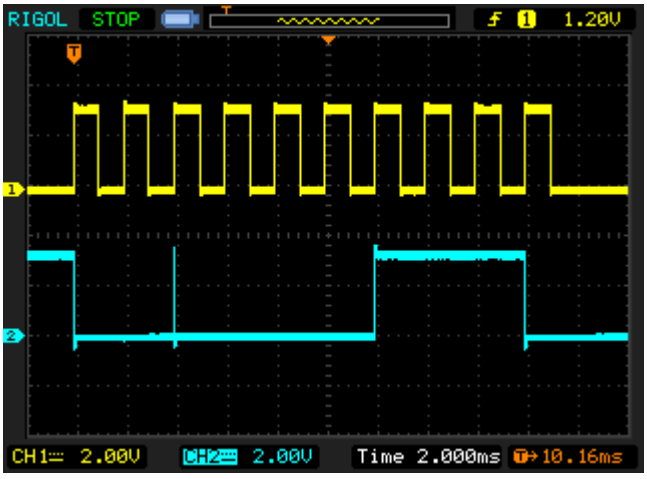

Figure 11. DCMP Glitch

3.6.4. Workaround

Synchronize the data source clock with the DCMP clock source using 2 DFF cells as shown in Figure 12.

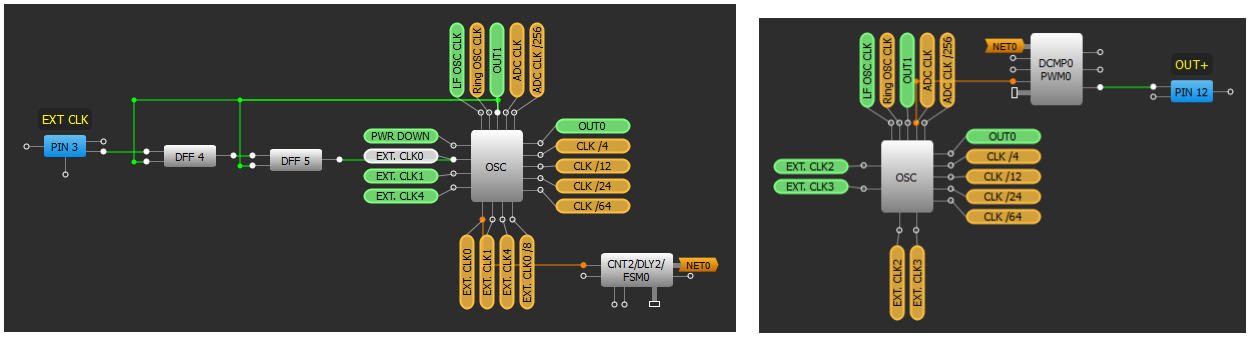

Figure 12. DCMP with Sync Circuit

4. Revision History

Revision	Date	Description
1.00	Mar 20, 2023	Initial release.

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