SLG47115 Errata Note

Abstract

This document contains the known errata for SLG47115 and the recommended workarounds.

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1. Information

Package(s)	20-pin STQFN: 2 mm x 3 mm x 0.55 mm, 0.4 mm pitch

2. Errata Summary

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1	Abnormal ACMPs Behavior
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3	Abnormal GPO glitch when sleep signal release

3. Errata Details

3.1 Abnormal ACMPs Behavior

3.1.1. Effect

GPIO5, ACMP0H and ACMP1H

3.1.2. Conditions

The ACMP0H IN+ source is set to VDD and GPIO5 is set to Analog IO or 3-State Output

3.1.3. Technical Description

When GPIO5 is configured as “Analog Input/Output”, “Digital Input/Output in Analog Input Mode”, or “3-State Output” mode, ACMP behavior may be abnormal in the following cases:

1. ACMP0H IN+ source set to V_{DD}

2. ACMP1H IN+ source set to ACMP0H IN+ source.

Each of the two ACMPs has an input MUX which selects the IN+ source for the comparator. The MUX Options are shown in the Table 1.

Table 1 ACMP Input Options

ACMP IN+ MUX Options	
ACMP0H	GPIO5 V_{DD}
ACMP1H	GPIO6 ACMP0H IN+ source

In GreenPAK Designer, the input source is selected by the IN+ source dropdown within the ACMP’s properties window. When the input source is selected and ACMP is enabled, the analog switch connects the source to the ACMP’s IN+ port.

GPIO5 can be repurposed as Digital IO if the ACMPs are disabled or if another input source is selected for the ACMP by the IN+ input MUX. Whenever GPIO5 input mode is configured as an “Analog IO” in accordance with the register definition below then the ACMP behavior may be abnormal if the ACMP is enabled and connected to another input source.

Table 2 GPIO5 Input/Output Mode Configurations

Byte	Register Bit	Signal Function	Register Bit Definition
GPIO5			
0x6A	849:848	Input Mode Configuration	00: Digital without Schmitt Trigger 01: Digital with Schmitt Trigger 10: Low Voltage Digital In 11: Analog IO
	851:850	Output mode configuration	00: Push-Pull 1x 01: Push-Pull 2x 10: Open-Drain 1x 11: Open-Drain 2x

3 standard GPIO5 settings use the “Analog IO” configuration: Analog input/output, Digital input/output (with “Input mode” set to Analog input), and Digital output (with “Output mode” set to 1x/2x 3-State Output). The first setting is reserved for use with the ACMP, but the other two settings use the “Analog IO” configuration as a high-impedance input.

As an example Figure 1 shows the GreenPAK configured with GPIO5 as a Digital Input/Output (with “Input mode” set to Analog input and “Output mode” set to 1x Push Pull) with a 1M pull-down resistor. GPI0 is being used as a digital input and is connected to the OE input of GPIO5. This is used to determine the input/output mode:

1. when OE Input is LOW, then GPIO5 acts as Analog Input

2. when OE Input is High, then GPIO5 acts as 1x Push Pull Output.

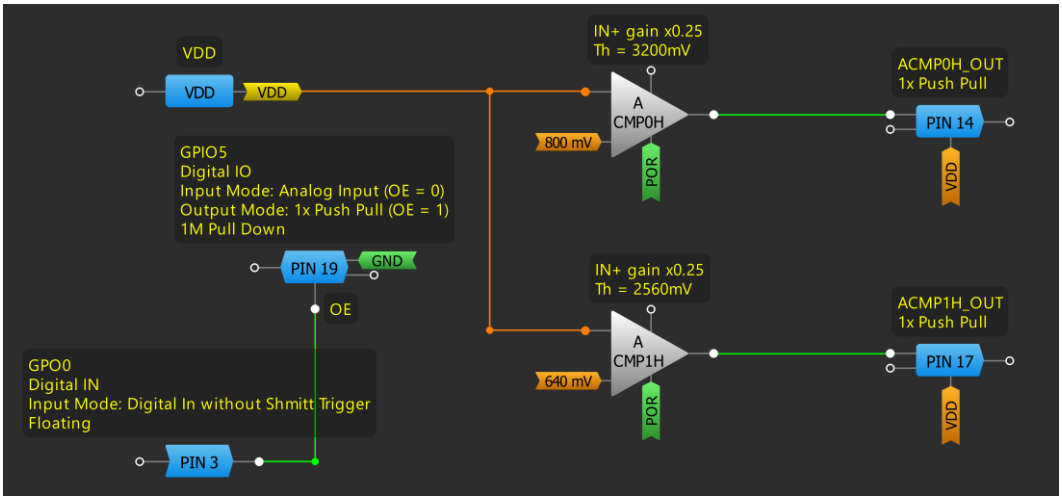

Figure 1 Testing Design

Figure 2 shows that when GPIO5 is in Analog input mode then abnormal ACMPs behavior.

Channel 1 (yellow/top line) – PIN#1 (V_{DD})

D10 – PIN#2 (GPO0)

D11 – PIN#14 (ACMP0H_OUT)

D12 – PIN#17 (ACMP1H_OUT)

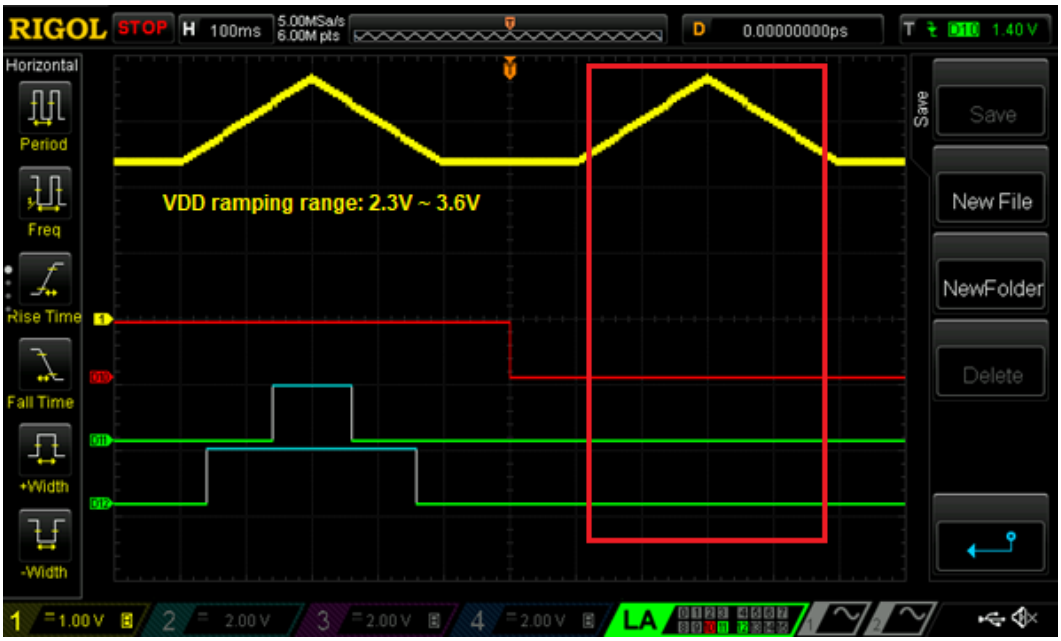

Figure 2 ACMPs Output Behavior

3.1.4. Workaround

There is no workaround for this behavior. With this in mind, the GPIO5 should not be used as Digital IO (with “Input mode” set to Analog input) or as digital outputs (with “Output mode” set to 1x/2x 3-State Output) if the respective ACMP is enabled and connected to another input source.

3.2 Shifted Falling Edge of the Cycle when the pulse width is too narrow

3.2.1. Effect

HV_GPO0 and HV_GPO1

3.2.2. Conditions

HV OUT CTRL is set to Full Bridge, the slew rate is Slow for the motor driver, VDD is larger than 6 V when off time is too low (less than 1 us), and the falling edge of HV_GPO1 will shift cycle by cycle.

3.2.3. Technical Description

When HV OUT CTRL is set to Full bridge, the slew rate is Slow for the motor driver, and the off time is too low. For example, the PWM frequency is 100kHz, the duty cycle is 92%, the off time is only 800 ns, and the HV_GPO1 falling edge will shift for around 100ns cycle by cycle.

As an example, with resistive and inductive load, the HV_GPOx works normally when PWM<90% (off time is larger than 1us), shown in Figure 3. When PWM>92% (off time is less than 1us), there will be abnormal falling edge shift happening cycle by cycle, shown in Figure 4. The reason for this behavior is the driver is not fast enough to handle high-frequency pulse width.

Channel 1 (yellow/top line) – EN Input

Channel 2 (blue/second line) – HV_GPO0

Channel 3 (magenta/third line) – HV_GPO1

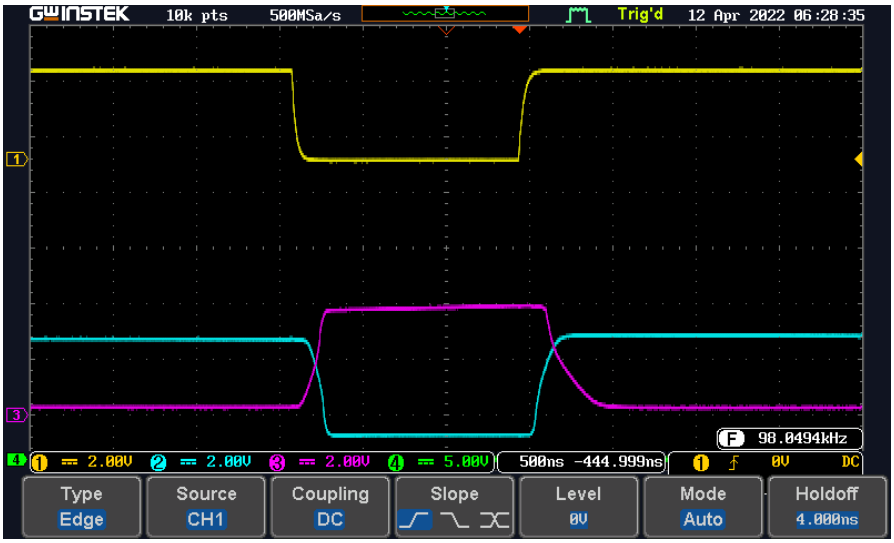

Figure 3 Normal operation

Figure 4 Shifted falling edge

3.2.4. Workaround

There is no workaround for this behavior. With this in mind, the PWM pulse is not suggested set too long or too narrow.

3.3 Abnormal GPO glitch when sleep signal release

3.3.1. Effect

HV_GPO0 and HVGPO1

3.3.2. Conditions

HV OUT CTRL is set to Full bridge, when the Sleep signal is released, there will be a small glitch at both of the HV_GPO pins.

3.3.3. Technical Description

When the Sleep signal is changing from High to Low, there will be a glitch at both of the HV_GPOs as soon as the Sleep signal falling edge. For example Figure 5 shown below, when the Pin 14 Sleep signal is High, the HV OUT CTRL is in sleep mode, and there will be no output in HV_GPOs. After the Sleep signal is changing from High to Low, the HV OUT CTRL is out of sleep mode and starts to work based on EN, PH, and Decay signals.

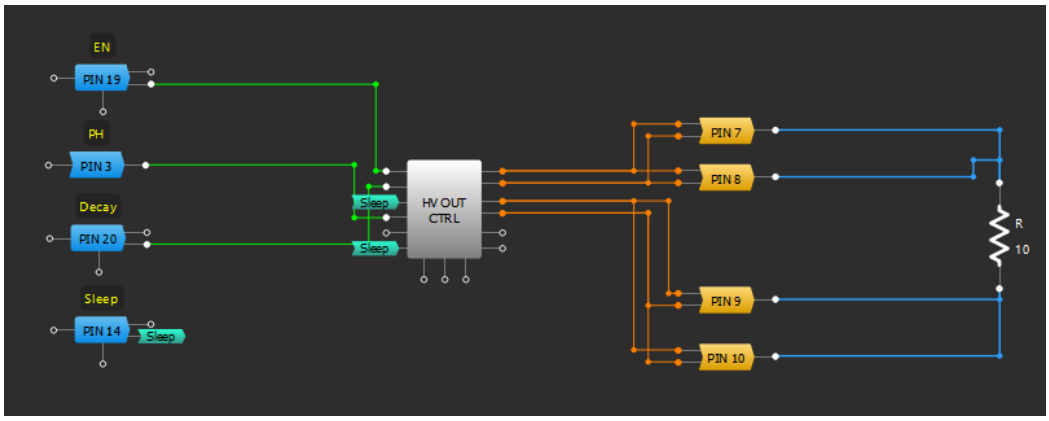

Figure 5 Testing Design

Figure 6 shows the glitch that happened at both HV_GPO as soon as the Sleep signal is from High to Low when Decay is High (Slow decay). Figure 7 shows the HV_GPOs behavior when Decay is Low (Fast decay). The reason for the glitches is when the Sleep signal goes from High to Low, the driver is powered on and the outputs will be kept in hi-z for a certain time letting the charge pump, regulator, and other circuits settle before releasing the outputs. During this wait time, both outputs are hi-z, but the charge pump is working, which injects the charges to the outputs and pulls up both outputs. After waiting time, outputs are released, so outputs go back to the correct states.

Note: The initial output current when the driver transfers from SLEEP to WAKE is around 100µA. So, for most loads, it is too weak to cause an issue.

Channel 1 (yellow/top line) – PIN#14 (Sleep)

Channel 2 (blue/second line) – PIN#19 (EN)

Channel 3 (magenta/third line) – PIN#7 and Pin8 (HV_GPO0)

Channel 4 (green/top line) – PIN#9 and Pin10 (HV_GPO1)

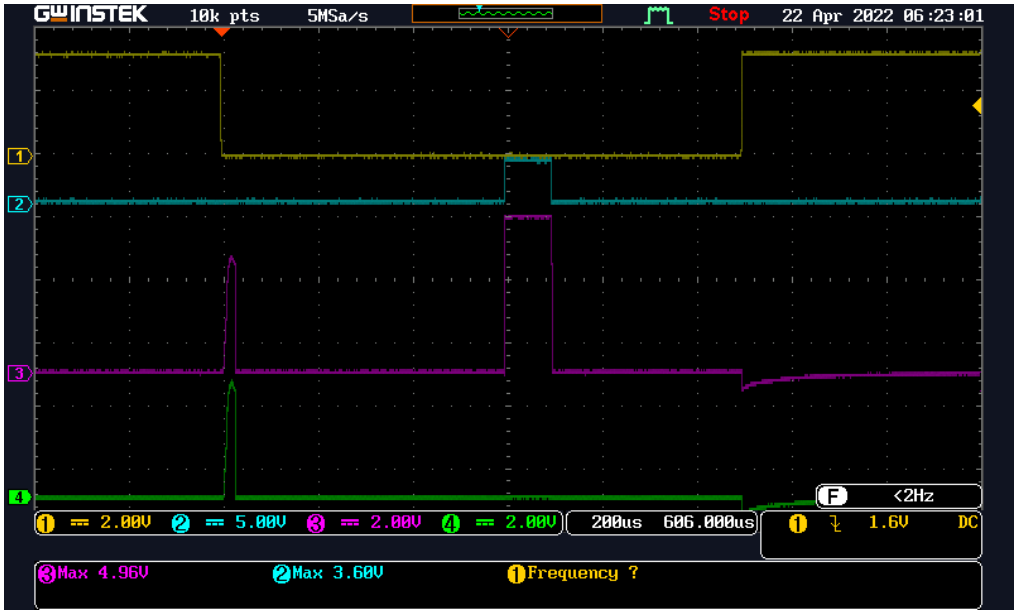

Figure 6 Glitch at HV_GPOx, decay = 1 (Slow decay)

Figure 7 Glitch at HV_GPOx, decay = 0 (Fast decay)

3.3.4. Workaround

There is no workaround for this behavior. But the high-level glitch is weak and can supply only 100 µA of current. So, for most loads, it is not an issue.

4. Revision History

Revision	Date	Description
1.01	Mar 21, 2023	Fixed typos Updated template
1.00	Mar 13, 2022	Initial release.

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