Deterministic SYSREF Alignment Using Multiple Clock Generators

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Abstract

This paper discusses the Renesas RC38312 FemtoClock™ 3 Wireless timing device and how multiple RC38312s coordinate to simultaneously output phase aligned SYSREF signals. Phase aligned SYSREF signals are key to achieving deterministic latency for JEDEC JESD204B/C applications.

Contents

JESD204B/C

JESD204B/C is a JEDEC standard that describes a serialized interface between data converters and logic devices. JESD204B/C supports deterministic latency which allows logic devices to relate data to specific instants at the analog input of each analog to digital converter (ADC) and at the analog output of each analog to digital converter (DAC) in a system.

Logic devices and converters in JESD204B/C subclass 1 systems manage latency using internal local multi-frame clock (LMFC) signals or local extended multi-block clock (LEMC) signals. Referring to Figure 1, device clocks are the timing reference for each logic device and converter in the system and SYSREF pulses identify the device clock edge used to align the phase of the LMFC/LEMC within the logic devices and converters.

Device clocks must meet converters' phase noise requirements to be the basis for their internal sample clocks.

Deterministic latency implies a known deterministic relation between SYSREF and device clock pairs within the system over temperature, supply voltage and power-up cycles. Latency uncertainty is minimized by the careful distribution of SYSREF and device clock pairs to the logic devices and converters in the system.

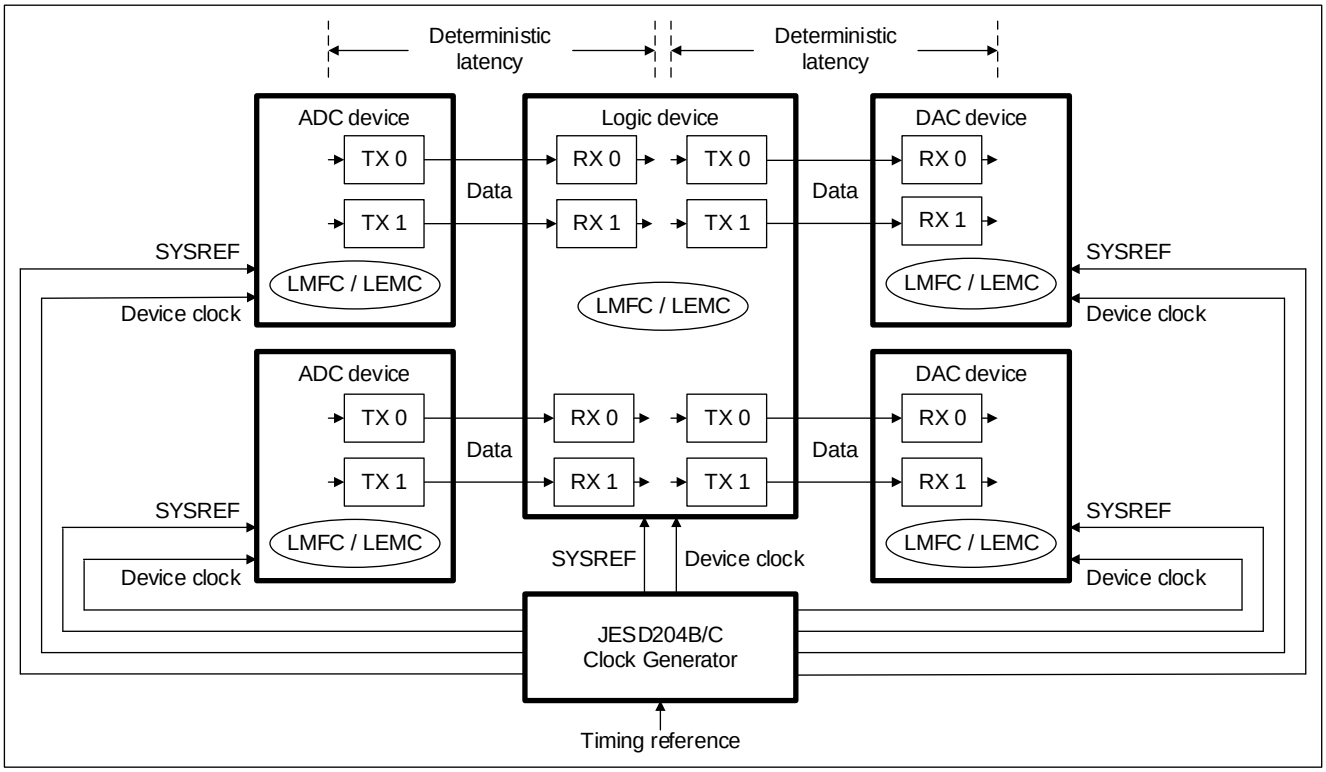

Figure 1. JESD204B/C Deterministic Latency

The SYSREF and device clock pairs at the logic and converter devices must satisfy the device setup and hold times, see Figure 2. SYSREF signals can be periodic, one-shot or gapped-periodic. The JESD204B/C specification recommends that SYSREF should be generated from the same source as the device clock.

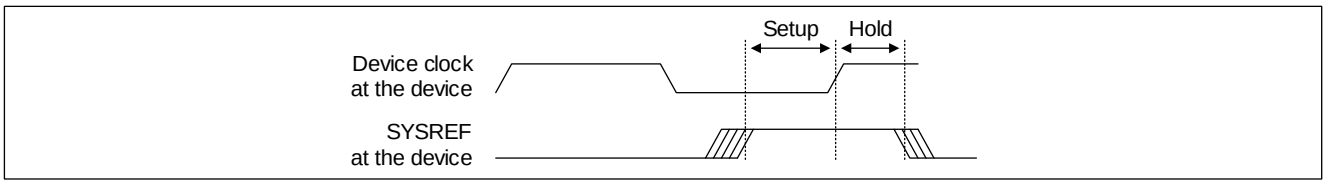

Figure 2. SYSREF and Device Clock Pair Timing

In some cases, it's necessary to use multiple timing devices to generate the required number of SYSREF and device clock pairs. When multiple timing devices are used, steps must be taken to ensure that deterministic latency is maintained at the receiving converters and logic devices.

RC38312 SYSREF Group

The Renesas RC38312 (FemtoClock™ 3 Wireless) timing chips support known and deterministic alignment of SYSREF and device clock pairs for a single RC38312 or for a group of RC38312s.

An RC38312 SYSREF group outputs SYSREF and device clock pairs with known deterministic phase alignment across multiple RC38312s, see Figure 3 and Figure 4. The RC38312s lock to a common timing reference (REF_CLK) and simultaneously start outputting SYSREF in response to an asynchronous hardware-based SYSREF trigger (EXT_SYS_ASYC) or an asynchronous software-based trigger via a serial port. The RC38312s will stop outputting SYSREF signals in a known deterministic manner according to their configuration.

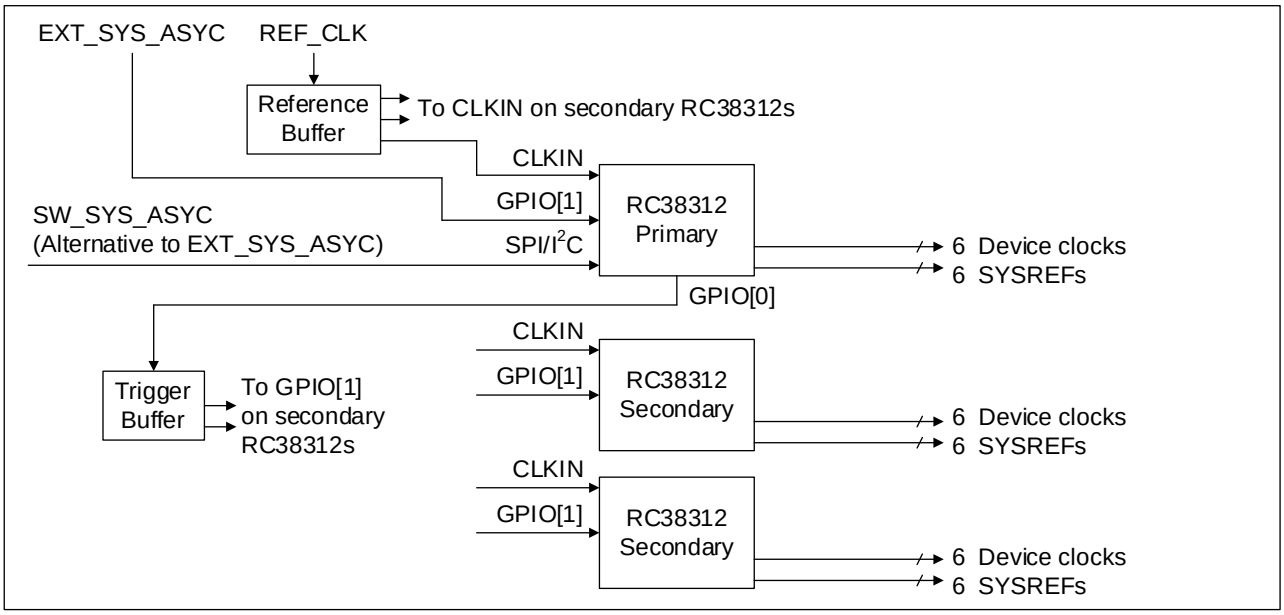

Figure 3. JESD204B/C Clock Generator Using RC38312 SYSREF Group (Option 1)

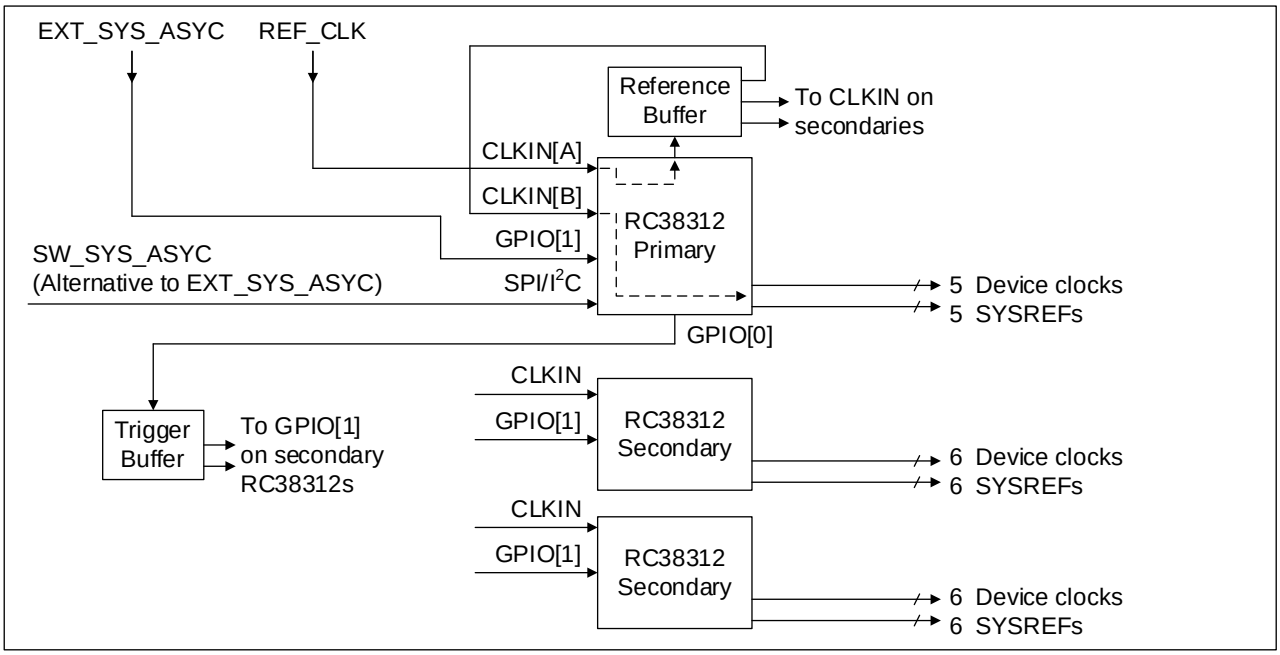

Figure 4. JESD204B/C Clock Generator Using RC38312 SYSREF Group (Option 2)

As illustrated in Figure 3 and Figure 4, RC38312 SYSREF groups consist of a primary device and one or more secondary devices. All RC38312s in a group lock to the same timing reference on CLKIN. The primary device

accepts the asynchronous SYSREF trigger on GPIO[1] and generates a retimed SYSREF trigger. The primary device coordinates SYSREF start for the group by using the retimed trigger internally and by outputting it on GPIO[0] for the secondary devices. In some cases, the primary also coordinates SYSREF stop or SYSREF pause for the group.

This document describes two options for SYSREF groups that differ in the implementation of the primary, the secondaries are the same for both options.

SYSREF group option 1 devotes all outputs on the primary RC38312 to SYSREF and device clock pairs, see Figure 3. This is the simplest implementation, but it might not meet the needs of some systems.

SYSREF group option 2 consumes one output of the primary for one of the following purposes: (a) to include the reference buffer in a DPLL external feedback path to eliminate reference buffer delay variation, (b) to rate convert the REF_CLK frequency to a more suitable CLKIN frequency for the primary and for the secondaries, (c) to support applications where REF_CLK is not present and the primary is steered by software (e.g., IEEE 1588) to output CLKIN for itself and the secondaries, see Figure 4.

Conditions for Phase Alignment within a SYSREF Group

To ensure known deterministic phase alignment of SYSREF within a SYSREF group across power-up cycles, the following conditions must be met:

1. The primary and secondaries must all use the same SYSREF frequency
2. The SYSREF frequency must be an integer multiple of the common timing reference frequency for the SYSREF group (i.e., REF_CLK for option 1, and CLKIN[B] and CLKIN for option 2)

Figure 5 illustrates condition 2 with four scenarios of SYSREF alignment between two RC38312s; each scenario represents a different ratio of SYSREF frequency to the common timing reference frequency. In the figure, CLKIN is the common timing reference for both RC38312s and SYSREF 0 and SYSREF 1 are their respective SYSREF outputs. For scenarios A and C, the SYSREFs are aligned regardless of which CLKIN rising edge each RC38312 DPLL tracks. For scenarios B and D, there is latency uncertainty (L_U), because after a power-up cycle, each RC38312 DPLL can start-up tracking different CLKIN rising edges resulting in misalignment between the SYSREF signals.

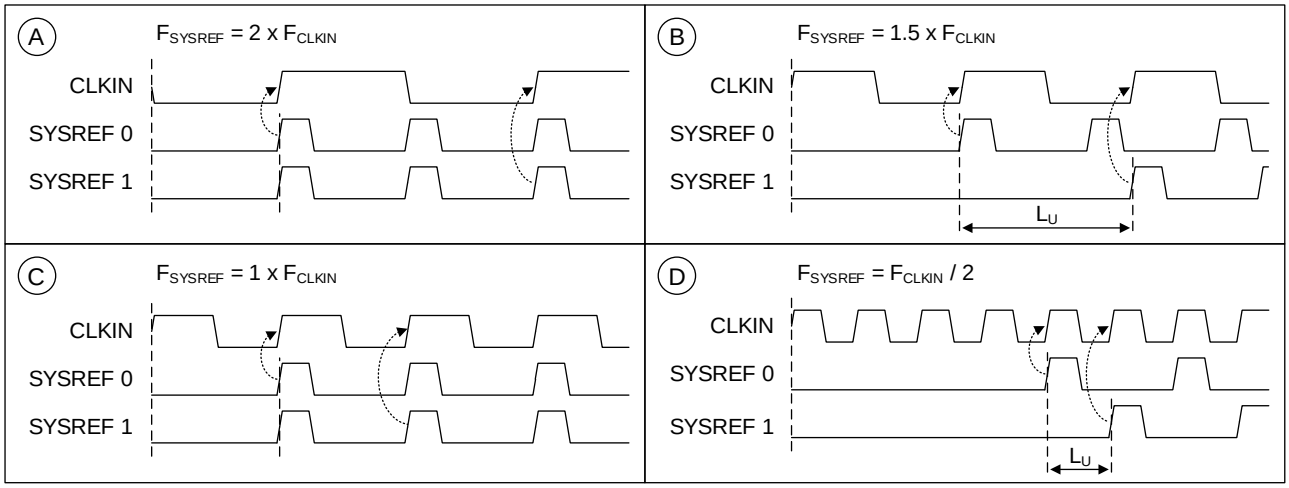

Figure 5. SYSREF Alignment Scenarios for CLKIN vs SYSREF Frequency

RC38312 FemtoClock™ 3 Wireless

The RC38312 is an ultra-low phase noise radio synchronizer and multi-frequency clock synthesizer. This flexible, low-power device outputs clocks with ultra-low in-band phase noise and spurious for 4G and 5G RF transceivers and with jitter below 25fs-rms for 112Gbps and 224Gbps SerDes. The device supports clocks for JESD204B/C subclass 1 systems. See Figure 6 for a simplified RC38312 block diagram.

The RC38312 has 12 clock outputs, OUT[11:0], that can output SYSREF or device clocks. The device can be configured to output up to six SYSREF and device clock pairs. Clock outputs OUT[5:0] are preferred for device clocks because they are most isolated from FOD noise. The supported output frequency range for device clocks is 1kHz to 2.5GHz, and the supported frequency range for SYSREF is 1kHz to 16.384MHz.

The RC38312 provides four synchronization channels consisting of three digital PLLs (DPLL) and a digitally controlled oscillator (DCO). It also provides four synthesizers consisting of an ultra-low phase noise analog PLL (APLL), and three low phase noise fractional output dividers (FOD). The synchronization channels and synthesizers can be combined to implement up to four independent timing domains. The lowest phase noise timing domain comprises DPLL0 and the APLL; this domain is the most suitable for producing JESD204B/C SYSREF and device clock pairs.

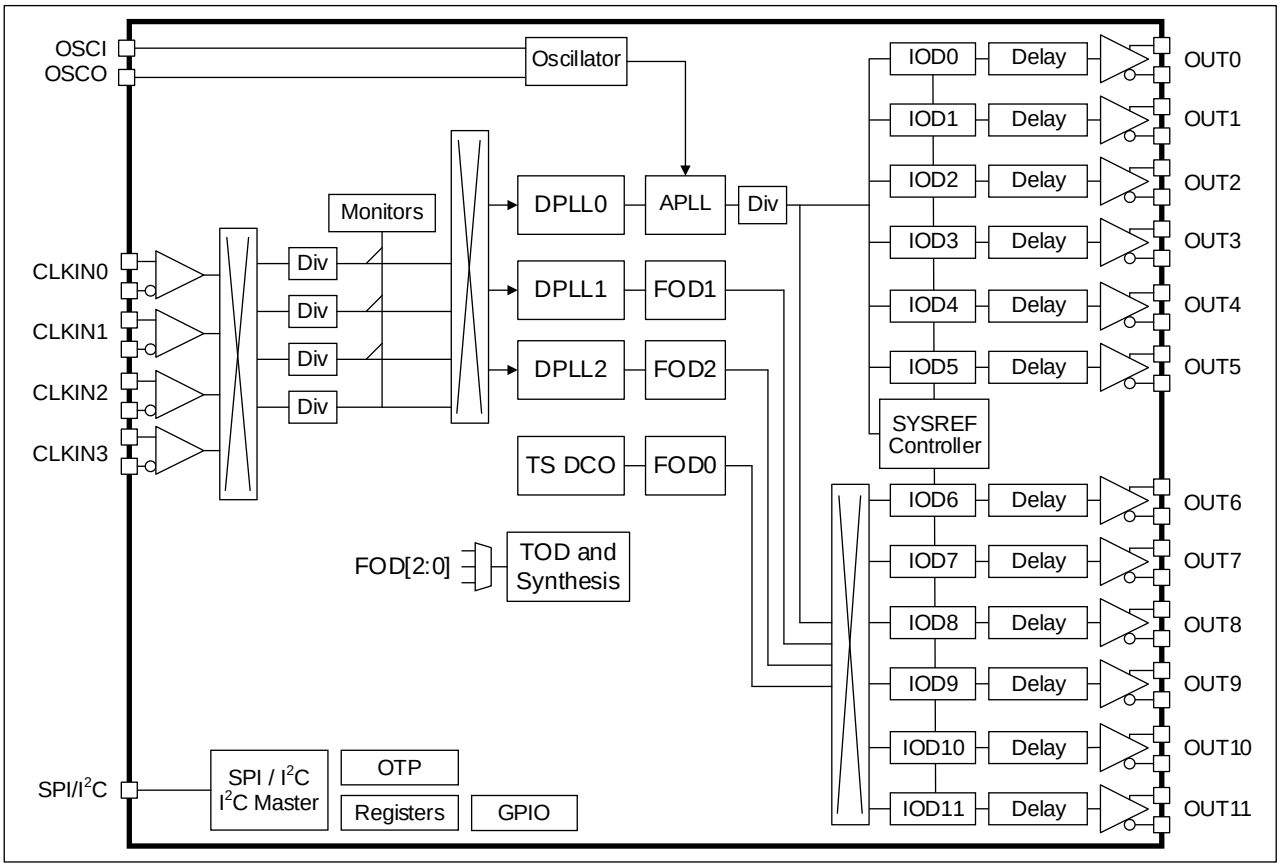

Figure 6. RC38312 Simplified Block Diagram

RC38312 SYSREF Phase Alignment

For JESD204B/C applications, the RC38312 derives SYSREF and device clocks from the DPLL0/APLL output clock, this allows the best control of their phase relationship. The phase relationship within a SYSREF and device clock pair is known, deterministic and adjustable.

Each RC38312 can support one SYSREF frequency and multiple device clock frequencies that are integer multiples of the SYSREF frequency. One of the DPLLs, usually DPLL0, locks to a CLKIN reference and generates an internal clock (SYSREF_CLK_INT) with the SYSREF frequency, see Figure 7. By default, all SYSREF outputs are phase aligned with SYSREF_CLK_INT, and by default, the rising edges of all SYSREFs are coincident with rising edges of the device clocks.

The input-to-output delay for each DPLL from CLKIN to any CLKOUT is deterministic to within ±100ps, and for each DPLL the input-to-output delay can be independently adjusted in ±10ps steps.

Relative to the DPLL0 reference (CLKIN), the phase of the device clocks can be independently advanced or delayed using the respective integer output divider (IOD) in steps of the IOD input clock period, or they can be

delayed by 0ps, 50ps or 100ps using the respective output delay. Also relative to CLKIN, the phase of the SYSREFs can be independently delayed by 0ps, 50ps or 100ps using the respective output delay.

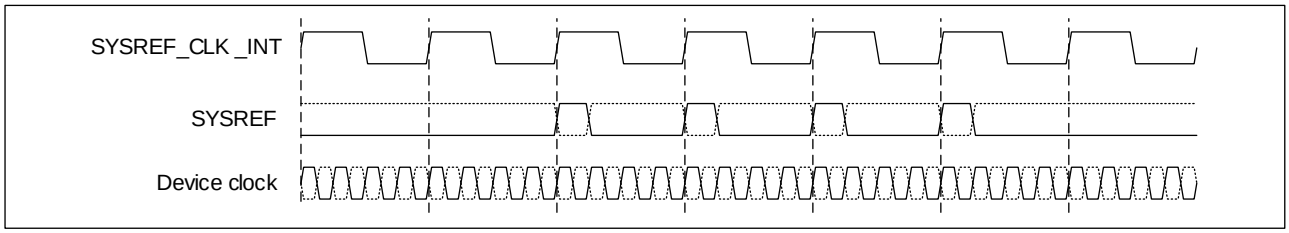

Figure 7. RC38312 SYSREF and Device Clock Default Alignment

SYSREF Operating Modes and SYSREF Start and Stop Triggers

The RC38312 supports counted SYSREF and two types of continuous SYSREF. Counted SYSREF outputs a programmable number (1 to 255) of SYSREF pulses in response to a start trigger. Continuous SYSREF outputs either a continuous train of SYSREF pulses, or a continuous programmable pattern of SYSREF pulses followed by pauses (non-pulses) in response to a start trigger.

Counted SYSREF and continuous SYSREF can start in response to a hardware start trigger on GPIO[1], or in response to a software start trigger by writing to the init_sysref register bit via the SPI/I^{2}C port.

The hardware start trigger can be configured to be rising-edge-sensitive or falling-edge-sensitive, or to be high-level-sensitive or low-level-sensitive. The software start trigger is a low-to-high transition of the init_sysref register bit. Another available start trigger is a time-of-day (TOD) comparison event that occurs when the device TOD reaches a programmed value.

Counted SYSREF stops when the device finishes outputting the programmed number of pulses.

Continuous SYSREF can stop in response to a hardware stop trigger on GPIO[1], or in response to a software stop trigger using a register write via the SPI/I^{2}C port. The hardware stop trigger can be configured to be rising-edge-sensitive or falling-edge-sensitive. The software stop trigger is high-to-low transition of the init_sysref register bit. Continuous SYSREF stops synchronously, and the device will not output a runt pulse.

SYSREF Primary – Option 1

Figure 8 shows detail of the primary RC38312 and buffers supporting SYSREF primary option 1.

For option 1, the REF_CLK signal is fanned-out by the REF_CLK buffer to the primary and secondary RC38312s so that each receives an identical copy of the REF_CLK signal. DPLL0/APLL of each RC38312 locks to the reference on CLKIN and generates the required ultra-low phase noise SYSREF and device clock frequencies.

The primary SYSREF controller accepts the EXT_SYS_ASYC trigger on GPIO[1] and generates a retimed trigger on GPIO[0] that is aligned with the next rising edge of the SYSREF_CLK_INT. The retimed trigger is fanned-out by the trigger buffer so each secondary starts to output SYSREF on the following rising edge of SYSREF_CLK_INT simultaneously with the output of SYSREF by the primary. See the timing diagrams in the Timing for SYSREF Groups section.

To ensure the SYSREF and device clock pairs from all RC38312s in the group are phase aligned, the following criteria must be observed:

1. The propagation delays from the REF_CLK buffer to each RC38312 CLKIN must be matched, or they must be known and the differences compensated (e.g., by DPLL0)
2. The REF_CLK buffer must exhibit low output-to-output skew
3. The DPLL0 bandwidth for each RC38312 in the SYSREF group should be the same

In cases where the SYSREF and device clock pairs need to closely track the phase of REF_CLK, noise on REF_CLK should be pre-filtered with a bandwidth lower than the primary and secondary DPLL0 bandwidths.

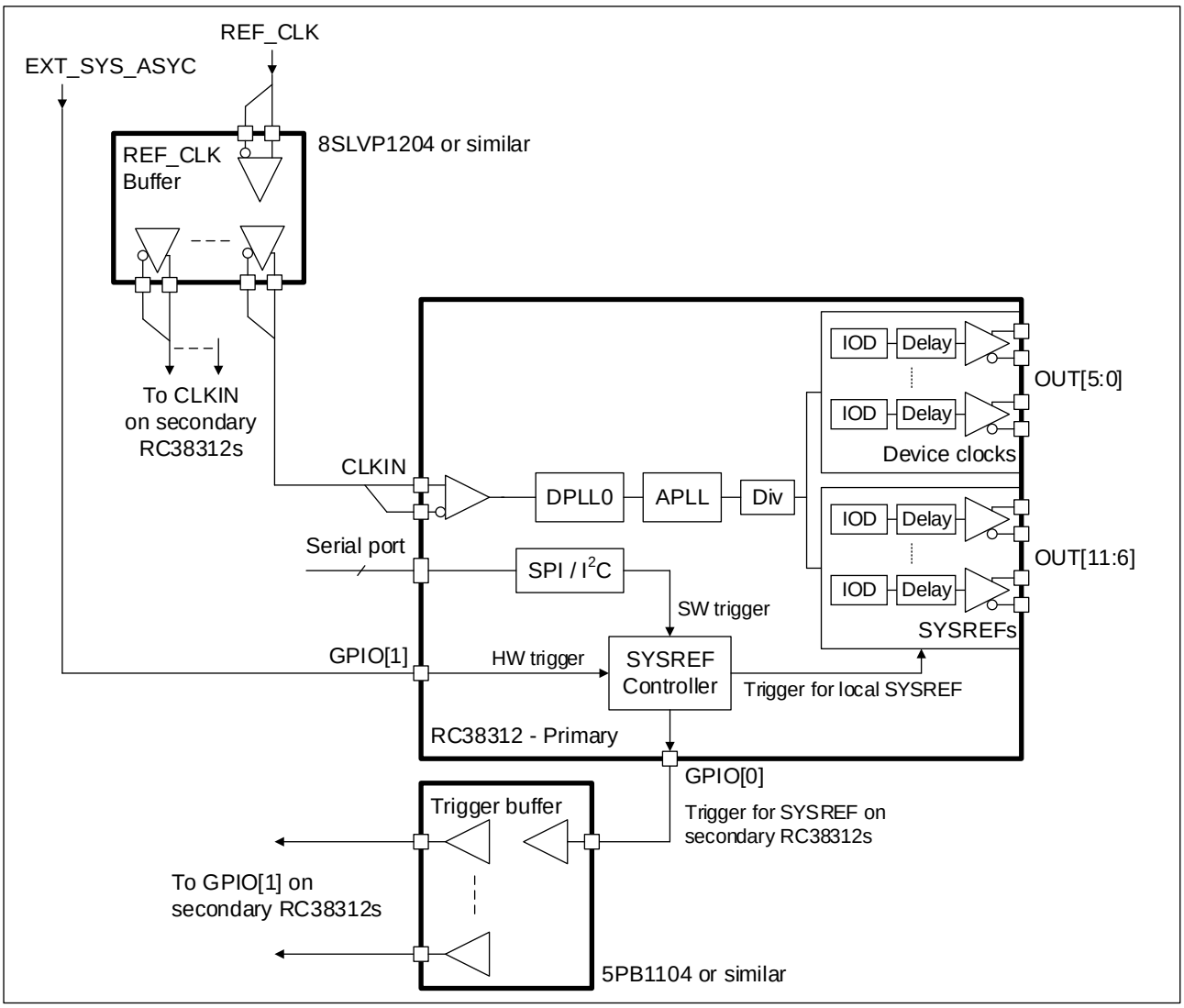

Figure 8. SYSREF Primary Using RC38312 – Option 1

SYSREF Primary – Option 2

Figure 9 shows detail of the primary RC38312 and buffers supporting SYSREF primary option 2.

Option 2(a)

Option 2(a) is intended for applications where delay variation due to the reference buffer needs to be eliminated.

For this option the primary implements a zero-delay buffer using the reference buffer and DPLL1/FOD1. DPLL1 is configured for external feedback, it locks to the reference on CLKIN[A] and FOD1 generates a clock at the REF_CLK frequency on OUT[6] (or any other clock output). The OUT[6] clock passes through the reference buffer and arrives at CLKIN[B] for DPLL1 feedback, thus closing the DPLL1 control loop.

To ensure the SYSREF and device clock pairs can closely track the phase of REF_CLK regardless of the delay through the reference buffer, the following conditions must be observed:

1. Noise on REF_CLK should be pre-filtered with a bandwidth below the bandwidth of the primary DPLL1
2. The propagation delays from the reference buffer to CLKIN[B] and from the REF_CLK input to CLKIN[A] must be known and digitally compensated by DPLL1

DPLL0/APLL locks to CLKIN[B] and generates SYSREF and device clock pairs as described for option 1.

Option 2(b)

Option 2(b) is intended for applications where the SYSREF frequency is not an integer multiple of the timing reference (REF_CLK) frequency.

For this option, the primary DPLL1/FOD1 is used to rate convert the REF_CLK frequency so the SYSREF frequency is an integer multiple of the common timing reference frequency applied at CLKIN[B] of the primary and CLKIN of the secondaries respectively.

Note that a known and deterministic phase relationship across power-up cycles between the REF_CLK and the SYSREFs in the group might not be possible depending on the REF_CLK and SYSREF frequencies.

DPLL0/APLL locks to CLKIN[B] and generates SYSREF and device clock pairs as described for option 1.

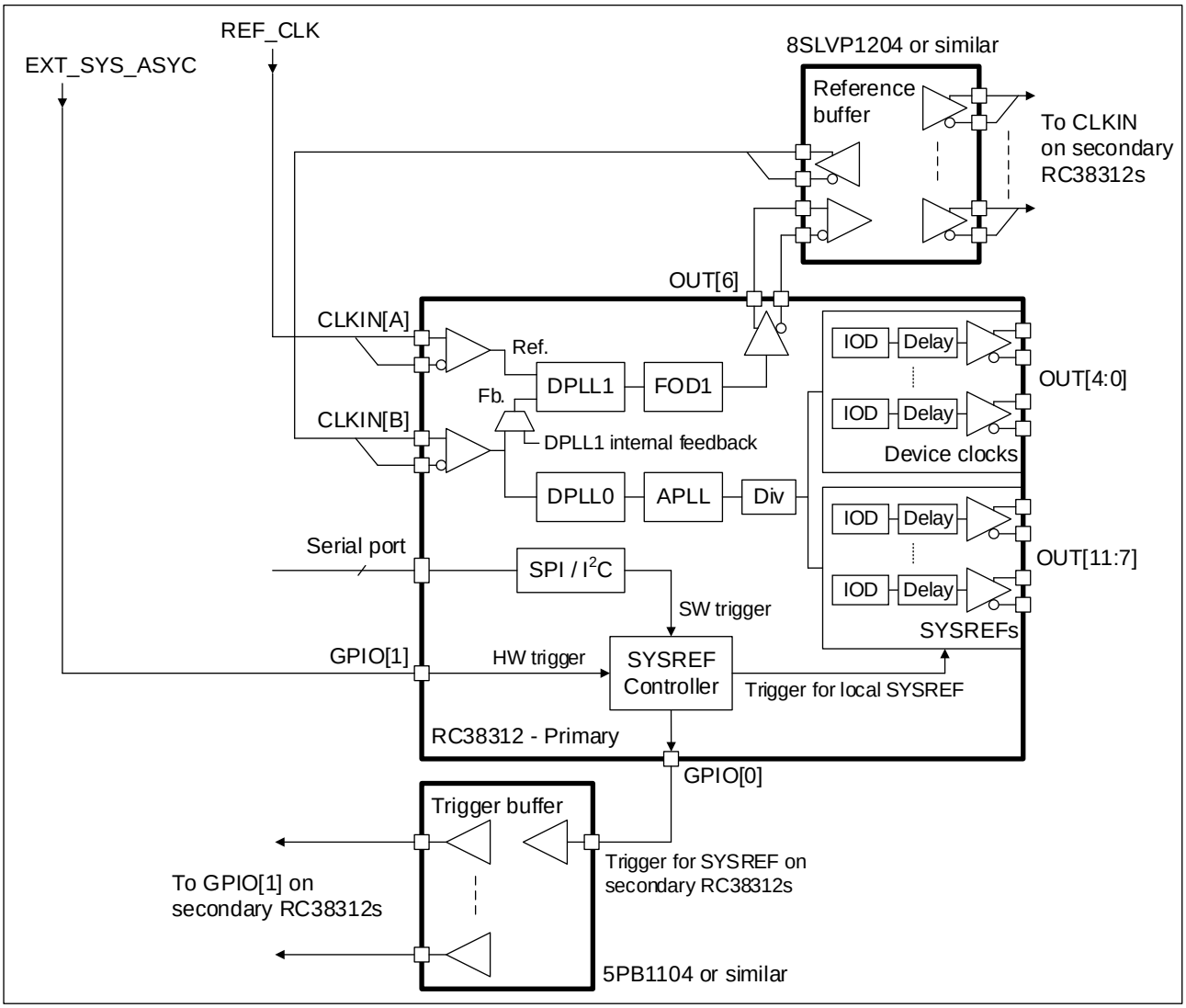

Figure 9. SYSREF Primary Using RC38312 – Option 2

Option 2(c)

Option 2(c) is intended for applications where there is no REF_CLK and the frequency of the SYSREF and device clock pairs is steered by software (e.g., IEEE 1588).

For this option, DPLL1 of the primary is configured as a DCO that steers FOD1. FOD1 generates a clock on OUT[6] (or any other clock output) with a frequency that can be multiplied by an integer to equal the SYSREF

frequency. The OUT[6] clock passes through the reference buffer and becomes the common timing reference for DPLL0 on all RC38312s in the group.

DPLL0/APLL locks to CLKIN[B] and generates SYSREF and device clock pairs as described for option 1.

All Option 2 Variants

To ensure all SYSREF and device clock pairs in the group are aligned, the following criteria must be observed:

1. The reference clock buffer must exhibit low output-to-output skew
2. The propagation delays from the reference buffer to CLKIN[B] and CLKIN on the secondaries must be matched, or they must be known and the differences compensated by each secondary DPLL0
3. The bandwidth of the DPLL0s in the group should be the same and they should be higher than the primary DPLL1 bandwidth (if applicable)

SYSREF Secondary

Figure 10 shows detail of the secondary RC38312s supporting Option 1 and Option 2.

If simultaneous SYSREF start and stop is required across the SYSREF group, then the propagation delay from GPIO[0] on the primary to GPIO[1] on each secondary must be less than one SYSREF period.

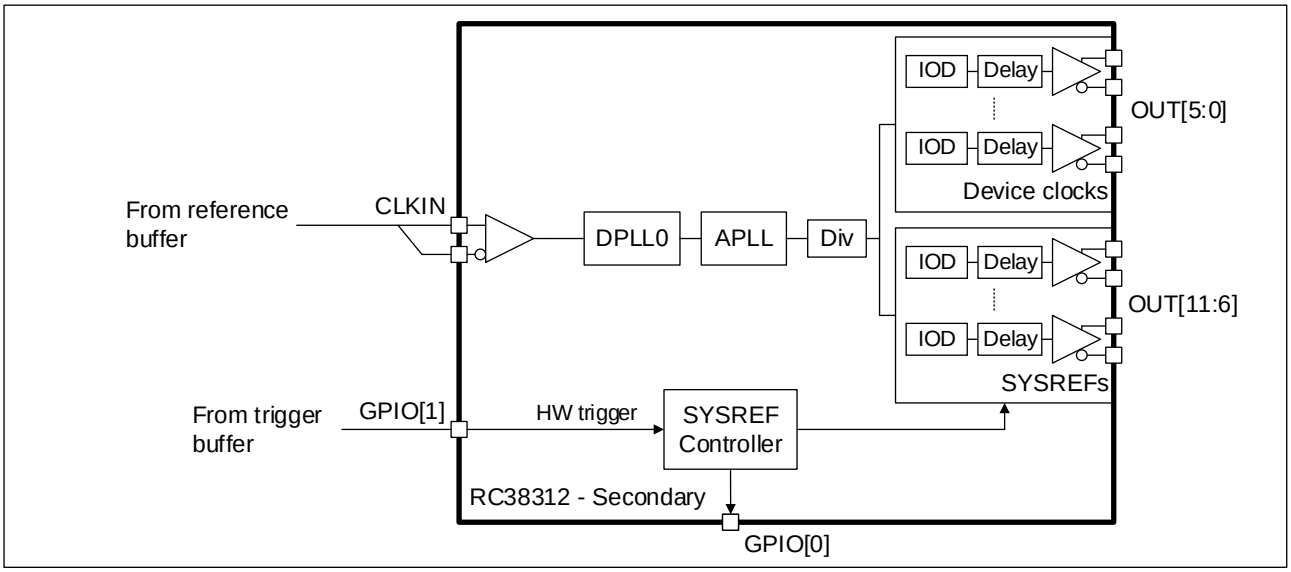

Figure 10. SYSREF Secondary using RC38312

Timing for SYSREF Groups

Timing for Counted SYSREF

The primary and secondary RC38312s are configured for counted SYSREF with hardware start triggers rising-edge-sensitive. Figure 11 and Figure 12 show the timing for a primary device and a secondary device respectively when both are configured to output a count of 3 SYSREF pulses in response to a start trigger on GPIO[1].

Referring to Figure 11, when the primary detects a rising edge on GPIO[1], it waits until the first following rising edge of SYSREF_CLK_INT then it outputs a retimed rising edge on GPIO[0]. On the subsequent rising edge of SYSREF_CLK_INT the primary begins outputting counted SYSREF pulses. The primary outputs the programmed the number of SYSREF pulses and then stops. When the primary finishes outputting SYSREF pulses, it waits 1.5 SYSREF periods and then takes the GPIO[1] output low indicating that the SYSREF event is complete, and the group is ready for another.

Referring to Figure 12, when the secondary detects a rising edge on GPIO[1], it waits until the first following rising edge of SYSREF_CLK_INT then it begins outputting counted SYSREF pulses. In this way the primary and all secondary RC38312s in the group simultaneously start outputting SYSREF pulses. The secondary outputs the programmed number of SYSREF pulses and then stops.

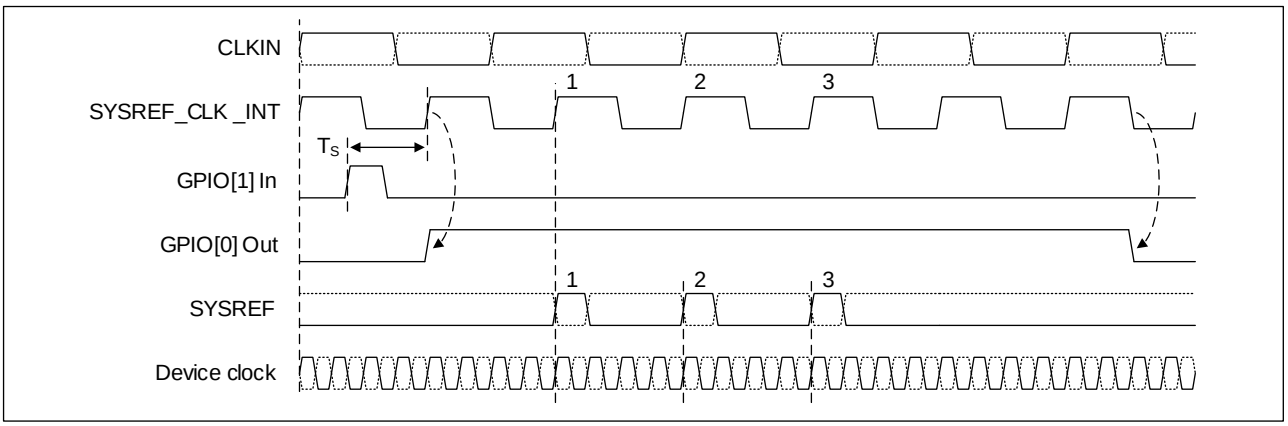

Figure 11. Counted SYSREF Timing for Primary RC38312

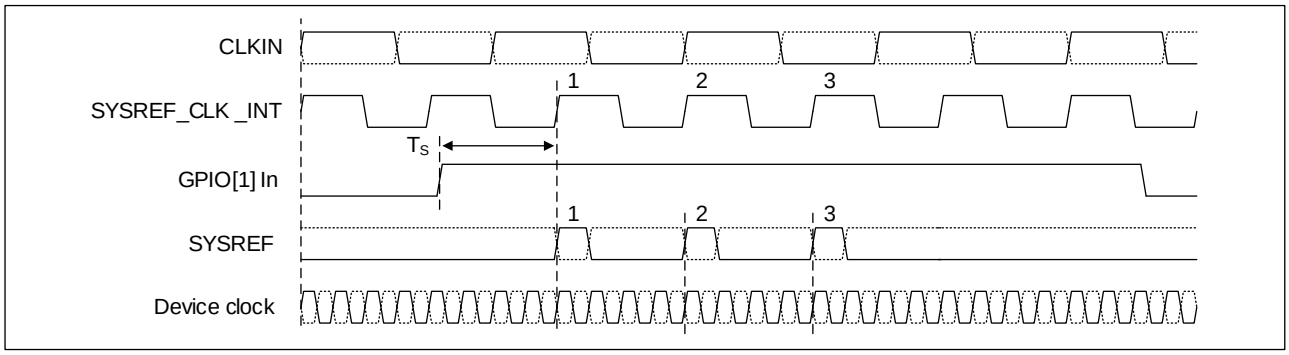

Figure 12. Counted SYSREF Timing for Secondary RC38312

Timing for Continuous SYSREF

The primary and secondary RC38312s are configured for continuous SYSREF with hardware start triggers high-level-sensitive, and hardware stop triggers low-level-sensitive. Figure 13 and Figure 14 show the timing for a primary device and a secondary device respectively when both are configured to output continuous SYSREF pulses in response to a start trigger on GPIO[1] and to stop outputting SYSREF pulses in response to a stop trigger on GPIO[1].

Referring to Figure 13, when the primary detects a high level on GPIO[1], it outputs a high level on GPIO[0] on the next rising edge of SYSREF_CLK_INT. While the primary continues to detect a high level on GPIO[1] it outputs one SYSREF pulse for each subsequent rising edge of SYSREF_CLK_INT. When the primary detects a low level on GPIO[1], it outputs a low level on GPIO[0], and it stops outputting SYSREF pulses beginning with the next rising edge of SYSREF_CLK_INT. The primary RC38312 will not output a runt SYSREF pulse.

Referring to Figure 14, when the secondary detects a high-level on GPIO[1], it outputs one SYSREF pulse for each rising edge of SYSREF_CLK_INT. In this way the primary and secondary RC38312s simultaneously start outputting SYSREF pulses. When the secondary detects a low level on GPIO[1] it stops outputting SYSREF pulses beginning with the next rising edge of SYSREF_CLK_INT. The secondary RC38312s will not output a runt SYSREF pulse.

Depending on when a secondary detects a falling edge on GPIO[1], it is possible for it to output one more SYSREF pulse after the primary has output its last SYSREF pulse.

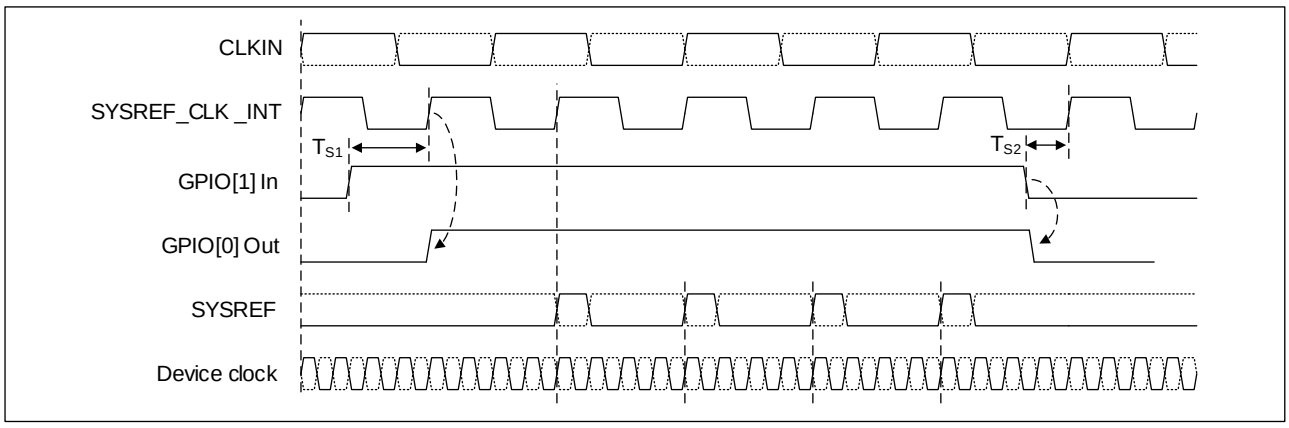

Figure 13. Continuous SYSREF Timing for Primary RC38312

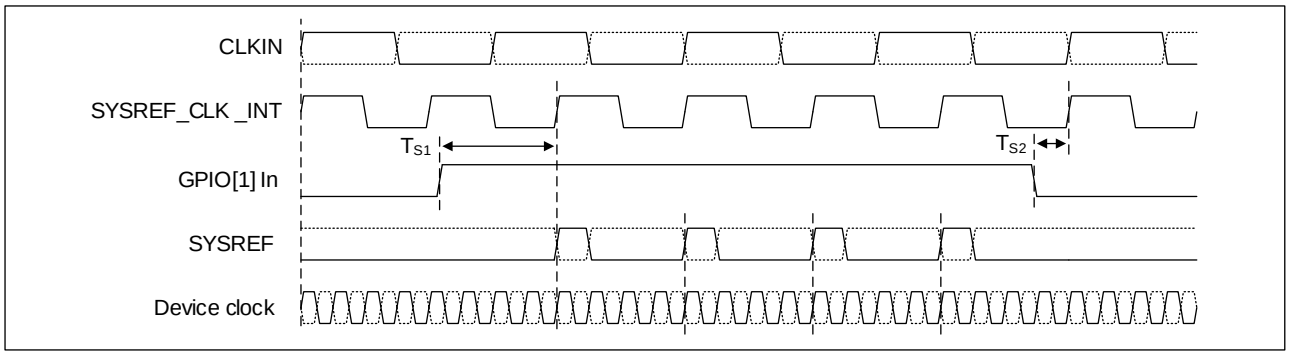

Figure 14. Continuous SYSREF Timing for Secondary RC38312

Revision History

Revision	Date	Description
1.00	September 30, 2024	Initial release.