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**Wafer by Wafer Low Dose Rate Acceptance Testing in a  
Production Environment**

*Abstract—This White Paper describes technical details of a wafer by wafer low dose rate acceptance testing program being implemented for all Intersil radiation hardened products. We also discuss the design and construction details of a vault-type <sup>60</sup>Co irradiator facility currently on line at the Intersil Palm Bay facility to support these acceptance testing activities.*

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## I. INTRODUCTION

The low dose rate ionizing dose response of semiconductors has become a key issue in space applications. Routine  $^{60}\text{Co}$  acceptance testing at high dose rate has been demonstrated to be nonconservative for some technologies, and is increasingly being regarded as a classical accelerated test that has transitioned into a nonlinear range. The actual dose rate in space is many orders of magnitude below these acceptance testing levels. Intersil is addressing this changed market using a three-phase approach.

First, a low dose rate testing program of thirteen selected legacy parts was initiated in 2009 [1, 2] and has now been concluded. These tests were performed in accordance with the MIL-STD-883 Test Method 1019.7 diagnostic protocol. In all cases the experimental matrix consisted of five samples irradiated at high dose rate with all pins grounded, five samples irradiated at high dose rate under bias, five samples irradiated at low dose rate with all pins grounded, five samples irradiated at low dose rate under bias and one control unit. The majority of the Legacy parts being tested under this program are implemented in dielectrically isolated complementary bipolar processes. Two of the Legacy ELDRS tests were performed on HS26CxRH parts, which use junction-isolated (bulk) epi CMOS technology. At this time all thirteen tested parts have completed 150krad(Si) at low dose rate, and reports are posted on the Intersil Web site [3].

As a second phase, all new development parts such as the ISL70001SRH [4] and the ISL7884xASRH [5] are now characterized at both high and low dose rate as a routine part of the product development. These parts use a 0.6 $\mu\text{m}$  bulk BiCMOS power management process and represent an extension of the Intersil RHA product line into much higher levels of integration. Both parts were found to be ELDRS-free, and reports summarizing the results for these two products are posted on the Intersil Web site [3] for ready reference.

As a third step, Intersil is introducing wafer by wafer low dose rate acceptance testing as a complement to current high dose rate acceptance testing. A vault-type  $^{60}\text{Co}$  low dose rate irradiator to support this work has been completed at the Intersil Palm Bay facility. The balance of this note discusses the design and construction of this facility and the test methodologies to be used for acceptance testing work.

## II. CURRENT HIGH DOSE RATE QUALIFICATION PROCEDURES

Current Intersil high dose rate total dose acceptance testing is performed on a wafer by wafer basis. This procedure provides RHA assurance at the wafer level, which is the most basic level of the IC fabrication process. Following probe and die separation, sample die are selected at random from each wafer; the sample size is based on transistor count (4 die/wafer for chips with less than 4000 transistors or 2 die/wafer for chips with greater than 4000 transistors) as outlined in MIL-STD-883, TM 5005, Group E, Subgroup 2. The samples are assembled and

characterized using the production automated test equipment (ATE) and are then irradiated at high dose rate to the maximum level specified in the applicable Standard Microcircuit Drawing (SMD). The irradiation is performed under bias. A second round of ATE testing is then performed, at room temperature only. Any rejects in the sample fail the wafer.

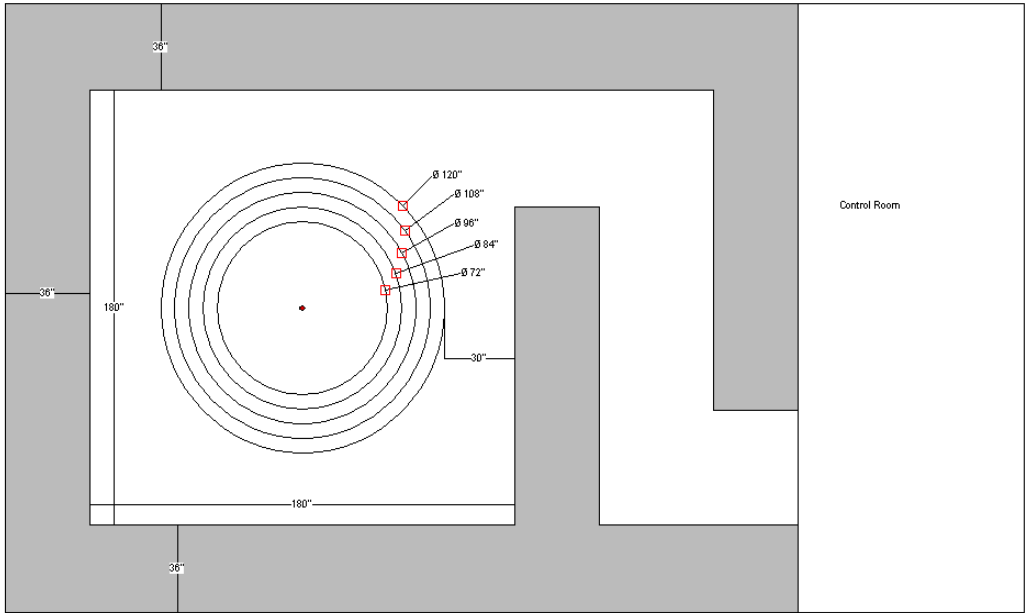
High dose rate testing at the Palm Bay, Florida Intersil facility has historically been performed using Gammacell 220 <sup>60</sup>Co irradiators. Initial low dose rate testing at Intersil was performed using a J. L. Shepherd and Associates model 484 research <sup>60</sup>Co low dose irradiator, which is not suited to volume long-term testing. Low dose rate testing has also performed on an outsourced basis at White Sands Missile Range SVAD (White Sands, NM).

An extension of the current high dose rate wafer acceptance procedure to the low dose rate regime is not straightforward. Current high dose rate tests are performed to a level of 300krad(Si), in nearly all cases, and such a test can be performed in an afternoon. An equivalent 300krad(Si) test at 0.01rad(Si)/s takes some 347 days. The current low dose rate level of general interest to the user and research communities is in the 50 to 100krad(Si) range. An initial decision was thus made to acceptance test all wafers to 50krad(Si) at low dose rate, which strikes a balance between TID level, test duration and cost. Note that all products will be acceptance tested at low dose rate, including not only bipolar and BiCMOS products that are considered to be an ELDRS risk, but CMOS parts as well.

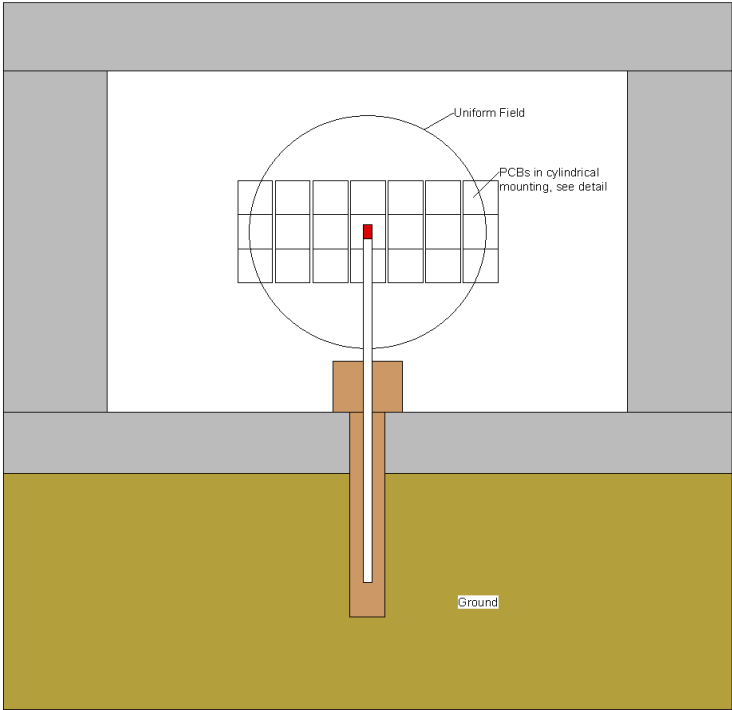
Since the exposure time at 50krad(Si) at .01rad(Si/s is some 60 days, roughly 40 tests must be run in parallel on average for current production volumes, requiring a large isodose test volume irradiator. Supporting this large number of parallel tests required extensive test automation, both from the scheduling and power supply control and sequencing standpoints. To support the low dose rate wafer level RHA acceptance testing program, Intersil has completed the construction and activation of a vault-type <sup>60</sup>Co irradiator and associated equipment and fixturing.

### **III. LOW DOSE RATE IRRADIATION FACILITY**

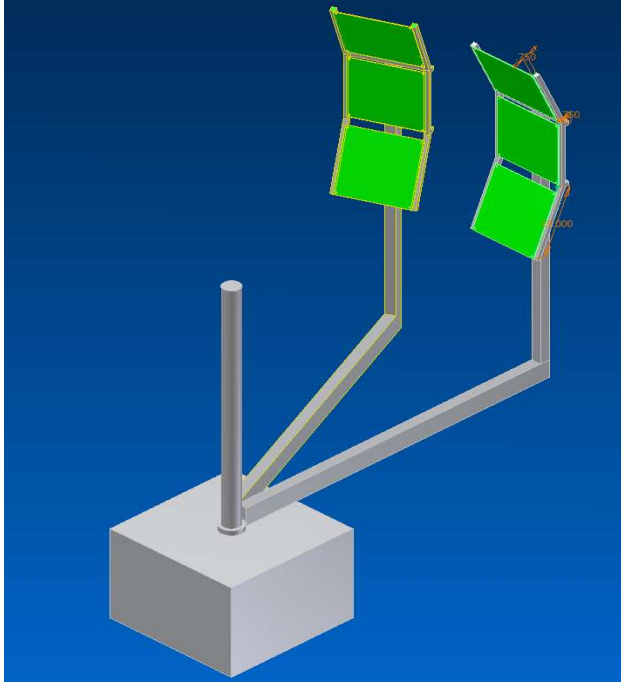
Construction and activation of the Intersil Palm Bay, Florida low dose rate facility is complete. The prime contractor was Hopewell Designs, Inc. (5940 Gateway Drive, Alpharetta, GA 30004; [www.hopewelldesigns.com](http://www.hopewelldesigns.com)). Figs. 1 - 3 provide conceptual CAD drawings of the facility. The vault structure has 36" high-density concrete walls and a 48" roof, both constructed of high-density concrete. This shielding structure provides an estimated 10,000x reduction in dose rate measured at 11 feet from the pop-up source.



**Fig. 1:** CAD drawing of low dose rate irradiator vault floor plan showing the vault and source, concentric fixturing, the labyrinth entrance and the adjacent control room. Doors are not shown for clarity. The inside dimensions of the vault are 15 x 15 feet (5 x 5m).



**Fig. 2:** Conceptual CAD drawing (not to scale) of room layout showing the central 'pop-up'  $^{60}\text{Co}$  source and the approximately spherical device under test (DUT) board mounting structure. The source has a lower storage position in a 12" welded stainless steel well below grade. The 36" concrete walls and 48" roof provide a 10,000x estimated reduction in outside exposure rate.



**Fig. 3:** Conceptual CAD drawing of two segments of the DUT board mounting system. The board holders are arranged in a partial sphere surrounding the  $^{60}\text{Co}$  source. All DUT boards are enclosed in individual PbAl spectrum hardening boxes to filter out secondary radiation. Note that the final version of this design has four DUT boards per arm for a total DUT board capacity of 64.

The radiation source consists of 50 Curie (Cy) of  $^{60}\text{Co}$  radioisotope in an air-actuated aluminum 'pop-up' pellet. The pellet is housed in a stainless steel tube, which is in turn centrally located in a 12" welded stainless steel well (Fig. 2). The recurved SS tube minimizes radiation leakage while the source is in the 'down' position. The exposure rate inside the concrete vault with the source in the shielded ('down') storage position is estimated at 0.1mR/hr. Estimated exposure rate at the exterior of the vault is 0.45mR/hr while the irradiator is in operation. The design field uniformity within the irradiator test volume is +/-10%, while the calculated uniformity is +/-2.5%. The design dose rate is 0.01rad(Si)/s (10mrad(Si)/s) at the device under test (DUT) board location. The separate source pellet design greatly simplifies source replacement.

The DUT boards are supported on aluminum structures; the horizontal distance between the source and the board location is designed to be changed to maintain the required dose rate as the source loses activity. The DUT board fixturing (Figs. 3, 7 and 8) is designed to accommodate a total 64 9"x12" PC boards. All DUT boards are enclosed in a spectrum hardening PbAl box to filter out secondary radiation. The fixturing system approximates an isodose sphere centered on the source pellet and consists of sixteen 'wings' each supporting one PbAl box enclosing four DUT board holders. Design calculations indicate that a new 50 Curie source will result in a dose rate of .0097rad(Si)/s at 48", while a 22.5Cy source (representative of a 50Cy source after 5 years of decay) will result in the same dose rate at 36". Predicted total dose uncertainty was calculated at +/- 3% or better, depending on data collection tools. All irradiations are overtested by 3% to compensate for this uncertainty.

Operator safety is a key issue in the design of any irradiation facility. All doors have interlocks and position sensors, and the facility is operated entirely from the control room. Emergency stop buttons are provided, which will immediately drop the source into the shielding well. Loss of power or air pressure, actuation of an emergency stop button or any attempts to open any of the doors will drop the source and force the system into a safe state. All systems including biasing power supplies and control computers are operated from dedicated uninterruptible power supplies (UPS), with long-term power outages (recall we're in a hurricane zone) handled by on-site Diesel power generating facilities. Hopewell Designs have a long history of building reliable and robust systems. Figs. 4 - 5 show images of the irradiation facility taken during construction, while Fig. 6 shows the completed facility.



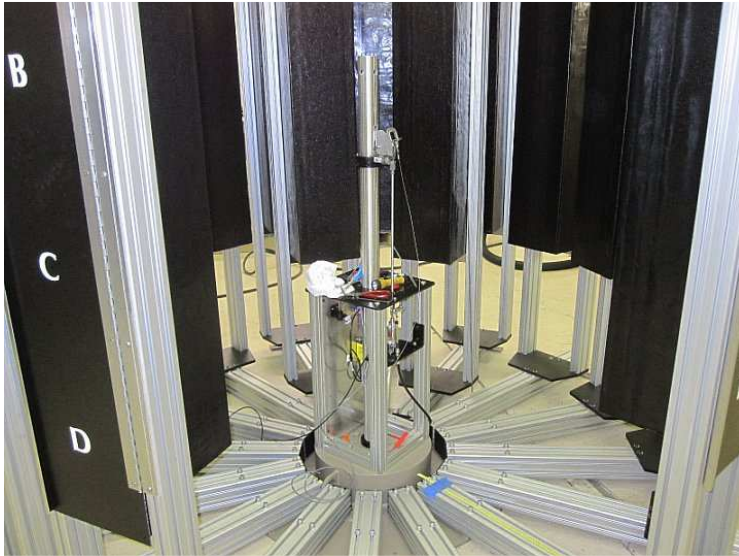
**Fig. 4:** Site excavation before pouring the vault foundation. The top of the source well is clearly visible to the left of image center. The PVC piping provides cable raceways between the vault and the Intersil Palm Bay building 58 control room (right).



**Fig. 5:** View of wall forms before the second (wall) concrete pour. The labyrinth vault access architecture can be clearly seen.



**Fig. 6:** External view of the completed low dose rate irradiator.



**Fig. 7:** View of 'pop-up' source (center) and surrounding test racks. The vertical test board holder and their PbAl spectrum hardening filter boxes are shown. The holders are on rails and can be moved towards the centrally located source as it loses activity. The curvature of the DUT rack is not apparent as the rack is hidden by the PbAl box. The system supports 64 simultaneous tests.



**Fig. 8:** Internal view of a PbAl box and enclosed DUT board rack. The curvature of the test rack can be clearly seen; this curvature combines with the circular arrangement of the racks to generate an approximately spherical isodose profile at the DUT boards.



Control and scheduling of 64 two-month acceptance tests (maximum) in parallel while taking source activity into account would be problematic at best. The Hopewell irradiator design puts most operations under computer control. The operator continues to have full control over the system, but is able to focus on areas where expertise is most needed. The automated irradiator control system is based on the National Instruments LabVIEW environment. Features include automatic calibration and calibration report generation, dose rate calculation and source decay correction. The irradiator calibration procedure uses an ion chamber and electrometer and is fully automated.

The irradiator has 64 board positions available, each of which can have up to 8 different power supply voltages. Control and tracking of exposure time, total dose and dose rate are vitally important. Each DUT board is uniquely identified by a bar-coded label which enables the control computer to track all boards while in the chamber. Each DUT board socket is verified as meeting the ELDRS irradiation diagram (SMD or internal specification) before each new lot is loaded, and DUT board supply currents are recorded before initiating irradiation.

Other capabilities are system status, system safety and interlock status, exposure status and source position. Exposure rate and distance are linked so that when one is changed, the other is calculated and updated. Exposure and time are also linked. When an exposure rate is specified, the system calculates a position, automatically compensating for source decay.

Products with multiple power supply requirements typically require individual power supply power-up and power-down sequences. A dedicated power supply control computer determines and controls the supply voltages and power sequencing for the individual board. The power supply control computer records voltages and currents to insure correct system operation. Figs. 7 - 8 show the centrally located 'pop-up'  $^{60}\text{Co}$  source and DUT board fixturing detail.

#### **IV. LOW DOSE RATE WAFER ACCEPTANCE TESTING PROCEDURE**

The Intersil low dose rate acceptance testing procedure is similar to the current high dose rate procedure. Four sample die are drawn from each probed wafer and are processed through the entire high-reliability Class V screening sequence. TM 5005 allows a sample size of 2 for parts with greater than 4000 transistors, but as both biased and unbiased tests are performed, this would reduce the effective sample size to 1; hence, a uniform sample size of 4 is used for all products. The samples (2 die are biased and 2 die are grounded) are then irradiated to 50krad(Si) at 0.01rad(Si)/s. A second round of room temperature ATE testing is then performed, and any rejects fail the wafer.

It is important to note that all Intersil RHA parts will eventually be qualified using this procedure. This reflects the increased emphasis on low dose rate performance within our customer base and also reflects recent results [6, 7] suggesting low dose rate sensitivity in advanced shallow trench isolated CMOS processes. The existing high dose rate acceptance testing procedure will continue, with a decision point some three years in the future when the current Gammacell 220 will go out of dose rate specification.

As a part of the low dose rate qualification, Intersil will provide an enhanced data package that will accompany each shipment of QML class level V low dose rate qualified product. The data package will include an updated Radiation Effects Certificate of Compliance (C of C) for high and low dose rate testing. It will also provide high and low dose rate room temperature variables data for pre and post irradiation tests.

## V. CONCLUSION

This document discusses high dose rate total dose wafer acceptance testing at Intersil and the changes to these procedures necessitated by increased emphasis on low dose rate performance at the system level. We also discuss planning for wafer acceptance testing of Intersil parts at low dose rate, and the design and construction of a vault-type <sup>60</sup>Co irradiator to support these plans.

## VI. REFERENCES

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