Altera and IDT Synchronous Ethernet Solution for ITU-T G.8262

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Introduction

Synchronous Ethernet (SyncE) is a set of ITU-T standards for networking that enable the synchronization of clock frequencies in an Ethernet network. The standards allow use of Ethernet networks, which are inexpensive compared to traditional synchronized networks, for applications such as cellular telephony.

The principle behind SyncE is simple: one node in the network is connected to a primary reference clock source; all other nodes synchronize to the primary reference by using a clock that is recovered from the physical layer.

There are a few challenges to implementing SyncE networks:

- ITU-T G.8261 defines the architecture and wander performance of a SyncE network.
- Since clock jitter/wander is additive, the quality of clock synchronization must be carefully controlled at each node. ITU-T G.8262 specifies the clocking at each individual Ethernet node.
- A message protocol is needed in the network to control and monitor clock synchronization. The protocol for these messages is defined in ITU-T G.8264.

Altera® FPGAs can be used in conjunction with the IDT 82P33731 Synchronous Equipment Timing Source (SETS) for 1G, 10G, 40G, or 100G SyncE to design flexible Ethernet nodes. The FPGAs can be programmed to implement or offload the protocols required by ITU-T G.8264, and can be added to a network according to ITU-T G.8261.

The IDT 82P33731 SETS device acts as an Ethernet Equipment Clock source for the FPGA, and performs clock cleanup, advanced clock monitoring, and switchover functions. The 82P33731 is pin compatible with 82P33831, which is suitable for IEEE 1588 Precision Timing Protocol (PTP) applications. PTP is often used along with SyncE in applications that need time and phase synchronization.

The sections that follow describe the Altera and IDT SyncE solution in more detail, including test results that show that the solution complies with the recommendation for SyncE clocking in ITU-T G.8262.

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The Altera and IDT SyncE Solution

Figure 1 is a block diagram of an Ethernet line card built using the Altera and IDT SyncE solution. The line card includes an Altera FPGA with multiple integrated high-speed serial transceivers that can be used to implement Ethernet links, a built-in processor (the SoC CPU), on-chip fractional phase-locked loops (PLLs), and programmable logic. It also includes an IDT 82P33731 SETS device, and a set of local reference clock sources.

In this system, the programmable logic in the FPGA is loaded with a design that includes one or more Ethernet cores, along with any other application logic needed on the card. Altera offers a variety of Ethernet intellectual property (IP) cores, including 10 Gb Ethernet MAC with 10GBASE-R PCS and PMA (PHY), 40 Gb Ethernet MAC and 40GBASE-R4 PHY, and 100 Gb Ethernet MAC and CAUI or CAUI-4 PHY, which can be used with the IDT SETS device. ITU-T G.8264 defines the Ethernet synchronization messaging channel (ESMC), the protocol behavior, and the message format for SyncE that can be implemented in the programmable logic, or in the built-in SoC CPU.

Each serial transceiver recovers a clock from the data it receives, using one of the clock sources on the line card to initialize its clock/data recovery (CDR) circuit. The recovered clocks are connected to the IDT SETS using external pins on the FPGA. A PLL on the FPGA reduces the rate of the recovered clocks to simplify routing PCB routing between the FPGA and SETS device. SETS clock inputs can accept a variety of recovered clock rates, from 1 pulse per second (PPS) to 650 MHz.

Figure 1. Altera and IDT Synchronous Ethernet Solution

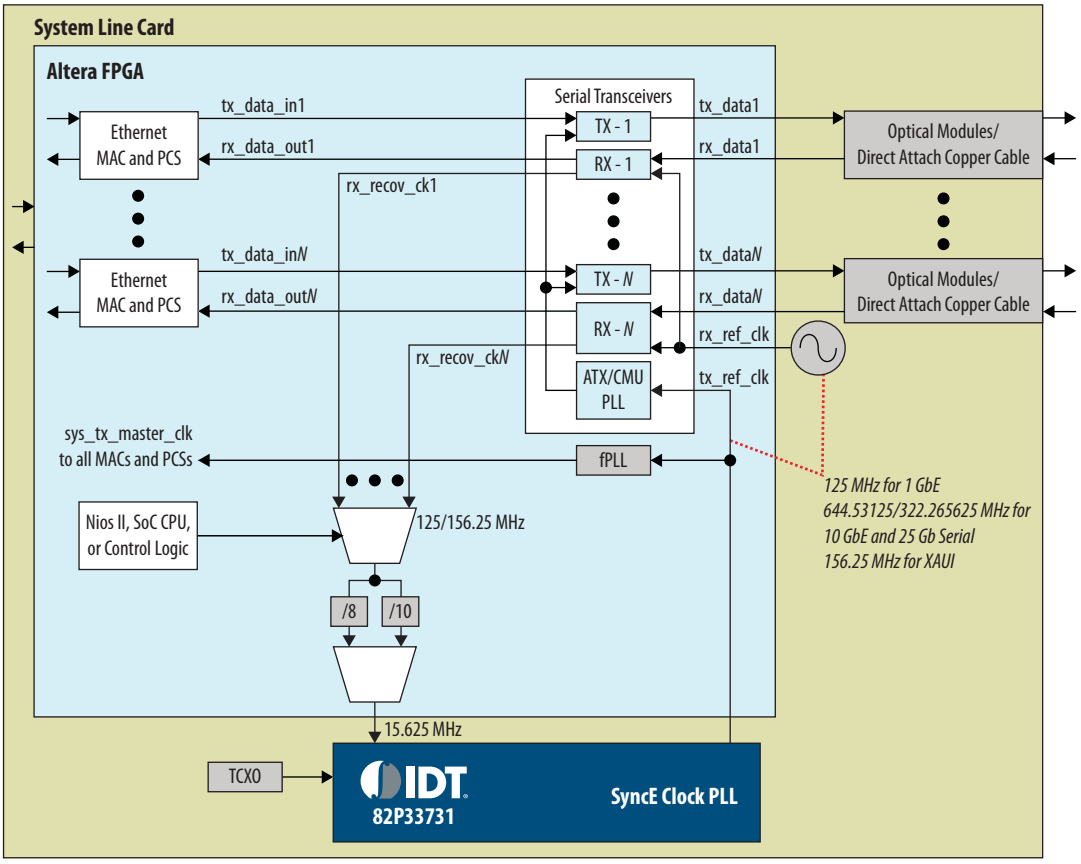
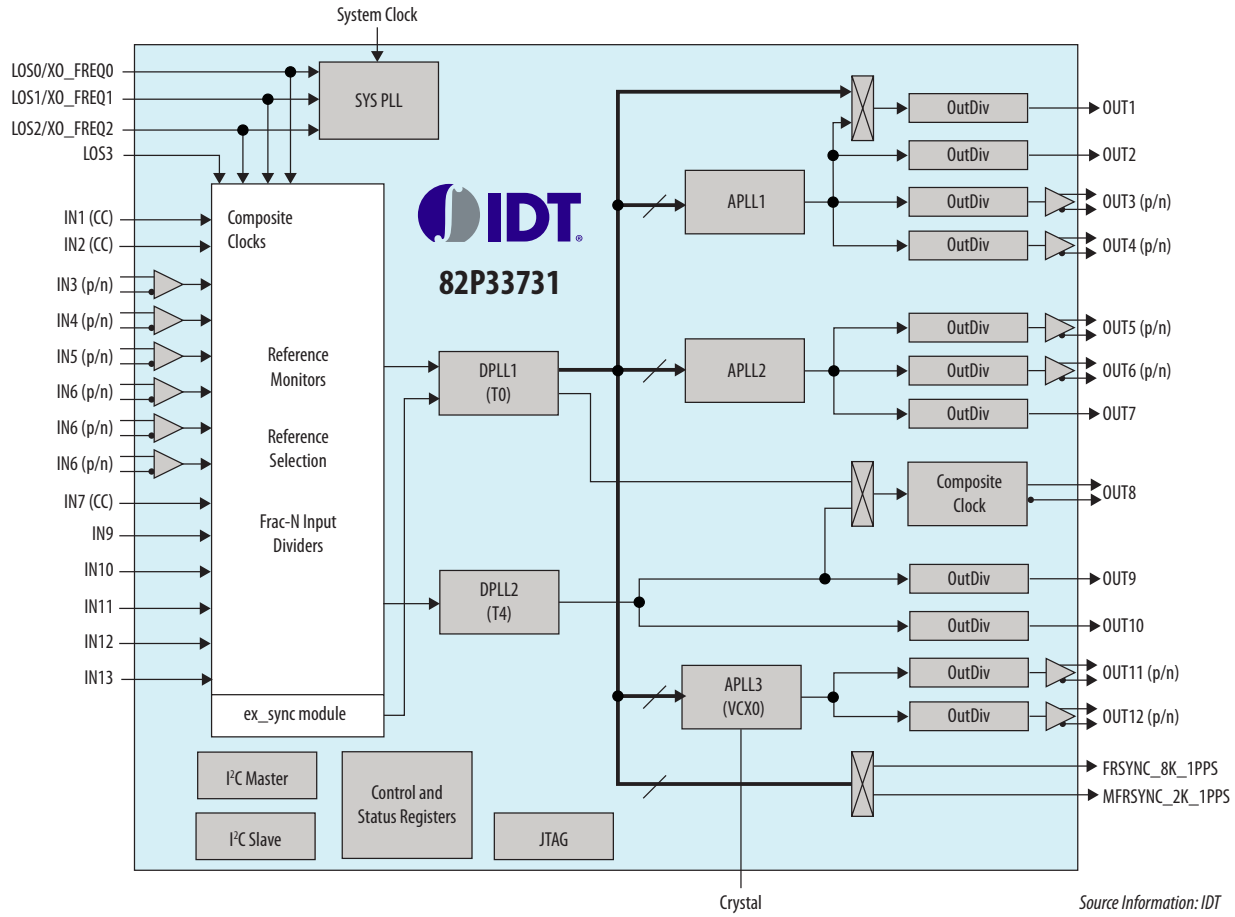


Figure 2. 82P33731 Synchronous Equipment Timing Source



As shown in Figure 2, the SETS has multiple clock inputs, both single-ended and differential, that can be driven by recovered clocks from the Altera FPGA. The SETS uses DPLL1 to clean a selected recovered clock. DPLL1 meets the frequency accuracy, pull-in, hold-in, pull-out, noise generation, noise tolerance, transient response, and holdover performance requirements of ITU-T G.8262.

The next stage of cleanup after DPLL1 is APLL3, which is a voltage controlled crystal oscillator (VCXO) based jitter attenuating analog PLL. APLL3 can be provisioned with one or two selectable crystal resonators to support up to two base frequencies. The output clocks generated by APLL3 are suitable for serial 40GBASE-R and lower rate interfaces. These are used to drive the reference clock inputs for the ATX PLLs on the FPGA, which in turn drive the clocks on the FPGA, synchronizing the line card logic to the SyncE master clock.

One of the requirements of ITU-T G.8262 is that an Ethernet endpoint be able to switch gracefully from one clock source to another in case of link failure. To enable switchover, the FPGA provides multiple recovered clocks to the SETS, along with LOS signals to indicate whether each recovered clock comes from a working Ethernet link.

The SETS can be directed to use a specific recovered clock, or programmed to automatically select a clock based on pre-programmed priorities and locking allowances. The SETS continually monitors its input clocks to determine whether they are within pre-programmed frequency thresholds.

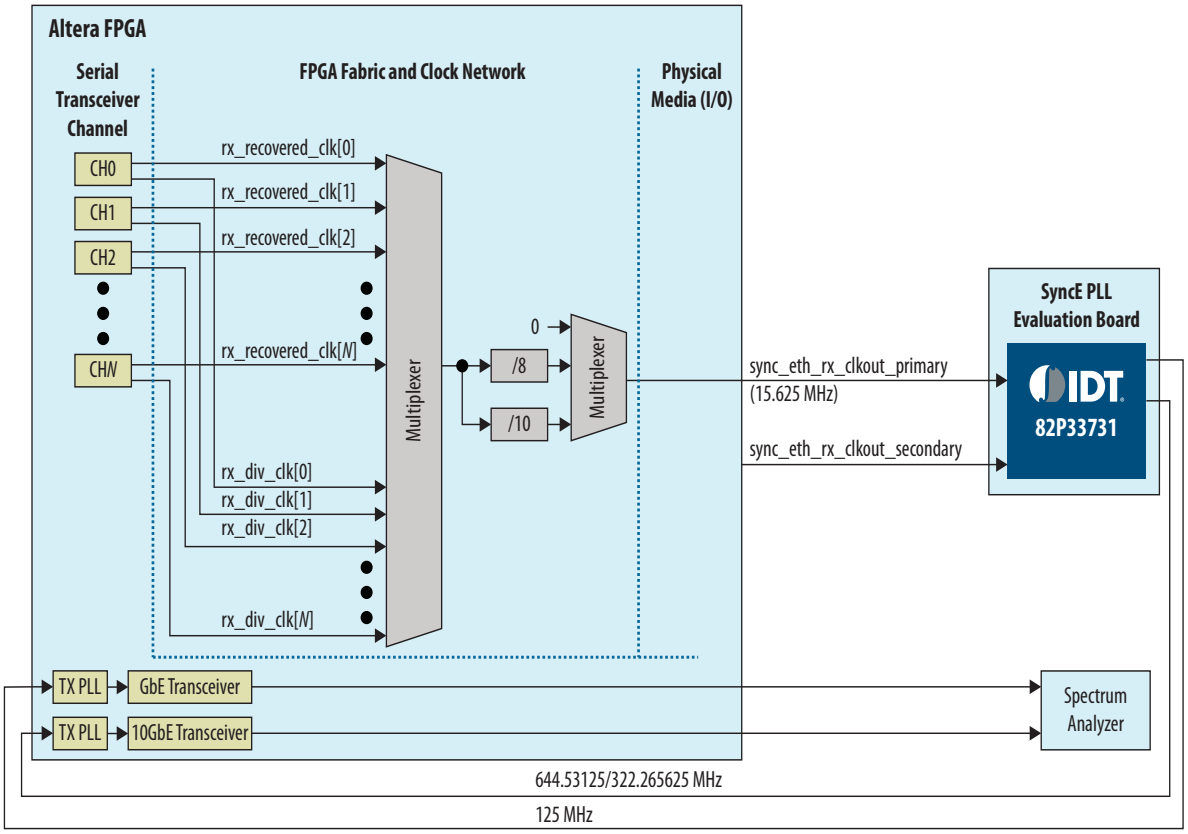
ITU-T G.8262 Test Results

A series of tests were performed jointly by Altera and IDT to show that the Altera and IDT SyncE solution meets the requirements of ITU-T G.8262 for an Ethernet Equipment Clock.

Many G.8262 requirements depend only on the capabilities of the DPLL and APLL on the IDT SETS device. These tests were performed by IDT at their laboratory. A full compliance report from the IDT tests is available under non-disclosure agreement (NDA).

Figure 3 shows the block diagram of the test setup that was used for jitter tests that require the FPGA and SETS to work together. The setup used an Altera Stratix® V FPGA, and an IDT 82P33731 SETS device.

Figure 3. Jitter Test Setup



The FPGA implemented 16 Ethernet 10GBASE-R channels using the Altera 1G/10Gb Ethernet MAC core with the Altera 10GBASE-R PHY IP core. Because the Ethernet cores are small, a Gray-code noise generation core was added to the design so that 71% of the FPGA resources were used, mimicking the switching noise that might be present in a line card with additional application logic.

The FPGA provided two recovered clocks to the IDT SETS device, one for 1GbE and one for 10GbE. The 1GbE recovered clock was divided by 8 before driving it on the PCB to the IDT SETS; the 10GbE recovered clock was divided by 10.

Table 1. G.8262 Test Results (Part 1 of 2)

ITU-T Recommendation G.8262	Requirements	Compliance
Frequency accuracy (section 6)	Under free-running and prolonged holdover conditions, the EEC output frequency accuracy should not be greater than 4.6 ppm with regard to a reference traceable to a [ITU-T G.811 - PRC] or [ITU-T G.8272 - PRTC] clock, over a time period of 1 year.	Yes, with EEC capable TCXO (see IDT AN-807)
Pull-in range (section 7.1)	The minimum pull-in range should be ±4.6 ppm with regards to the local oscillator frequency offset.	Yes
Hold-in range (section 7.2.2)	The hold-in range for EEC-Option 2 should be ±4.6 ppm with regards to the local oscillator frequency offset.	Yes
Wander generation (section 8.1, 8.2)	Represents the amount of phase noise produced at the output when there is an ideal input reference signal. Considers both constant (within ±1 ^{0}K) and variable temperature.	Yes
Jitter generation (section 8.3)	In the absence of input jitter at the synchronization interface, the intrinsic jitter at the synchronous Ethernet output interfaces, as measured over a 60-second interval, should not exceed the 1G limits of 0.5UIp-p using measuring filter of 2.5 kHz to 10 MHz.	Yes (Altera + IDT test)
	In the absence of input jitter at the synchronization interface, the intrinsic jitter at the synchronous Ethernet output interfaces, as measured over a 60-second interval, should not exceed the 10G limits of 0.5 UIp-p using measuring filter of 20 kHz to 80 MHz.	Yes (Altera + IDT test)
Noise tolerance (section 9)	Indicates the minimum noise (wander and jitter) at the input of the clock that should be accommodated while: ■ Maintaining the clock within prescribed performance limits ■ Not causing any alarms ■ Not causing the clock to switch reference ■ Not causing the clock to go into holdover	Yes
Noise transfer (section 10)	The minimum bandwidth requirement for an EEC-option 1 is 1 Hz. The maximum bandwidth requirement is 10 Hz.	Yes
	The maximum bandwidth requirement for an EEC-option 2 is 0.1 Hz.	Yes
	In the passband, the phase gain of the EEC should be smaller than 0.2 dB (2.3%).	Yes
Short-term phase transient response (section 11.1)	Reflects the performance of the clock in cases when the (selected) input reference is lost due to a failure in the reference path and a second reference input signal, traceable to the same reference clock, is available simultaneously, or shortly after (maximum 15 seconds) the detection of the failure (for example, in cases of autonomous restoration).	Yes
Long-term phase transient response (Holdover) (section 11.2)	Bounds the maximum excursions in the output timing signal when no reference input signal is available. Additionally, it restricts the accumulation of the phase movement during input signal impairments or internal disturbances. Considers both constant (within ±1 ^{0}K) and variable temperature.	Yes, with EEC capable TCXO (see IDT AN-807)

Table 1. G.8262 Test Results (Part 2 of 2)

ITU-T Recommendation G.8262	Requirements	Compliance
Phase response to input signal interruptions (section 11.3.1)	For short-term interruptions on synchronization input signals that do not cause reference switching, the output phase variation should not exceed 120 ns, with a maximum frequency offset of 7.5 ppm for a maximum period of 16 ms.	Yes
Phase discontinuity (section 11.4)	In cases of infrequent internal testing or rearrangement operations within the slave clock, the phase transient at the output of EEC should meet the specifications as specified in section 11.4.	Yes
External synchronization interfaces (section 12.1)	Synchronization Ethernet equipment will require a range of external synchronization interface types to be supported that will allow synchronization to be derived from an [ITU-T G.812] SSU/BITS clock, from the output of an [ITU-T G.813] SEC or from another [ITU-T G.8262] EEC.	Yes

Document Revision History

Table 2 shows the revision history for this document.

Table 2. Document Revision History

Date	Version	Changes
November 2015	1.0	Initial release.