Intersil Integrated FET DC/DC Converters

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Introduction

Designing a switching regulator can be a daunting task! Decisions must be made concerning circuit configuration - buck, boost, flyback, SEPIC, etc. A method of control must be determined - Pulse Width Modulation (PWM), hysteretic, Pulse Frequency Modulation (PFM), current mode, voltage mode, etc. Once the method of control is determined, a controller integrated circuit (IC) must be selected. Then, power switches such as MOSFETs must be selected, their power dissipation calculated, and the gate drive circuit designed. Inductance and capacitance must be calculated, then the components must be selected for saturation current, RMS ripple current, DCR, ESR, physical size, etc. And then, just when you thought you were done, loop compensation rears its ugly head! Is the circuit stable? How do I ensure stability? Where are the bode plots for the internal circuits of the controller IC? How does my load effect stability? What about short circuit protection or current limiting?

Just when you thought you were done with the design, the PCB layout designer asks you about the PCB layout requirements for the FETs, the inductor, the loop compensation components, the grounding scheme, etc. He says the inductor and output capacitor you selected are too big for the space allowed for the power supply and he wants to place the FETs 2 inches from the IC controller chip. And, what is a Kelvin connection for the current sense resistor? What about the thermal design? Where is the heatsink? Do you realize that vias are really inductors?

Yes, designing a switching regulator can be a daunting task! And, making the task even more difficult is the fact that most embedded switching power supplies are designed by the digital hardware engineer, and not by an analog or power supply engineer.

The purpose of this Application Note is to show how the Intersil Integrated FET DC/DC Converters can make the task of designing an embedded step down (buck) DC/DC converter much easier. Most of the difficult design decisions are included in the regulator chip, such as FETs, current sense elements, loop compensation, current limiting, and over temperature protection. By using fixed inductor and capacitor values, their selection process is eliminated. FETs are internal so their characteristics and internal connections are optimized for the design. High frequency switching up to 1.5MHz allows the use of very small inductors and capacitors. Finally, there are evaluation boards and recommended PCB layouts for most of the Intersil Integrated FET DC/DC Converters.

This Application Note will also share simple test circuits to quickly evaluate loop stability without the headaches of Bode plots and phase margin measurements. The correct technique for connecting an oscilloscope probe to measure output noise will be shown with actual scope photos of good and bad probing techniques. To minimize the difficulty of sequencing multiple power supplies, a simple circuit for tracking the output voltages with a common ramp circuit will be shown.

Intersil Integrated FET DC/DC Converter Product Family

(Parts highlighted are in this Application Note)

DEVICE	V_{IN} RANGE (V)	V_{OUT} RANGE (V)	I_{OUT} (MAX) (A)	FREQ. (kHz)	POR	LOW I_Q MODE	MARGIN	TRACK	SYNC	PACKAGE
EL7535	2.5 - 5.0	0.8 - V_{IN}	0.35	1500	Yes					10 Ld MSOP
ISL6413	3.0 - 3.6	Fixed 1.8, 2.84, 2.84	0.4 0.3, 0.2	750	Yes				Yes	24 Ld QFN
ISL8010	2.5 - 5.5	0.8 - V_{IN}	0.6	1500		Yes			Yes	10 Ld MSOP
EL7534	2.5 - 5.5	0.8 - V_{IN}	0.6	1500	Yes					10 Ld MSOP
ISL6410	3.0 - 3.6	Fixed 1.2, 1.5, 1.8	0.6	750	Yes				Yes	10 Ld MSOP, 16 Ld DFN
ISL6410A	4.5 - 5.5	Fixed 3.3, 1.8, 1.2	0.6	750	Yes				Yes	10 Ld MSOP, 16 Ld DFN
ISL6455	3.0 - 3.6	0.8 - 2.5	0.6, 0.3, 0.3	750	Yes				Yes	24 Ld QFN
ISL6455A	4.5 - 5.5	0.8 - 3.3	0.6, 0.3, 0.3	750	Yes				Yes	24 Ld QFN
EL7531	2.5 - 5.0	0.8 - V_{IN}	1	1500		Yes			Yes	10 Ld MSOP
EL7536	2.5 - 5.0	0.8 - V_{IN}	1	1500	Yes					10 Ld MSOP
ISL8011	2.7 - 5.5	0.8 - V_{IN}	1.2	1500	Yes					10 Ld DFN
EL7532	2.5 - 5.0	0.8 - V_{IN}	2	1500	Yes					10 Ld MSOP
ISL8013	2.5 - 5.5	0.8 - V_{IN}	3	1400					Yes	14 Ld HTSSOP
EL7554	3 - 6	0.8 - V_{IN}	4	200 - 1000			Yes	Yes	Yes	28 Ld HTSSOP
ISL65426	2.375 - 5.5	Fixed 0.6, 1.2, 1.5, 1.8	6	1000						50 Ld QFN
		Fixed 0.6, 1.8, 2.5, 3.3								
EL7566	3 - 6	0.8 - V_{IN}	6	200 - 1000			Yes	Yes		28 Ld HTSSOP

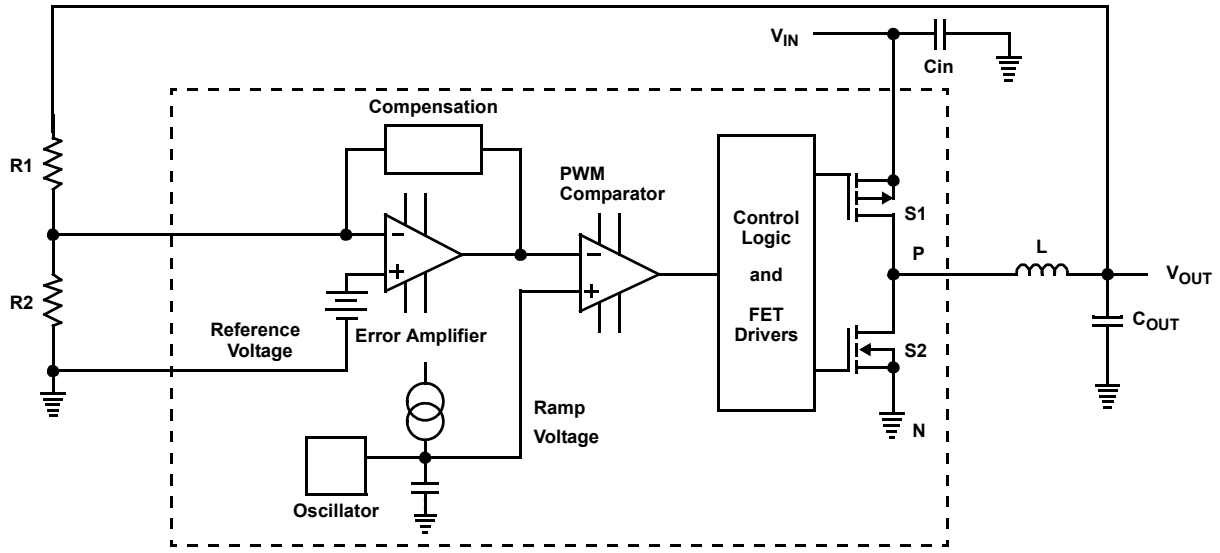


FIGURE 1. SIMPLIFIED SCHEMATIC

Features and Advantages of Intersil Integrated FET DC/DC Converters

Figure 1 is a simplified schematic for a typical buck regulator using an Intersil Integrated FET DC/DC Converter.

Ease of Design

Notice the ease of use for this circuit since there are only 4 external components required for the design - an output inductor (L), an output capacitor (C_{OUT}), and two resistors (R1, R2) to set the output voltage. Additionally, the circuit should include bypass capacitors because this is a must.

Internal FETs

Notice the use of internal FETs so there is no need for FET selection. The internal FETs are optimized for the circuit parameters such as input voltage, load current, switching frequency, etc. Also, since the FETs are internal, there are no PCB traces required to connect the FETs to the controller.

Synchronous Rectification for High Efficiency

Synchronous rectification (S1 and S2) is used for high efficiency in all the Intersil Integrated FET DC/DC Converter products. The advantage of high efficiency is long battery life in portable applications and very low temperature rise at high currents.

100% Duty Cycle Operation

The use of a P-channel FET for S1 allows 100% duty cycle operation so the output voltage range can include the input voltage for very low dropout operation.

Internal Loop Compensation

Internal loop compensation frees the design engineer from struggling with the difficult task of ensuring closed loop stability. It also simplifies the inductor and output capacitor selection since there are fixed minimum values shown on the device data sheet. Increasing the inductance or capacitance only increases the loop stability (at the expense of transient response and physical size).

Ceramic Capacitor Design

Due to the high switching frequency and internal loop compensation, the use of small ceramic capacitors is possible for both the input and output capacitor.

Small Form Factor

Very small physical size is possible due to tiny IC packages (QFN and MSOP), high switching frequency (up to 1.5MHz) which allows very small inductors and ceramic capacitors, and excellent thermal performance. For example, the EL7532 is available in the 10 Ld MSOP package, making the entire converter occupy less than $0.18in^2$ of PCB area with components on one side only.

Thermal Performance (θ_{JA})

Thermal performance of the Intersil Integrated FET DC/DC Converters has been greatly improved with the use of improved thermal management packaging techniques such as the QFN package and the fused lead MSOP.

PART #	I_{OUT} (A)	PACKAGE	θ_{JA} (°C/W)	MAX T_J
ISL6410	0.6	10 Ld MSOP	128	150
	0.6	16 Ld QFN	45	150
ISL8010	0.6	10 Ld MSOP	115	125
ISL6455	0.6, 0.3, 0.3	24 Ld QFN	36	150
ISL8011	1.2	8 Ld MSOP	160	150
EL7532	2	10 Ld MSOP Fused Lead	115	125
ISL8013	3	14 Ld HTSSOP	TBD	125
EL7566	6	28 Ld HTSSOP	30	135
ISL65426	6	50 Ld QFN	45	150

External Frequency Synchronization

External frequency synchronization is possible with many of the Intersil Integrated FET DC/DC Converters, providing the user with the option of improved EMI performance in both single or multiple DC/DC converter systems.

- External frequency synchronization allows the user to locate the switching noise at a “magic” frequency to avoid system interference in a single DC/DC converter system.
- In a multiple DC/DC converter system, external frequency synchronization can eliminate a beat frequency caused by the two switching regulators operating at different frequencies. Additionally, external frequency synchronization can provide multi-phase switching to reduce ripple currents and noise.
- The ISL8010 and ISL8013 synchronization feature allows the switching frequency to be increased to as high as 12MHz, allowing much smaller input and output filters to reduce the EMI.
- Table 1 summarizes the external frequency synchronization capability of the devices highlighted in this application note.

TABLE 1.

PART #	FIXED SWITCHING FREQUENCY	SYNC CAPABILITY	SYNC RANGE
ISL6410	750kHz	Yes	500kHz-1MHz
ISL8010	1.4MHz	Yes	12MHz, max
ISL6455	750kHz	Yes	500kHz-1MHz
ISL8011	1.5MHz	No	
EL7532	1.5MHz	No	
ISL8013	1.4MHz	Yes	12MHz, max
EL7566	200kHz-1MHz	Yes	0.8 • Fset
ISL65426	1MHz	No	

Advanced Control Functions (UVLO, overcurrent and over temperature protection, tracking, etc.)

Intersil Integrated FET DC/DC Converters offer advanced control functions as shown in Table 2.

TABLE 2.

PART #	ISL6410	ISL8010	ISL6544	ISL8011	EL7532	ISL8013	EL7566	ISL65426
Output Current (amp)	0.6	0.6	0.6, 0.3, 0.3	1.2	2	3	6	6
Enable Input	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Soft-Start	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Overcurrent Protection	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Thermal Protection	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Adjustable Output		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Input UVLO	Yes	Yes	Yes	Yes	Yes	Yes	Yes	
Power Good Output	Yes	Yes	Yes			Yes	Yes	Yes
Sync Input	Yes	Yes	Yes			Yes	Yes	
Output Overvoltage Protection	Yes		Yes				Yes	Yes
Fixed Output	Yes							Yes
Power on Reset Output			Yes	Yes	Yes			
Temperature Indicator							Yes	
Output Undervoltage Protection								Yes
Output Capacitor Discharge				Yes				
Tracking							Yes	
Margining							Yes	

Technical Discussion
ISL6410 and ISL6410A (600mA)

The ISL6410 and ISL6410A are 600mA integrated FET synchronous buck regulators using current mode PWM technology. The ISL6410 should be used for an input voltage of +3.3V ±10%, and the ISL6410A should be used for an input voltage of +5V ±10%. A single pin (VSET) programs the output voltage for 1.2V, 1.5V, or 1.8V (ISL6410) and 1.2V, 1.8V, or 3.3V (ISL6410A). An internally programmed switching frequency of 750kHz allows the use of small value inductors and capacitors; however, an external synchronizing frequency of 500kHz to 1MHz can be used if desired. Internal loop compensation is provided so there are no external components required for stabilizing the feedback loop. Likewise, slope compensation, as required for current mode control, is set internally. Extensive control and protection features include undervoltage lockout (UVLO), overvoltage, overcurrent, Power Good monitor, external Enable, supervisory Reset output, and thermal shutdown. The ISL6410 and ISL6410A are packaged in either a 10 Ld MSOP package or 16 Ld QFN package.

The schematic in Figure 2 shows a typical ISL6410A DC/DC converter for 5V to 3.3V at 600mA.

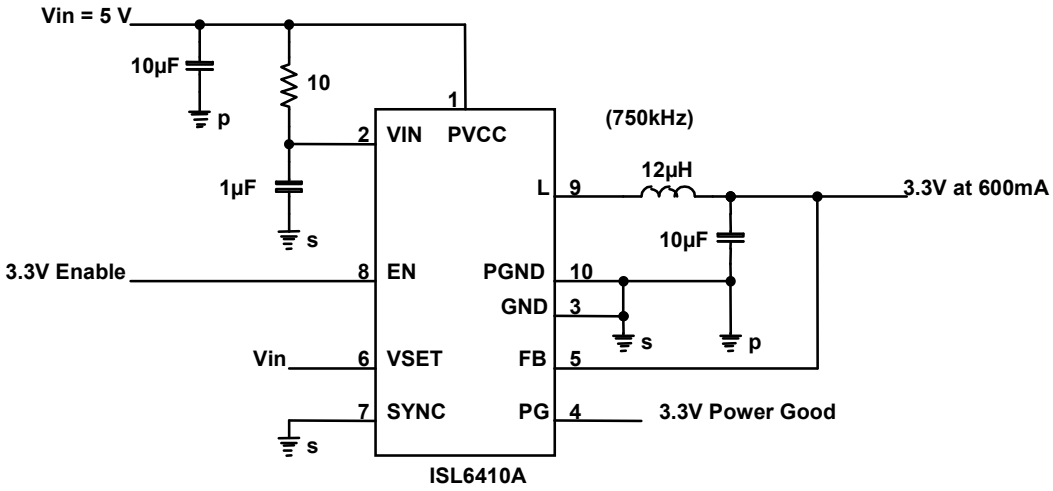


FIGURE 2.

Technical Discussion
ISL6455, ISL6455A (600mA and two 300mA LDOs)

The ISL6455 is a highly integrated triple output regulator which provides a single chip solution for FPGAs and wireless chipset power management. The device integrates a high efficiency 600mA synchronous buck regulator (adjustable) with two ultra low noise 300mA LDO regulators (adjustable). Either the ISL6455 or ISL6455A can be selected based on whether 3.3V ±10% or 5V ±10% is required as an input voltage. The PWM output voltage is resistor adjustable from 0.8V to 2.5V for the ISL6455 with a +3.3V input, and 0.8V to 3.3V for the ISL6455A with a +5V input. The ultra low noise LDO regulators are resistor adjustable from 1.2V to V_{IN}-0.3V (3.3V max).

The synchronous current mode control PWM regulator with integrated N- and P-channel power MOSFETs provides adjustable voltages based on external resistor setting. Synchronous rectification with internal MOSFETs is used to achieve high efficiency and reduced number of external components. Operating frequency is typically 750kHz allowing the use of smaller inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500kHz to 1MHz. The PG_PWM output indicates loss of regulation on the PWM output.

The ISL6455 also has two LDO adjustable regulators using internal PMOS transistors as the pass devices. The EN_LDO pin controls LDO1 and LDO2 outputs. The ISL6455 also integrates a RESET function, which eliminates the need for additional RESET IC required in µP, µC, or ASIC based applications. The IC asserts a RESET signal whenever the V_{IN} supply voltage drops below a preset threshold, keeping it asserted for at least 25ms after V_{IN} has risen above the reset threshold. The PG_LDO output indicates loss of regulation on either of the two LDO outputs. Other features include overcurrent protection and thermal shutdown for all the three outputs.

The ISL6455 provides an ultra compact DC/DC converter design which uses small ceramic capacitors.

A typical schematic for 3.3V to 2.5V at 600mA and two low noise outputs at 1.8V and 2.5V at 300mA is shown in Figure 3.

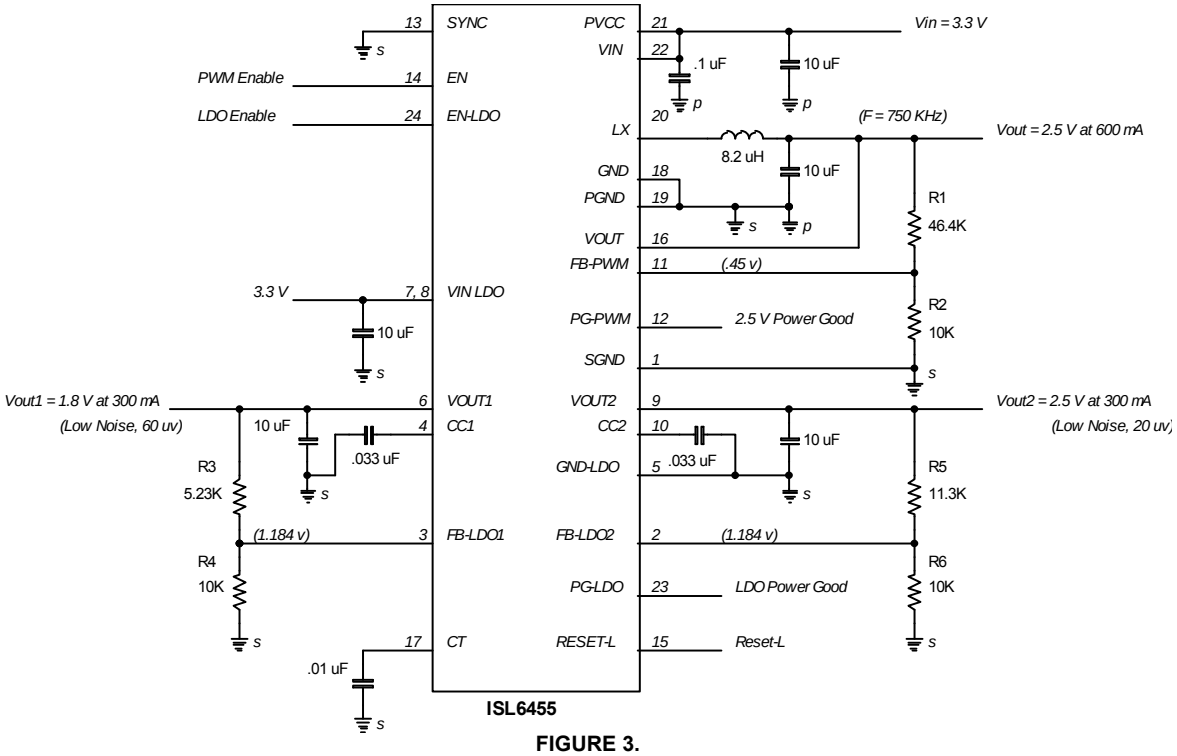
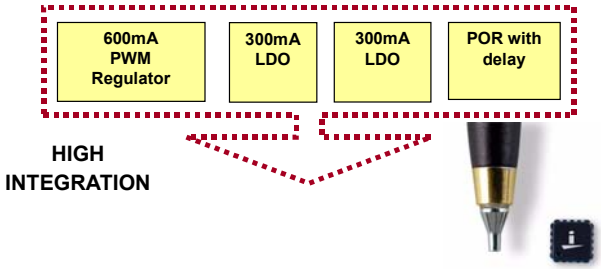


FIGURE 3.



Technical Discussion
ISL8011 (1.2A)

ISL8011 is a high-efficiency 1.2A, 1.5MHz synchronous buck regulator that is ideal for powering low-voltage microprocessors. It is optimized for generating low output voltages down to 0.8V. The supply voltage range is from 2.7V to 5.5V allowing the use of a single Li+ cell, three NiMH cells or a regulated 5V input. It has guaranteed minimum output current of 1.2A. 1.5MHz pulse-width modulation (PWM) switching frequency allows the use of small external components. Internal loop compensation minimizes the number of external components and provides ease of design. A 200ms Reset Timer is provided for system reset applications. An Enable pin provides a low current shutdown to less than 1µA supply current.

Protection features include digital soft-start to limit inrush current, peak current limiting, short circuit protection, over temperature monitoring, and output capacitor discharge in shutdown.

The ISL8011 is packaged in a tiny 8 Ld MSOP package. The high 1.5MHz switching frequency and all ceramic capacitor designs provides an ultra small solution for point of load regulation.

A typical application for the ISL8011 is shown in Figure 4; notice there are only six external components required for this design.

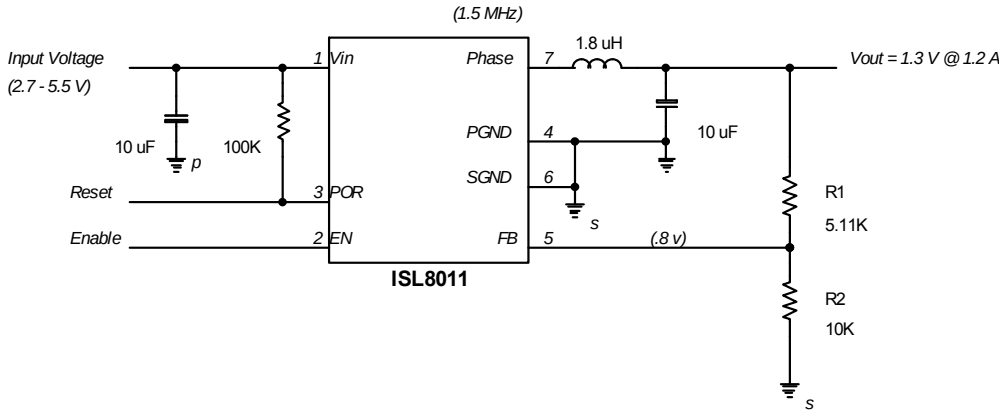


FIGURE 4.

Technical Discussion EL7532 (2A)

The EL7532 is a synchronous, integrated FET 2A step-down regulator voltage mode controller with internal compensation. Efficiency can exceed 94% due to the synchronous rectifier FET. It operates with an input voltage range from 2.5V to 5.5V, which accommodates supplies of 3.3V, 5V, or a single Li-Ion battery source. The output can be externally set from 0.8V to V_{IN} with a resistive divider. The EL7532 features fixed-frequency PWM mode control. The operating frequency is typically 1.5MHz. Additional features include a 100ms Power-On-Reset output, <1µA shut-down current, short-circuit protection, and over-temperature protection.

The EL7532 is available in the 10 Ld MSOP package, making the entire converter occupy less than 0.18in^2 of PCB area with components on one side only as shown in the schematic (Figure 5).

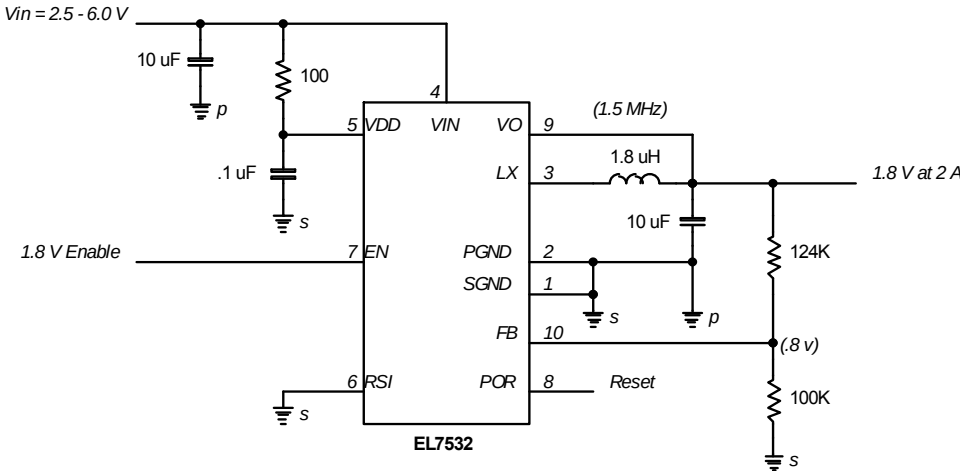


FIGURE 5.

Technical Discussion ISL8013 (3.0A)

ISL8013 is a high-efficiency 3.0A, 1.4MHz synchronous buck regulator that is ideal for powering low-voltage microprocessors. It is optimized for generating low output voltages down to 0.8V. The supply voltage range is from 2.5V to 5.5V allowing the use of a single Li+ cell, three NiMH cells or a regulated 5V input. It has guaranteed continuous output current of 3.0A. 1.4MHz pulse-width modulation (PWM) switching frequency allows the use of small external components. A SYNC pin allows a synchronizing frequency up to 12MHz for improved EMI performance with smaller input and output filters, and multi-phase operation for reduced ripple current and noise. Internal loop compensation minimizes the number of external components and provides ease of design. A Power Good output (PG) monitors the output voltage. An Enable pin provides a low current shutdown to less than 1µA supply current.

Protection features include digital soft-start to limit inrush current, peak current limiting, hiccup mode in overcurrent and over temperature conditions.

The ISL8013 is packaged in a 14 Ld HTSSOP package for high thermal performance. The high switching frequency and all ceramic capacitor designs provides an ultra small solution for point of load regulation.

A typical application schematic for a 3.3V to 1.8V output at 3A is shown in Figure 6. The Ext Sync input is an optional feature synchronizing two ISL8013 devices together or increasing the clock up to 12MHz.

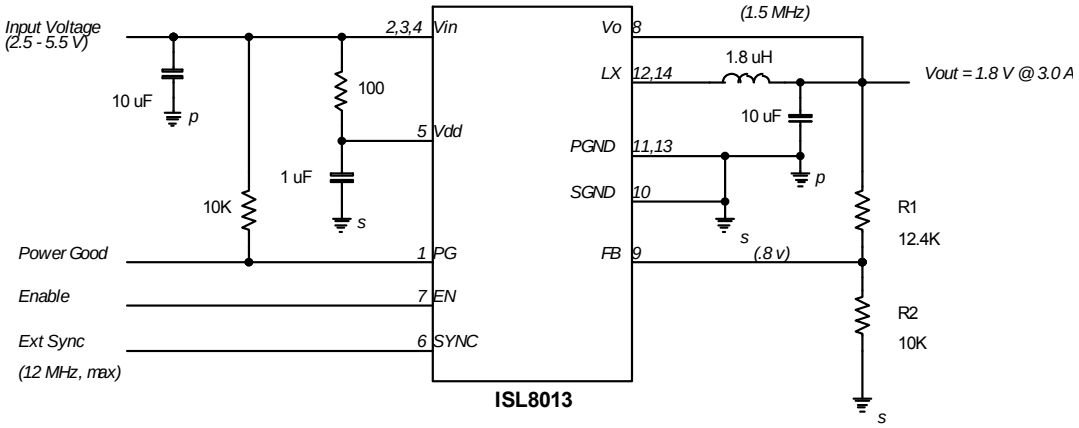


FIGURE 6.

Technical Discussion EL7566 (6A)

The EL7566 is a full-feature synchronous step-down regulator capable of up to 6A and 96% efficiency. The device operates from 3V to 6V input supply (VIN). With internal CMOS power FETs, the device can operate at up to 100% duty ratio, allowing for an output voltage range of 0.8V to nearly VIN. An adjustable switching frequency up to 1MHz enables the use of small components, thereby reducing board area consumption to under 0.72in^2 on one side of a PCB.

The EL7566 operates in constant frequency PWM mode, and includes a SYNC input making external synchronization possible. A soft-start feature is integrated in the EL7566 to limit in-rush currents and allow for a smooth voltage ramp from zero to regulation. Output voltage tracking is integrated to add flexibility for synchronizing many supplies in multiple output voltage configurations. The EL7566 also offers a voltage margining capability that shifts the output voltage ±5% for validation of system card performance and reliability during manufacturing tests. A junction temperature indicator conveniently monitors the silicon die temperature, saving time in thermal characterization. The IC will also automatically shut down if the die temperature exceeds 135°C.

Loop compensation the EL7566 is external so that the output voltage dynamics can be optimized for the application. Since the EL6566 utilizes current mode control, the loop compensation is a simple RC network.

For applications that only require a maximum of 4A output current, the pin compatible EL7554 can be used; the EL7554 has all the same features as the EL7566 described above.

The schematic in Figure 7 shows a typical circuit for a high frequency (550kHz) switching regulator for a 2.5V, 6A microprocessor core voltage derived from a input voltage of 3-6V. By using the STN and STP pins, a start-up ramp of 10ms is achieved; see “Voltage Sequencing and Tracking” for tracking waveforms. Output voltage margining of ±5% is achieved with the TM and SEL pins.

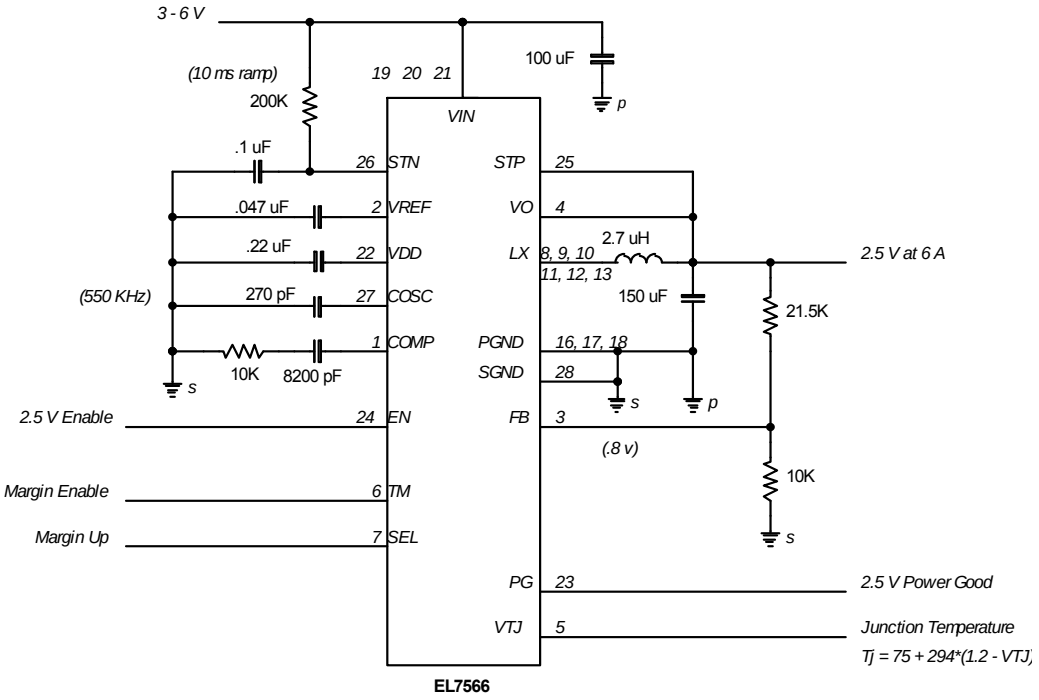


FIGURE 7.

Technical Discussion
ISL65426 (building blocks for dual outputs at up to 6A total)

The ISL65426 is a high-efficiency, dual output monolithic synchronous buck converter employing a constant frequency, current mode architecture. Operating from an input bias ranging from 2.375V to 5.5V, the single chip solution provides two output voltages which are selectable or externally adjustable from 0.8V to 80% of the supply voltage while delivering up to 6A of total output current. Unique to the ISL65426 is the ability to pin program both the output voltage and output current.

The ISL65426 switches at a fixed frequency of 1MHz and utilizes current-mode control with integrated compensation to minimize the size and number of external components and provide excellent transient response. The internal synchronous power switches are optimized for good thermal performance, high efficiency, and eliminate the need for an external Schottky diode.

A unique power block architecture allows partitioning of six blocks to support one of four configuration options. One master power block is associated with each synchronous converter channel. Four floating slave power blocks allow the user to assign them to either channel as shown in Table 3. Proper external configuration of the power blocks is verified internally prior to soft-start initialization.

TABLE 3.

ISET1	ISET2	I_{OUT1} (A)	CHANNEL 1 CONNECTIONS	I_{OUT2} (A)	CHANNEL 2 CONNECTIONS
1	1	3	LX1, LX2, LX3	3	LX4, LX5, LX6
1	0	2	LX1, LX2	4	LX3, LX4, LX5, LX6
0	1	5	LX1, LX2, LX3, LX4, LX5	1	LX5
0	0	4	LX1, LX2, LX3, LX4	2	LX5, LX6

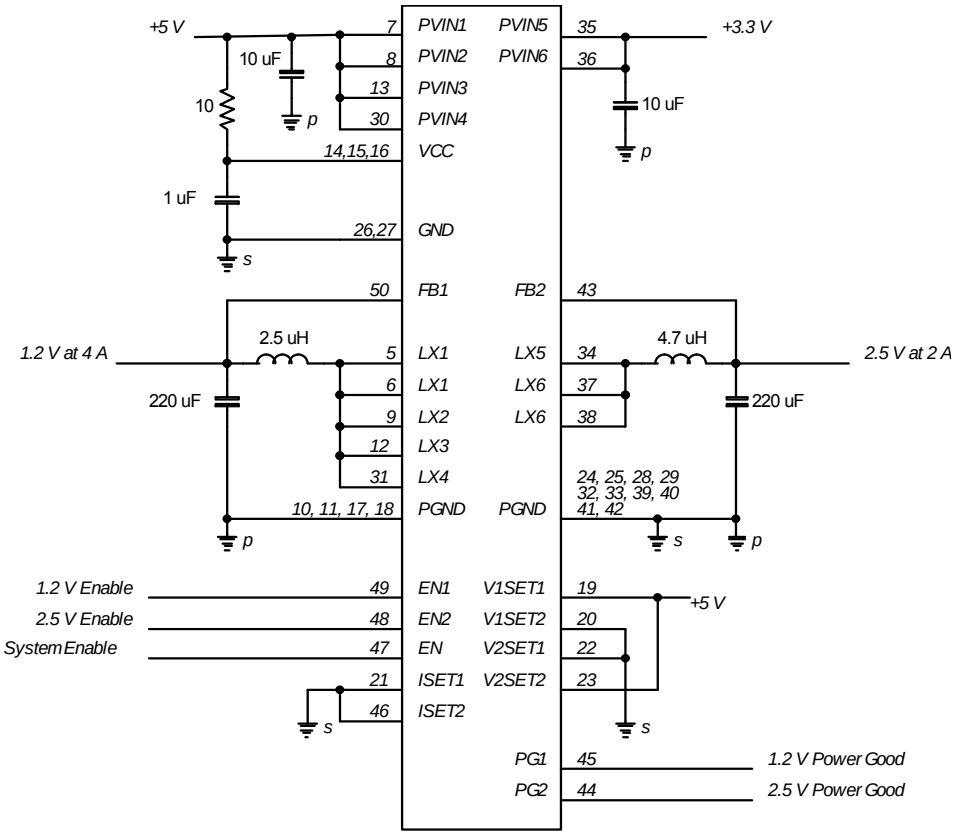
Additionally, the output voltage of each channel can be set with an external resistor network or pin-programmed as shown in Table 4.

TABLE 4.

V_{OUT1}	V1SET1	V1SET2	V_{OUT2}	V2SET1	V2SET2
1.8V	1	1	3.3V	1	1
1.5V	0	1	2.5V	0	1
1.2V	1	0	1.8V	1	0
0.8V or Adj.	0	0	0.8V or Adj.	0	0

Independent enable inputs allow for synchronization or sequencing of the soft-start intervals of the two converter channels. A third enable input allows additional sequencing for multi-input bias supply designs. Individual power good signals (PG1, PG2) indicate the regulation of the respective output voltage. The ISL65426 integrates protection for both synchronous buck regulator channels. If one or both channels encounter a fault condition, both channels are shutdown. The fault conditions include overcurrent, overvoltage, undervoltage, and IC thermal monitor.

The schematic in Figure 8 shows a typical example generating 1.2V at 4A (FPGA core) and 2.5V at 2A (FPGA I/O power) from input voltages of 3.3V and 5.0V.



ISL65426

FIGURE 8.

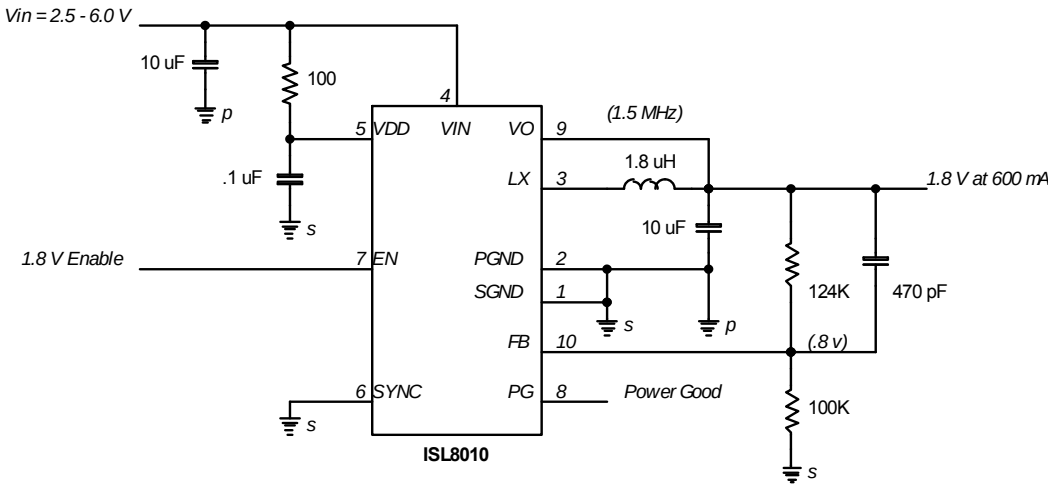
Technical Discussion
ISL8010 (600mA with PWM/PFM Mode)

The ISL8010 is a synchronous, integrated FET 600mA step-down regulator with internal compensation. It operates with an input voltage range from 2.5V to 5.5V, which accommodates supplies of 3.3V, 5V, or a Li-Ion battery source. The output can be externally set from 0.8V to VIN with a resistive divider.

The ISL8010 features automatic PFM/PWM mode control, or PWM mode only. When operating in the PFM mode, the typical no load quiescent current is reduced to only 120µA. The PWM frequency is typically 1.4MHz and can be synchronized up to 12MHz. The operating mode is set by the state of the SYNC pin as shown in the Table below. Additional features include a Power-Good output, <1µA shut-down current, short-circuit protection, and over-temperature protection.

The ISL8010 is available in the 10 Ld MSOP package, making the entire DC/DC converter occupy less than 0.18in^2 of PCB area with components on one side only. The 10 Ld MSOP package is specified for operation over the full -40°C to +85°C temperature range.

The schematic in Figure 9 shows a typical ISL8010 DC/DC converter for 2.5V-6.0V to 1.8V at 600mA with less than 120µA no load quiescent current.



Sync Pin	Operating Mode
High	*Forced PWM Mode*
Low	*Aoto PWM/PFM Mode*
Ext Clk	*Synchorize to External Clock, 12 MHz max*

SYNC Pin Programming

FIGURE 9.

Intersil Integrated FET DC/DC Converters Design Procedure

The Intersil Integrated FET DC/DC Converters product family provides a highly integrated power system, with most devices containing internal loop compensation. Therefore, the component selection process is very simple since most applications use fixed component values.

Inductor Selection

For the parts with internal loop compensation (ISL6410, ISL6455, ISL8011, ISL8013, ISL65426, and EL7532) use the inductor as shown in Table 5.

Once the inductance value is calculated, the inductor ripple current and peak current should be calculated to select the correct inductor. The selected inductor must have a saturation current rating that is greater than I_L(max), and an average current (or RMS current) that is greater than the load current. Often inductor vendors supply different methods for specifying these parameters, so care must be exercised in reading and understanding the inductor data sheet.

The inductor ripple current is: $dI_L = \frac{V_O \bullet (1 - V_O/V_{IN})}{F \bullet L}$

The peak inductor current is: $I_L(max) = I_{OUT} + \frac{1}{2} \bullet dI_L$

TABLE 5.

DEVICE	FREQ.	INDUCTANCE	TYPICAL VENDOR PART NUMBER
ISL6410	750kHz	8.2µH	Coilcraft MSS5131-822MX
ISL6410A	750kHz	12µH	Coilcraft MSS6122-123MX
ISL8010	1.5MHz	1.8µH	Coilcraft 1008PS-182M
ISL6455	750kHz	8.2µH	Coilcraft MSS5131-822MX
ISL8011	1.5MHz	1.8µH	Coilcraft 1008PS-182M
ISL8013	1.4MHz	1.8µH	Coilcraft MSS1260-222NX
EL7532	1.5MHz	1.8µH	Coilcraft 1008PS-182M
ISL65426	1MHz	2.5µH 4.7µH (Note 1)	Coilcraft MSS1260-222NX Coilcraft MSS1260-472MX

NOTE:

1. Since the ISL65426 is a building block part, the inductor value should be based on the switching frequency, output current, input voltage, and output voltage. The inductor shown is for the typical application schematic.

Due to the internal compensation, the inductor values shown should be used for the inductance. Lower phase margin (i.e., decreased stability) will result with lower inductor values. Higher values of inductance could be used; however, they will result in potential instability in the current mode control loop, slower transient response, and potentially larger size.

For the EL7566 with external loop compensation, the procedure outlined in the EL7566 data sheet should be used.

Output Capacitor Selection

The output capacitor must be a low ESR capacitor (<50mΩ is recommended) to minimize output voltage ripple, minimize load step transients, and provide proper loop stability. In addition, the output capacitor must have an RMS current rating that is greater than the inductor RMS current. This can be approximated by:

$I_{CO}(RMS) = 0.3 \bullet dI_L$

Since ceramic capacitors should be used for small size and have very low ESR, the capacitor ripple current rating is almost always satisfied.

The output voltage ripple will be equal to:

$dVo = dI_L \bullet ESR + dI_L/(8 \bullet C_O \bullet F)$.

For example, with the ISL8011 schematic, the output voltage ripple will be 290mA • 3mΩ + 290mA/(8 • 10µF • 1.5MHz) = 0.87mV + 2.4mV = 3.3mV! In reality, due to parasitic effects (PCB trace resistance and inductance, vias, etc.), the output voltage ripple may be slightly higher. However, the effect of a ceramic capacitor's very low ESR and high switching frequency in reducing output voltage ripple is clearly illustrated by this example.

Input Capacitor Selection

Since the input current in a buck converter is swinging between zero and full load current, the input capacitor RMS current rating can be as high as on-half the output load current. An equation to calculate the exact RMS current rating required can be found in the data sheets, but a safe assumption is to choose the input capacitor with an RMS rating of 0.5 • I_{OUT}. The input capacitor should be 10µF minimum; higher capacitor values will result in lower input voltage ripple. Ceramic capacitors are preferred since they have very low ESR, and, therefore, higher RMS ripple current capability.

Setting the Output Voltage

Set the output voltage by using logic levels (ISL6410, ISL65426) as shown in the following tables or external resistors (ISL6455, ISL8010, ISL8011, ISL8013, EL7532, EL7566) as described below. The ISL65426 is unique because its output voltages can be programmed with either logic levels or external resistors.

For the ISL6410 and ISL6410A logic level output voltage programming:

TABLE 6.

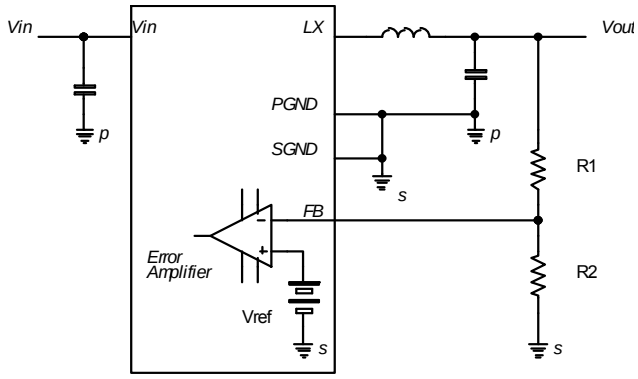
VSET	ISL6410 V_{OUT}	ISL6410A V_{OUT}
1	1.8V	3.3V
Open (n/c)	1.5V	1.8V
0	1.2V	1.2V

For the ISL65426 logic level output voltage programming:

TABLE 7.

V_{OUT1}	V1SET1	V1SET2	V_{OUT2}	V2SET1	V2SET2
1.8V	1	1	3.3V	1	1
1.5V	0	1	2.5V	0	1
1.2V	1	0	1.8V	1	0
0.8V or Adj	0	0	0.8V or Adj.	0	0

To set the output voltage with external resistors, a pair of feedback resistors are used to monitor the output voltage and regulate the output voltage with a fixed voltage reference as shown in Figure 10.



Integrated FET DC/DC Converter

FIGURE 10.

The output voltage is set by the following equation:

$$V_{OUT} = V_{REF} \bullet (1 + R1/R2), \text{ or}$$

$$R1 = R2 \bullet \frac{(V_{OUT} - V_{REF})}{V_{REF}}$$

Usually, R2 is set to a convenient value such as 10kΩ, and R1 is then calculated. Since tight initial output voltage is required, R1 and R2 should be 1% tolerance (or better if required). Often the R1 calculation will yield a non-standard 1% resistor value so the next highest standard 1% value is used in order to raise the output voltage slightly which can compensate for I • R drops on the PCB. If tighter initial tolerance is required than can be achieved with standard 1% values, a high value resistor across R1 could be used to tweak the effective value of R1 to the exact calculated value. Alternately, a new value for R2 could be used and R1 could be recalculated until the minimum output voltage error is achieved.

The value of V_{REF} is different for the various regulators as summarized in Table 8.

TABLE 8.

PART NUMBER	V_{REF}
ISL6455 PWM	0.45V
ISL6455 LDO's	1.184V
ISL8010	0.80V
ISL8011	0.80V
ISL8013	0.80V
EL7532	0.80V
EL7566	0.80V
ISL65426	0.80V

Miscellaneous Control Connections

Connect the control pins as required for the application.

TABLE 9.

PART #	ISL6410	ISL8010	ISL6544	ISL8011	ISL8013	EL7532	EL7566	ISL65426
OUTPUT CURRENT (A)	**0.6**	**0.6**	**0.6, 0.3, 0.3**	**1.2**	**3**	**2**	**6**	**6**
Enable Input	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Sync Input	Yes	Yes	Yes		Yes		Ext ckt	
Power Good Output	Yes	Yes	Yes		Yes		Yes	Yes
Power on Reset Output	Yes		Yes	Yes		Yes		
Power on Reset Timer	Yes		Yes					
Temperature Indicator							Yes	
Tracking							Yes	
Margining							Yes	

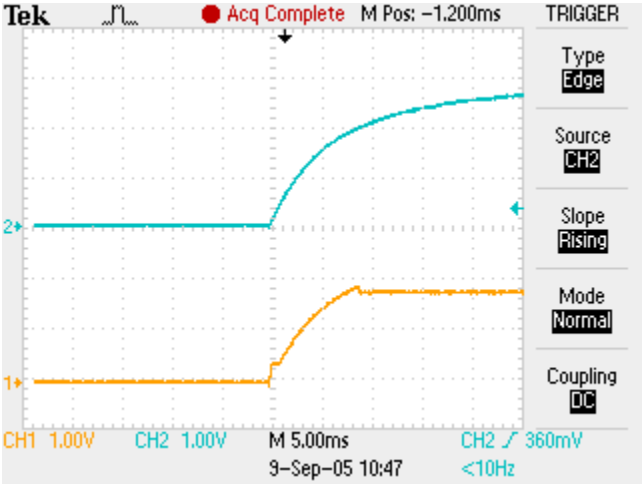
Voltage Sequencing and Tracking

Many of today's microprocessors, gate arrays, and other logic devices require multiple supply voltages for their core and I/O voltages. To eliminate latch-up conditions internal to the logic devices, the power supply voltages may need to be turned on and off in a particular sequence. Sequencing the power supply voltages can be accomplished by using the Enable pins of the Intersil Integrated FET DC/DC Converters products and the Intersil Voltage Sequencing Controllers such as the ISL61xx product family.

However, often there is also a voltage tracking requirement for the microprocessors, gate arrays, and other logic devices. For example, "the differential voltage between the 2.5V core voltage and 3.3V I/O voltage must be less than 0.7V under all conditions". A tracking requirement like this can not be satisfied by sequencing the 3.3V and 2.5V power supplies because it will violate the 0.7V maximum voltage differential specification.

Therefore, it is often prudent to track all the output voltages in a system to a common ramp so they all track together in turn on and turn off. The EL7566 and EL7554 have the ability for voltage tracking via the STN and STP pins so it is an easy task to provide voltage tracking. In the circuit (Figure 12), the Track Ramp is generated with R1 and C1, which is connected to the STN pin.

The waveform in Figure 11 shows the relationship between the Track Ramp (STN pin) and the output voltage.



TOP TRACE - TRACK RAMP (STN PIN)
BOTTOM TRACE - OUTPUT VOLTAGE

FIGURE 11.

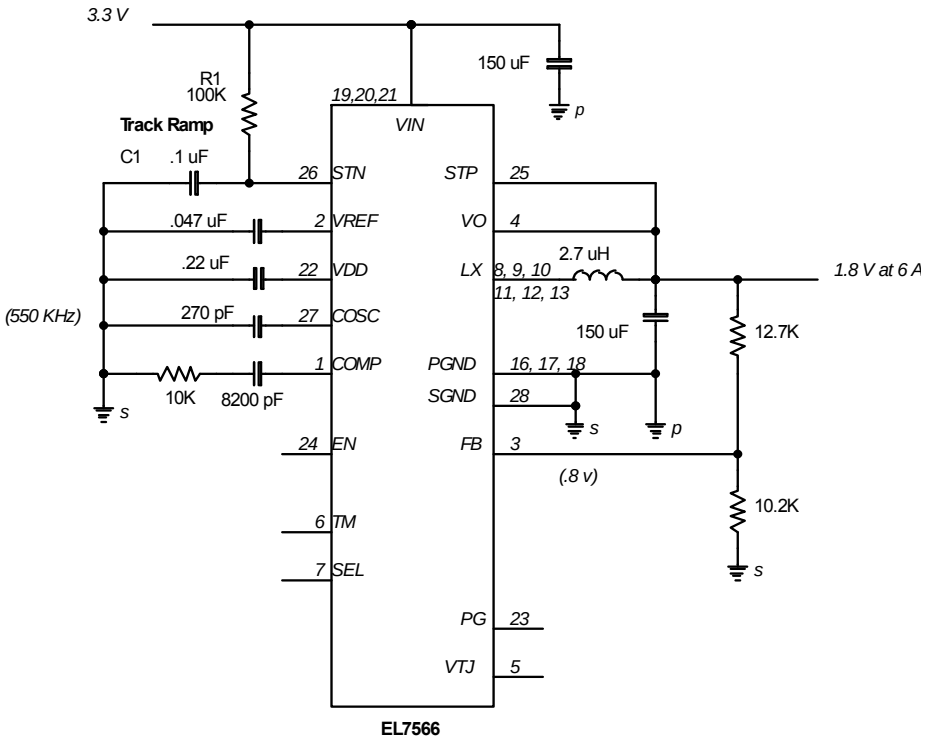


FIGURE 12.

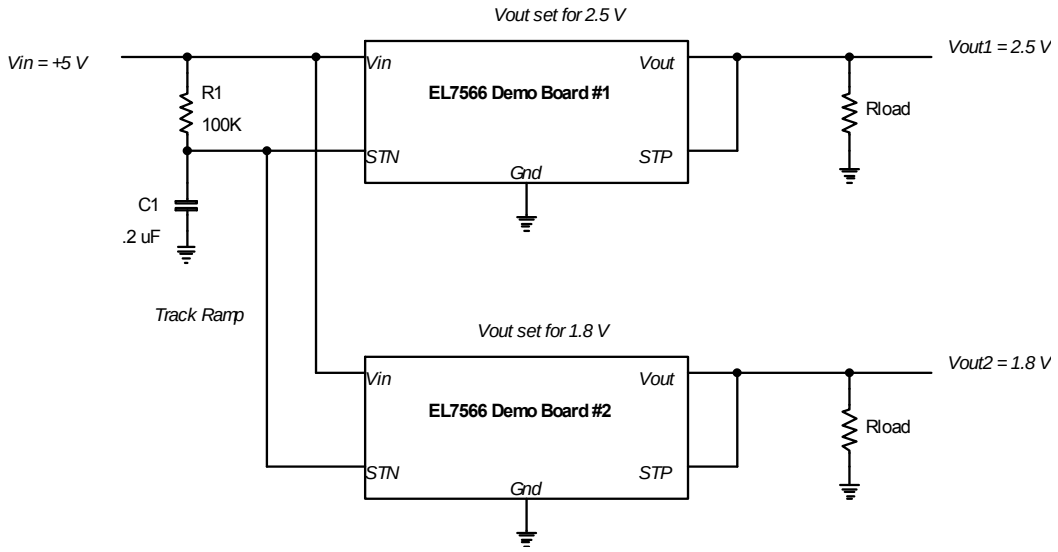
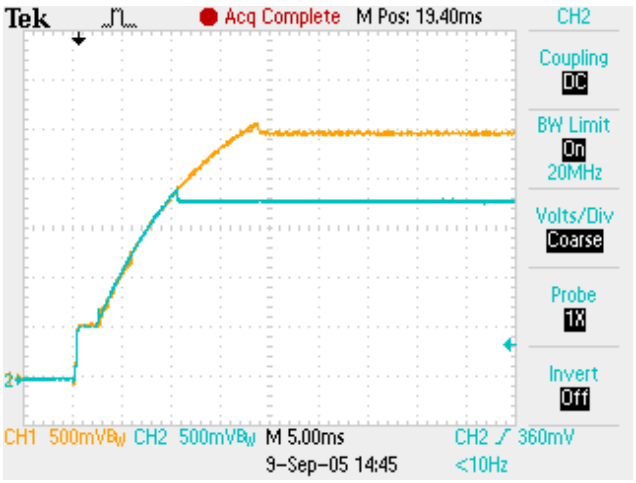


FIGURE 13.

To illustrate the tracking capability of two output voltages, two EL7566 Eval Boards were connected together as shown in Figure 13, and the following output voltage tracking waveform (Figure 14) was measured.



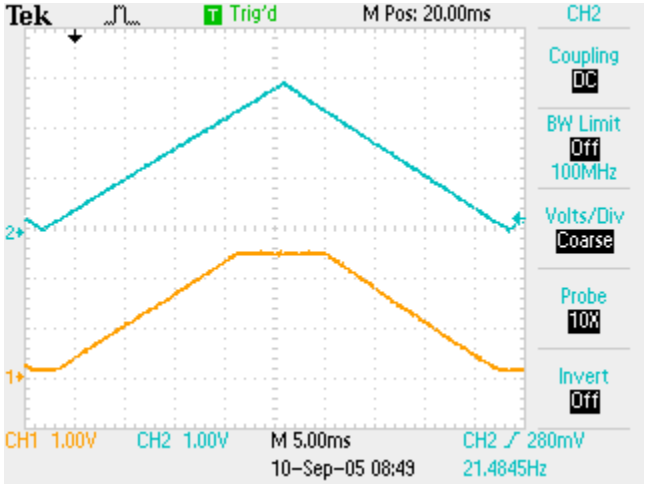
TOP TRACE - V_{OUT1}, 2.5V
BOTTOM TRACE - V_{OUT2}, 1.8V

FIGURE 14.

Other devices without the tracking functions can be used with the circuit shown in Figure 17 to provide the voltage tracking. It must be noted that this will only work with Intersil Integrated FET DC/DC Converters that use external resistors to set the output voltage since you must have access to the feedback resistors.

The V_{REF} voltage can be shared with other DC/DC converter ramp circuits in a multi-output voltage system. If there are other DC/DC converters in the same system with a different internal reference voltage (i.e., 0.60V, 1.25V, etc.) or if offset tracking is required, the resistor ratios (R1:R3, and R2:R4) can be adjusted to ensure the desired tracking.

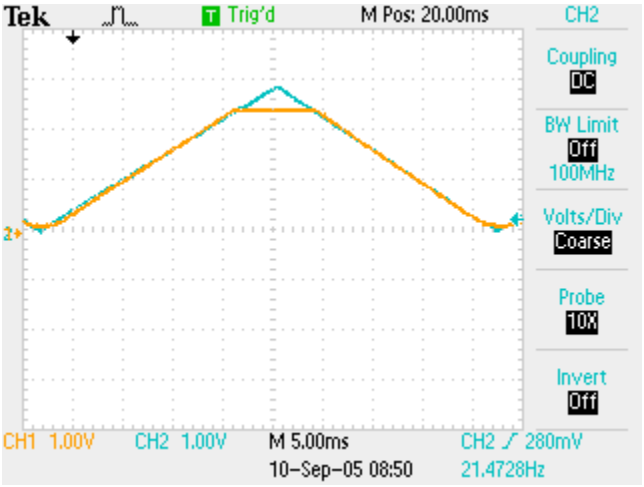
The output voltage waveform in Figure 15 uses a triangular wave as the Track Ramp; notice the output voltage tracking occurs on both the turn on ramp and the turn off ramp.



TOP TRACE - TRACK RAMP
BOTTOM TRACE - OUTPUT VOLTAGE

FIGURE 15.

By superimposing the Track Ramp and the Output Voltage, the waveform in Figure 16 illustrates the tracking accuracy.



TOP TRACE - TRACK RAMP
BOTTOM TRACE - OUTPUT VOLTAGE

FIGURE 16.

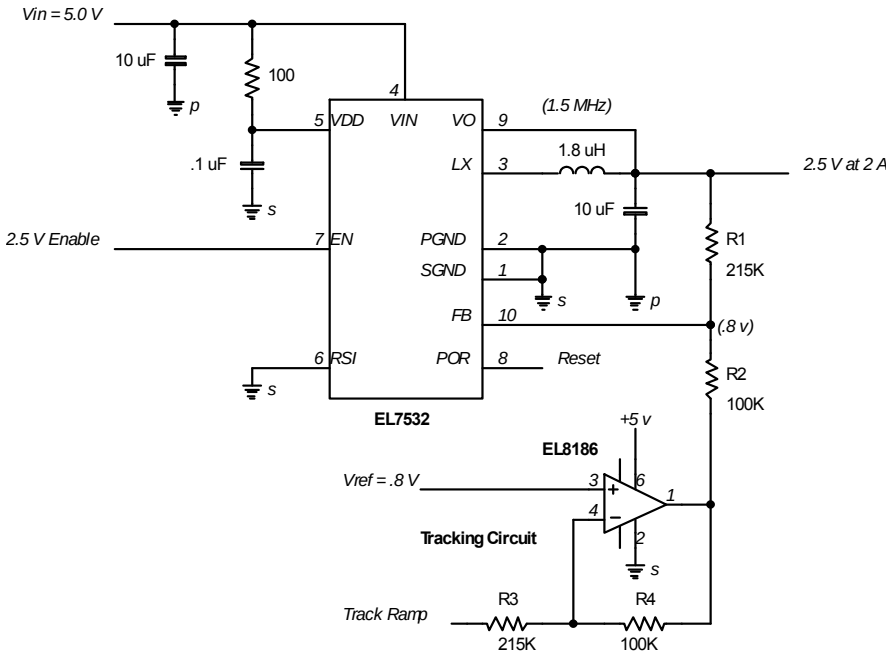


FIGURE 17.

A complete analysis of the EL8186 op amp tracking circuit is available on request.

PCB Design/Layout Considerations

The PCB layout must be considered an active component in any switching regulator design due to concerns with stability, low noise, and thermal management. Disaster will result if the PCB layout is left to the hands of a PCB designer who uses automatic placement and auto-routing software. There is no way around it - the hardware design engineer must be involved in all aspects of the PCB layout.

Most of the Intersil Integrated FET DC/DC Converters products have data sheets and Evaluation Boards which show a proven PCB layout. Use them if possible!

The PCB layout starts with a well drawn schematic. A schematic tells a story; it is more than just a way to generate a Net List for the PCB. The schematic should show ground systems, Kelvin connections, proper component placement, and all the components must be shown locally to the DC/DC converter circuit. Critical bypass capacitors should not be shown 10 pages from the controller chip!

First, a two ground system must be established. A Power Ground (PGND) should connect all the high frequency and high current paths. The PGND must be a plane or copper flood area. A Signal Ground (SGND) should connect all the low current signal interconnections. A plane or copper flood area can be used but is not required for the SGND connections. The PGND and SGND must be connected together at only one point - usually at the controller chip PGND pin. Often, a 0Ω resistor will be used to create a separate SGND Net List and force a single point connection to PGND.

Second, all the power components (Controller chip, inductor, output capacitor, and input capacitor) should be placed on the same side of the PCB to eliminate the need for interconnections with vias that are both resistive and inductive. The input voltage, output voltage, and ground can be stitched to inner layers with multiple vias after the DC/DC conversion process has taken place. The idea is to eliminate high frequency switching currents from flowing through vias, if possible.

Third, the ground side of the input capacitor, PGND pin, and output capacitor should be as close together as possible to avoid switching noise generated by discontinuous current flow.

Fourth, all the “sensitive” nodes should be as short as possible. Critical components must be located as close to the controller chip as possible; these include feedback resistors, decoupling capacitors, and loop compensation components. Fortunately, the use of a highly integrated controller minimizes the number of external components.

Fifth, it must be recognized that the PCB is the thermal management system (heatsink) and the proper amount of copper etch must be placed around the controller chip to dissipate the heat that is generated. Thermal management is discussed on many of the Intersil Integrated FET DC/DC Converters product data sheets; in addition, there are two very good Applications Notes.

- AN1096, “Thermal Design Considerations - EL75XX”
- TB379, “Thermal Characterization of Packaged Semiconductor Devices”

Proper Scope Probe Grounding Techniques

Essential to the design and evaluation process is the ability to properly measure the output noise and load transient response. These are difficult to measure because they are low level signals in the presence of high common mode voltage, high frequency switching currents, and large electromagnetic fields. Simply clipping a scope probe onto a measurement point and the use of a 4” ground lead will not suffice as shown in the output voltage waveform (Figure 18), taken from the EL7566 Eval Board.

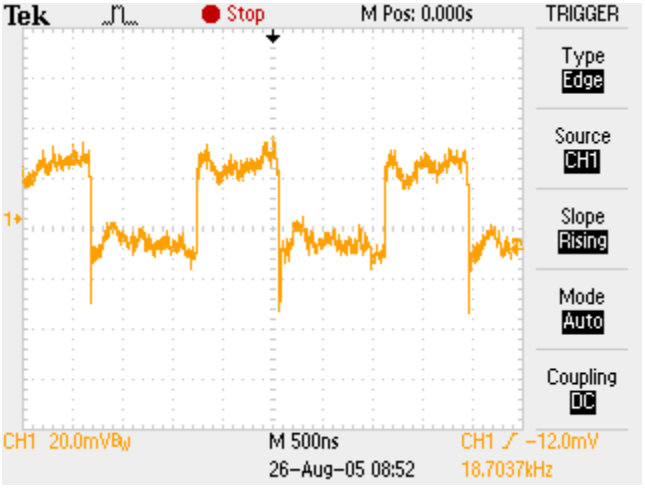


FIGURE 18. POOR V_{OUT} RIPPLE MEASUREMENT

In order to make this measurement for output voltage ripple and noise, the ground lead of the probe must not be used; instead, the ground collar on the probe must make direct contact to the output ground measurement point. It may be necessary to take the probe apart to gain access to the ground collar. A probe clip should not be used to make the connection to the measurement point; instead, the tip of the probe must be connected directly to the measurement point. Often there are accessories with the probe to make these direct measurements easier. The waveform in Figure 19 is the same circuit and test conditions as the waveform above, but the probe is connected properly.

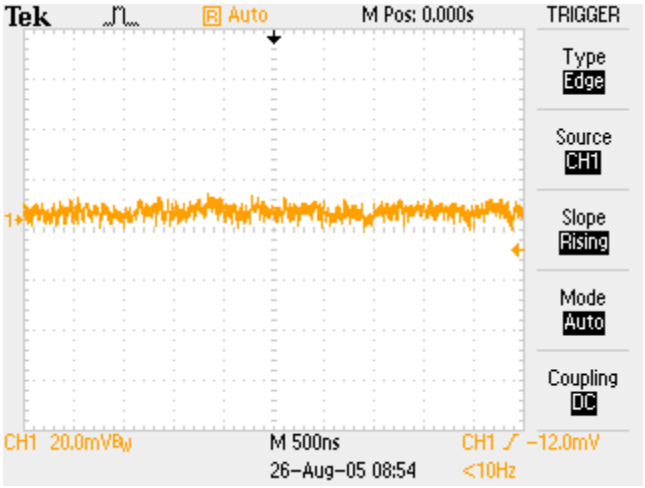


FIGURE 19. PROPER V_{OUT} RIPPLE MEASUREMENT

Power Calculations and Efficiency Estimation

This section will describe an empirical approach to estimate the power dissipation of main components that determine the overall efficiency of the converter and the temperature rise of the controller chip.

The major contributors to power dissipation are listed in Table 10, with equations to approximate the power:

TABLE 10.

Input capacitor ESR power loss	P1 = $(I_{OUT}/2)^2$ • ESR
Top side FET ON resistance power loss, (where DC = Duty cycle = V_{OUT}/V_{IN})	P2 = I_{OUT}^2 • Ron • DC
Top side FET transition power loss, (where Ts = rise and fall time on the LX pin)	P3 = V_{IN} • I_{OUT} • Ts • F
Bottom side FET ON resistance power loss	P4 = I_{OUT}^2 • Ron • (1- DC)
Inductor DCR and AC power loss, (assumes DC losses = AC losses)	P5 = 2 • I_{OUT}^2 • DCR

Total controller chip power dissipation = P1+P2+P3+P4+P5.

As an example, consider the Evaluation Board for the EL7566 for:

TABLE 11.

V_{IN}	+5V	C_{IN} ESR	0.018Ω
V_{OUT}	+1.8V	Top FET RON	0.03Ω
I_{OUT}	4.7A	Bottom FET RON	0.025Ω
DC	36%	Inductor DCR	0.012Ω
Switching Frequency	525kHz		
Rise, Fall Time	10ns (measured)		
Input Current	1.93A (measured)		

1. P1 = $(4.7/2)^2$ • 0.018 = 0.10W
2. P2 = $(4.7)^2$ • 0.03 • 0.36 = 0.24W
3. P3 = 5 • 4.7 • 10ns • 525kHz = 0.12W
4. P4 = $(4.7)^2$ • 0.025 • (1 - 0.36) = 0.35W
5. P5 = 2 • $(4.7)^2$ • (0.012) = 0.53W

   Total Power loss = 1.34W

Calculated Efficiency = output power/(output power + total power loss)
= 1.8V • 4.7A /(1.8V • 4.7A + 1.34W)
= 86.3%

Measured Efficiency = 1.8V • 4.7A/(5.0 • 1.93A)
= 87%

The EL7566 power dissipation, P2 + P3 + P4 = 0.71W. The temperature rise of the EL7566 can be estimated by using θ_{JA} = 30°C/W from the data sheet curve. The temperature rise will be 0.71W • 30°C/W = 21.3°C; the EL7566 case temperature was measured at 53°C at an ambient temperature of 28°C for a measured temperature rise of 25°C. The estimated temperature rise is a good approximation for reality.

As shown, by simple measurements of LX pin rise time and fall time, it is possible to estimate the power dissipation of circuit components, temperature rise of the controller chip, and overall efficiency.

Loop Compensation Evaluation with Load Step Test

Even though most of the Intersil Integrated FET DC/DC Converters products have internal loop compensation, it is prudent to evaluate the overall loop stability with the actual input circuitry, PCB layout and load. The classic approach to check loop stability is to measure the system transfer function by breaking the feedback loop, inserting a test signal into the network, and measuring the gain and phase of the overall system transfer system. Bode plots are generated to graphically show the phase and gain characteristics and measure the phase margin. This process has been automated with computerized network analyzers, but the process is still difficult at best. As a result, it is usually ignored in the design evaluation process and rarely understood by all but the serious analog guru.

A much simpler approach to evaluating loop stability uses a load step to inject a stimulus into the overall closed loop system, and then the transient response is measured for excessive ringing (potential instability) or slow response (over compensated). This approach is valid because there is a direct transformation from the H(s) frequency domain to the h(t) time domain via the Laplace Transform. Fortunately, it is not necessary to evaluate a Laplace Transform to evaluate loop stability!

The easiest method to test load transient response uses an Electronic Load. But if you do not have access to this piece of equipment, a simple circuit (Figure 20) can be used to inject a load step into the output of a DC/DC converter (or any power

supply), and an oscilloscope measures the resultant transient response.

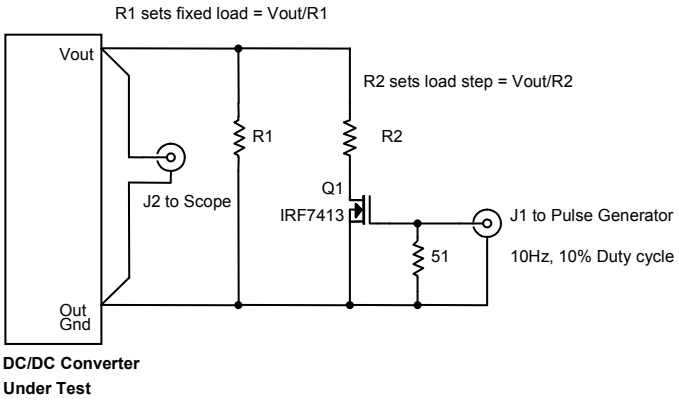
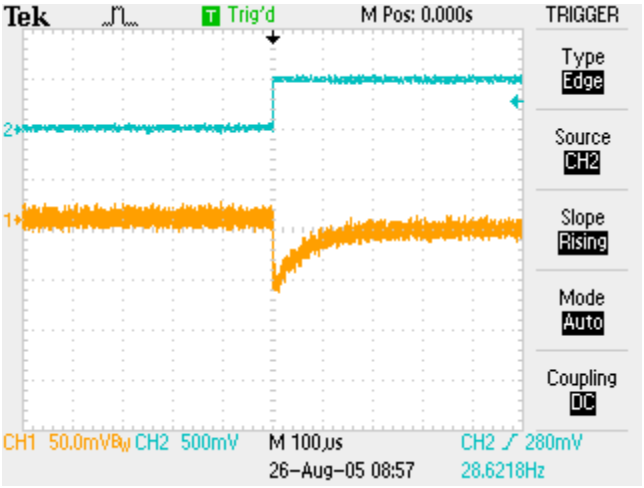


FIGURE 20.

In this circuit, R1 sets a fixed base level load current = V_{OUT}/R1 and R2 sets the load step amplitude = V_{OUT}/R2.

As an example of this technique, the EL7566 Evaluation Board was tested with the load step circuit as shown above; R1 = 1Ω for a fixed load current of 1.8A, and R2 = 0.62Ω for a load step of 2.9A. Therefore, for these tests the load was stepped from 1.8A to 4.7A in less than 250ns (the pulse generator slew rate controls the load di/dt). The loop compensation components (R0, C0) were adjusted to show various conditions of stability.

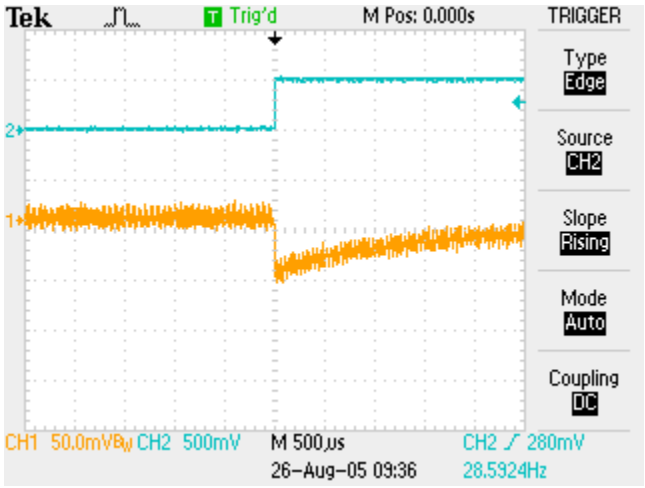
The scope waveform in Figure 21 shows stable loop compensation; there is a sag in the output voltage when the load step is applied and the recovery is fast with no overshoot or ringing.



TOP TRACE - LOAD STEP
BOTTOM TRACE - OUTPUT VOLTAGE
R0 = 7.68k C0 = 8200pF

FIGURE 21.

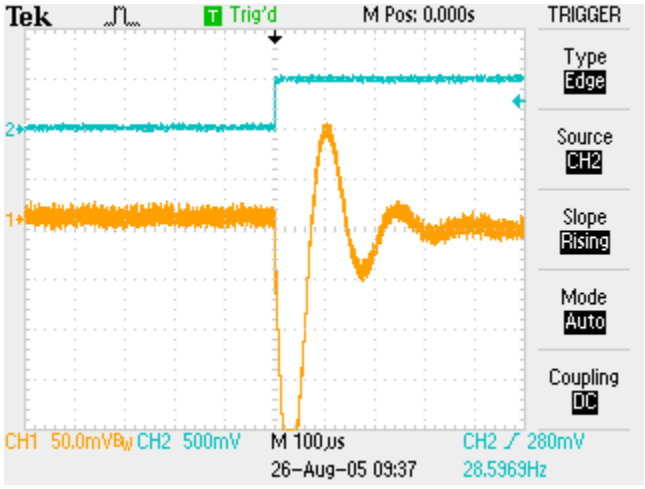
When the control loop is over-compensated, the loop is stable, but the recovery time is much longer as shown in Figure 22; note the time base change to 500µs/div.



TOP TRACE - LOAD STEP
BOTTOM TRACE - OUTPUT VOLTAGE
R0 = 7.68k C0 = 0.1µF

FIGURE 22.

If the control loop is under-compensated, the control loop exhibits a tendency to ring which indicates the approach of an unstable condition as shown in Figure 23.



TOP TRACE - LOAD STEP
BOTTOM TRACE - OUTPUT VOLTAGE
R0 = 7.68k C0 = 8200pF

FIGURE 23.

As an example of using this technique in evaluating a DC/DC converter circuit, the EL7532 Evaluation Board was tested with the load step test circuit (Figure 24).

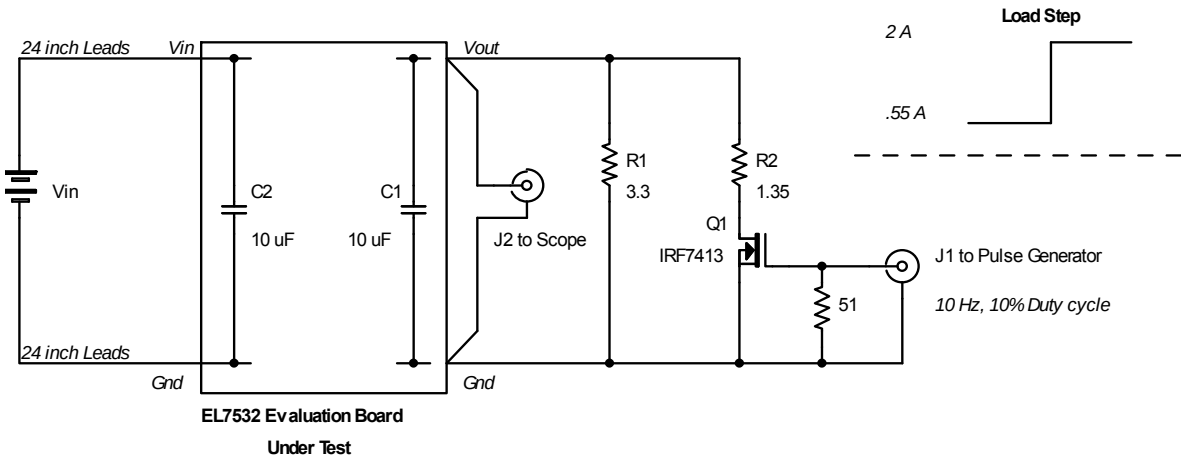


FIGURE 24.

The scope waveform in Figure 25 shows the load transient response with V_{IN} = 5.0V.

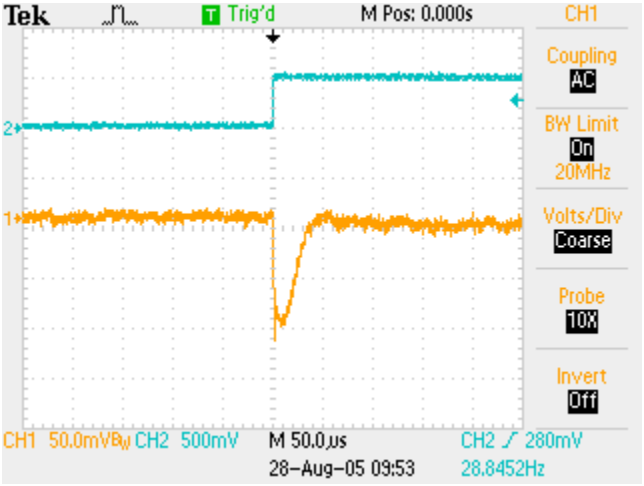
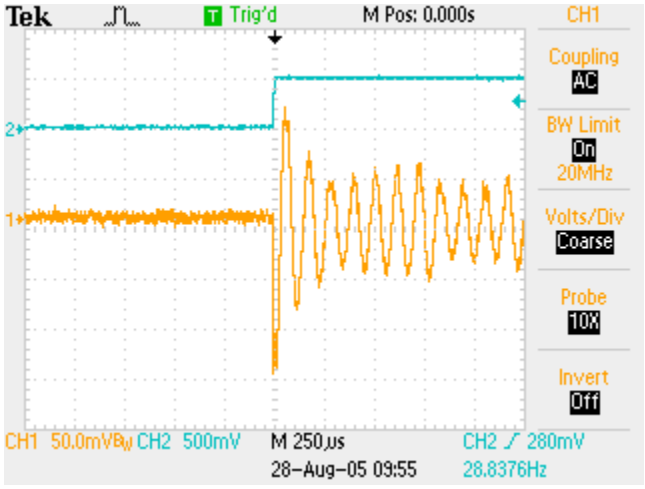


FIGURE 25.

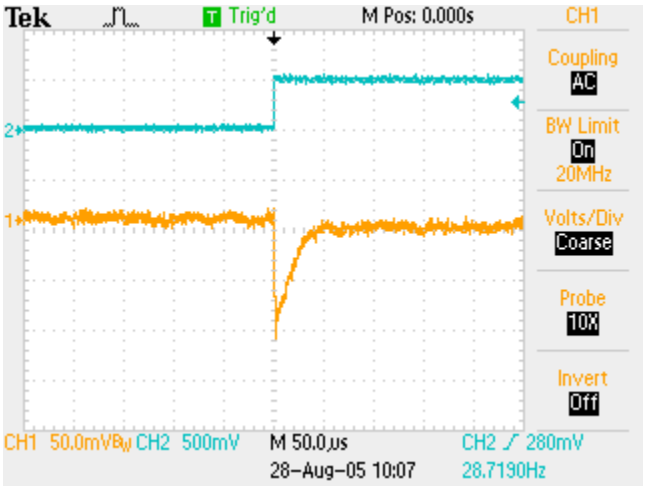
However, when the input voltage, V_{IN} was decreased from 5.0V to 3.3V, the load transient response showed increasing peaking, and broke into an oscillatory response as shown in the following scope waveform (Figure 26) with V_{IN} = 3.3 V.



TOP TRACE - LOAD STEP
BOTTOM TRACE - OUTPUT VOLTAGE

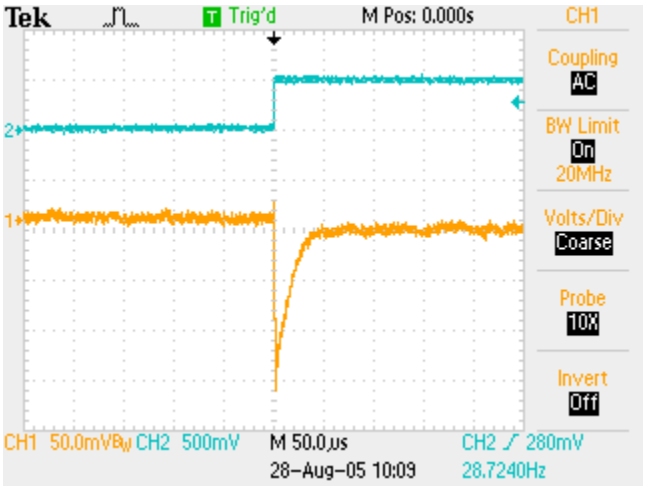
FIGURE 26.

Obviously this is not an acceptable situation! Since there was 48" of lead length between the input power supply and the Evaluation Board, a 1000µF capacitor was added across the V_{IN} and Gnd terminals of the Evaluation Board to stabilize the input supply. Instantly the oscillatory response went away, and the following stable load step response was recorded with the input voltage adjusted from 3.3V to 5.0V as shown in Figures 27 and 28.



TOP TRACE - LOAD STEP
BOTTOM TRACE - OUTPUT VOLTAGE

FIGURE 27. V_{IN} = 5.0V

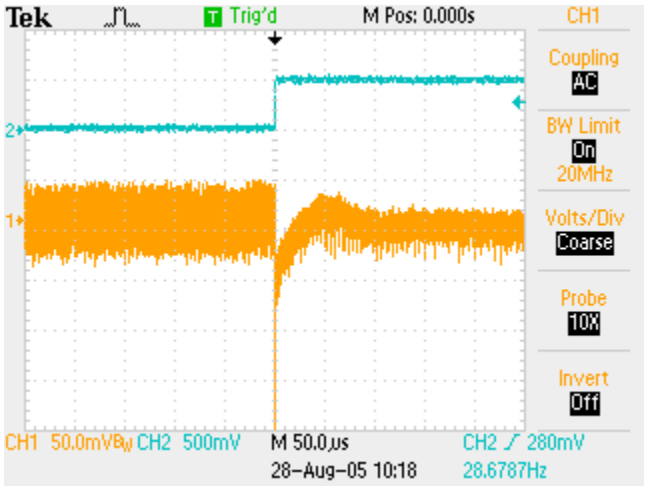


TOP TRACE - LOAD STEP
BOTTOM TRACE - OUTPUT VOLTAGE

FIGURE 28. V_{IN} = 3.3V

This simple load transient tests show the importance of input filter parameters on the stability of a switching regulator, as discussed in Appendix B.

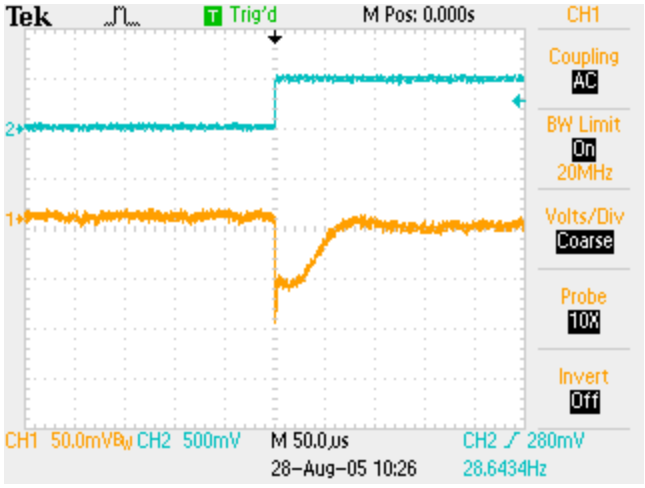
To further evaluate the stability of the EL7532 Evaluation Board, a 100µF output capacitor (POS-CAP #6TPE100M) was used instead of the 10µF ceramic capacitor (C1) on the Evaluation Board. The Figure 29 waveform was recorded; notice the increased output ripple as a result of the increased ESR of the output capacitor. The load transient response shows a slight overshoot, but there is no ringing or tendency to oscillate so this is a stable response. Notice that two parameters have been measured with this test - output ripple and stability!



TOP TRACE - LOAD STEP
BOTTOM TRACE - OUTPUT VOLTAGE

FIGURE 29. V_{IN} = 3.3V

To decrease the output voltage ripple, C1 was added back with the 100µF output capacitor still in place; the following load transient response was recorded (Figure 30). Notice the output ripple has decreased dramatically due to the low ESR of the ceramic output capacitor (C1), the load transient response is stable, and the voltage sag is three times less due to the additional bulk capacitance.



TOP TRACE - LOAD STEP
BOTTOM TRACE - OUTPUT VOLTAGE

FIGURE 30. V_{IN} = 3.3V

Design Software Available; i-Sim

i-Sim PE is the Personal Edition of the Intersil's i-Sim product simulation tool. This is available as a free download from Intersil that you can install and run on your Windows based PC. Design software capabilities include:

- An applications-based Intersil Power Management Product Selector with dynamic input fields to match your input and output requirements. A reference schematic will be generated based on your selections.
- A Schematic Editor which allows complete customization of your application schematic and provides a Bill of Materials for the design. The schematic can be downloaded for a fully back-annotated version of any on-line schematics that you have created.
- A Parts Library for common circuit elements for placement and modification to capture your exact circuit and parasitic elements. You also have the ability to create your own library of parts using existing templates. At the time of this writing, there are over 80 Intersil parts that are part of the library; more are being added on a regular bases.
- A Simulation Tool with the capabilities for DC, AC, and load-step transient analysis. Post simulation analysis allows probe placement and mathematical operations on node voltages and currents.

Typical Applications Circuits

miniPCI or CardBus WLAN Power Supply for 3.3V to 1.2V, 2.5V, and 2.8V

Input Voltage: 3.3V ±10%

Output Voltage: 1.2V at 600mA or 1.8V at 600mA (R1 = 30k)
2.5V at 300mA
2.8V at 150mA

Enables: 1.2V shutdown
2.5V and 2.8V shutdown

Power Good: 1.2V power good
2.5V and 2.8V power good

Reset Output: 3.3V input monitor and Reset

Due to the use of a switching regulator for the 1.2V output, the overall efficiency for this circuit is 84%. If an all LDO circuit is used, the efficiency drops to 54.5%.

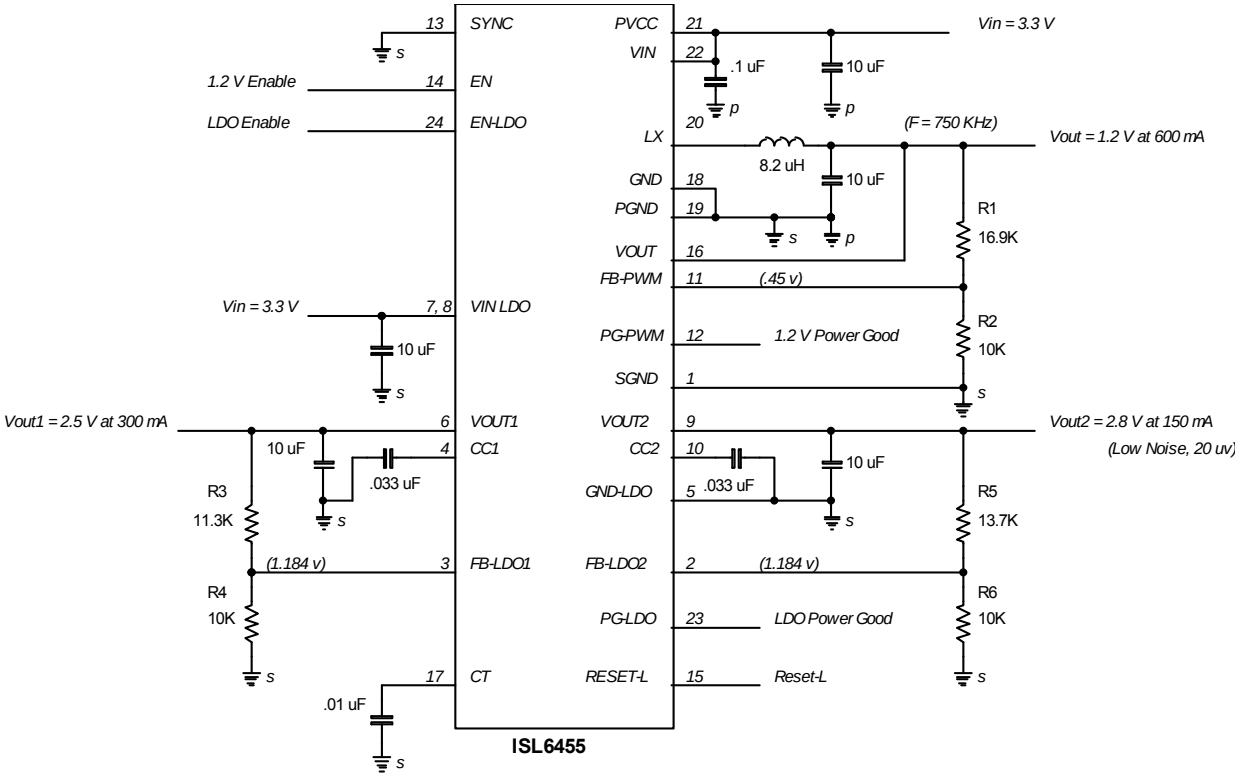


FIGURE 31. miniPCI OR CardBus WLAN POWER SUPPLY

Ultra Small Size Processor Power Supply with Output Voltage Tracking for 3.3V to 1.8V and 2.5V

Input Voltage: 3.3V ±10%

Output Voltage: 2.5V at 1.5A

1.8V at 1.0A

Tracking: 1.8V and 2.5V outputs track each other 200ms after power-up

Reset Output: System RESET-L 200ms after 1.8V and 2.5V outputs regulated

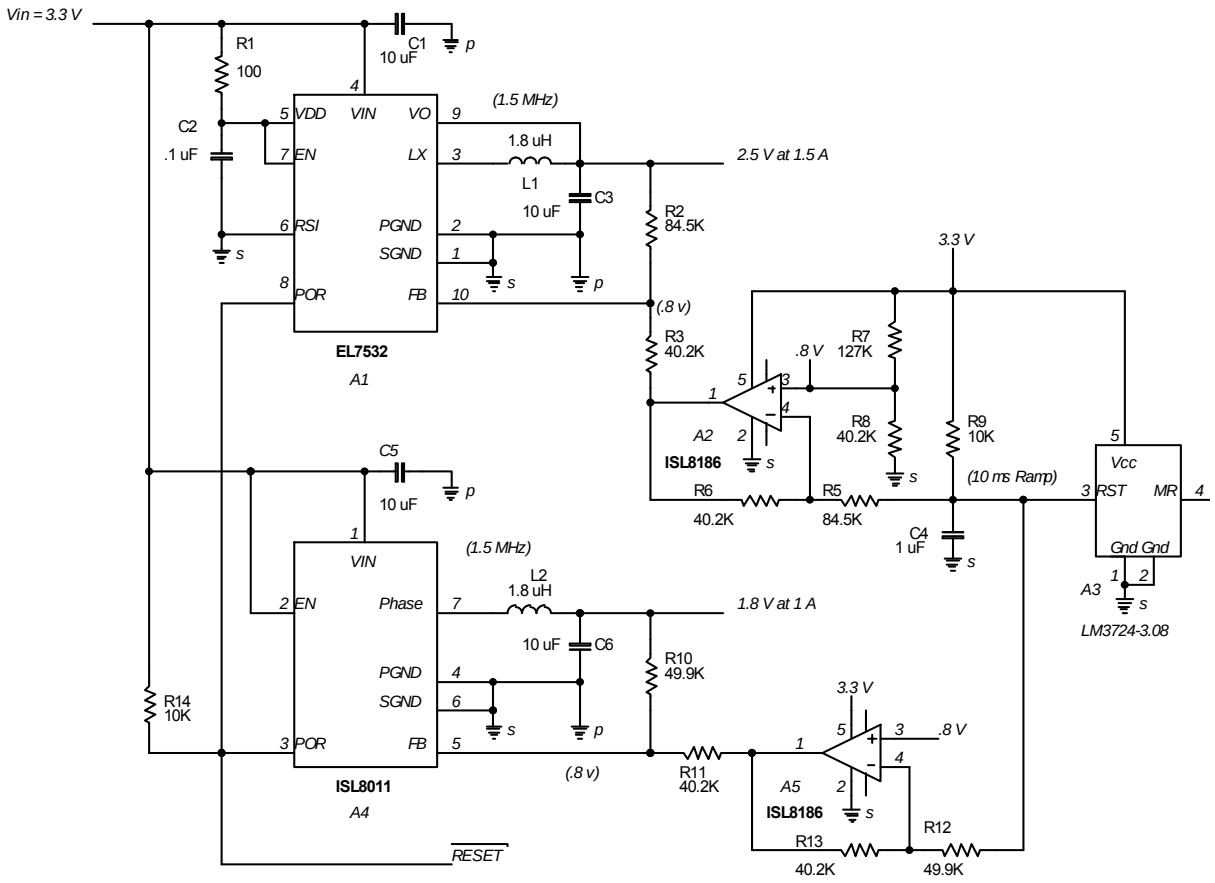


FIGURE 32.

ADSL Modem for +5V to 1.8V, 2.5V, Ultra Low Noise 2.5V, and Low Noise 3.3V

Input Voltage: 5.0V ±10%

Output Voltage: 1.8V at 2A

2.5V at 600mA (Core)

2.5V at 150mA with ultra low noise output

3.3V at 200mA with low noise output

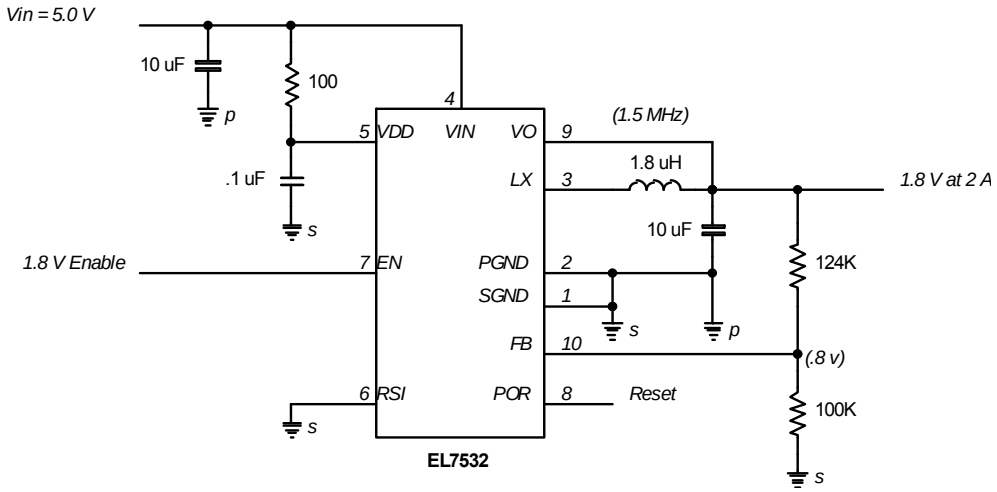


FIGURE 33.

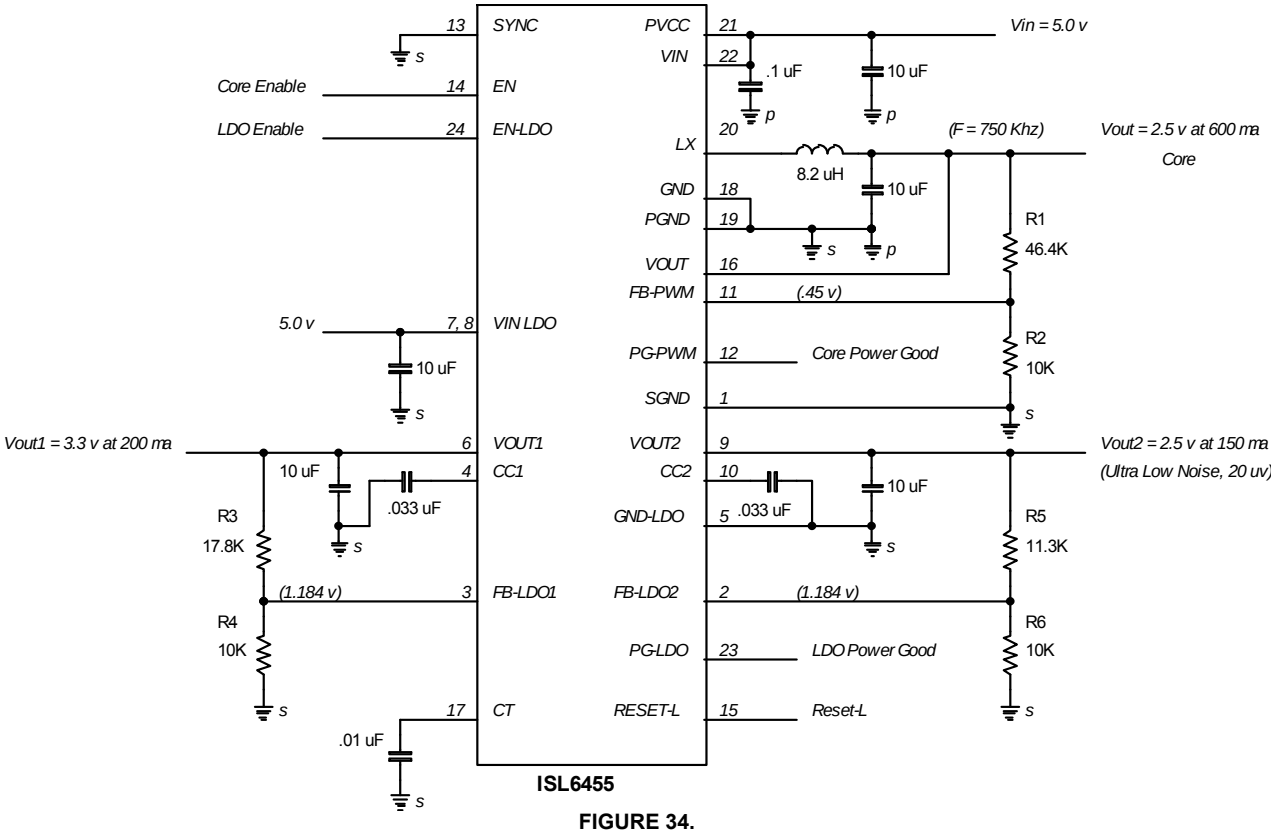


FIGURE 34.

USB Wireless LAN (WLAN) Power Supply for +5V to 3.3V, 1.8V, and 2.84V

Input Voltage: 5.0V ±10%, 500mA maximum input current

Output Voltage: 3.30V at 80mA

1.80V at 330mA (MAC)

2.84V at 120mA (ZIF)

2.84V at 100mA (Memory)

By using the ISL6413 SYNC pin, the switching frequency is synchronized for 1.5MHz (ISL8010) and 750kHz (ISL6413). The estimated input current from the 5.0V (USB) is less than 350mA. The soft-start feature of the ISL8010 ensures less than 500mA input current on start-up.

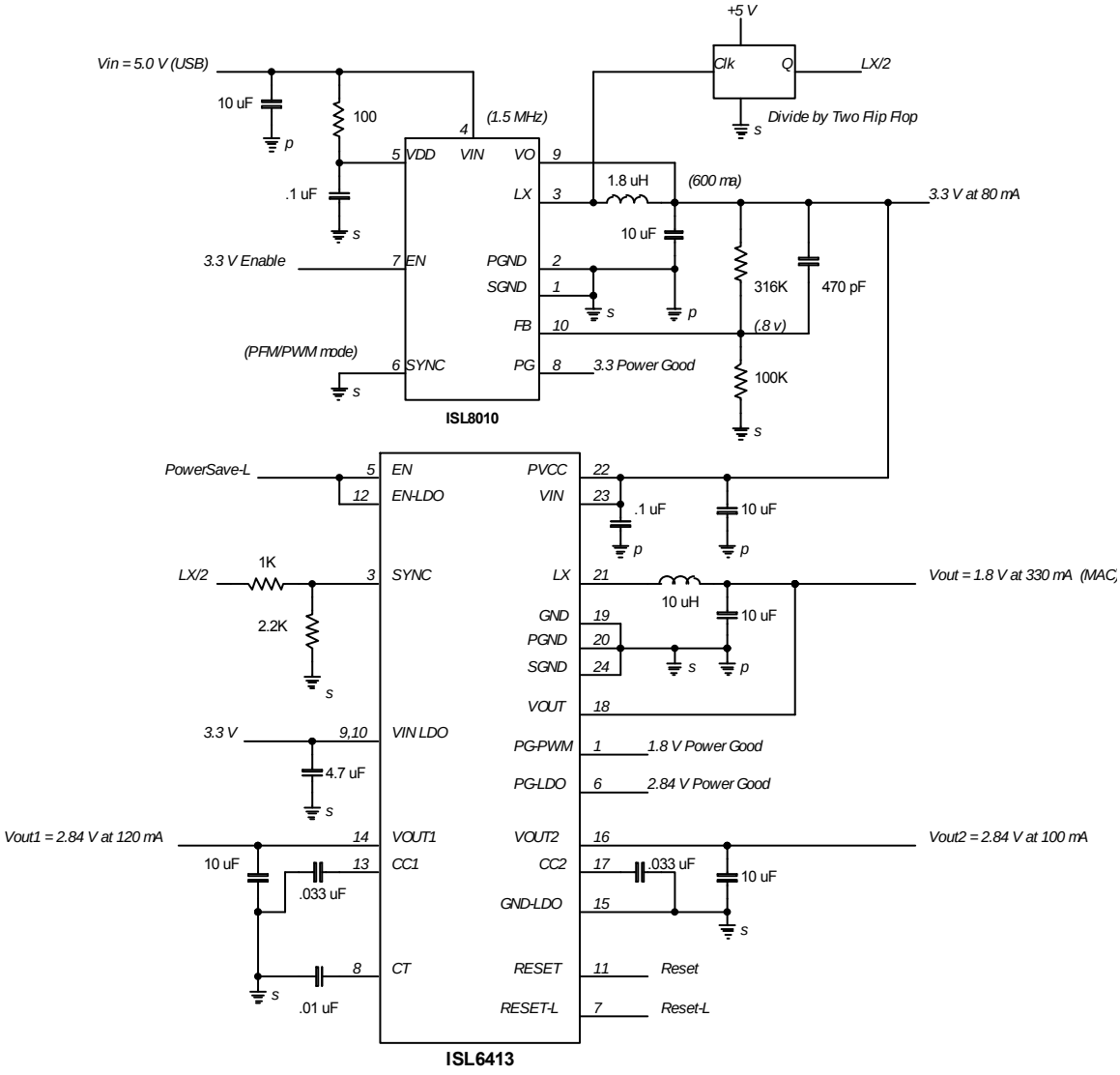


FIGURE 35.

Programming Soft-Start

Designing for minimum size with a high level of integration does have its drawbacks. Flexibility can suffer due to pin limitations, especially in the lower current devices, such as the ISL8010 and EL7531. One potential limitation in these ICs is the lack of programmable soft-start; they have an internally fixed soft-start time. Some applications require large output capacitance to meet their design constraints. If the capacitance is too large, the inrush current during soft-start may exceed the current limit of the IC. Figure 36 illustrates the inrush current in a DC-to-DC buck application.

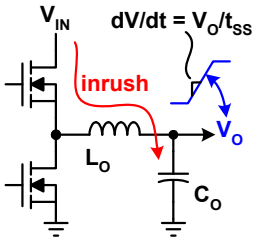


FIGURE 36.

Using the voltage to current relationship for capacitors (Equation 1) will determine the amount of current needed to initially charge the output capacitance (C_O) from 0V to the desire output voltage.

$$I_C = C \bullet dV_C / dt \quad \text{(EQ. 1)}$$

The ISL8010 soft-start time (t_{SS}) is between 250µs and 400µs (dependent on input voltage) and the current-limit is approximately 1.5A. Substituting the values of $I_{C(MAX)}$, V_O and t_{SS} into Equation 1 will determine the maximum capacitance the ISL8010 can handle for a specific application.

Example:

$I_{C(MAX)}$ = 1.5A

t_{SS} (worst case) = 250µs

V_O (desired) = 2.5V

$\therefore C_{O(MAX)} = (1.5/2.5) \bullet 250x10^{-6} = 150\mu F$

This example shows that for an output voltage of 2.5V, the maximum allowable capacitance for the ISL8010 is 150µF. Figures 37 and 38 graphically show the allowable ranges for output capacitance and voltage to successfully keep start-up inrush current below the current limit threshold for the ISL8010.

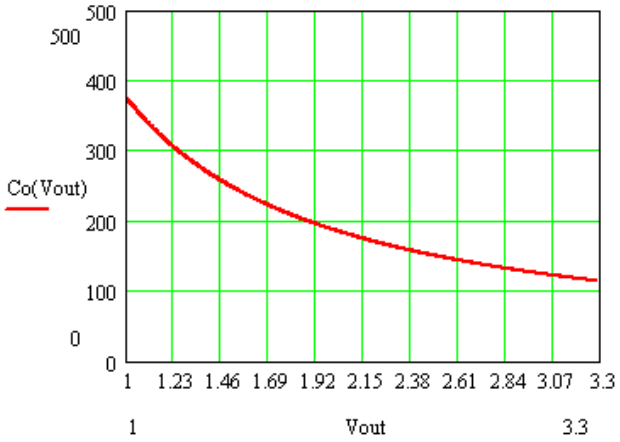


FIGURE 37.

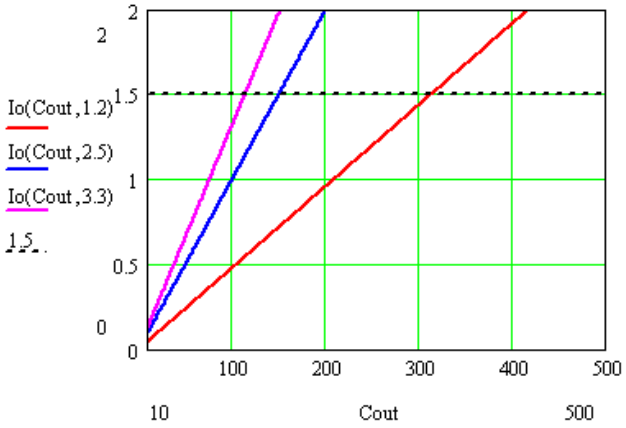


FIGURE 38. INRUSH CURRENT vs C_O AND V_O

NOTE: Some of these capacitance values exceed the data sheet recommended values for loop stability. Each design case that exceeds the recommended values must be qualified in the end application.

If an IC without programmable soft-start (e.g. ISL8010) is used in an application where the required output capacitance is large enough to produce inrush currents in excess of the current limit threshold, an external solution must be implemented to reduce the soft-start time, and therefore reduce the inrush current.

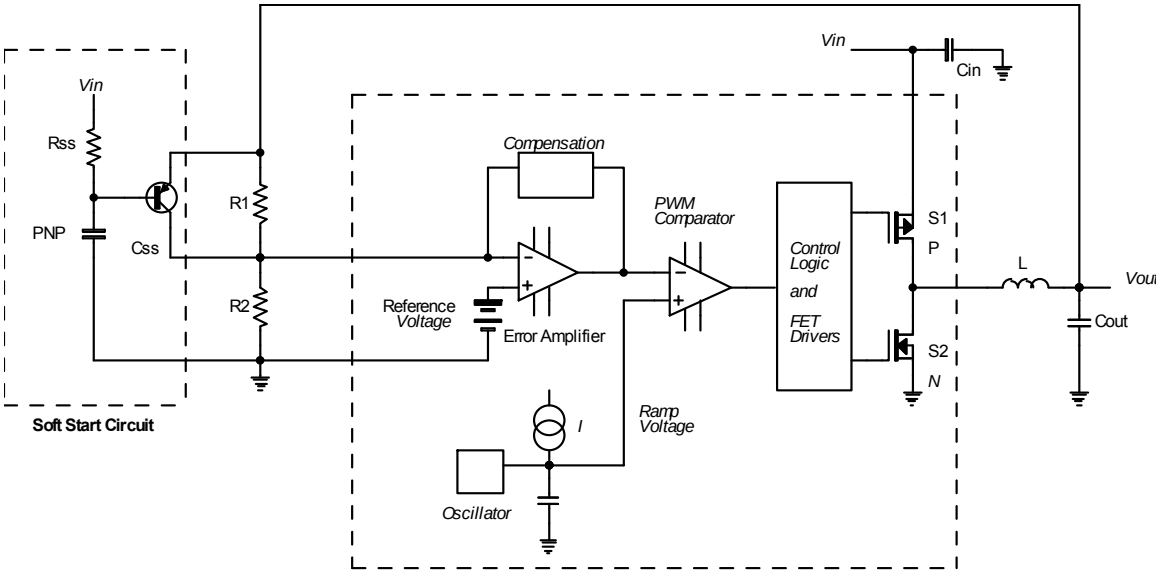


FIGURE 39. EXTERNAL PROGRAMMABLE SOFT-START CIRCUIT

Figure 39 illustrates a circuit implementation to allow programmable soft-start.

The PNP transistor in this circuit provides a low impedance path between the output voltage and the feedback pin. This has the effect of regulating the output very near the reference voltage of 0.8V. As the voltage on C_{SS} is charged through the resistor R_{SS}, the base voltage of the PNP transistor rises. The collector current will be continually reduced as the base voltage increases, causing more current to flow in R1 and subsequently increase V_O. The output voltage will track the R-C ramp on C_{SS} until the PNP is completely turned off, and all the current from V_O to FB is flowing in R1. At this point, the soft-start circuit has no effect, and the converter acts normally. Figure 40 shows the start-up event with the addition of the R-C network and PNP transistor.

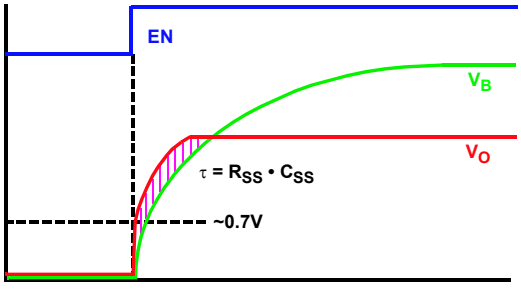


FIGURE 40.

As shown in Figure 40, the time constant of the start-up (T) is the product of the magnitudes of R_{SS} and C_{SS}. Making either of these two values larger will slow the soft-start time, and subsequently reduce the inrush current according to Equation 1.

Conclusion

Hopefully this Application Note has made designing a switching regulator with Intersil Integrated FET DC/DC Converters a little less daunting. The use of internal loop compensation has eased the burden of loop stability, easy to use Tables have been shown for inductor selection, setting the output voltage, and Feature selection. Simple test circuits for evaluating loop stability and input filter stability have been shown and demonstrated. PCB layout guidelines and techniques have been discussed for the PCB designer. Circuits such as output voltage tracking have been shown to reduce the headaches with power on sequencing and latch-up in digital ICs.

The Appendixes that follow discuss the theory and analysis of buck regulators using PWM control and the often ignored input filter stability.

FIGURE 41. A TYPICAL POWER SUPPLY DESIGN BENCH (BUT, WHERE'S THE PIZZA?)

Appendix A - Buck Mode Regulator Analysis

A buck mode switching regulator is used to very efficiently reduce a higher input voltage to a lower output voltage such as 5V to 3.3V or 2.5V to 1.8V. While this can be done with a pass transistor operating in the linear mode (ie, linear regulator or LDO), a buck mode switching regulator does the conversion process with very little power loss – high efficiency. Efficiency is defined as the ratio of output power to input power; i.e.:

$E = P_{OUT}/P_{IN}$

$(V_{OUT} \bullet I_{OUT})/(V_{IN} \bullet I_{IN})$

For a linear regulator (assuming no quiescent current losses):

$I_{OUT} = I_{IN}$ and

$E = V_{OUT}/V_{IN}$

For a 5V to 3.3V linear regulator, E = 3.3V/5V = 67%; one third of the power is lost as heat! It gets even worse at high input voltages; for example, for a 12V to 3.3V linear regulator, E = 3.3V/12V = 28%. Even for moderate load currents, a heat sink or thermal management is almost always required. For a battery operated system, the lost power makes a linear regulator very impractical.

The buck mode switching regulator performs an almost lossless voltage conversion with efficiency exceeding 95%; for a 10W DC/DC converter this is only 0.5W power lost.

Buck Mode Regulator Theory

The basic topology for a buck mode regulator is shown in Figure 42.

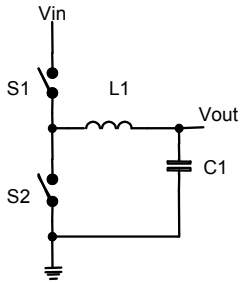


FIGURE 42.

Complement switches S1 and S2 are driven with pulse-width modulation (PWM) to regulate the output voltage, V_{OUT}. S1 is usually a bipolar transistor or MOSFET; S2 is either a diode or MOSFET. Inductor L1 and capacitor C1 provide energy storage and filter the output voltage to a DC level. The output voltage is set by the duty cycle of the PWM as shown in the following.

Duty Cycle Relationship

Assuming ideal elements (i.e., no voltage drop in the switches, infinitely fast switches, and no IR losses in L1 or C1), the inductor energy must be conserved in each switching cycle. The Energy In during the S1 ON time must equal the Energy Out during the S1 OFF time.

Energy In during S1 ON time = Energy Out during S1 OFF time.

$E = ½ Li^2$ for an inductor

$½ Li(on)^2 = - ½ Li(off)^2$

Notice the Energy Out must be negative since it is energy released during the OFF time, and not stored energy.

$i(on)^2 = - i(off)^2$

For an inductor, $i(t) = 1/L \int v(t)\, dt$

Since V_{IN} and V_{OUT} are constants in the integration,

$i(on) = 1/L \cdot (V_{IN} - V_{OUT}) \cdot T_{ON}$

$i(off) = 1/L \cdot (0 - V_{OUT}) \cdot T_{OFF}$

$1/L \cdot (V_{IN} - V_{OUT}) \cdot T_{ON} = - 1/L \cdot (0 - V_{OUT}) \cdot T_{OFF}$

$(V_{IN} - V_{OUT}) \cdot T_{ON} = V_{OUT} \cdot T_{OFF}$

$T_{OFF} = Tp - T_{ON}$ where Tp is the period of the switching frequency

$(V_{IN} - V_{OUT}) \cdot T_{ON} = V_{OUT} \cdot (Tp - T_{ON})$

Solving for V_{OUT}/V_{IN},

$V_{OUT}/V_{IN} = T_{ON}/Tp$ = Duty cycle

This equation is one of the fundamental relationships for a buck mode regulator; it says that the inductor value, capacitor value, and load current do not affect the basic duty cycle relationship, and only the duty cycle and input voltage determine the output voltage. Notice the load current has no effect on the duty cycle relationship for a buck mode regulator. If second order effects are considered (switch voltage loss, DCR losses in the inductor, ESR losses in the capacitor, etc.) then there will be a minor deviation from the duty cycle relationship.

Generating the PWM Signal

Most switching regulators use a PWM control method to adjust the duty cycle with a negative feedback loop to stabilize the output voltage. The PWM generator compares a ramp voltage with the output of an error amplifier to adjust the duty cycle in order to regulate the output voltage as shown in Figure 43.

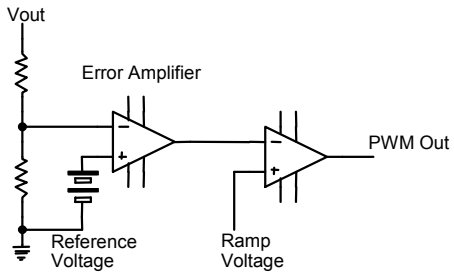


FIGURE 43.

The source of the ramp generator is critical to the topology and design of a buck mode regulator.

Voltage Mode Control

In a voltage mode regulator, the ramp voltage is derived from a triangle wave generator (see Figure 44). EL7532 is an example of a voltage mode buck regulator.

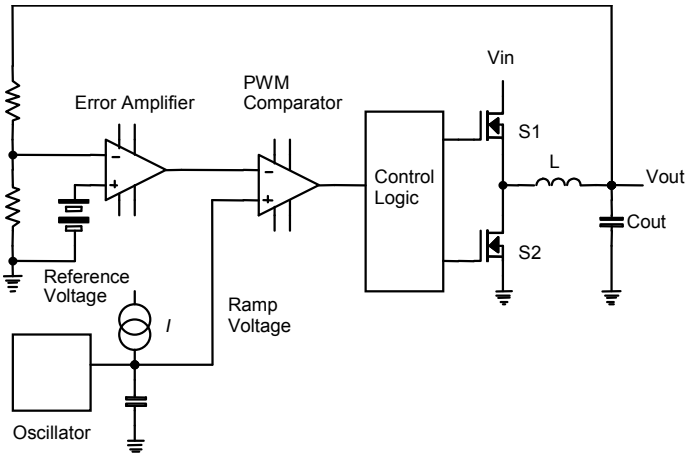


FIGURE 44. VOLTAGE MODE PWM GENERATOR

The advantages of a voltage mode buck are simplicity, no power loss in a current sensing element, and no need for slope compensation (this will be explained in more detail in the current mode control section to follow). The main disadvantages of voltage mode control are reduced dynamic line regulation, the open loop gain is a function of the input voltage, and a nasty two pole roll-off caused by the output inductor (L) and output capacitor (C_{OUT}). The disadvantages can be overcome with circuit design techniques, but the advantage of simplicity goes away. Additionally, to implement overcurrent or short circuit protection, it is necessary to sense the output current, which requires additional circuitry.

Current Mode Control

In a current mode regulator, the ramp voltage is directly proportional to the inductor current. The inductor current information is derived with various methods. The most popular techniques are a current sense resistor in series with the inductor, the DC resistance (DCR) of the inductor, and the ON resistance of the FETs (S1 or S2). In Figure 45, the inductor current is sensed across the ON resistance of S1, the top side switch. A current sense amplifier is used so the sense voltage can be very small to minimize power loss. The ramp voltage at the output of the current sense amplifier is used as the control ramp in the PWM generator. EL7566, EL6455, and EL6410 are examples of current mode buck regulators.

The advantages of current mode control are cycle by cycle current limiting, fast dynamic response to input voltage changes, and the output filter is a single pole response since the output inductor is inside the feedback loop. The disadvantages of current mode control are increased circuitry, the need to sense the inductor current which may add dissipative elements (sense resistors), and the need for slope compensation to eliminate sub-harmonic oscillations for duty cycle > 50%.

The Intersil Integrated FET Product line has both voltage mode and current mode products. The internal circuitry of the regulators is designed to overcome the disadvantages of both control techniques, making the choice invisible to the user.

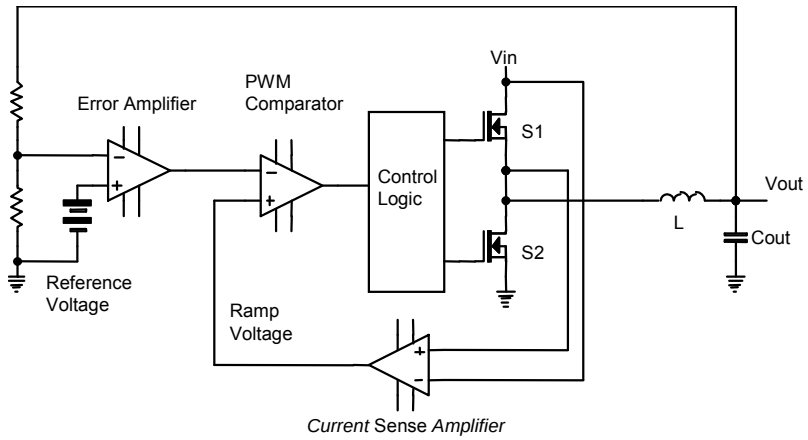


FIGURE 45. CURRENT MODE PWM GENERATOR

Continuous Mode vs Discontinuous Mode Operation

In a buck regulator, the average inductor current is equal to the load current since there can be no DC current in the output capacitor.

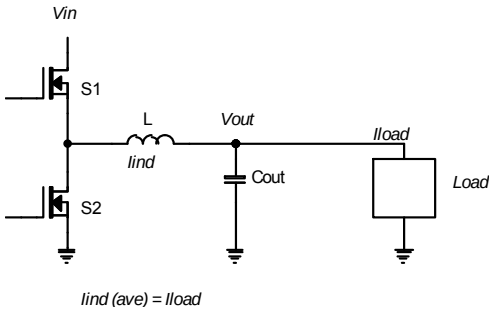


FIGURE 46.

Consider the inductor current during S1 ON time:

$i(t) = 1/L \int (v(t)\, dt$

The voltage imposed across the inductor is $V_{IN} - V_{OUT}$.

Since V_{IN} and V_{OUT} are constants in the integration, $i_{on}(t) = 1/L \bullet (V_{IN} - V_{OUT}) \bullet t$, which is a linear ramp during the S1 ON time.

The peak-peak inductor current during the S1 ON time is:

$dI = 1/L \bullet (V_{IN} - V_{OUT}) \bullet T_{ON}$

From the duty cycle relationship, duty cycle = $V_{OUT}/V_{IN} = T_{ON}/Tp$

or, $V_{OUT}/V_{IN} = T_{ON} \bullet F$

$T_{ON} = V_{OUT}/V_{IN} \bullet F$

$$dI = \frac{(V_{IN} \bullet V_{OUT}) \bullet V_{OUT}}{F \bullet L \bullet V_{IN}}$$

dI is referred to as the inductor ripple current; typically the design engineer will set the inductor ripple current to be 20-40% of the load current.

When S1 is first turned ON, the inductor current is:

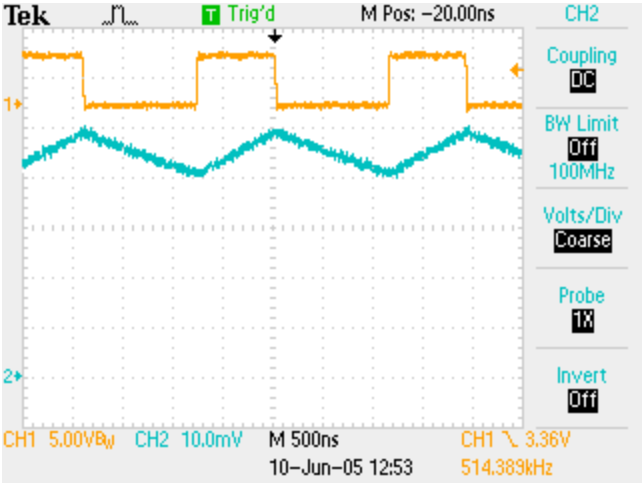
$I_{IND} = I_{LOAD} - ½ \bullet dI$

At the end of the ON cycle, the inductor current is:

$I_{IND} = I_{LOAD} + ½ \bullet dI$

As the load current is varied up and down, the average value of the inductor current moves up and down also. The inductor ripple current waveform does not change since there is no load current dependency. In reality, there will be a slight change in the inductor ripple current due to slight changes in S1 and S2 ON state voltage drop and the changes in the inductor's inductance due to DC current in the inductor.

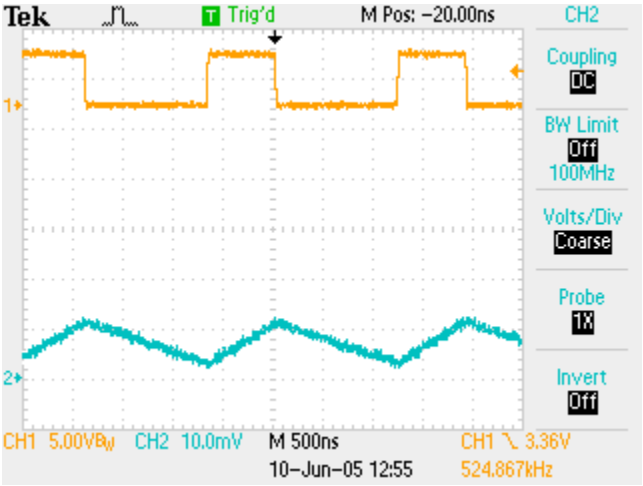
For an input voltage of 5.0V, an output voltage of 1.8V, and a load current of 4.7A, the waveform in Figure 47 was recorded for a typical buck regulator:



TOP TRACE - LX NODE
BOTTOM TRACE - INDUCTOR CURRENT (1A/DIV)

FIGURE 47.

Notice as the load current is reduced to 0.70A, the average value of the current waveform is reduced; however, the inductor ripple current and duty cycle do not appreciably change.



TOP TRACE - LX NODE
BOTTOM TRACE - INDUCTOR CURRENT (1A/DIV)

FIGURE 48.

As the load current is decreased or the input voltage is increased, at some point the inductor current will go to zero during S1 OFF time; this will occur when:

$$I_{LOAD} < \frac{V_{OUT} \bullet (1 - V_{OUT}/V_{IN})}{2 \bullet F \bullet L}$$

This is a critical point in the operation of a buck mode regulator. If S2 is a diode as shown in Figure 49, the inductor current will remain at zero during the remainder of S1 OFF time. At this point, the buck mode regulator enters Discontinuous Mode operation because the inductor current has dropped to zero. The switch node (S1, S2. and L) node will show a ringing waveform that is often confused as noise or loop instability.

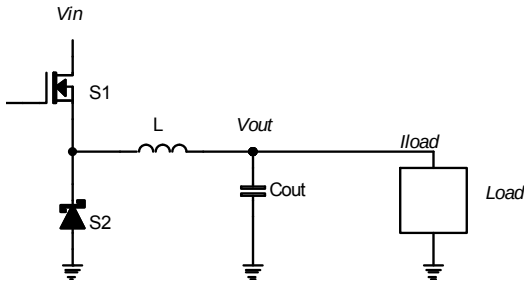
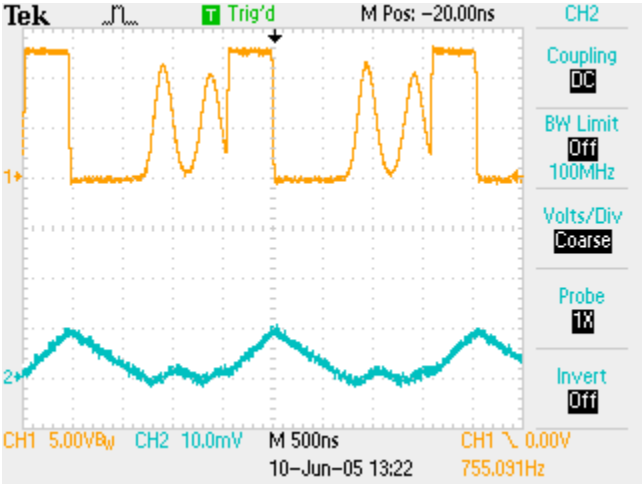


FIGURE 49.

A typical discontinuous mode waveform is shown in the scope photograph (Figure 50); notice the ringing on the LX pin when the inductor current goes to zero during the switch off time. This condition is often mis-diagnosed as being a loop instability or “noise problem” because of the ringing or difficulty with a scope trigger producing a stable waveform.



TOP TRACE - LX NODE
BOTTOM TRACE - INDUCTOR CURRENT (1A/DIV)

FIGURE 50.

The Intersil Integrated FET products (EL7532, EL7566, ISL6410, etc.) do not use a diode for S2. To reduce the diode voltage drop and improve efficiency, these parts employ a technique known as Synchronous Rectification where the diode is replaced with a low ON resistance FET. The improvements in efficiency are dramatic; depending on the input and output voltages, the efficiency can improve from 85% to over 95%.

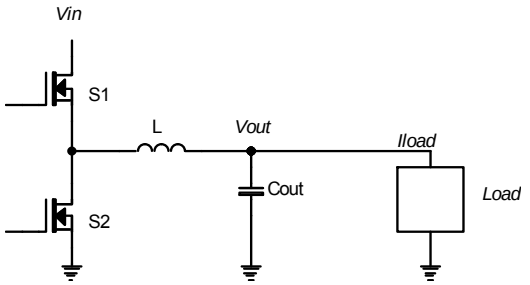
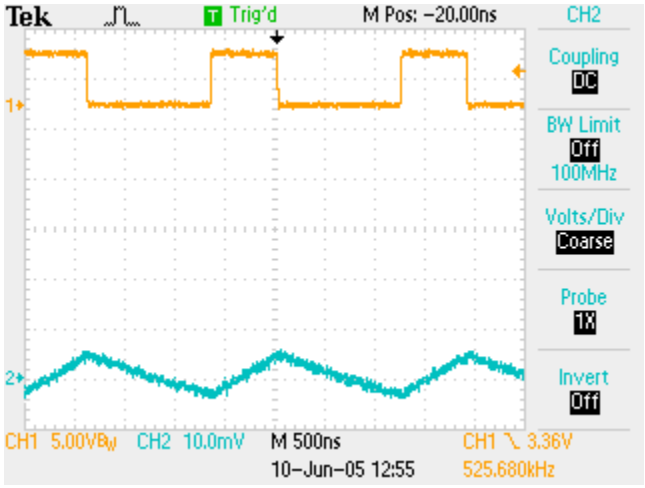


FIGURE 51.

However, there is a penalty to be paid for the efficiency improvement! Once the bottom side FET (S2) has been turned on with a gate drive voltage, it does no care which direction current is flowing in its channel. Current can flow from Drain to Source or from Source to Drain. Unlike using a diode for S1, the inductor current will continue to flow after the point of “discontinuous mode” operation is reached as shown in the scope waveform below under no load conditions.



TOP TRACE - LX NODE
BOTTOM TRACE - INDUCTOR CURRENT (1A/DIV)

FIGURE 52.

Even with no output current (i.e., no load operation), there can be significant current flowing in the FETs and inductor resulting in a large power loss without generating any output power. In this mode, the input current can still be substantial even though the output current is very small. This can cause very poor efficiency when operating under very light load conditions.

Several of the Intersil Integrated FET regulators (ISL8010, EL7531) employ a PFM (**P**ulsed **F**requency **M**ode) mode of operation to reduce the power loss when operating at very light load currents. The regulators can automatically switch between standard PWM or PFM mode when the load current is reduced.

In the automatic PFM/PWM operation, when the load is light, the regulator operates in the PFM mode to achieve high efficiency. The top P-channel MOSFET is turned on first, and the inductor current increases linearly to a preset value before it is turned off. Then, the bottom N-channel MOSFET turns on, and the inductor current linearly decreases to zero current. The N-channel MOSFET is then turned off, and an anti-ringing MOSFET is turned from the LX pin to V_O. In the PFM mode, the inductor current is a triangular pulse, and the frequency of the pulses is mainly a function of the output current. The higher the load current, the higher the frequency of pulses until the inductor current becomes continuous. At this point, the controller automatically changes to PWM mode of operation.

The waveforms in Figures 53 and 54 show the ISL8010 operating at a load current 100mA in PFM mode and operating at a load current of 600mA in PWM mode.

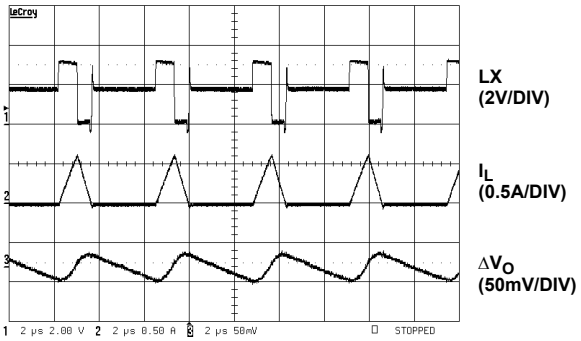


FIGURE 53. PFM MODE OPERATION (I_{OUT} = 100mA)

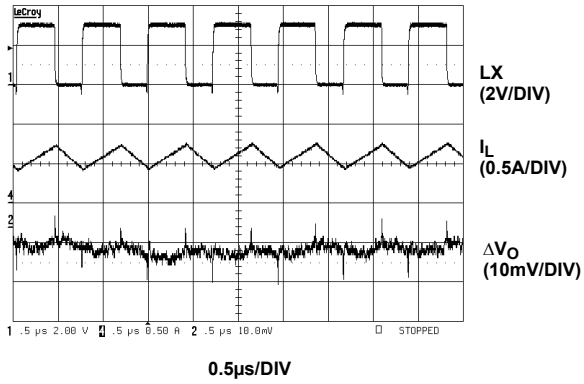


FIGURE 54. PWM MODE OPERATION (I_{OUT} = 600mA)

As the following ISL8010 graphs show, the efficiency improvement at light load currents is very significant when operating in the PFM/PWM mode.

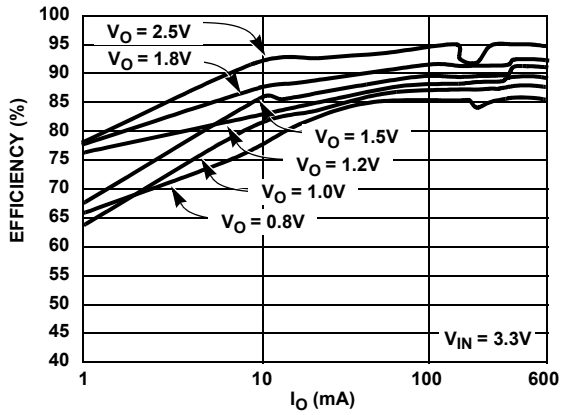


FIGURE 55. PFM MODE OPERATION

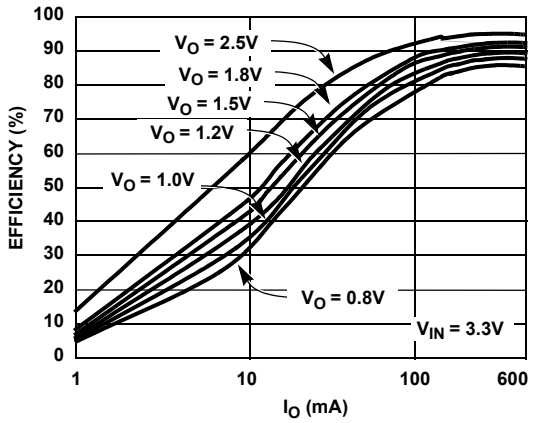


FIGURE 56. PWM MODE OPERATION

Appendix B - Input Filter Stability

Input filter stability is another factor that is often ignored, but must be considered in a buck regulator due to the negative input impedance of a switching regulator. The use of small value ceramic capacitors for the input filter capacitor makes this issue even more important.

The output impedance (Z_{OUT}) of the input source impedance and input filter must be much less than the input impedance (Z_{IN}) of the switching regulator.

$Z_{OUT} << Z_{IN}$

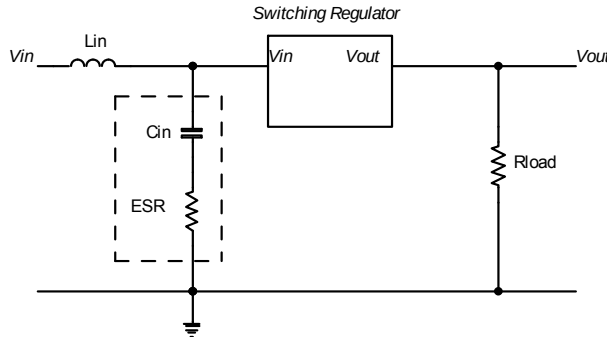


FIGURE 57.

The input filter output impedance, Z_{OUT}, will have a peak impedance of

$Z_{OUT} = L_{IN}/(ESR \bullet C_{IN})$

The switching regulator input impedance, $Z_{IN} = V_{IN}^2/(V_{OUT} \bullet I_{OUT})$

Therefore, $L_{IN}/(ESR \bullet C_{IN}) << V_{IN}^2/(V_{OUT} \bullet I_{OUT})$

Consider the stability problem encountered in the EL7532 Load Transient Tests as described previously in this application note.

L_{IN} = 4.8µH (approx. 48” of wire, or 2 foot lead)

C_{IN} = 10µF, ESR = 0.01Ω

V_{IN} = 3.3V

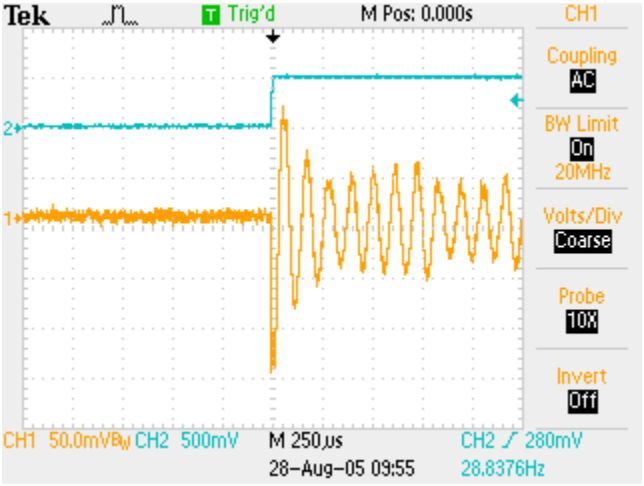
V_{OUT} = 1.8V, I_{LOAD} = 2A

$Z_{OUT} = 4.8\mu H/(0.01 \bullet 10\mu F)$

$= 48\Omega$

$Z_{IN} = 3.3^2/(1.8V \bullet 2A) = 2.8\Omega$

Since 48Ω (Z_{OUT}) is NOT much less than 2.8Ω (Z_{IN}), the input filter produced an unstable condition and the oscillations shown in the scope pictures resulted.



TOP TRACE - LOAD STEP
BOTTOM TRACE - OUTPUT VOLTAGE

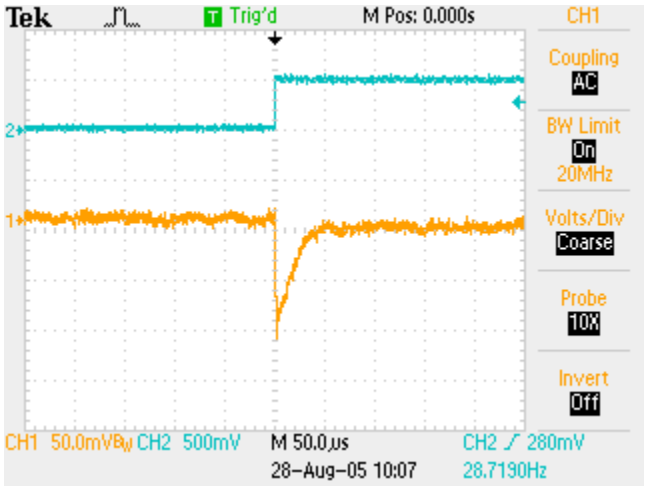
FIGURE 58.

When a 1000µF capacitor was added to the input terminals, the input filter output impedance, Z_{OUT}, was reduced to:

$Z_{OUT} = 4.8\mu H/(0.01\Omega \bullet 1000\mu F)$

$= 0.48\Omega$

Now, Z_{OUT} (0.48Ω) is less than Z_{IN} (2.8Ω), and the input filter provided a stable system.



TOP TRACE - LOAD STEP
BOTTOM TRACE - OUTPUT VOLTAGE

FIGURE 59.

The use of high frequency and small size DC/DC converters make the use of ceramic capacitors for the input capacitor highly desirable. However, due to their very low ESR and low capacitance value, ceramic input capacitors can lead to instability with the DC/DC converter.

With this in mind, there are three things which can be done to improve the input filter stability issue:

1. When you are evaluating a DC/DC converter on the lab bench, be sure the input source impedance is similar to the final system design.
2. Ensure the lead inductance between the input voltage source and the DC/DC converter circuit is as small as possible. This is particularly important when evaluating a DC/DC converter with a lab power supply and long test leads. It is not cheating to stabilize the lab power supply output with a 1000µF capacitor at the test fixture!
3. Increase the input capacitance value.
4. Increase the ESR of the input capacitor either with a small value resistor in series with the input capacitor or using a capacitor with a higher ESR. This is often not a good choice since increasing the capacitor ESR will result in a larger temperature rise of the capacitor due to ripple current and higher reflected input noise.

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