Use of HSP50216 and ISL5216 QPDC in Wideband Applications - UMTS

AN9927
Rev 0.00
April 2001

Description

This document will explain how to use Intersil's Quad Programmable Down Converters, the HSP50216 and ISL5216, for the Wideband Applications, in particular UMTS. It will explain in detail on how to combine channels in order to increase the output rate.

Configuration 1

Input Rate: 61.44MSPS (16x)

Output Rate: 7.68MSPS (2x)

This configuration implements a UMTS receiver in the HSP50216 using all of the four available channels. The block diagram of the implementation is shown in Figure 1.

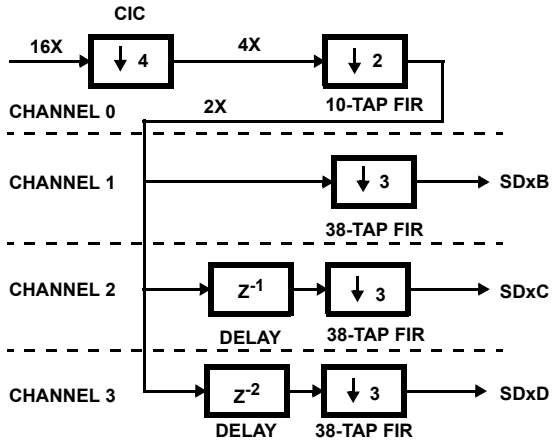

FIGURE 1. FILTER CONFIGURATION BLOCK DIAGRAM

In general it is best to perform as much of the decimation as possible in the CIC since this avoids having to use clock cycles to write data to the filter compute engine's (FCE) RAM, but this is limited by the tolerable alias level. The chosen CIC decimation of 4 yields a first alias level of about -85.6dB (see HSP50216 data sheet, Table 45 with fS/R = 0.5 / 4 = 0.125). For comparison, a CIC decimation of 8 would have given a first alias level of -52.269dB (for fS/R = 0.5 / 2 = 0.25).

Channel 0's 10-tap FIR serves as a low-pass filter for the decimation by 2. Its frequency response is provided in Figure 2. From this figure it can be seen that the first alias level is approximately -80dB. This 10-tap FIR, if implemented using the evaluation board software's "basic" filter configuration, would require 9 clocks (5 for computation, 2 for wait and loop steps, and 2 for the 2 input writes required by a decimate-by-2 filter). Only 16X / 2X = 8 clocks per output are available, however, so a hand-coded filter sequence is used to take advantage of a trick. The hand-coded filter sequence is included as an imported filter file. Instead of calculating one output in 9 clocks as just described, it calculates two outputs at a time to spread out the 2 clocks of overhead (wait and loop steps) over two output computations. The imported filter program requires 2 clocks for wait and loop, 4 clocks for 4 inputs (2 per filter run), and 10 clocks for computation (5 per run) for a total of 16 clocks per 2 outputs calculated. This is 8 clocks per output, which is exactly what is available.

Channel 0's output is cascaded to channels 1, 2, 3 which are configured to form a three-branch systolic array. Each of these channels runs a 38-tap filter whose frequency response is plotted in Figure 3. The 38-tap response is the result of a 36-tap filter convolved with a 3-tap CIC compensation filter which provides gain at the higher frequencies where the CIC rolls off. Channels 1, 2, 3 have their filter inputs delayed (or read pointers offset) by 0, 1 and 2 samples, respectively, making channel 3's output the first (oldest) data and channel 1's output the last (newest) data.

The configuration provided with this example routes channel 1's I and Q outputs to output pair SDxB, channel 2's to pair SDxC and channel 3's to pair SDxD, where x = 1 or 2. From above, an external multiplexer would take output D first, then C and finally B. Since the decimation from input to outputs SDxB, SDxC and SDxD is 4 x 2 x 3 = 24, 24 bits of data are available on each output. This example provides 24 bit I samples on outputs SD1D, SD1C and SD1B, and 24 bit Q samples on outputs SD2D, SD2C and SD2B. An external multiplexer is required in this configuration to combine all the I and Q outputs.

Alternatively, if only 8 bit I and Q outputs are required then they may be multiplexed on chip in the output formatter, providing I samples on one pin (for example SD1D) and Q samples on another (such as SD2D). To use outputs SDxD, the procedure would be to set channel 3 to output 8 bit I and Q samples to SD1D and SD2D, respectively, in the 1st slot followed by 16 bits of zeros in the next slot for a total data frame length of 24 bits. Channel 2 would also be routed to SDxD, and would be configured to output 8 bits of zeros to slot 1, 8 bits of I and Q to slot 2, and 8 bits of zeros to slot 3. Finally, channel 3 would route to SDxD with 16 bits of zeros in slot 1 and 8 bits of I and Q in slot 3. The end result, when all 3 channel outputs are OR'ed together onto SDxD, is 8 bit I samples on output SD1D from channels 3, 2, and 1, and 8 bit Q samples on output SD2D. The sync pulse can be programmed as needed, but would typically be activated only on channel 3 and would be set to output on each 8 bit slot. It is also possible to multiplex all the data onto a single serial output, providing 4 bit I and 4 bit Q samples.

Analysis of Computation Clock Usage

Channel 0

Available Clocks Per Output = 16X / 2X = 8

CLOCKS	FUNCTION
2	Overhead (Wait, Loop)
4	Input Writes from CIC to FCE (2 Inputs Per Run x 2 Runs of the Filter)
10	10-Tap FIR Computation (5 Clocks Per Run x 2 Runs of the Filter)
16	Total Clocks to Compute 2 Outputs

This configuration makes full use of channel 0, providing an output every 8 clock cycles.

Channels 1, 2 and 3

Available clocks per output = 4 x 2 x 3 = 24

CLOCKS	FUNCTION
2	Overhead (Wait, Loop)
3	Input Writes from Channel 0's FCE to Channel 1's FCE
19	38-tap Filter Computation
24	Total Clocks

Channels 1, 2 and 3 use every available clock.

A sweep of the composite CIC and FIR filter response is provided in Figure 4. This is an actual plot of the HSP50216's output magnitude as the input frequency is swept DC to 7.68MHz. 16 bit I and Q samples were captured for this example.

Figure 10 is a screen shot from the HSP50216 eval board software while receiving a UMTS signal from an ISL5217 quad programmable upconverter eval board. The four-point constellation is clearly visible in the I vs Q box, along with randomly scattered points from the mid-symbol samples. The HSP50216 eval board software does not determine symbol timing - it only plots the I and Q outputs, I vs. Q, and FFTs of 256 point captures. To obtain a plot such as that in Figure 10, the symbol timing on the ISL5217 upconverter is intentionally offset by about 1Hz so that the HSP50216 eval board slices at exactly the middle of the symbol once a second. The screen is captured at this moment. The tightness of the constellation points can be used to judge the match between the transmit and receive filters.

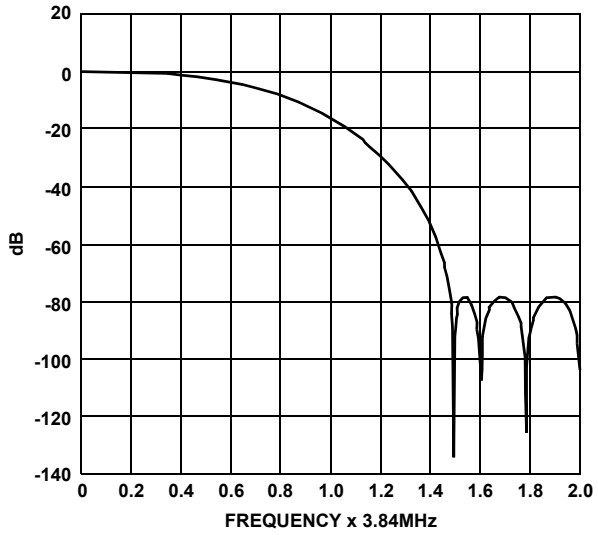

FIGURE 2. 10-TAP FIR FREQUENCY RESPONSE

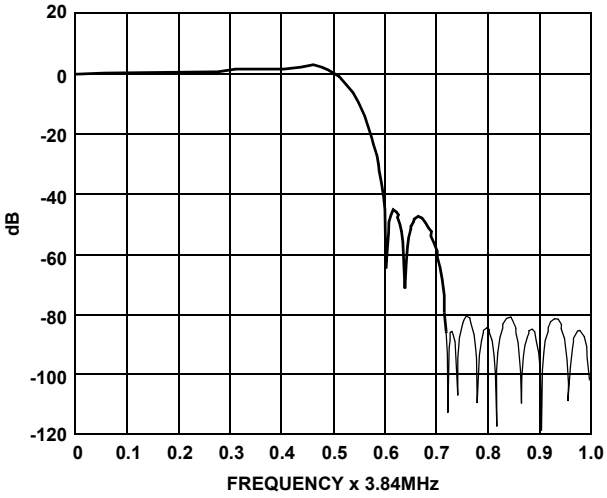

FIGURE 3. 38-TAP FIR FREQUENCY RESPONSE

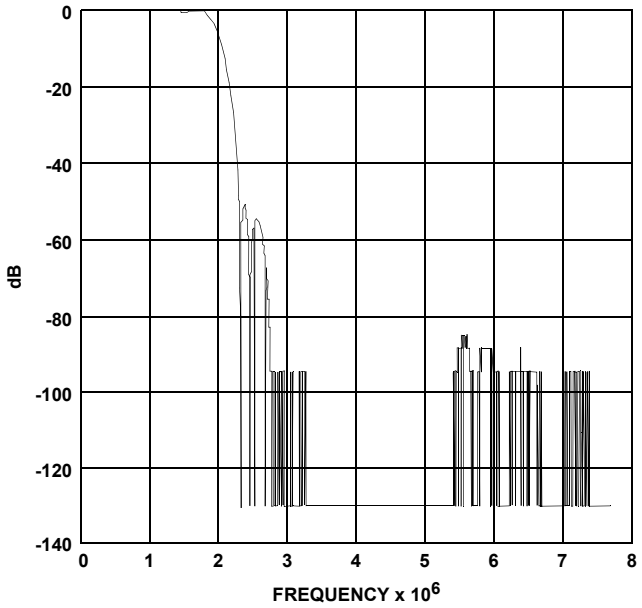

FIGURE 4. FREQUENCY SWEEP OF UMTS CONFIGUATION ON AN HSP50216

Configuration 2

Input Rate: 76.8MSPS (20x)

Output Rate: 7.68MSPS (2x)

Because of the 76.8MSPS input rate, this configuration is suitable only for the ISL5216. This example implements a UMTS receiver in the ISL5216 using only two of the four available channels. The block diagram of the implementation is shown in Figure 5.

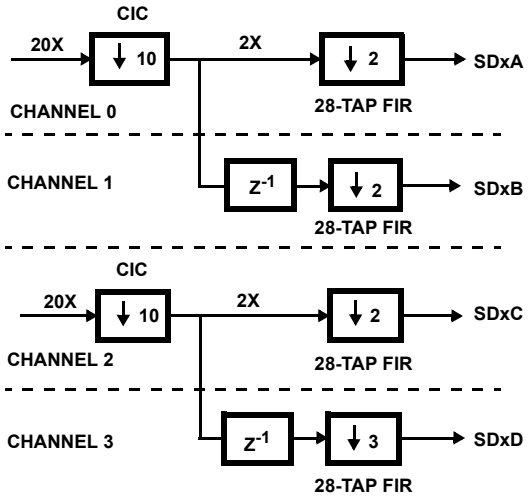

FIGURE 5. FILTER CONFIGURATION BLOCK DIAGRAM

The chosen CIC decimation of 10 in this configuration yields a first alias level of about -52.269dB (see HSP50216 data sheet, Table 45 with fS/R = 0.5 / 2 = 0.25).

The configuration is implemented in two of the four available channels, allowing two channels to be received per ISL5216. Channels 0 and 2 are the input channels and the NCOs from these channels are used for tuning. Channels 0 and 1, and 2 and 3 function as 2 branch systolic arrays whose outputs are multiplexed together to form the 2X output. The 28-tap FIR's frequency response is shown in Figure 6. In each channel, the decimation is 20X / 1X = 20, allowing up to 20 bits to be clocked out per output sample. As an example, it is possible to get 20 bit I samples from outputs SD1A and SD1B and 20 bit Q samples from SD2A and SD2B. An external multiplexer is required in this case to combine the SD1A, SD1B and SD2A and SD2B pairs. Multiplexing could also be done inside the ISL5216's output formatter if outputs of 10 bits or less are required. One example of this would be to set channels 0 and 1 to output to pair SDxB. Channel 1 would be programmed to output 10 bit I followed by 10 zeros to SD1B and 10 bit Q followed by 10 zeros to SD2B. Channel 0 could then be programmed to output 10 zeros followed by 10 bits of I onto SD1B and 10 zeros followed by 10 bits of Q on SD2B. When the two channels are OR'ed together at the output, the result is a 2X rate output with 10 bit I data on SD1B and 10 bit Q data on SD2B. The sync pulse would be programmed as needed, typically a pulse on each 10 bit output.

Analysis of Computation Clock Usage

Channels 0, 1, 2 and 3

Available clocks per output = 20X / 1X = 20

CLOCKS	FUNCTION
2	Overhead (Wait, Loop)
2	Input Writes from CIC to FCE
14	28-Tap FIR Computation
18	Total Clocks

This configuration leaves 2 clocks available on each channel's FCE, allowing an additional 4 taps to be added to the 28-tap filter response if desired.

A sweep of the composite CIC and FIR filter response is provided in Figure 7. This is an actual plot of the ISL5216's output magnitude as the input frequency is swept from DC to 7.68MHz. 16-bit I and Q samples were captured for this example.

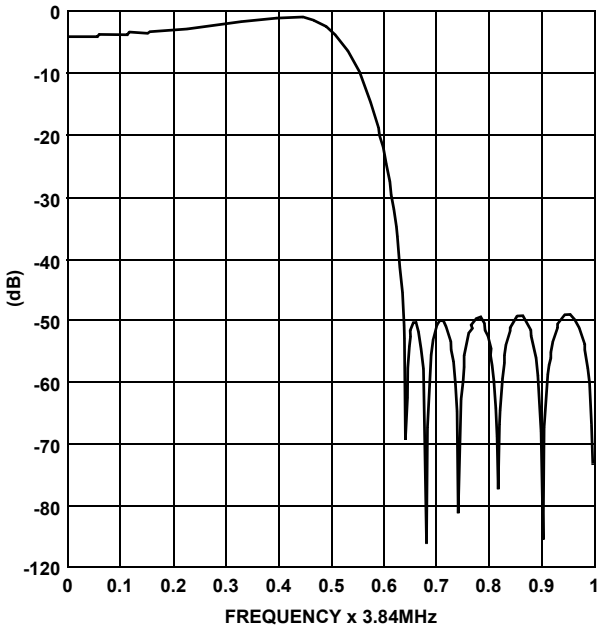

FIGURE 6. 28-TAP FIR FREQUENCY RESPONSE

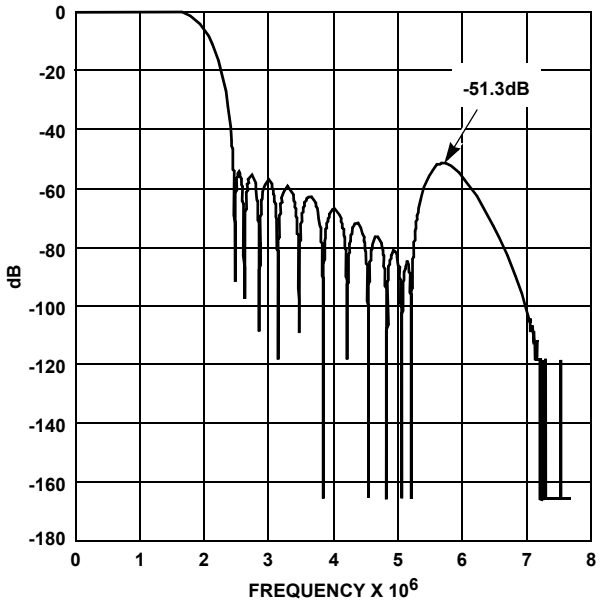

FIGURE 7. FREQUENCY SWEEP OF UMTS CONFIGUATION ON AN ISL5216

Use of HSP50216 EVAL Software for this Application

The eval board software is the perfect tool to evaluate performance of the part, configure registers, verify filter designs, and display the I/Q constellation and spectrum of the output. Connectivity to the eval board is supported only by Windows 95 and 98, however Windows NT and 2000 may be used for generating the register value files which may be downloaded to the chip with the user's own hardware.

NOTE: The software can configure the register value files even if the HSP50216/ ISL5216 Evaluation Board is not connected.

The configuration file is loaded by selecting option 8 in the main menu of the software. Enter only the root name of the configuration, where the root name is the file name preceding the .0, .1, .2, .3 and .top file extensions.

Figure 9 shows the channel 0 data path settings for Configuration 1. It shows the 61.44MSPS input rate, 5th order CIC decimation of 4, and an NCO center frequency of -4MHz (which serves to shift the signal centered at 4MHz down to DC). The imported filter program specified in options 13, 27 and 28 contains both the FCE program and the 10-tap FIR coefficients (see Figure 1). Imported filters are hand-coded filter programs which bypass the software's automatic register value generation.

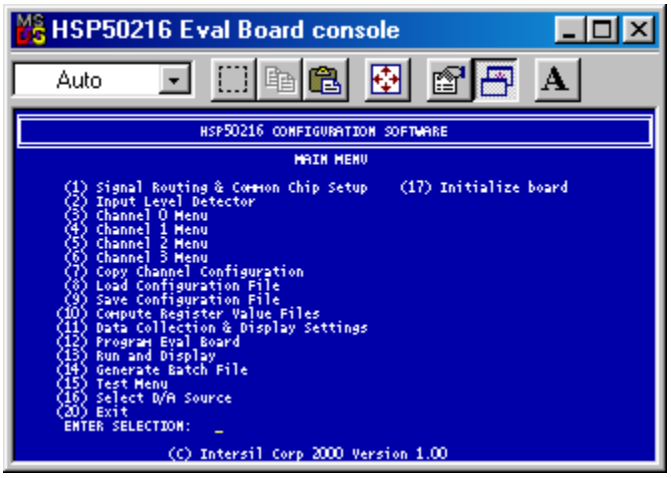

FIGURE 8. EVALUATION BOARD SOFTWARE MAIN MENU

FIGURE 9. DATA PATH MENU SCREEN

The data path menus for channels 1, 2, and 3 in Configuration 1 use the basic filter type option (option 13 "spec type" is "basic"), which loads the filter impulse response from an IMP file. Any filter file may be used as long as it satisfies the .IMP

format (first seven lines blank for comments, followed by a single column filter coefficients).

When loading of the configuration is completed (main menu option 8), initialize the eval board using option 17, compute the register value files using option 10, and download the register values to the ‘216 using option 12. Finally, select run and display (option 13) to see the ‘216 output in real time.

As noted previously, if only register values are needed, option 10 in the Main Menu will compute register values for each of the channels, and store them in the files file_name.r0, file_name.r1, file_name.r2, file_name.r3 and file_name.rtp where file_name is name entered into the load or save configuration options (8 and 9) from the main menu. These files are human readable text files containing register numbers and values in hex.

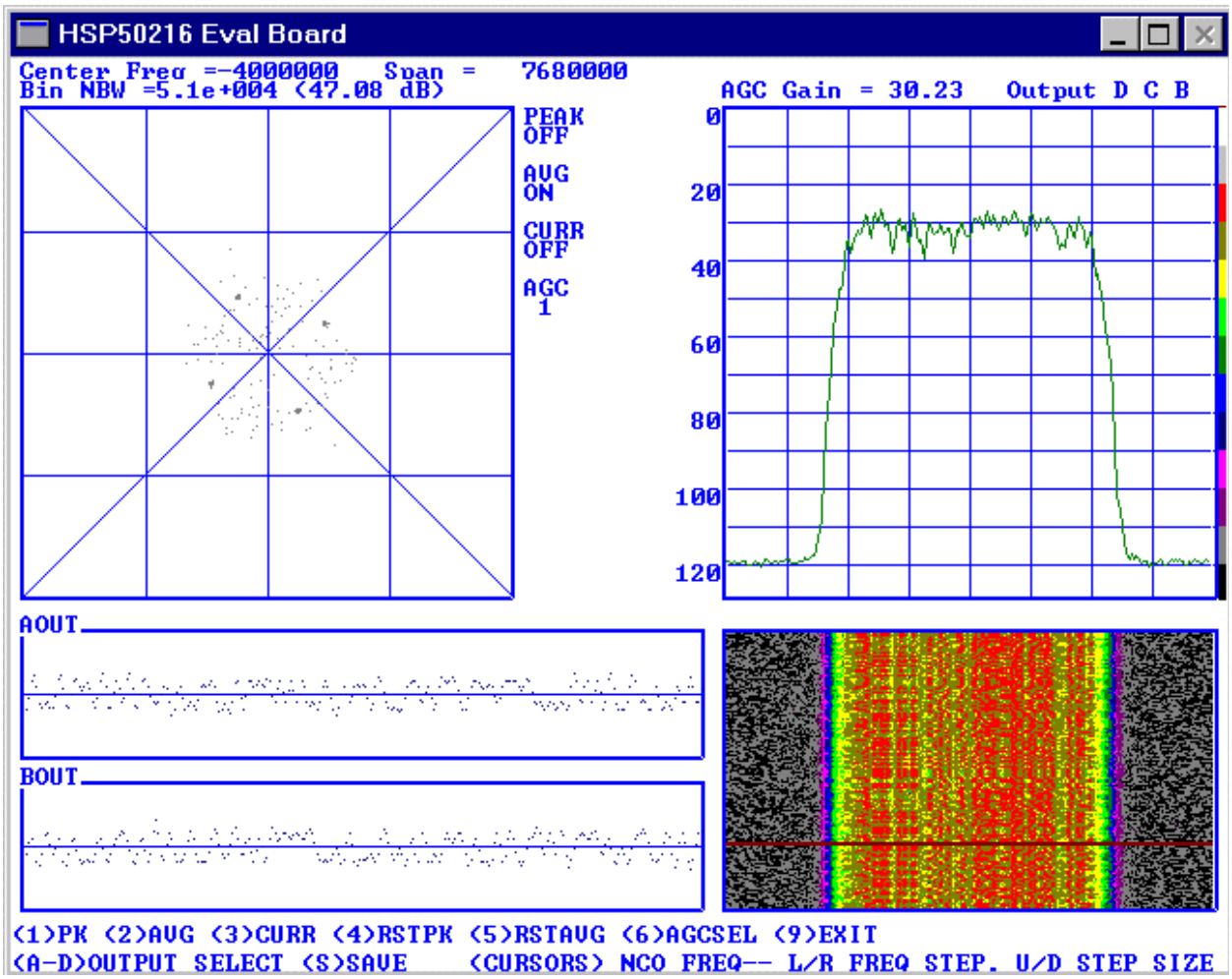

FIGURE 10. EVALUATION BOARD SOFTWARE IN DISPLAY MODE

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(Rev.4.0-1 November 2017)

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
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Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

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Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
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