ClockMatrix Combo Mode Filter

This application note explains how to configure the Combo Mode Filter when using the Combo bus of ClockMatrix devices.

Contents

1. Introduction

The ClockMatrix architecture allows the option for the Master Combo channel to filter the frequency information before it is transferred to the Slave Combo channel. Figure 1 shows a filter between the Combo Mode master and the Combo Mode slave. This low pass filter provides a lower bandwidth than what is used in the regular loop filter, without affecting the DPLL's output clock. The filter feature was included in the ClockMatrix device with the anticipation that the ITU standards committee would recommend such a filter in the future to filter syncE phase transients. However, enhanced syncE has a tighter specification for phase transients.

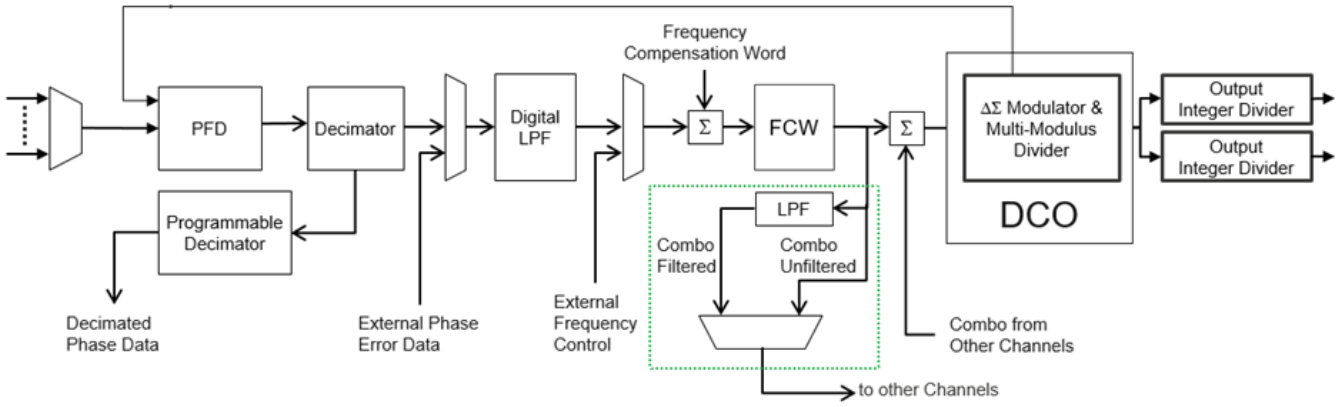

Figure 1. Block Diagram of One Channel of ClockMatrix

The filtered output provides an additional low-pass filter that can filter some of the Combo Master SyncE noise before the frequency information is passed to the Combo Slave. For example, if the combo filter is set to attenuate down to 1100mHz before it passes the frequency information to the Slave Time (PTP) PLL Channel, then it will eliminate noise from 1100mHz on the output of the master combo SyncE PLL. The combo low pass filter is in addition to the regular DPLL loop filter.

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2. Filter Configuration Steps with Example

2.1 Step 1

The input to the combo filter type can be selected by setting the DPLL_CTRL_{x}.DPLL_COMBO_MASTER_CFG bit, where “x” is the DPLL channel. It can be selected between the integrator value or the sum of the proportional and the integrator values. The integrator value is the frequency offset (holdover value), as it is integrated over time. The sum of the proportional and the integrator value is the loop filter output value of the DPLL. An excerpt from the *8A3xxx Family Programming Guide* is shown in Figure 2. By default, the “integrator value only” is selected, with a bandwidth setting of 0, which means the filter is bypassed.

DPLL_CTRL_0.DPLL_COMBO_MASTER_CFG

DPLL combo master configuration.

Table 274: DPLL_CTRL_0.DPLL_COMBO_MASTER_CFG Bit Field Locations and Descriptions

Offset Address (Hex)	DPLL_CTRL_0.DPLL_COMBO_MASTER_CFG Bit Field Locations							
	D7	D6	D5	D4	D3	D2	D1	D0
03Ah	RESERVED[7:2]						FILTER_IN_SELECT[1]	HOLD_EN[0]

DPLL_CTRL_0.DPLL_COMBO_MASTER_CFG Bit Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
RESERVED	N/A	-	This field must not be modified from the read value
FILTER_IN_SELECT[1]	R/W	0	Select filtered DCO value as combo source. 0 = integrator value only 1 = sum of proportional and integrator

Figure 2. Register Description for the Combo Master Configuration

Figure 3 is the DPLL configuration window in Timing Commander, showing Channel 4 as the Master SyncE Channel.

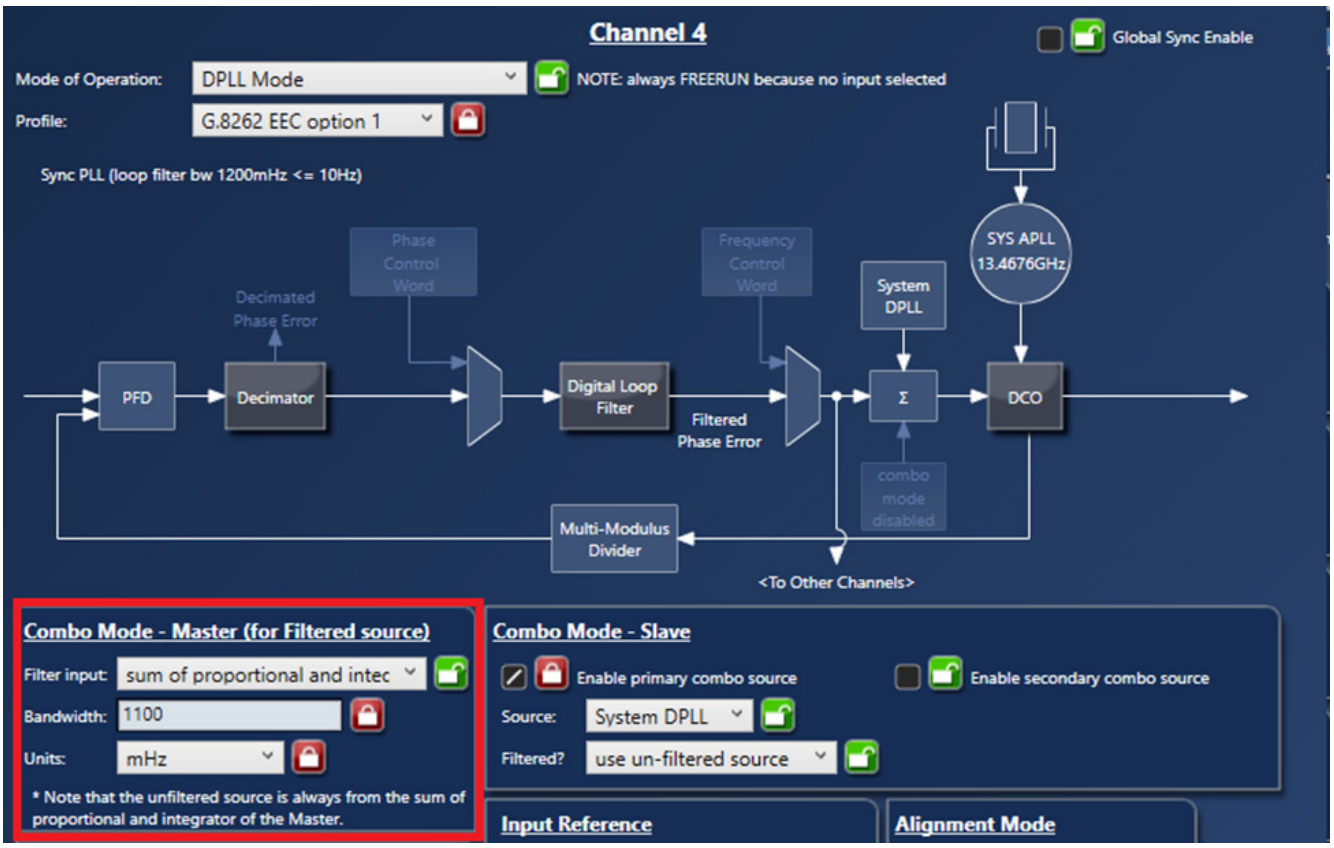

Figure 3. Channel 4 as the Combo Master Showing the Location of the Combo Master Settings in the GUI

The SyncE loop filter bandwidth is 10Hz (G.8262 EEC Option 1) in this example. The combo filter must be smaller than the Master DPLL loop filter bandwidth. In this example, the combo filter bandwidth is 1100mHz.

In the GUI, select the input to the filter as shown in Figure 4.

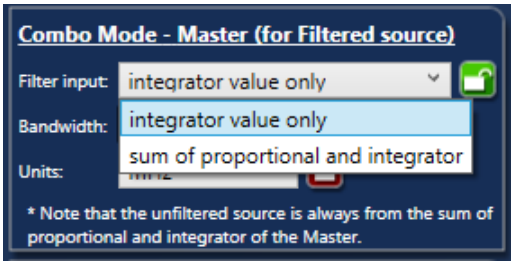

Figure 4. Filter Input Combo Master Settings as Shown in the GUI

2.2 Step 2

Set the Filter bandwidth using the DPLL_CTRL_{x}.DPLL_COMBO_MASTER_BW and the DPLL_CTRL_{x}.BW_UNIT settings as shown in Figure 5.

Table 273: DPLL_CTRL_0.DPLL_COMBO_MASTER_BW Bit Field Locations and Descriptions

Offset Address (Hex)	DPLL_CTRL_0.DPLL_COMBO_MASTER_BW Bit Field Locations							
	D7	D6	D5	D4	D3	D2	D1	D0
038h	DPLL_COMBO_MASTER_BW[7:0]							
039h	BW_UNIT[15:14]		DPLL_COMBO_MASTER_BW[13:8]					

DPLL_CTRL_0.DPLL_COMBO_MASTER_BW Bit Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
BW_UNIT[15:14]	R/W	0	Combo filter bandwidth unit. 0 = uHz 1 = mHz 2 = Hz 3 = kHz
DPLL_COMBO_MASTER_BW[13:0]	R/W	0	Unsigned 14-bit Combo filter bandwidth value.

Figure 5. Register Description for the Combo Master Filter Bandwidth

These are the settings in the GUI as shown in Figure 6.

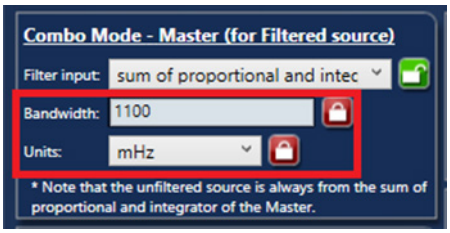

Figure 6. Filter Bandwidth Combo Master Settings as shown in the GUI

2.3 Step 3

The Combo mode slave primary source configuration can be set through the DPLL_{x}.DPLL_COMBO_SLAVE_CFG_{x} register, where “x” is the DPLL channel as shown in Figure 7.

DPLL_0.DPLL_COMBO_SLAVE_CFG_0

Combo mode slave primary source configuration.

Table 215: DPLL_0.DPLL_COMBO_SLAVE_CFG_0 Bit Field Locations and Descriptions

Offset Address (Hex)	DPLL_0.DPLL_COMBO_SLAVE_CFG_0 Bit Field Locations							
	D7	D6	D5	D4	D3	D2	D1	D0
032h	RESERVED[7:6]		PRI_COMBO_SRC_EN[5]	PRI_COMBO_SRC_FILTERED_CNFG[4]	PRI_COMBO_SRC_ID[3:0]			

DPLL_0.DPLL_COMBO_SLAVE_CFG_0 Bit Field Descriptions			
Bit Field Name	Field Type	Default Value	Description
RESERVED	N/A	-	This field must not be modified from the read value
PRI_COMBO_SRC_EN[5]	R/W	0	Enable this source. 0 = disabled 1 = enabled
PRI_COMBO_SRC_FILTERED_CNFG[4]	R/W	0	Use filtered source. 0 = use un-filtered source 1 = use filtered source
PRI_COMBO_SRC_ID[3:0]	R/W	0	Primary combo source DPLL index.

Figure 7. Register Description for the Combo Slave Configuration

Figure 8 shows the DPLL configuration window in Timing Commander, with Channel 5 displayed as the Slave Time (PTP) PLL Channel. Notice how the filtered source is used, which means the 1100mHz combo filter is used as defined in Channel 4 above. If an unfiltered source is used, the combo filter is bypassed.

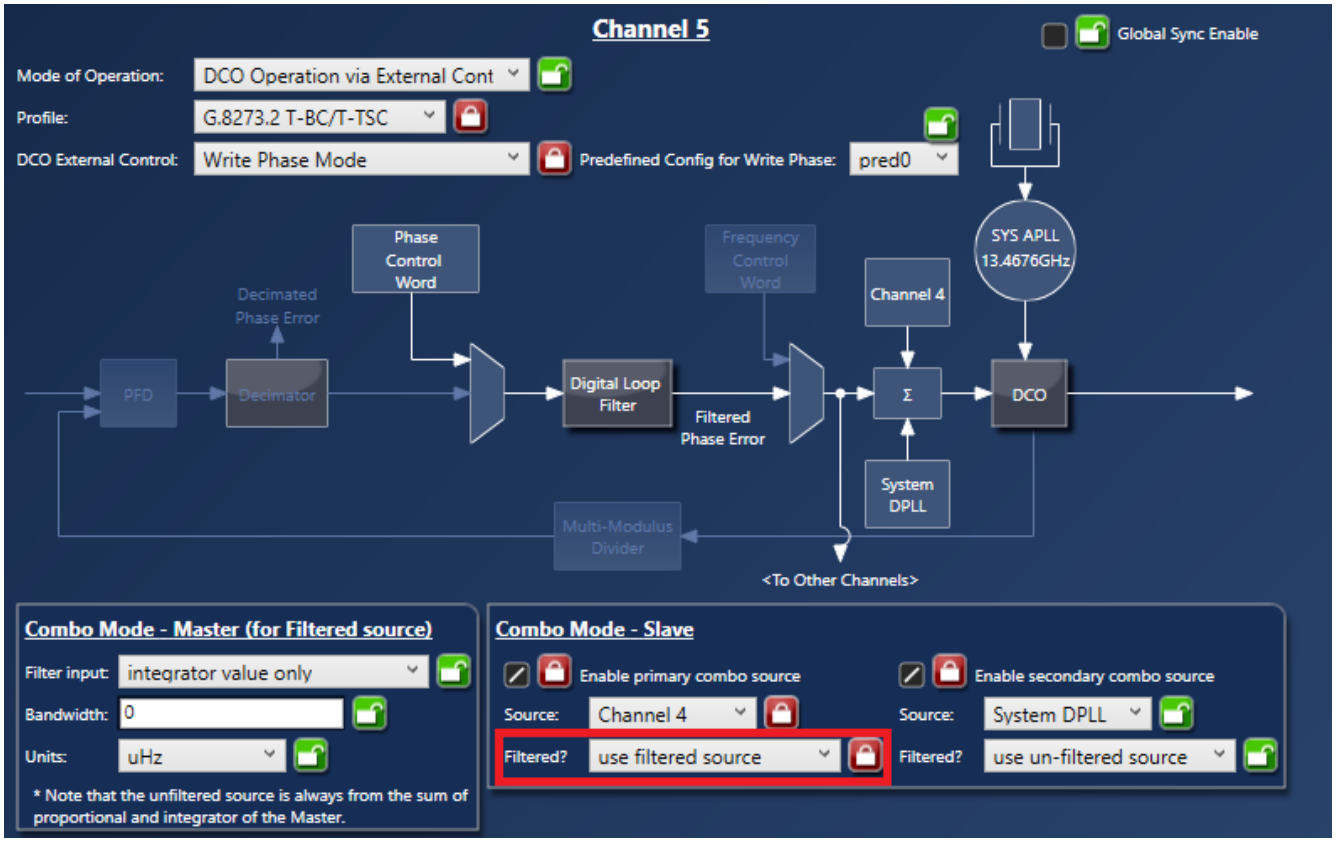

Figure 8. Filter Selection Combo Slave Settings as Shown in the GUI

3. Revision History

Revision	Date	Description
1.0	Jul 21, 2021	Initial release.

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