Application note provides the definitions and default values of the registers that are required to be re-programmed after a solder reflow process using the Renesas Serial MRAM product family.

1. Introduction

The Renesas High Performance (HP) and Ultra Low Power (ULP) Serial P-SRAM products require all writable non-volatile bits in the status register and the configuration registers (HP Serial P-SRAM devices) to be re-initialized to factory default values upon power up after high temperature solder reflow process. This re-initialization process allows the P-SRAM to power up in a known and defined state.

For soldering the P-SRAM parts during board manufacturing, Renesas recommends users to follow the JEDEC J-STD-020 reflow profiles with peak reflow temperature not to exceed three reflow cycles at 260°C for a total of three seconds.

This application note provides the definition and factory default values for each writable non-volatile bit in the configuration registers and status register. For reference, sample code is provided in section 2.6.

Table 1: Applicable Part Numbers

Product Type	Renesas P/N
HP Serial MRAM	M3xxx204-xxxxxxxxxx M1xxx204-xxxxxxxxxx
ULP Serial MRAM	M1xxx101-xxxxxxxxxx M3xxx101-xxxxxxxxxx

2. Register Overview

Table 2 below shows the registers that are required to be reset upon power up after high temperature solder reflow process for the ULP and HP Serial P-SRAM products.
First, the Status register needs to be reset to 00h. After resetting the Status register to 00h, the Configuration registers 1,2,3 and 4 need to be reset to (00h, 00h, 60h or 00h and 05h) respectively. Resetting the Configuration registers are required for the HP Serial P-SRAM devices.

Table 2: Register Comparison

Register Name	ULP Serial P-SRAM[1]	HP Serial P-SRAM[2]
Status Register	√	√
Configuration Registers (1-4)	Not applicable	√

Note 1: For ULP Serial P-SRAM devices, only the Status register is required to be reset.
Note 2: For Configuration register 3, set the register to 60h for 3.0V devices and 00h for 1.8V devices.
Refer to sections 2.1 to 2.5 for the detailed register descriptions.

2.1 Status Register (SR)

The register bits can be read and changed using the Read Status command or Write Status Register command.

Table 3: Status Register

Bit	Description	Field Name	Memory Type	R/W	Factory Default State
7	Write Protect Status & Configuration Registers 1 = Protected when WP# is low 0 = Not protected even WP# is low	WP#EN	NV	R/W	0
6	Serial Number Protection 1 = Serial Number locked 0 = Serial Number not locked	SNPEN	NV	R/W	0
5	Top or Bottom Memory Array Protection 1 = Bottom blocks protection (low address) 0 = Top blocks protection (high address)	TBSEL	NV	R/W	0
4	Block Protect Bits	BPSEL[2]	NV	R/W	0
3		BPSEL[1]	NV	R/W	0
2		BPSEL[0]	NV	R/W	0
1	Write Operation Protection 1 = Write operation enabled 0 = Write operation disabled	WREN	V	R	0
0	Reserved	RSVD	V	R	0

Write Operation Protection - The WREN bit indicates the state of the Write Enable Latch and is a volatile bit. The Write Enable command sets the WREN bit to 1 to enable a write memory array or Write Register commands. The Write Disable command resets the WREN bit to "0" to prevent all write commands from execution. The Write Status Register command does not affect the WREN bit.

WREN bit is clear after the following operations:

- POR, Hardware Reset or Software Reset
- RESET# pin is driven low
- WRDI command completion
- After any write register completion

Software-based Data Protection - Block Protection (BPSEL[2], BPSEL[1], BPSEL[0]) - The Block Protect (BPSEL[2], BPSEL[1], BPSEL[0]) bits are non-volatile. They define the size of the area to be software protected against any write operations. These bits are written with the Write Register command. When one or more of the Block Protect (BPSEL[2], BPSEL[1], BPSEL[0]) bits is set to 1, the relevant memory area becomes protected. These bits can be written provided that the hardware protected mode has not been set.

Top or Bottom Protection (TBSEL) Bit - The TBSEL bit is non-volatile. When set to 1, this bit indicates that the block protection starts at bottom (low address range). When set to 0, the bit indicates that the block protection starts at top (high address range).

Serial Number Lock - When set to 1, the serial number is locked and write-protected.

Hardware-based Data Protection - Write Protect Enable (WP#EN) Bit - The Write Protect Enable (WP#EN) bit is operated in conjunction with the Write Protect (WP#) signal. The Write Protect Enable (WP#EN) bit and the Write Protect signal allow the device to be put in the Hardware Protected Mode (HPM). The HPM mode write-protects the Status Register, and Configuration Register 1/2/3/4. The Hardware Protected (HPM) Mode can be entered:

- By setting the Write Protect Enable (WP#EN) bit to 1 after driving Write Protect (WP#) low
- OR by driving Write Protect (WP#) low after setting the Write Protect Enable (WP#EN) bit to 1

The only way to exit the Hardware Protected Mode (HPM) once entered is to drive Write Protect (WP#) high. If Write Protect (WP#) is permanently tied high, the Hardware Protected Mode (HPM) can never be activated, and only the Software Protected Mode (SPM), using the block protect (BPSEL[2], BPSEL[1], BPSEL[0]) bits of the Status Register, can be used.
If the Write Protect Enable (WP#EN) is set to 1, protection cannot be changed until both the QPI bit the Configuration Register 2 (CR2) is reset to 0. The Hardware Protected Mode is disabled if the device is in QPI mode.

2.2 Configuration Register 1 (CR1)

The register bits can be read and changed using the Read Configuration Register 1/2/3/4 command or Write Configuration Register 1/2/3/4 command.

Table 4: Configuration Register 1

Bit	Description	Field Name	Memory Type	R/W	Factory Default Value
[7:3]	Reserved	RSVD	--	--	0
2	Memory Array Data Protect 1 = Locked 0 = Unlocked	MAPLK	NV	R/W	0
1	Reserved	RSVD	--	--	0
0	Augmented Storage Array Data Protection 1 = Locked 0 = Unlocked	ASPLK	NV	R/W	0

Augmented Storage Array Data Protection – When set to 1, the ASPLK bit locks all sections. Either Hardware Reset, JEDEC Reset or Software Reset will not change the state of this bit.

Memory Array Data Protection – When set to "1", this bit locks block protection and all three Block Protection Bits.

2.3 Configuration Register 2 (CR2)

The register bits can be read and changed using the Read Configuration Register 1/2/3/4 command or Write Configuration Register 1/2/3/4 command.

Table 5: Configuration Register 2

Bit	Description	Field Name	Memory Type	R/W	Factory Default State
7	Reserved	RSVD	-	-	0
6	QPI or SPI Selector 1 = QPI (4-4-4) mode 0 = Legacy SPI mode	QPISL	V	R	0
5	Reserved	RSVD	-	-	0
4	DPI or SPI Selector 1 = DPI (2-2-2) mode 0 = Legacy SPI mode	DPISL	V	R	0
3	Memory Latency Cycle (Configuring number of Latency Cycles)	MLAT[3]	NV	R/W	0
2		MLAT[2]	NV	R/W	0
1		MLAT[1]	NV	R/W	0
0		MLAT[0]	NV	R/W	0

Memory Latency Cycle – these bits dictate the memory read latency cycles. As CLK frequency increases, read commands require additional latency cycles to complete the initial read access the memory array before data can be transferred to the SPI host.

DPI or SPI Select – When this volatile bit is set to 1, the DPI is enabled in which all transfers between the host and the Serial MRAM are 2-bit wide on I/O0 and I/O1 including command, address, mode byte, and data. This DPI bit is automatically set to 1 when DPI mode is enabled by executing the Enable DPI Command (DPIE – 37h) command. Exiting DPI mode by executing either the Enable QPI command (QPIE-38h) or the Enable SPI command (SPIE – FFh) will reset the DPI bit to 0.

QPI or SPI Select – When this volatile bit is set to 1, the QPI is enabled in which all transfers between the host and the Serial MRAM are 4-bit wide on 4 I/Os including command, address, mode byte, and data. This QPI bit is automatically set to 1 when QPI mode is enabled by executing the Enable QPI command (QPIE – 38h) command. Exiting QPI mode by executing either the Enable DPI command or the Enable SPI command (SPIE – FFh) will reset this QPI bit to 0.

The Write Configuration Register 1/2/3/4 command does not affect the DPI or SPI select bit or the QPI or SPI select bit.

2.4 Configuration Register 3 (CR3)

The register bits can be read and changed using the Read Configuration Register 1/2/3/4 command or Write Configuration Register 1/2/3/4 command.

Table 6: Configuration Register 3

Bit	Description	Field Name	Memory Type	R/W	Factory Default State	
					1.8V	3.0V
7	Output Driver Strength Selector	ODSEL[2]	NV	R/W	0	0
6		ODSEL[1]	NV	R/W	0	1
5		ODSEL[0]	NV	R/W	0	1
4	Read WRAP Enable/Disable 1 = Enable 0 = Disable (in continuous bursts read/write mode)	WRAPS	NV	R/W	0	
3	Reserved	RSVD	-	-	0	
[2:0]	Wrap Length Selector 000 = 16-byte boundary aligned wrap 001 = 32-byte boundary aligned wrap 010= 64-byte boundary aligned wrap 011 = 128-byte boundary aligned wrap 100 = 256-byte boundary aligned wrap 101 = Reserved 110 = Reserved 111 = Reserved	WRPLS[2:0]	NV	R/W	0	

Wrap Around Select – When this bit is set to 1, the Serial MRAM is booted into a Wrapped Burst Mode rather than a sequential read mode. When this bit is reset to 0, the wrap mode is disabled, and the device is in a continuous read/write mode. The Wrap Around Unit is defined within the wrap length field with random initial address.

Wrap Length – After the command opcode and 3-byte address, the output data starts to wrap within an aligned 16/32/64/128/256-byte boundary at any address. The starting address of the read command selects the group of bytes and the first data returned is the addressed bytes. Bytes are then read sequentially until the end of the group boundary is reached. If the read continues the address wraps to the beginning of the group and continues to read sequentially. To exit wrap around mode, bit 4 of the Configuration Register 3 (CR3[4]) must be reset to 0. Otherwise, the wrap around progress will continue until power down or reset command or returning CS# High.

2.5 Configuration Register 4 (CR4)

The register bits can be read and changed using the Read Configuration Register 1/2/3/4 command or Write Configuration Register 1/2/3/4 command.

Table 7: Configuration Register 4

Bit	Description	Field Name	Memory Type	R/W	Factory Default State
7	Reserved	RSVD	-	R/W	0
6	Reserved	RSVD	-	R/W	0
5	Reserved	RSVD	-	R/W	0
4	Reserved	RSVD	-	R/W	0
3	Reserved	RSVD	-	R/W	0
2	Reserved	RSVD	-	R/W	1
1	Back-to-Back Write Mode 1 = Back-to-Back write mode enabled 0 = Back-to-Back write mode disabled	WRENS[1]	NV	R/W	0
0	SRAM Mode 1 = SRAM mode enabled 0 = SRAM mode disabled	WRENS[0]	NV	R/W	1

SRAM Mode – WRENS[0] bit, when set to 1, enables the Serial MRAM to operate in SRAM mode in which write commands can be executed without issuing prior WREN command. WREN bit is Don't Care. The WREN bit is required to be set to "1" prior to any write register command.

Back-to-Back Write Mode – WRENS[1] bit, when set to 1, enables the Serial MRAM to operate in a back-to-back write mode in which subsequent write commands can be executed without issuing prior WREN command. The WREN bit will not be reset to "0" on the rising edge of CS# following subsequent write commands. The WREN bit however will be automatically reset to "0" on the rising edge of CS# following any Write Register commands.

If both bit 0 and bit 1 are accidentally set to 1, then the Serial MRAM will automatically operate in the SRAM mode.

Note, Bit 2 must be set to "1". Writing a "0" to this bit may impact device functionality.

2.6 Sample Code (Arduino Platform)

The Status register should be reset first, before resetting the Configuration registers.

```
void resetStatus(void)
{
   uint8_t sr;
   Serial.print(F("Status Register Read Before Reset\r\n"));
   sr = MRAM_Status_Reg_Read();
   if(sr<=0xF)
     Serial.print(F("0x0"));
   else
     Serial.print(F("0x"));
   Serial.print(sr,HEX);
   crlf();
   MRAM_Status_Reg_Write(0x00);
   Serial.print(F("Status Register Read After Reset\r\n"));
   sr = MRAM_Status_Reg_Read();
   if(sr<=0xF)
     Serial.print(F("0x0"));
   else
     Serial.print(F("0x"));
   Serial.print(sr,HEX);
   crlf();
}
void resetConfig(void)
{
   CFGREG_T cfgreg;
   int i;

   Serial.print(F("Config Registers Read Before Reset\r\n"));
   MRAM_Config_Reg_Read(&cfgreg);
   for(i=0;i<4;i++){
      if(cfgreg.cr[i]<=0xF)
        Serial.print(F("0"));
      Serial.print(cfgreg.cr[i],HEX);
      Serial.print(F(" "));
   }
     crlf();
     cfgreg.by.cr1=0x00;
     cfgreg.by.cr2=0x00;
     if(ava3)cfgreg.by.cr3=0x60;
     else cfgreg.by.cr3=0x00;
     cfgreg.by.cr4=0x05;
     MRAM_Config_Reg_Write(&cfgreg);
     Serial.print(F("Config Registers Read After Reset\r\n"));
     MRAM_Config_Reg_Read(&cfgreg);
     for(i=0;i<4;i++){
       if(cfgreg.cr[i]<=0xF)
         Serial.print(F("0"));
       Serial.print(cfgreg.cr[i],HEX);
       Serial.print(F(" "));
   }
   crlf();
     }
```

3. Summary

Renesas Serial MRAM HP and ULP Serial P-SRAM products require all writable non-volatile bits in the status register and the configuration registers (HP Serial P-SRAM devices) to be re-initialized to factory default values upon power up after high temperature solder reflow process. This re-initialization process ensures the Renesas Serial P-SRAM powers up in a known and defined state.

4. Revision History

Revision	Date	Change Summary
REV A	10/23/2019	Initial release
REV B	11/1/2019	Changed default to CR4[0]=1
REV C	04/29/2020	Added 1.8V part numbers Added ULP part numbers Removed SPnvSRAM Added Table 2