ISL70005SEH, ISL73005SEH

iSim:PE Model vs Silicon Application Report

Abstract

The ISL70005SEH and ISL73005SEH are radiation hardened dual output Point-of-Load (POL) regulators combining the high efficiency of a synchronous buck regulator with the low noise of a Low Dropout (LDO) regulator. They are suited for systems with 3.3V or 5V power buses and can support continuous output load currents of 3A for the buck regulator and ±1A for the LDO. The buck regulator uses a voltage mode control architecture and switches at a resistor adjustable frequency of 100kHz to 1MHz. Externally adjustable loop compensation allows for an optimum balance between stability and output dynamic performance. The internal synchronous power switches are optimized for high efficiency and excellent thermal performance. The LDO is completely configurable independent of the switching regulator. It uses NMOS pass devices and separate chip bias voltage (L_VCC) to drive its gate, enabling the LDO to operate with a very low voltage at the L_VIN input. The LDO can sink and source up to 1A continuously, making it an ideal choice to power DDR memory.

The iSim:PE model for the ISL70005SEH and ISL730005SEH was developed to help system designers evaluate the operation of this IC in a simulation environment prior to or in conjunction with proto-typing a system design. This model simulates typical performance characteristics such as start-up, steady-state operation, transient operation, AC performance, and loop stability analysis at room temperature (T = 25°C).

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Related Literature

For a full list of related documents, visit our website:

- ISL70005SEH, ISL73005SEH device pages

1. License Statement

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2. Model Revision

At the date of this application report being published, the latest ISL70005SEH iSIM:PE model revision is Version 1.0 (12/30/2019). For simulation accuracy, download the latest model at the ISL70005SEH Download page.

3. Schematic File

The schematic file: **ISL70005SEH_FPGA_Bode**, **ISL70005SEH_FPG_Load-Step**, or **ISL70005SEH_DDR_Tracking** is the main application schematic that should be used in the iSim:PE simulator. The FPGA schematic is set up for a dual independent 3A Buck + 1A LDO regulator. The DDR schematic is set up for the LDO to track the Buck for DDR regulator applications. The schematic mimics the ISL70005SEHENG2Z and ISL70005SEHDEMO1Z evaluation board and is designed for 3V to 5V input voltages. The simulation profile is setup to run POP/AC or POP/Transient for load transient and Bode Plot analysis. Figure 5 through 72 show a comparison of the simulation results for specified operating conditions versus the actual bench validation data. For more information on iSim:PE visit the iSim online home page.

4. Simulation Schematic

Figure 1 is the base ISL70005SEH iSim:PE model schematic for the dual independent Buck and LDO regulator for FPGA power supplies. The DDR Tracking schematic is nearly identical, changing the LDO input voltage and reference voltage to track the Buck output voltage.

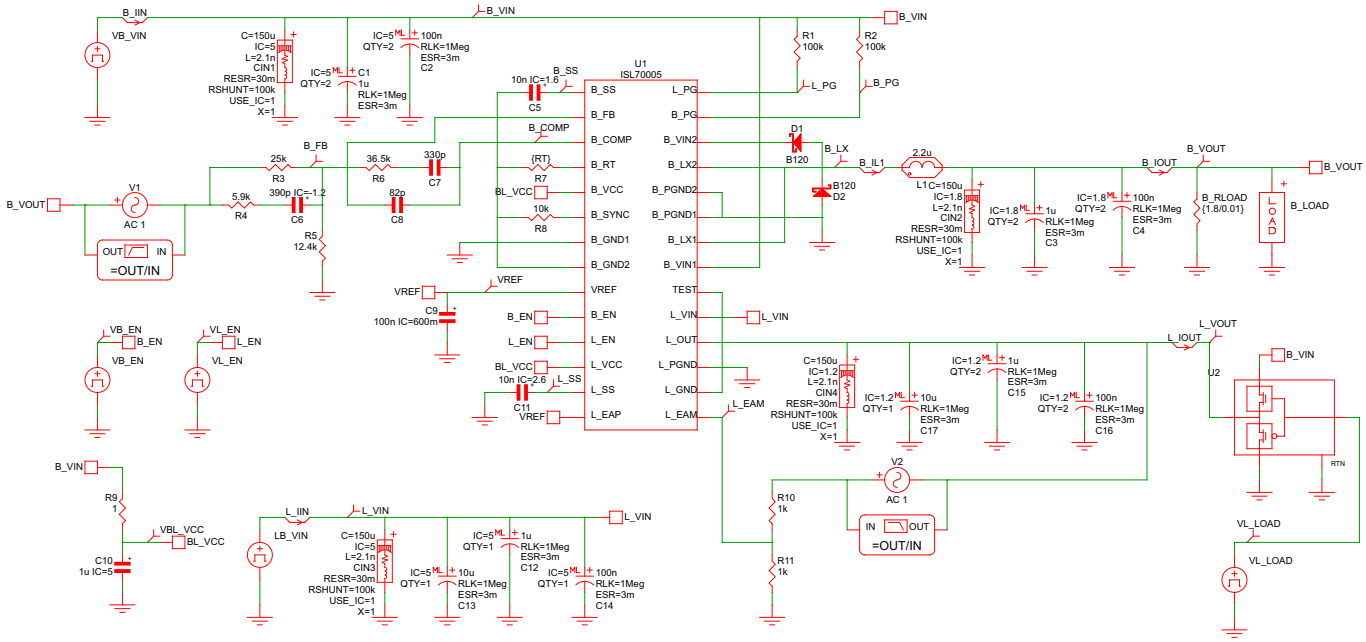

Figure 1. Base ISL70005SEH iSim:PE Model Schematic

5. Using The Model

The ISL70005SEH_FPGA_Load_Step and ISL70005SEH_FPGA_Bode have nearly identical schematics. The only difference is in the B_RLOAD and B_LOAD parameters. For a load transient analysis the B_LOAD is used to generate a transient load current with the B_RLOAD set as a high impedance. For a Bode analysis the B_RLOAD is used to generate a static load current with the B_RLOAD disabled. See Figure 2.

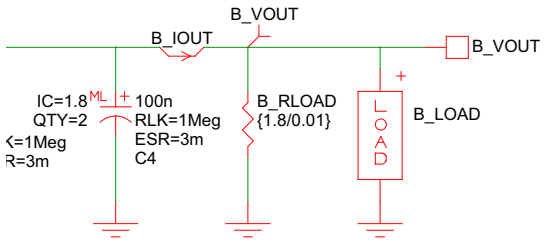

Figure 2. ISL7005SEH_FPGA Schematic Buck Output Loading

The ISL70005SEH_DDR_Tracking modifies the schematic for a DDR VDDQ and VTT rail application. In this schematic, the Buck output has a 2A transient load. The LDO output voltage tracks the Buck output voltage during this load transient. The Buck VOUT is the input to the LDO L_VIN and the LDO reference (L_EAP) is resistor divided from Buck VOUT. The LDO is set in unity gain configuration so LDO VOUT tracks the Buck VOUT at 1:2 ratio. See Figure 3.

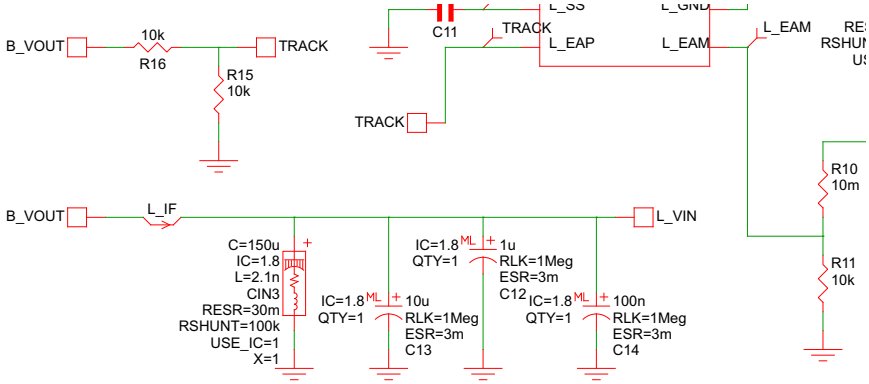

Figure 3. ISL70005SEH_DDR_Tracking Schematic

The LDO output should be loaded with a source or sink current to keep it out of the dead-band zone.

R14 is the load resistor for sourcing (connect to GND) or sinking (connect to B_VOUT) current. As B_VOUT is twice L_VOUT, the source or sink current is L_VOUT / R14. See Figure 4.

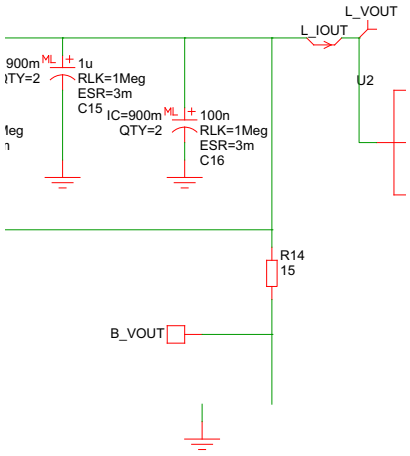

Figure 4. ISL70005SEH_DDR_Tracking Setting Source or Sink Current

6. Silicon vs Simulation Performance Curves

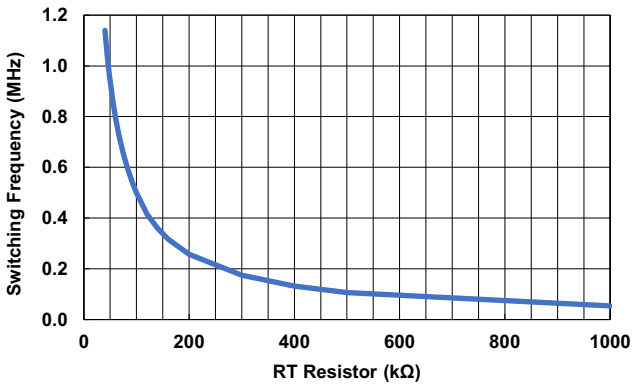

Figure 5. Buck f_{SW} vs RT Resistor (Silicon)

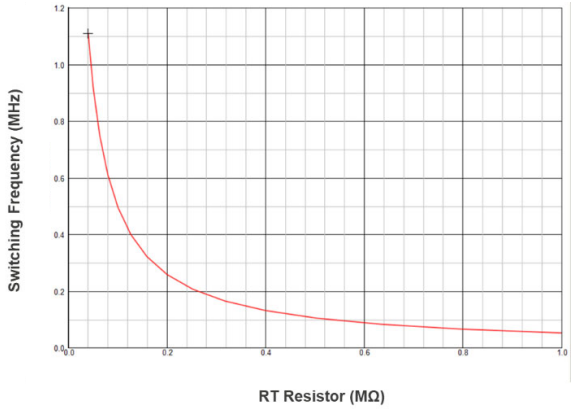

Figure 6. Buck f_{SW} vs RT Resistor (Simulation)

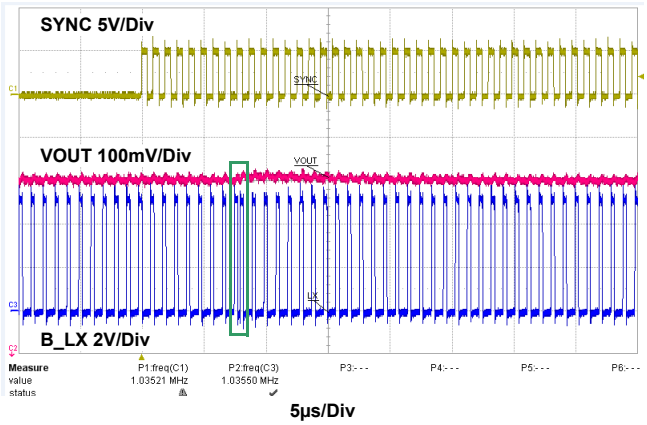

Figure 7. Buck Internal to External Synchronization After Eight External Clock Cycles (Silicon)

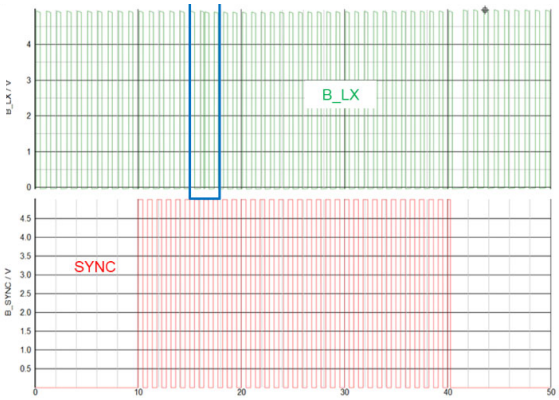

Figure 8. Buck Internal to External Synchronization After Eight External Clock Cycles (Simulation)

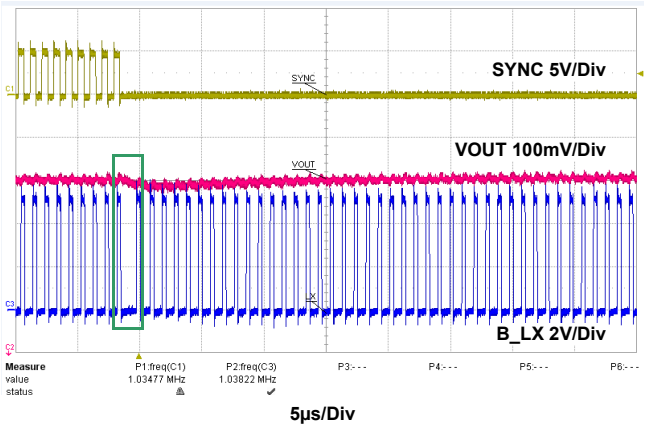

Figure 9. Buck External to Internal Synchronization After One Internal Clock Cycle (Silicon)

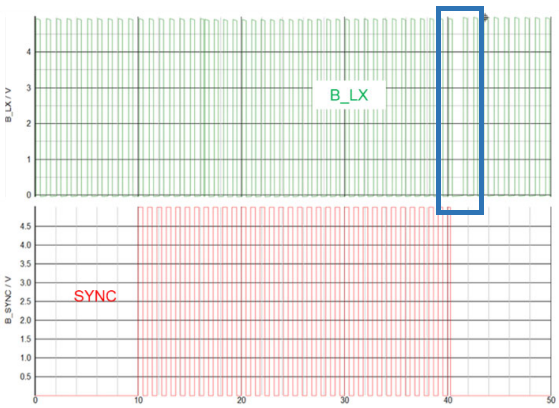

Figure 10. Buck External to Internal Synchronization After One Internal Clock Cycle (Simulation)

The iSim model increases the inductor's DCR from 21.5mΩ to 60mΩ to better match the Buck Bode plot and load transient response of the silicon. The results can be seen on Figures 12, 14, and 16.

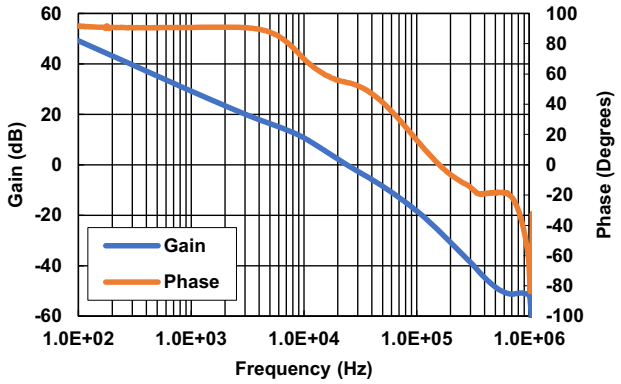

Figure 11. Buck Bode Plot; V_{IN} = 5V, V_{OUT} = 1.8V, Load = 3A, PM = 54.5°; GM = 26db; BW = 24kHz (Silicon)

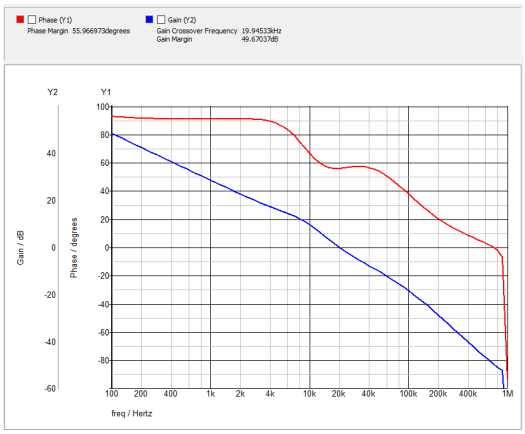

Figure 12. Buck Bode Plot; V_{IN} = 5V, V_{OUT} = 1.8V, Load = 3A, PM = 56°; GM = 49db; BW = 20kHz (Simulation)

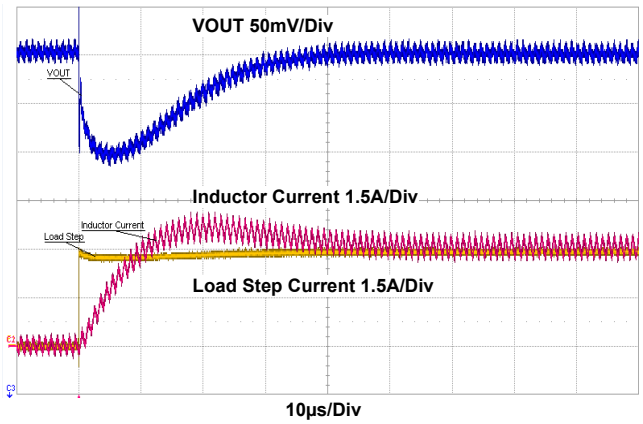

Figure 13. Buck Load Transient On; V_{OUT} = 1.8V; 3A Step (Silicon)

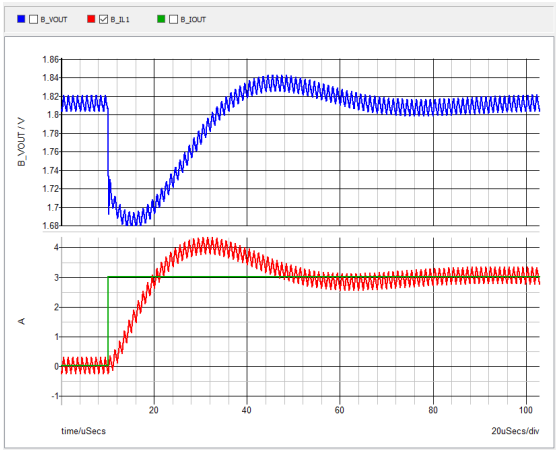

Figure 14. Buck Load Transient On; V_{OUT} = 1.8V; 3A Step (Simulation)

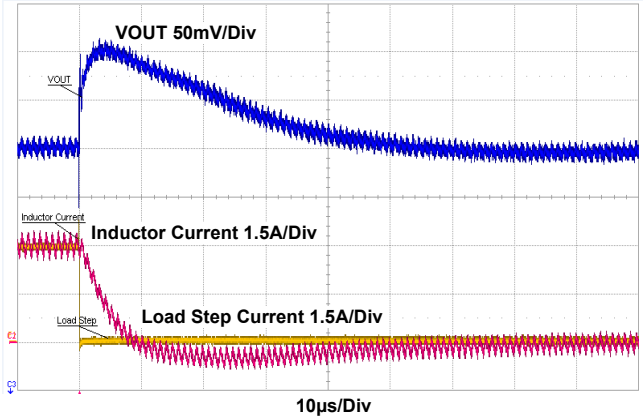

Figure 15. Buck Load Transient OFF; V_{OUT} = 1.8V; 3A Step (Silicon)

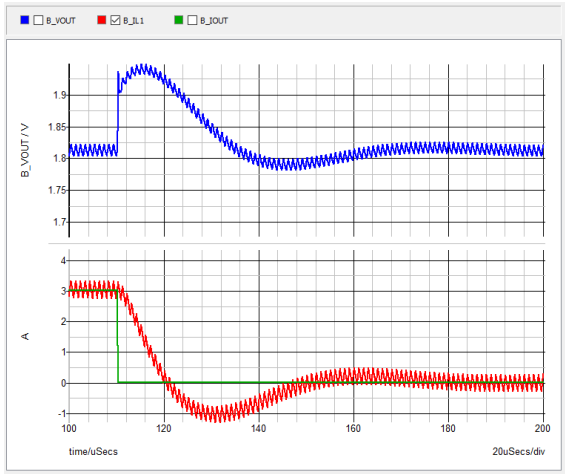

Figure 16. Buck Load Transient OFF; V_{OUT} = 1.8V; 3A Step (Simulation)

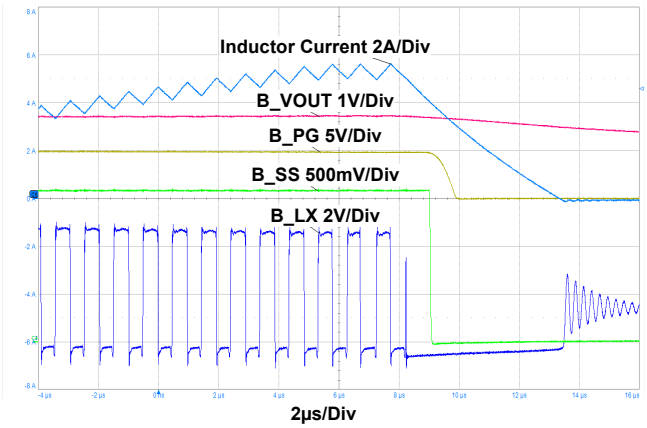

Figure 17. Buck Overcurrent Protection (Silicon)

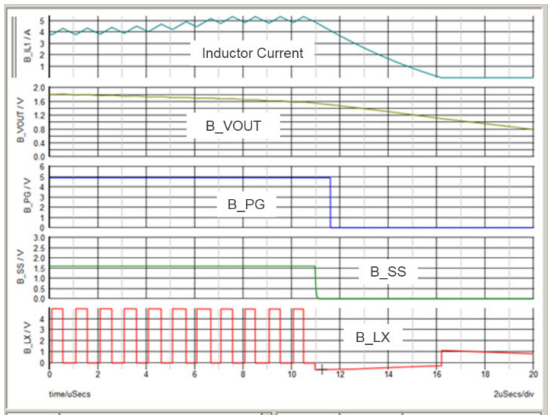

Figure 18. Buck Overcurrent Protection (Simulation)

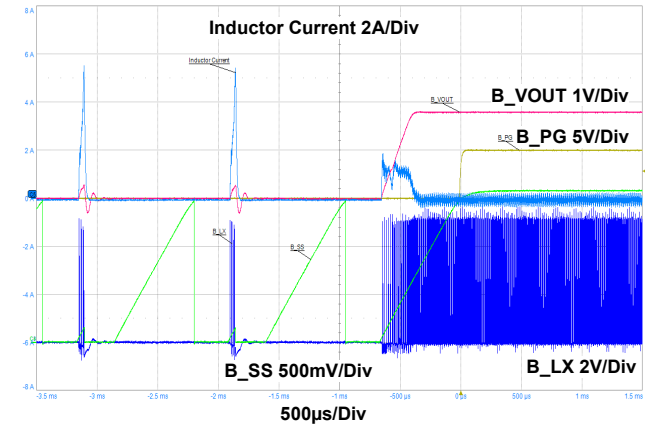

Figure 19. Buck Overcurrent Hiccup and Recovery (Silicon)

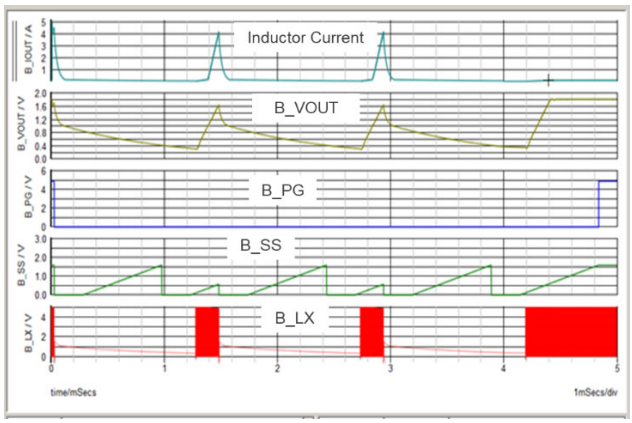

Figure 20. Buck Overcurrent Hiccup and Recovery (Simulation)

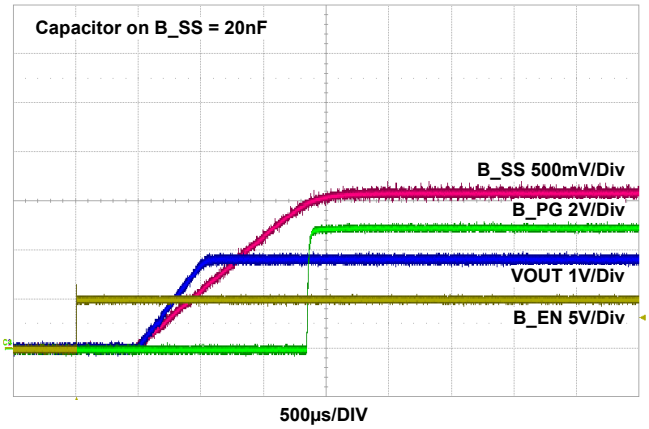

Figure 21. Buck Soft-Start; LDO Disabled; C_{SS} = 20nF (Silicon)

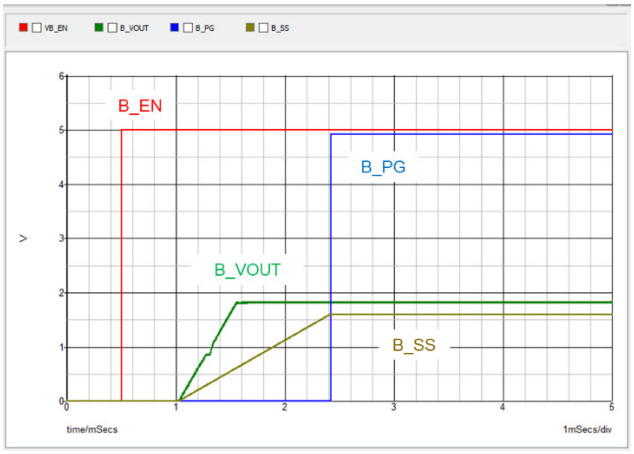

Figure 22. Buck Soft-Start; LDO Disabled; C_{SS} = 20nF (Simulation)

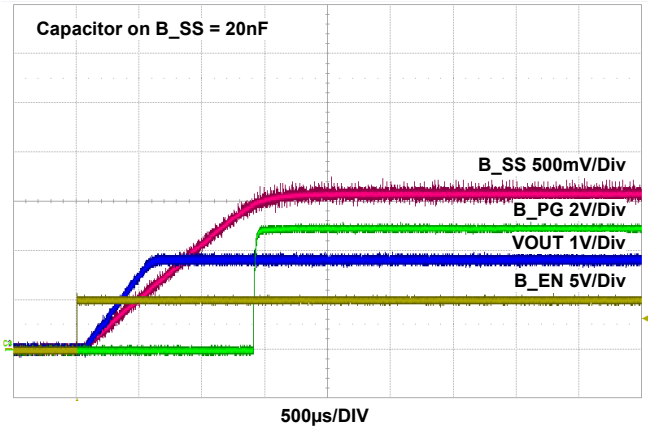

Figure 23. Buck Soft-Start; LDO Enabled; C_{SS} = 20nF (Silicon)

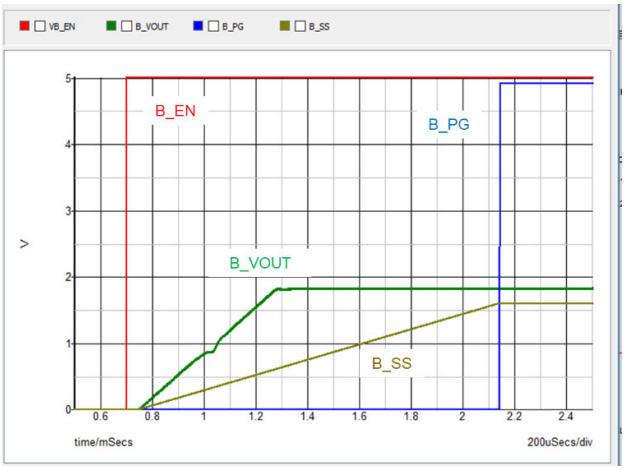

Figure 24. Buck Soft-Start; LDO Enabled; C_{SS} = 20nF (Simulation)

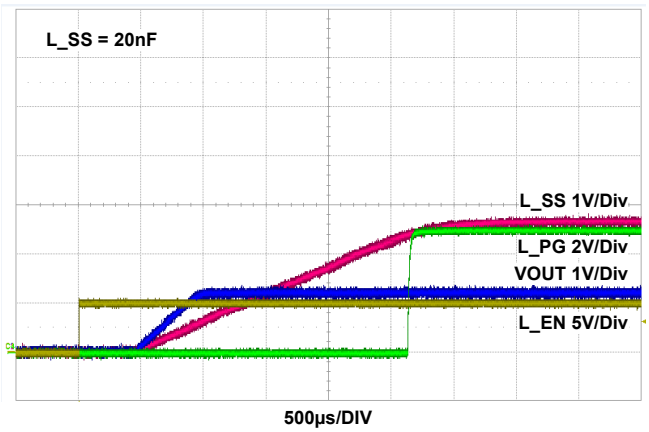

Figure 25. LDO Soft-Start; Buck Disabled; C_{SS} = 20nF (Silicon)

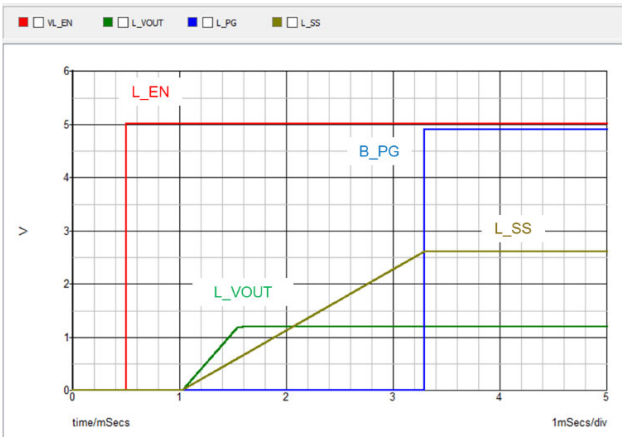

Figure 26. LDO Soft-Start; Buck Disabled; C_{SS} = 20nF (Simulation)

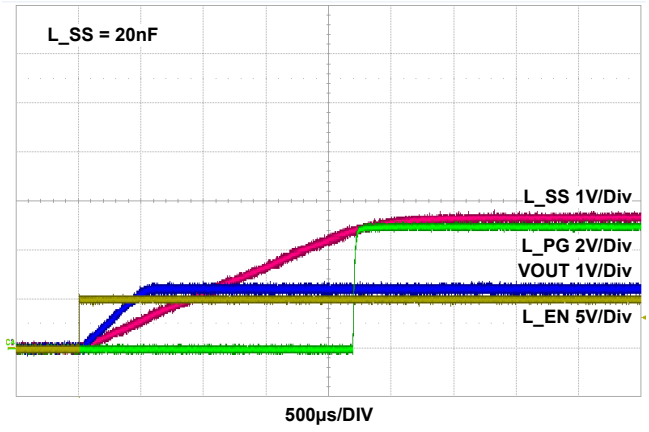

Figure 27. LDO Soft-Start; Buck Enabled; C_{SS} = 20nF (Silicon)

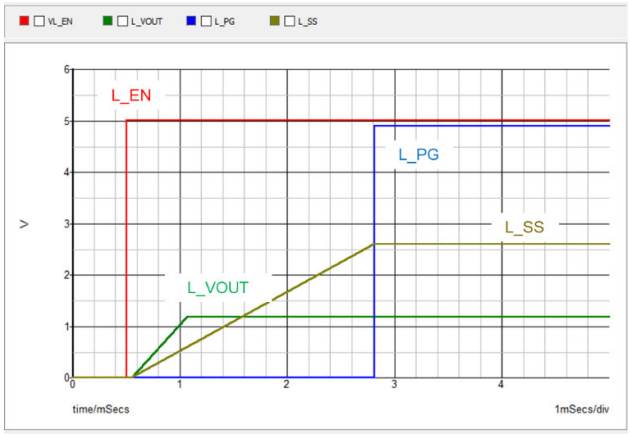

Figure 28. LDO Soft-Start; Buck Enabled; C_{SS} = 20nF (Simulation)

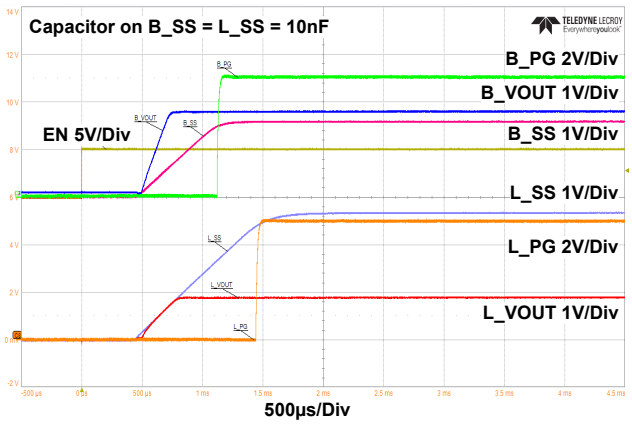

Figure 29. Soft-Start DDR Configuration; C_{SS} = 10nF (Silicon)

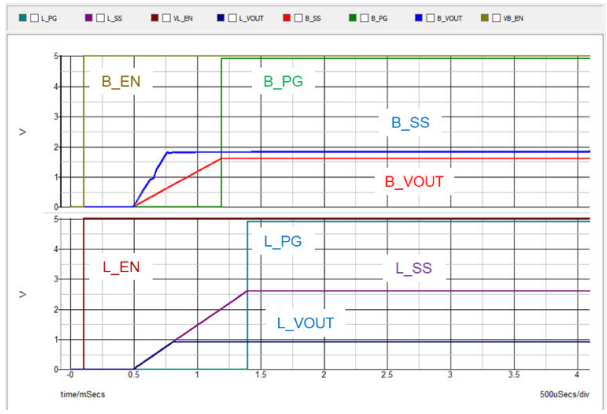

Figure 30. Soft-Start DDR Configuration; C_{SS} = 10nF (Simulation)

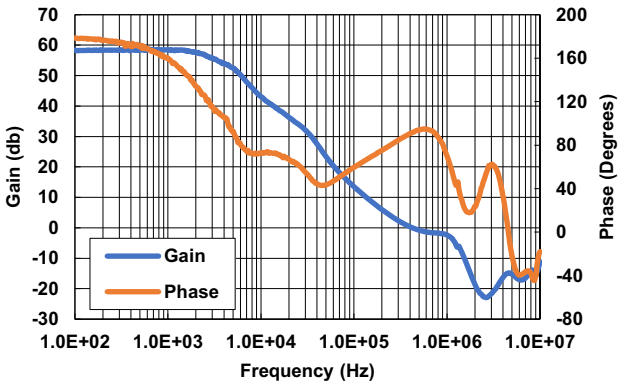

Figure 31. LDO Bode Plot; V_{OUT} = 1.2V; 1A Sourcing PM: 91 deg; GM: 14.8dB; BW: 430kHz (Silicon)

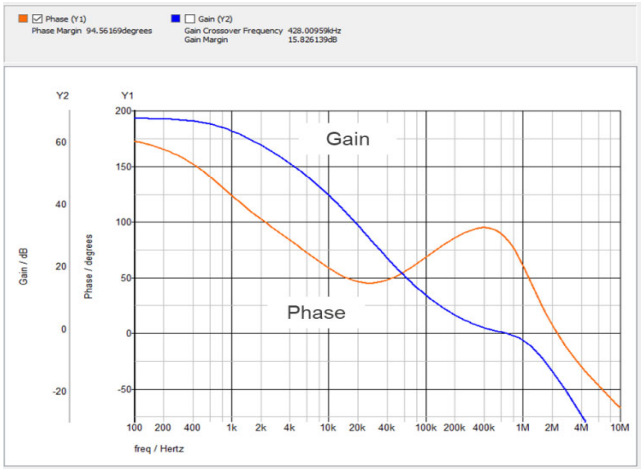

Figure 32. LDO Bode Plot; V_{OUT} = 1.2V; 1A Sourcing PM: 94.5 deg; GM: 15.8dB; BW: 428kHz (Simulation)

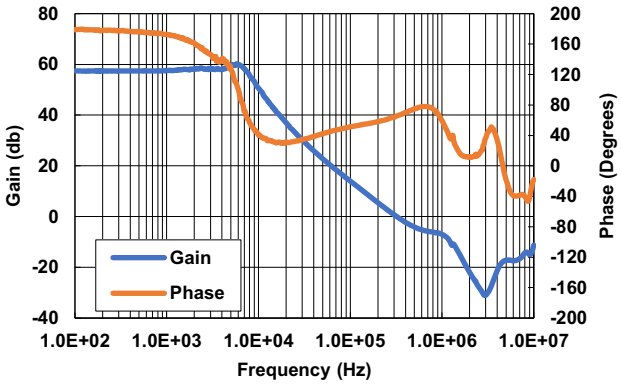

Figure 33. LDO Bode Plot; V_{OUT} = 1.2V; 1A Sinking PM: 65 deg; GM: 17.8dB; BW: 320kHz (Silicon)

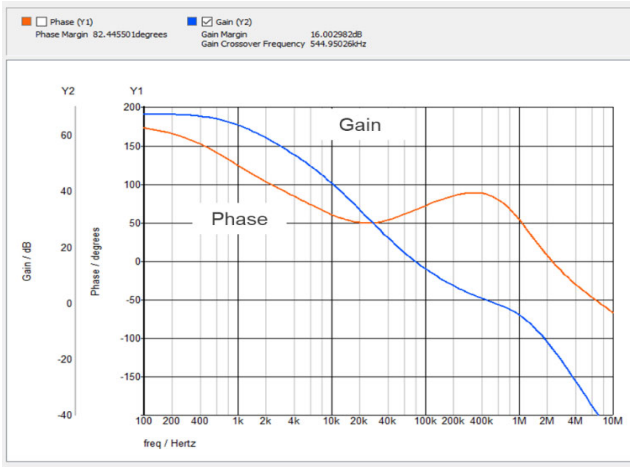

Figure 34. LDO Bode Plot; V_{OUT} = 1.2V; 1A Sinking PM: 82 deg; GM: 16dB; BW: 545kHz (Simulation)

Figures 35 and 36 show the same information. Figure 35 shows the DC operating point and Figure 36 shows a time domain sweep. Both graphs show the sourcing constant current limit of 1.65A typical.

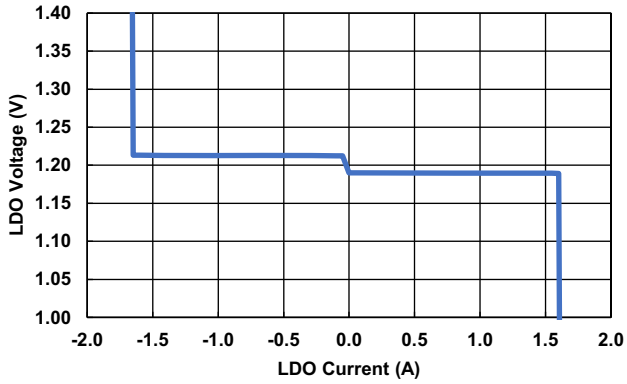

Figure 35. LDO Sourcing Constant Current Limit (Silicon)

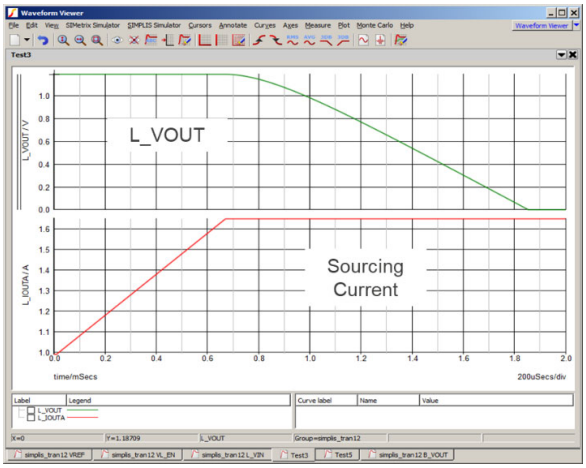

Figure 36. LDO Sourcing Constant Current Limit (Simulation)

Figures 37 and 38 show the same information. Figure 37 shows the DC operating point and Figure 38 shows a time domain sweep. Both graphs show the sinking constant current limit of 1.65A typical.

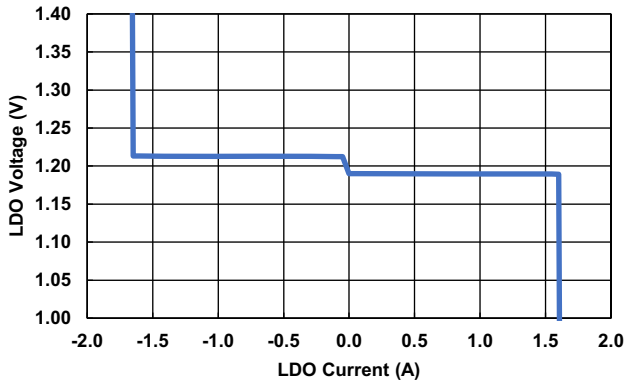

Figure 37. LDO Sinking Constant Current Limit (Silicon)

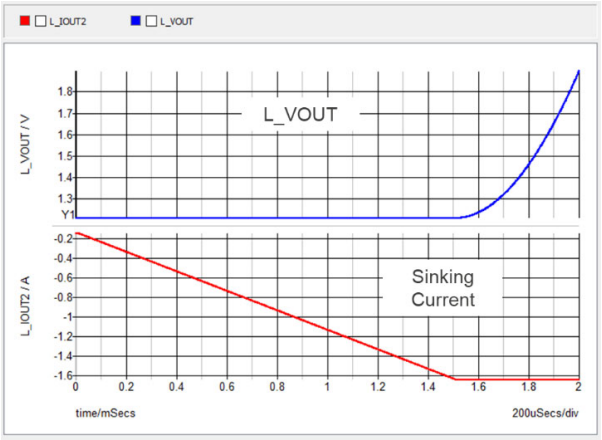

Figure 38. LDO Sinking Constant Current Limit (Simulation)

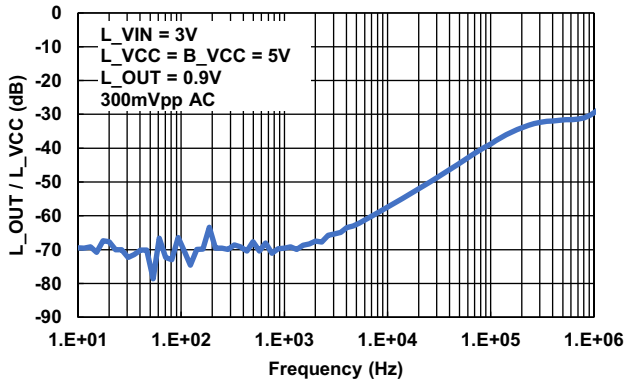

Figure 39. LDO L_VCC PSRR; 1A Sourcing (Silicon)

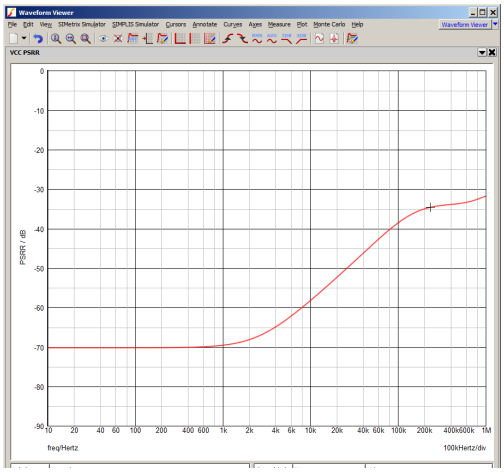

Figure 40. LDO L_VCC PSRR; 1A Sourcing (Simulation)

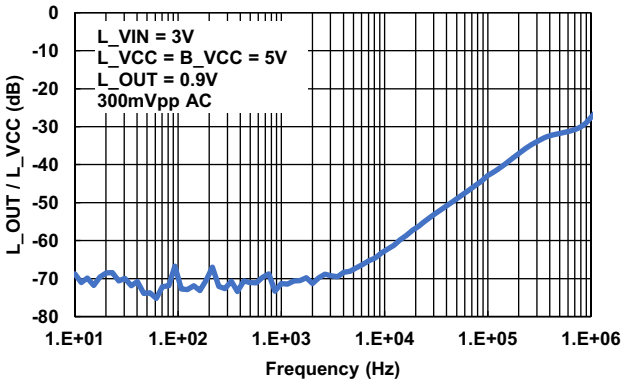

Figure 41. LDO L_VCC PSRR; 1A Sinking (Silicon)

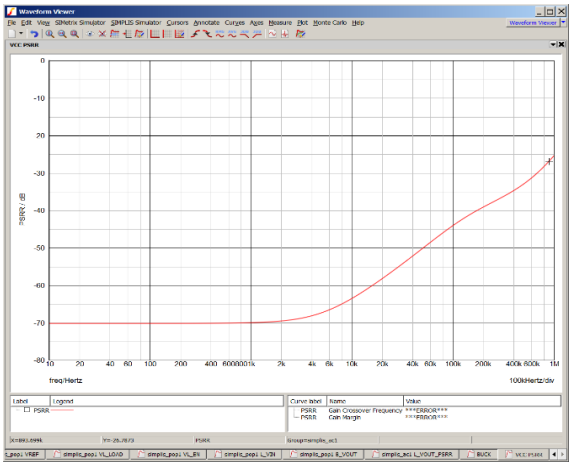

Figure 42. LDO L_VCC PSRR; 1A Sinking (Simulation)

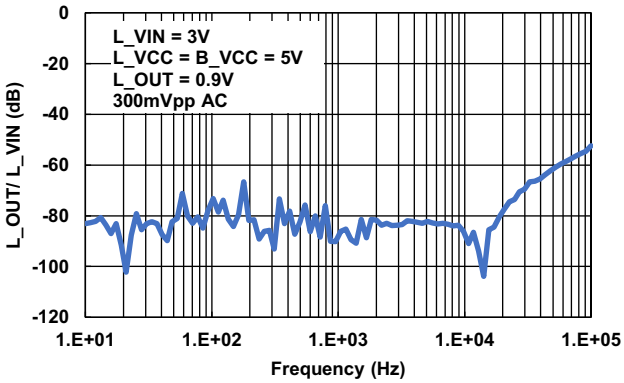

Figure 43. LDO L_VIN PSRR; 1A Sourcing (Silicon)

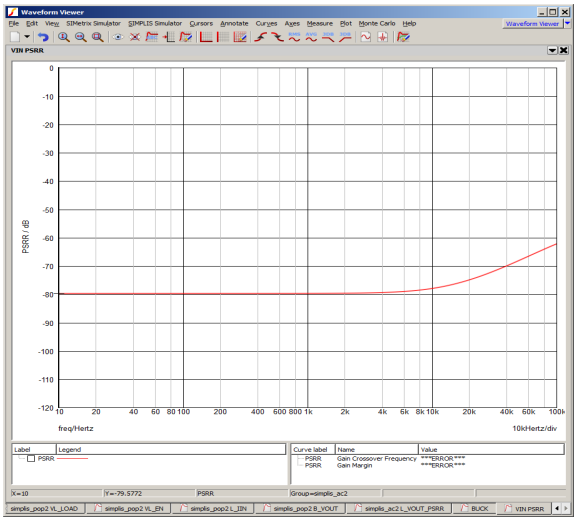

Figure 44. LDO L_VIN PSRR; 1A Sourcing (Simulation)

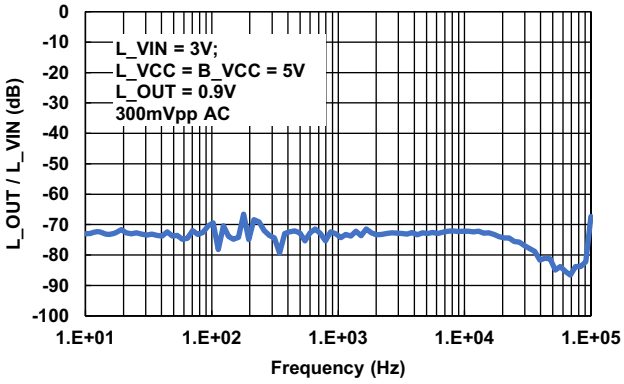

Figure 45. LDO L_VIN PSRR; 1A Sinking (Silicon)

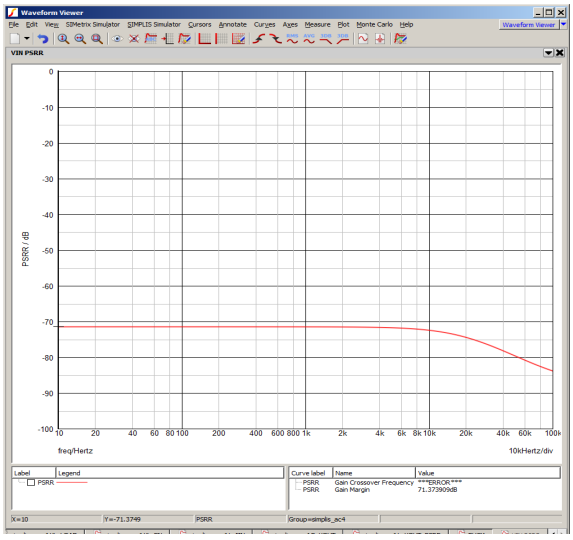

Figure 46. LDO L_VIN PSRR; 1A Sinking (Simulation)

Figures 47 and 48 show the same information. However, Figure 47 shows the DC operating point and Figure 48 shows a time domain sweep. Both graphs show the LDO L_VIN dropout voltage of approximately 80mV.

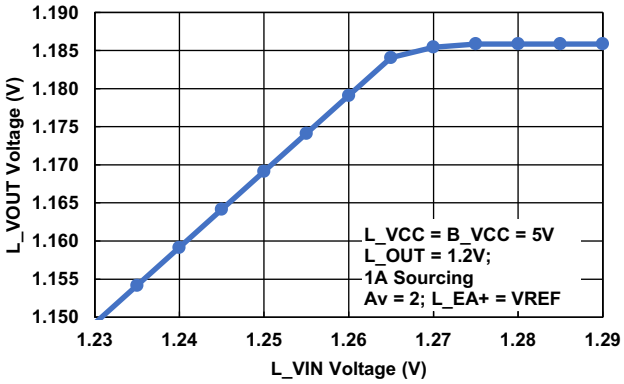

Figure 47. LDO L_VIN Dropout Voltage (Silicon)

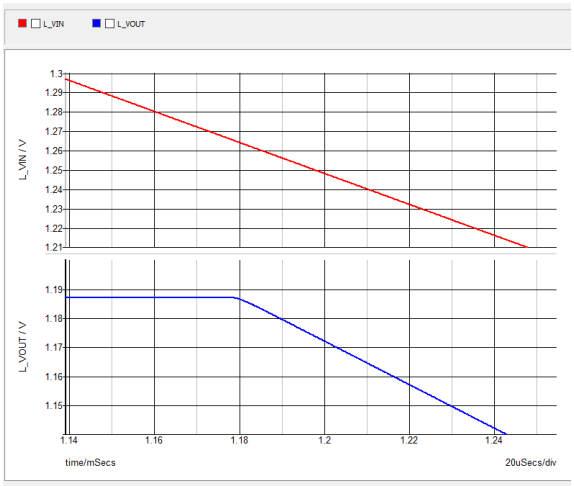

Figure 48. LDO L_VIN Dropout Voltage (Simulation)

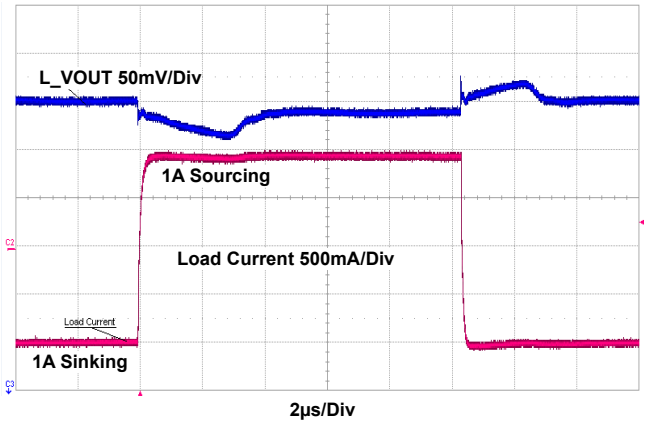

Figure 49. LDO Source-to-Sink Transient Response; L_OUT = L_EA- = L_EA+ = 0.6V (Silicon)

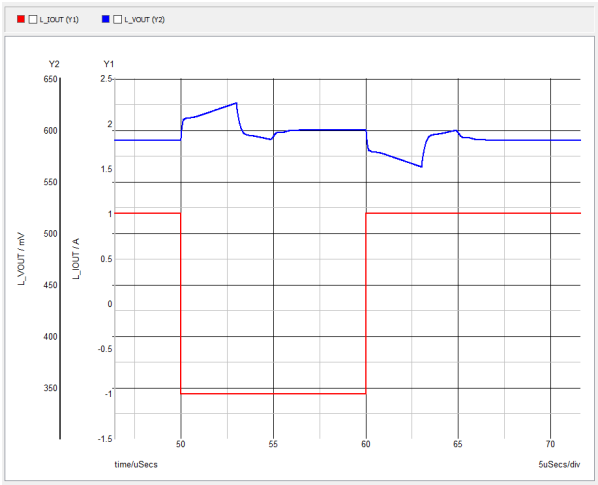

Figure 50. LDO Source-to-Sink Transient Response; L_OUT = L_EA- = L_EA+ = 0.6V (Simulation)

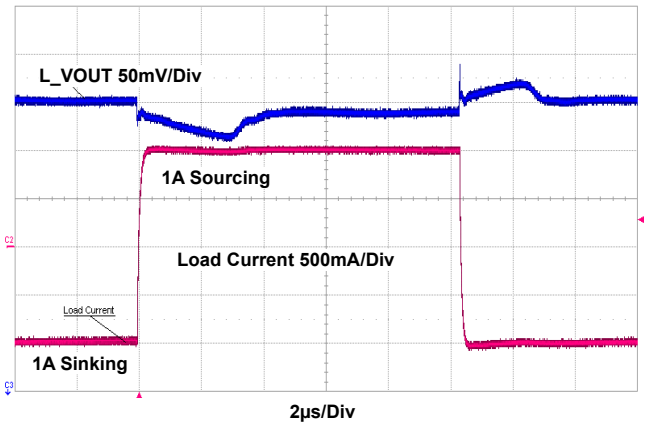

Figure 51. LDO Source-to-Sink Transient Response; L_OUT = L_EA- = L_EA+ = 0.75V (Silicon)

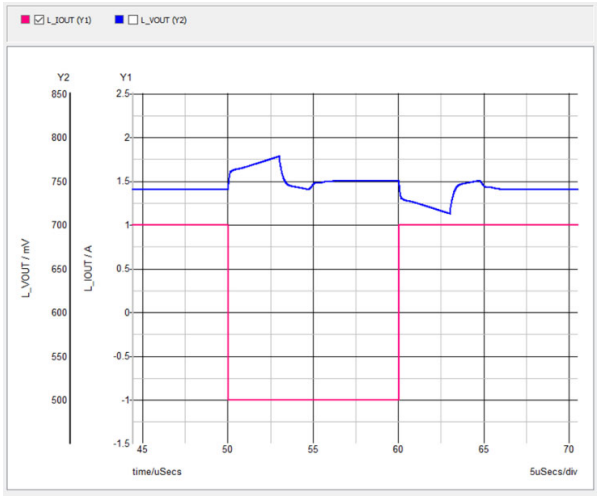

Figure 52. LDO Source-to-Sink Transient Response; L_OUT = L_EA- = L_EA+ = 0.75V (Simulation)

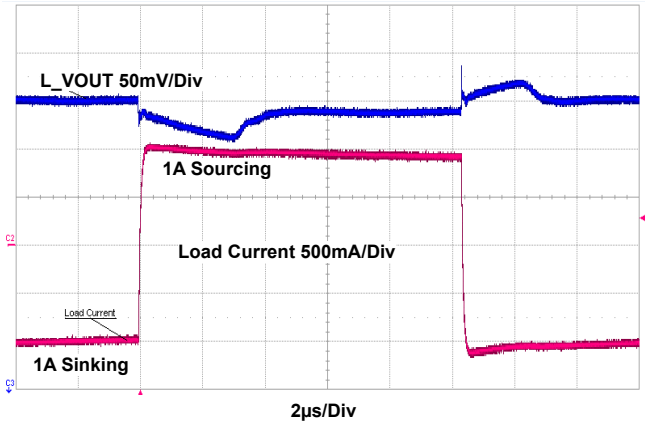

Figure 53. LDO Source-to-Sink Transient Response; L_OUT = L_EA- = L_EA+ = 0.9V (Silicon)

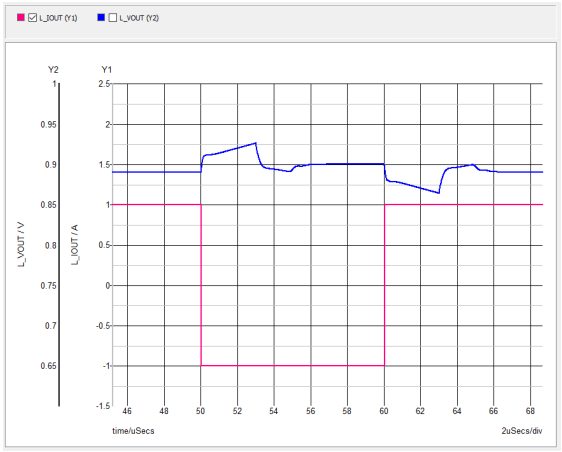

Figure 54. LDO Source-to-Sink Transient Response; L_OUT = L_EA- = L_EA+ = 0.9V (Simulation)

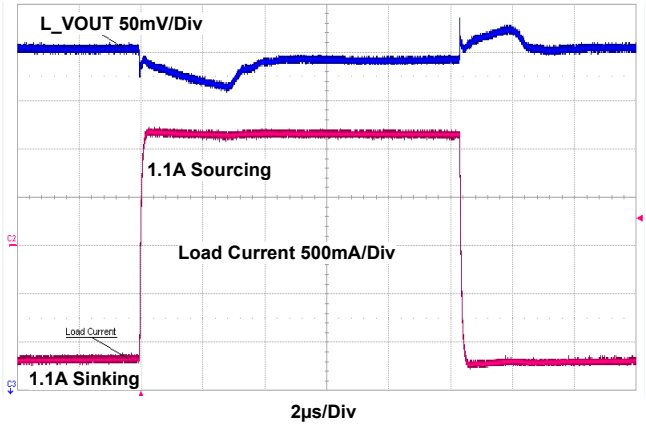

Figure 55. LDO Source-to-Sink Transient Response; L_OUT = L_EA- = L_EA+ = 1.25V (Silicon)

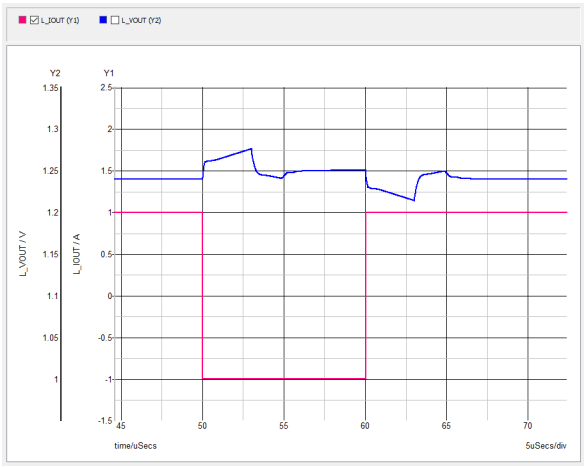

Figure 56. LDO Source-to-Sink Transient Response; L_OUT = L_EA- = L_EA+ = 1.25V (Simulation)

The noise spikes seen in the simulation result in Figures 58 and 64 are due to the model hitting the current limit during the transient that is not shown in silicon. Increasing the LDO loading current from 50mA to 200mA avoids this discrepancy between model and silicon.

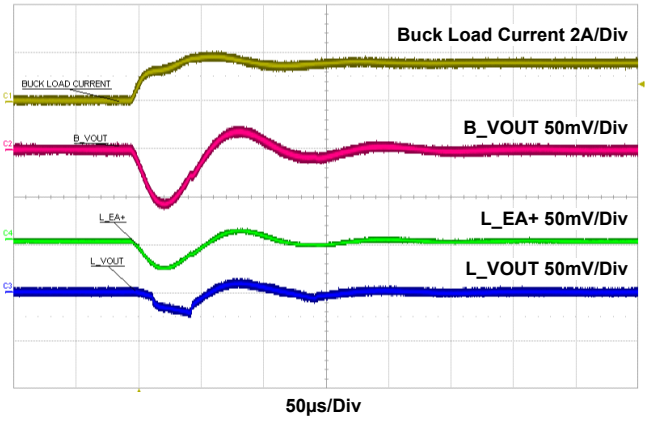

Figure 57. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.5V; LDO V_{OUT} = 0.75V; LDO Sourcing 50mA, Buck Load On (Silicon)

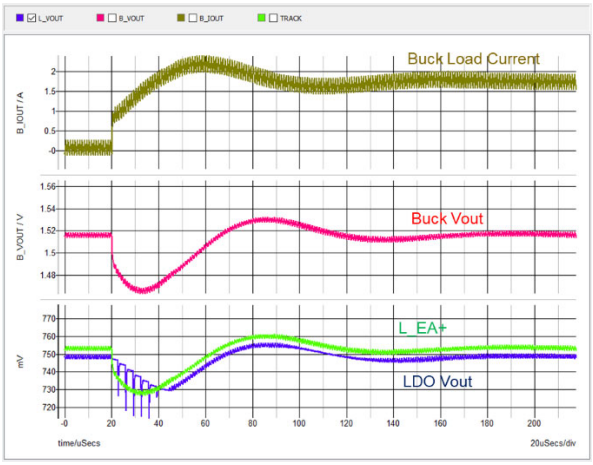

Figure 58. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.5V; LDO V_{OUT} = 0.75V; LDO Sourcing 50mA, Buck Load On (Simulation)

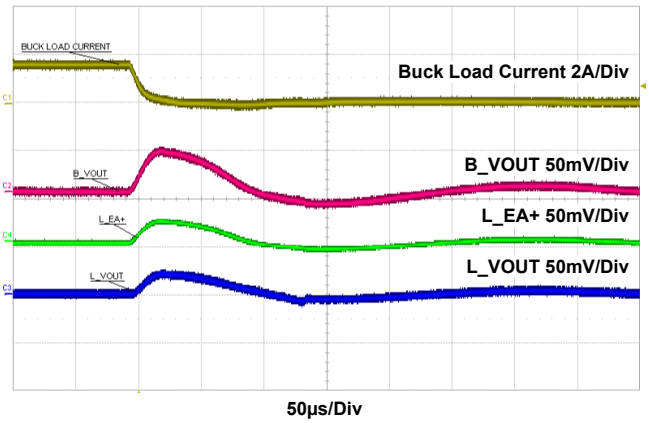

Figure 59. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.5V; LDO V_{OUT} = 0.75V; LDO Sourcing 50mA, Buck Load Off (Silicon)

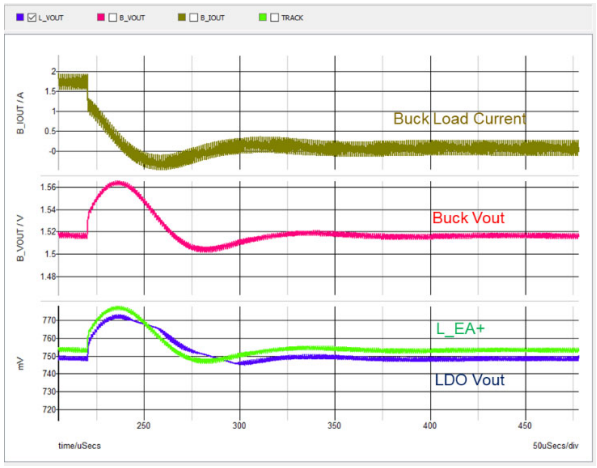

Figure 60. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.5V; LDO V_{OUT} = 0.75V; LDO Sourcing 50mA, Buck Load Off (Simulation)

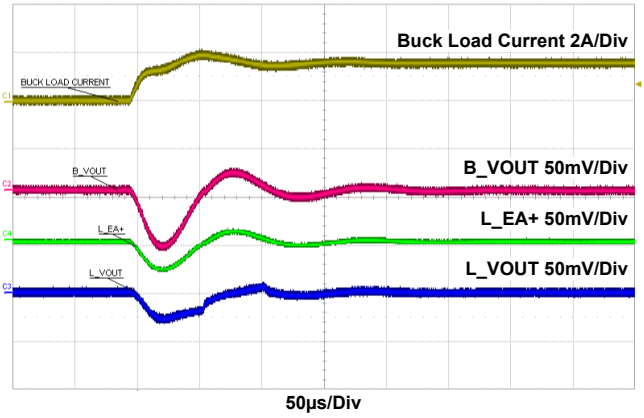

Figure 61. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.5V; LDO V_{OUT} = 0.75V; LDO Sinking 50mA, Buck Load On (Silicon)

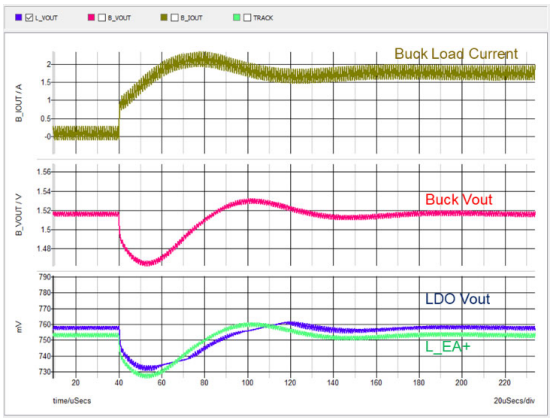

Figure 62. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.5V; LDO V_{OUT} = 0.75V; LDO Sinking 50mA, Buck Load On (Simulation)

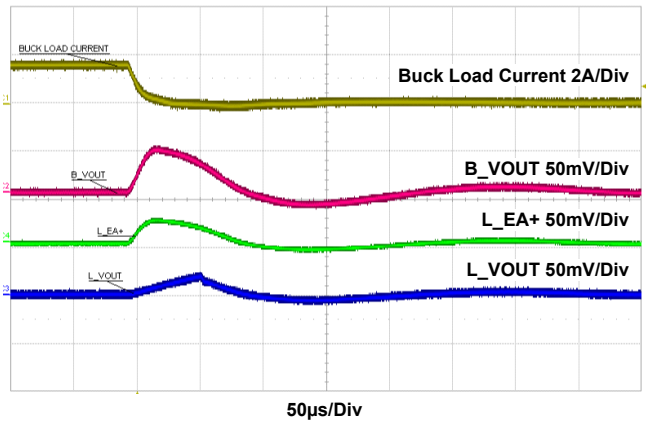

Figure 63. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.5V; LDO V_{OUT} = 0.75V; LDO Sinking 50mA, Buck Load Off (Silicon)

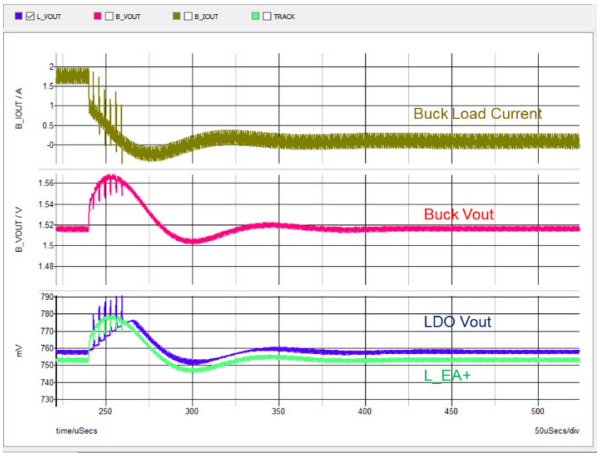

Figure 64. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.5V; LDO V_{OUT} = 0.75V; LDO Sinking 50mA, Buck Load Off (Simulation)

The noise spikes seen in the simulation result in Figures 66 and 72 are due to the model hitting the current limit during the transient that is not shown in silicon. Increasing the LDO loading current from 60mA to 240mA avoids this discrepancy between model and silicon.

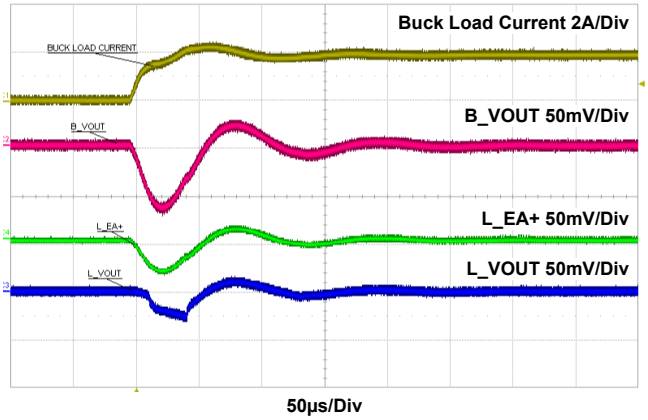

Figure 65. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.8V; LDO V_{OUT} = 0.9V; LDO Sourcing 60mA, Buck Load On (Silicon)

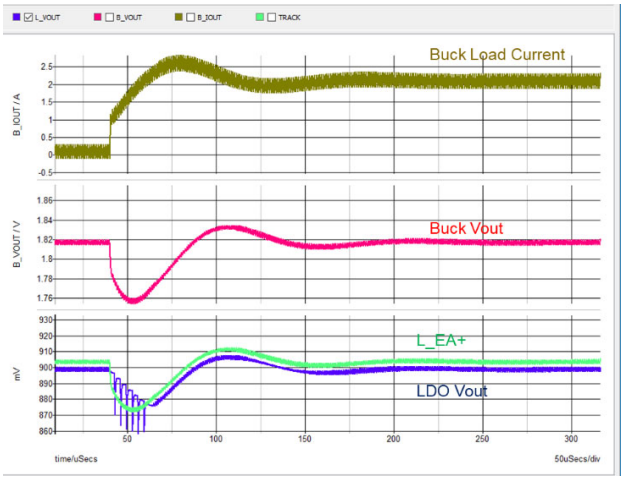

Figure 66. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.8V; LDO V_{OUT} = 0.9V; LDO Sourcing 60mA, Buck Load On (Simulation)

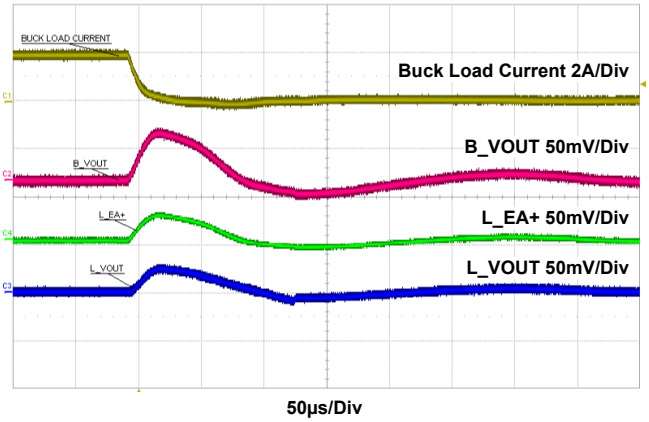

Figure 67. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.8V; LDO V_{OUT} = 0.9V; LDO Sourcing 60mA, Buck Load Off (Silicon)

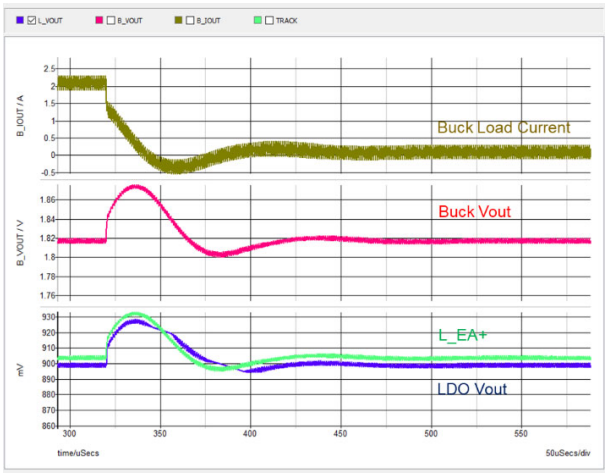

Figure 68. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.8V; LDO V_{OUT} = 0.9V; LDO Sourcing 60mA, Buck Load Off (Simulation)

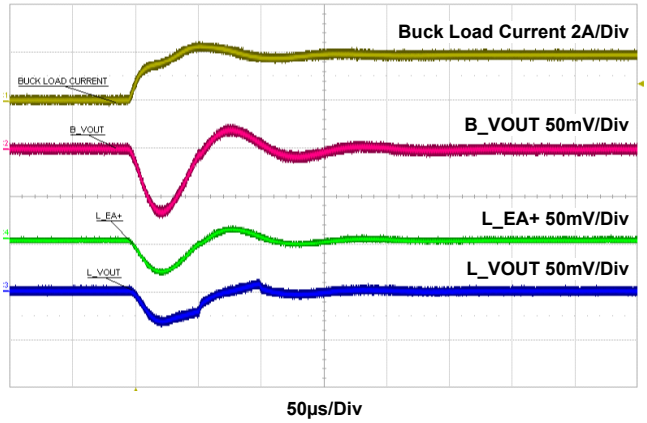

Figure 69. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.8V; LDO V_{OUT} = 0.9V; LDO Sinking 60mA, Buck Load On (Silicon)

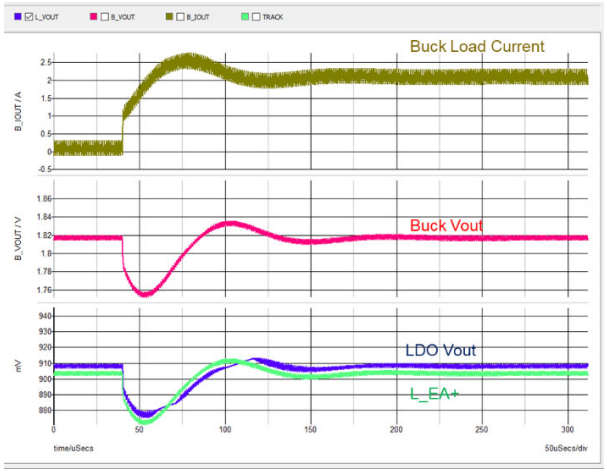

Figure 70. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.8V; LDO V_{OUT} = 0.9V; LDO Sinking 60mA, Buck Load On (Simulation)

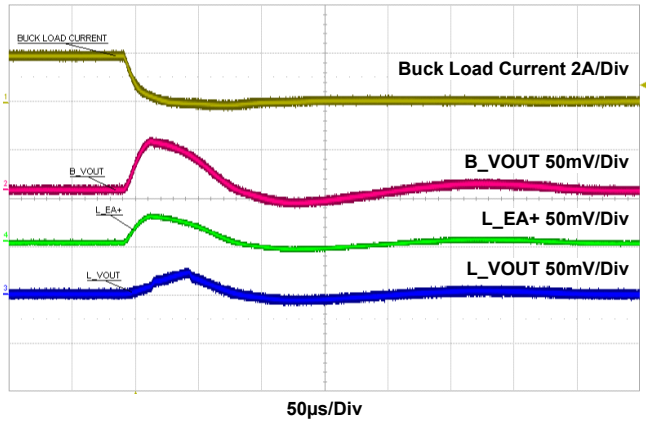

Figure 71. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.8V; LDO V_{OUT} = 0.9V; LDO Sinking 60mA, Buck Load Off (Silicon)

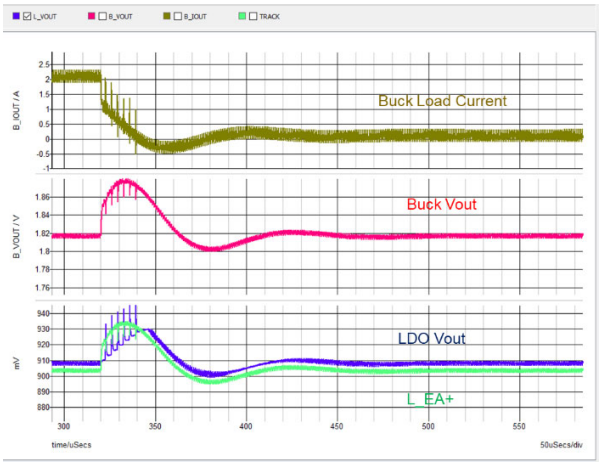

Figure 72. LDO Tracking Buck Transient Response Buck V_{OUT} = 1.8V; LDO V_{OUT} = 0.9V; LDO Sinking 60mA, Buck Load Off (Simulation)

7. Revision History

Rev.	Date	Description
1.01	Nov 4, 2022	Updated Header on page 1.
1.00	May 22, 2020	Initial release

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