

RZ/V

Release Note for RZ/V Flexible Software Package V2.0.0

Introduction

This is the release note for RZ/V Flexible Software Package V2.0.0 running on Arm® Cortex®-M33 core, Arm® Cortex®-R8 core of both RZ/V2L and RZ/V2H.

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1. Release Notes

Flexible Software Package (FSP) for Renesas RZ/V MPU version 2.0.0.

Refer to the [RZ/V Getting Started with Flexible Software Package](#) for setup instructions, hardware details, and related links.

2. Proven Environment

- [e² studio: e² studio 2024-04](#)
- [GCC Compiler: 12.2.Rel1](#)

3. Third Party Software

These third party software solutions are included alongside RZ/V2L FSP:

- [Amazon FreeRTOS Kernel: 10.4.6](#)
- [Arm CMSIS5: 5.7.0](#)
- [OpenAMP/open-amp: v2018.10](#)
- [OpenAMP/libmetal: v2018.10](#)
- [Segger J-Link: 7.96e](#)

4. Change to FSP License

The FSP license has been changed to BSD-3-Clause, allowing for more flexible use in open-source projects.

License terms (including exceptions) are available in the [LICENSE file](#).

5. Supported Components

Category	Components	Supported Devices		
		RZ/V2L	RZ/V2H (Cortex-M33)	RZ/V2H (Cortex-R8)
OS	FreeRTOS	✓	✓	✓
Middleware	OpenAMP	✓	✓	✓
	Sensor (rm_hs300x, rm_hs400x, rm_comms_i2c, rm_zmod4xxx)	✓	N/A	N/A
HAL Driver	ADC_C (r_adc_c)	✓	N/A	N/A
	ADC_E (r_adc_e)	N/A	✓	✓
	CANFD (r_canfd)	✓	✓	✓
	CMTW (r_cmtw)	N/A	✓	✓
	CRC (r_crc)	N/A	✓	✓
	DMAC_B (r_dmac_b)	✓	✓	✓
	ELC (r_elc)	N/A	✓	✓
	GPT (r_gpt)	✓	✓	✓
	GTM (r_gtm)	✓	✓	✓
	I3C_B (r_i3c_b)	N/A	✓	N/A
	INTC_IRQ (r_intc_irq)	✓	✓	✓
	INTC_NMI (r_intc_nmi)	N/A	✓	✓
	INTC_TINT (r_intc_tint)	N/A	✓	✓
	MHU (r_mhu_ns, r_mhu_s, r_mhu_ns_swint_get, r_mhu_ns_swint_set)	✓	N/A	N/A
	MHU_B (r_mhu_b_ns, r_mhu_b_s, r_mhu_b_ns_swint_get, r_mhu_b_ns_swint_set)	N/A	✓	✓
	MTU3 (r_mtu3)	✓	N/A	N/A
	PDM (r_pdm)	N/A	✓	N/A
	POEG (r_poeg)	✓	✓	✓
	I2C Master (r_riic_master)	✓	✓	✓
	I2C Slave (r_riic_slave)	N/A	✓	✓
	RSPI (r_rspi)	✓	N/A	N/A
	RTC (r_rtc)	N/A	✓	✓
	SCIF_uart (r_scif_uart)	✓	✓	✓
	SCI_B (r_sci_b_i2c, r_sci_b_uart)	N/A	✓	✓
	SPI_B (r_spi_b)	N/A	✓	✓
	TSU_B (r_tsu_b)	N/A	✓	N/A
	WDT (r_wdt)	N/A	✓	✓
xSPI_qsapi (r_xsapi_qsapi)	N/A	✓	N/A	

6. Feature Added

Support for new devices:

RZ/V2H MPU

Support for new development kits:

RZ/V2H Quad-core Vision AI MPU Evaluation Kit

The newly added modules are as follows.

Components	Related Devices		
	RZ/V2L	RZ/V2H (Cortex-M33)	RZ/V2H (Cortex-R8)
r_adc_c	✓	N/A	N/A
r_adc_e	N/A	✓	✓
r_cmtw	N/A	✓	✓
r_crc	N/A	✓	✓
r_dmac_b	✓	✓	✓
r_elc	N/A	✓	✓
r_mhu_b	N/A	✓	✓
r_mtu3	✓	N/A	N/A
r_i3c_b	N/A	✓	N/A
r_intc_nmi	N/A	✓	✓
r_intc_tint	N/A	✓	✓
r_pdm	N/A	✓	N/A
r_riic_slave	N/A	✓	✓
r_rtc	N/A	✓	✓
r_sci_b_i2c	N/A	✓	✓
r_sci_b_uart	N/A	✓	✓
r_spi_b	N/A	✓	✓
r_tsu_b	N/A	✓	N/A
r_wdt	N/A	✓	✓
r_xspi_qspi	N/A	✓	N/A

The following modules newly support DMA transfer.

- RZ/V2L:
 - r_riic_master
 - r_rsipi
 - r_scif_uart
- RZ/V2H:
 - r_riic_master
 - r_sci_b_i2c
 - r_sci_b_uart
 - r_spi_b

7. Features Modified

Components	Modified Feature	Related Devices	
		RZ/V2L	RZ/V2H
r_gpt	Supported to display an error on FSP Configurator when configuring Capture A/B Source Setting even though Capture A/B Interrupt Enable is configured is Disable.	✓	✓
r_gpt	Supported the enablement and disablement of GPT related interrupts on FSP Smart Configurator.	✓	✓
r_gtm	In RZ/V2L, GTM channel 0 is used by the main core (Cortex-A55). Therefore, FSP Configurator has been changed so that the channel cannot be selected in RZ/V2L.	✓	N/A
r_mhu	The storage format of communication data of the MHU driver has been changed to the following. From: CH0 Linux, CH0 FreeRTOS, CH1 Linux, CH1 FreeRTOS,.... To: CH0 RSP, CH0 MSG, CH1 RSP, CH1 MSG,.... The Linux side application of Multi-OS package has also been updated accordingly, so please use it in combination with Multi-OS package V2.0.0.	✓	N/A
r_poeg	Supported the enablement and disablement of POEG related interrupts on FSP Configurator.	✓	✓
r_rsipi	Supported the enablement and disablement of the function to keep SSL level on FSP Configurator.	✓	N/A

8. Features Removed

None

9. Bug Fixes

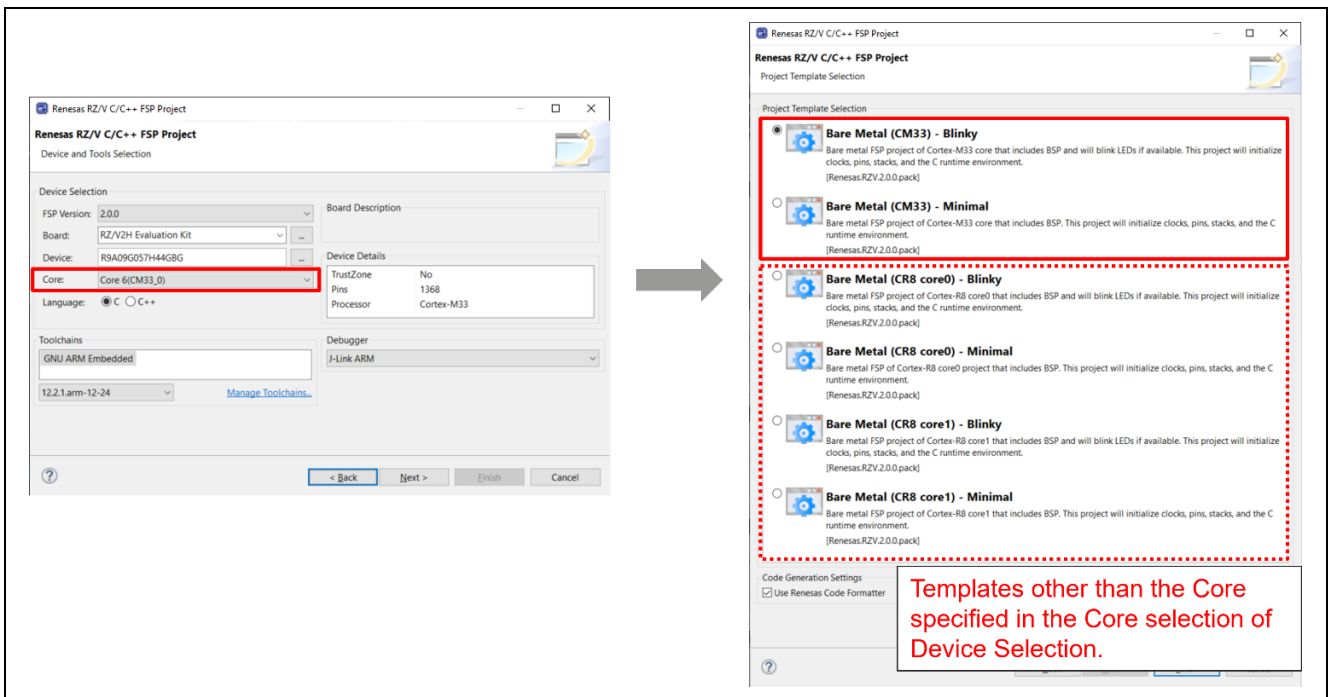
Components	Modified Feature	Related Devices	
		RZ/V2L	RZ/V2H
r_gpt	Fixed the issue that GPT counter period was NOT configured as expected when calling R_GPT_DutyCycleSet function to configure arbitrary duty ratio.	✓	✓
r_gpt, r_mhu_ns, r_mhu_s, r_mhu_ns_swint _get, r_mhu_ns_swint _set	Fixed the issue that parameter checking won't work even if it's enabled in BSP.	✓	✓
r_gtm	Changed to display an error if the wait time entered from the FSP Configurator property exceeds the upper limit of a 32-bit integer after being converted to the GTM counter register value.	✓	✓
r_rspi	Fixed the issue that the function to keep SSL level was unexpectedly enabled under slave mode.	✓	N/A
r_rspi	Changed the maximum supported bitrate to 25Mbps in accordance with the specification change of UM Rev.1.30.	✓	N/A
r_riic_master	Fixed the following issues caused by the wrong setting of WAIT bit. - When receiving by specifying 1 byte as the argument of R_RIIC_MASTER_Read function, the operation for SCL signal holding to low level could not be enabled when NACK output. - When receiving by specifying 3 or more bytes as the argument of R_RIIC_MASTER_Read function, the operation for SCL signal holding to low level was unexpectedly enabled between each reception and the next reception.	✓	✓

10. Limitations

None.

11. Known Issues

- The PDM and I3C which are dedicated component to Cortex-M33 core can be added in Cortex-R8 core project. Please do not use these components on Cortex-R8 core project.
- When creating RZ/V FSP project with selecting "RZ/V2H Evaluation Board Kit" at Board:, all the project templates can be selected at Project Template Selection regardless of the CPU core selected at Core:. For example, "Bare Metal (CR8 core 0) - Blinky", "Bare Metal (CR8 core 0) - Minimal", "Bare Metal (CR8 core 1) - Blinky" and "Bare Metal (CR8 core 1) - Minimal" are selectable even if "Core6(CM33_0)" is selected at Core: in Device Selection. Please don't select the Project Template which is NOT corresponding to the CPU core to be selected.



- On Cortex-R8 project, 16 or more can be specified for Interrupt Priority Property on FSP Smart Configurator even though the allowable value must be from 0 to 15. Thus, please don't specify 16 or more as Interrupt Priority on Cortex-R8 project.

Revision History

Rev.	Date	Description	
		Page	Summary
2.0	31.May.24	2	Added Change to FSP License section.
		3	Added Supported Components.
		4 to 7	Updated section 6, 7, 9 and 11 in accordance with the update in RZ/V FSP v2.0.0.
1.1	31.Jan.23	2	Update section 2, 4, 5 and 7 in accordance with the update in RZ/V2 FSP v1.1.0.
1.0	14.Jan.22	-	-

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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