RL78/G13

Basic Initialisation for GNURL78 v13.01 Toolchain

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Introduction

This application note describes the basic setting items that are necessary for initializing the RL78/G13.

The sample program discussed in this application note initializes the RL78/G13 and provides on/off control of three LEDs according to the combination of two switch input states.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

This application note has been updated for the RSKRL78/G13 hardware platform.

Contents

1. Installation

This application note and associated code has been written to work with GNURL78 v13.01 toolchain.

Create a new folder and name it as ‘RSKRL78G13_Workspace’. Copy the zipped file Application.zip, available in the Application Note package downloaded from the website, to this folder. Extract the Application.zip file to the RSKRL78G13_Workspace folder.

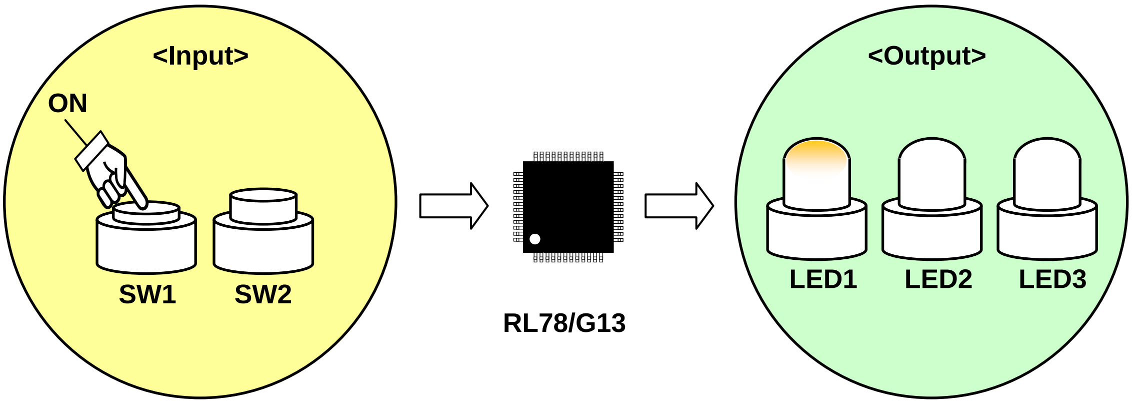
2. Specifications

The sample program described in this application note performs basic initialization steps such as the setup of the clock frequency and input/output ports. After the initialization, the program controls, in its main processing routine, the on/off of three LEDs according to the combination of two switch input states.

Table 2.1 lists the Peripheral Functions to be Used and their Uses and Figure 2.1 shows the outline of the initialization processing.

Table 2.1 Peripheral Functions to be used and their uses

Peripheral Function	Use
Port input/output	Switch input (SW1 and SW2) LED on/off control (LED1 to LED3)



Switch Input		LED Output		
SW1 (P50)	SW2 (P51)	LED1 (P53)	LED2 (P62)	LED3 (P63)
OFF	OFF	OFF	OFF	OFF
ON	OFF	ON	OFF	OFF
OFF	ON	OFF	ON	OFF
ON	ON	OFF	OFF	ON

Figure 2.1 Overview of Sample Code Operation

3. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 3.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (can run on a voltage range of 2.9 V to 5.5 V.) • LVD operation (V_{LVIH}): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environments	Renesas Electronics e^{2}studio 1.1.1.7
C compiler	GNURL78 v13.01

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used for this application note.

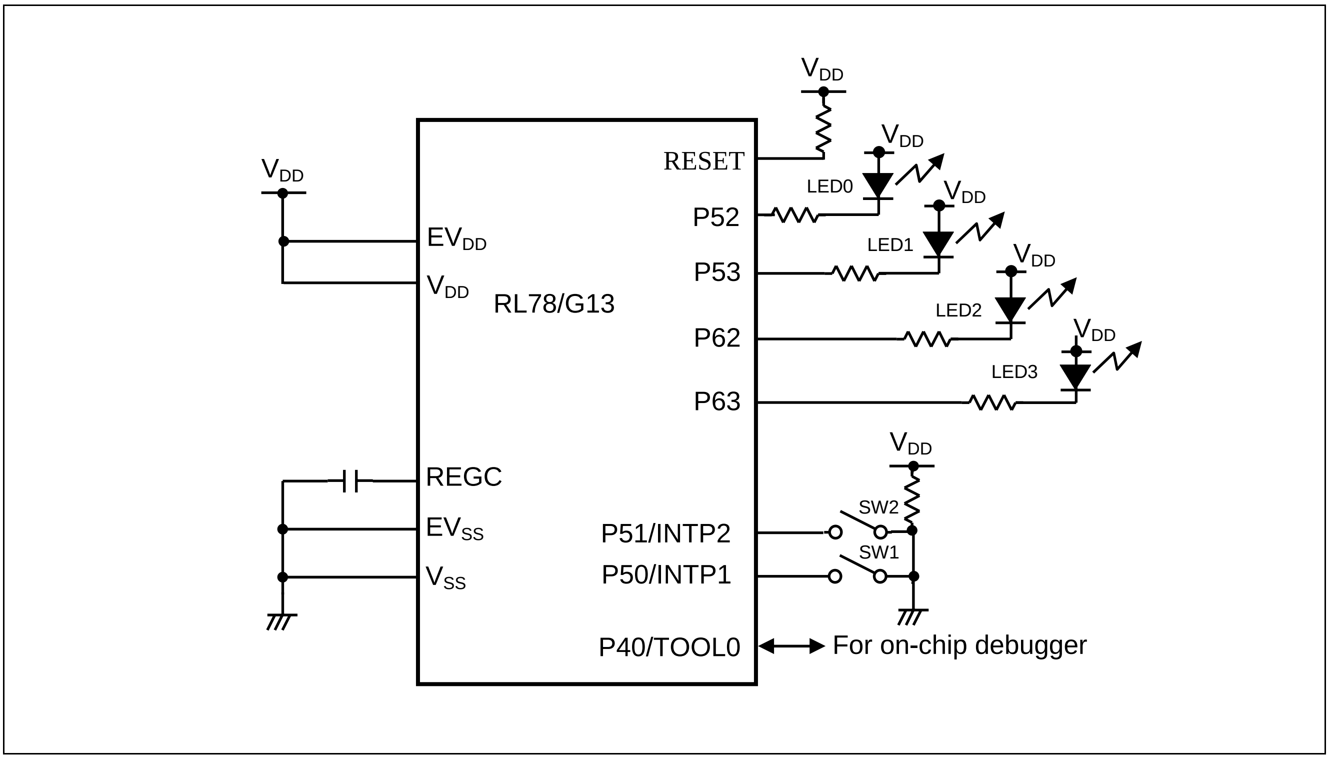


Figure 4.1 Hardware Configuration

Notes 1: The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical characteristics conditions are met (connect the input-dedicated ports separately to V_{DD} or V_{SS} via a resistor).

2: Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.

3: V_{DD} must be held at not lower than the reset release voltage (V_{LVI}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and Their Functions

Pin Name	I/O	Description
P52	Output	LED on (LED0) control port
P53	Output	LED on (LED1) control port
P62	Output	LED on (LED2) control port
P63	Output	LED on (LED3) control port
P50/INTP1	Input	Switch input (SW1) port
P51/INTP2	Input	Switch input (SW2) port

5. Description of the Software

5.1 Operation Outline

The sample program described in this application note initializes the CPU (e.g., selecting the CPU clock frequency) and sets up its I/O ports.

After completing the hardware setup, the sample program controls the on/off of three LEDs (LED1 to LED3) according to the combination of states of two switch inputs (SW1 and SW2).

(1) CPU initialization*

- Sets up the peripheral I/O redirection function.
- Sets up the I/O ports.
- Sets up the CPU clock.

Note: The option bytes are referenced before the CPU is initialized.

<Setup conditions>

- Sets the reset value because the CPU does not use the peripheral I/O redirection function (PIOR register).
- Makes the following configurations for the I/O ports:
  (1) Configures the ports that are configured for analog input after the release of the reset state for digital I/O (ADPC register and port mode control register).
  (2) Configures P50 and P51 which are to be used as switch inputs (SW1 and SW2) for input and the other ports for output (port mode register).
  (3) Connects on-chip pull-up resistors to P50 and P51 which are to be used as switch inputs (SW1 and SW2) (pull-up resistor option register).
  (4) Sets P53, P62, P63 which are to be used for on/off control of LEDs (LED1 to LED3) to 1 and the other unused pins to 0 (port register).
- Sets up the CPU clock.
  (1) Sets the reset value because the high-speed system clock and subsystem clock are not to be in use (clock operation mode control (CMC) register and clock operation status control (CSC) register).
  (2) Selects the main system clock (f_{MAIN}) as the CPU/peripheral hardware clock (f_{CLK}) and HOCO (f_{IH}) as the main system clock (f_{MAIN}) (system clock control (CKC) register).

(2) Executes the main processing.

- Performs the LED output control as summarized in Table 5.1 according to the state of the switch inputs (SW1 and SW2).

Table 5.1 Main Processing

Switch Input		LED Output		
SW1 (P50)	**SW2 (P51)**	**LED1 (P53)**	**LED2 (P62)**	**LED3 (P63)**
OFF	OFF	OFF	OFF	OFF
ON	OFF	ON	OFF	OFF
OFF	ON	OFF	ON	OFF
ON	ON	OFF	OFF	ON

Note: Refer to RL78/G13 User's Manual for notes on device use.

5.2 List of Option Byte Settings

Table 5.2 summarizes the settings of the option bytes.

Table 5.2 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Stops the watchdog timer operation. (Stops counting after the release of the reset state.)
000C1H/010C1H	01111111B	LVD reset mode 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugging function.

Option byte configuration outline

The option bytes of the RL78/G13 are made up of user option bytes (000C0H-000C2H/010C0H-010C2H[* 1 * 2 *3]) and on-chip debugging option bytes (000C3H/010C3H[* 4]).

The option bytes are automatically referenced and the pre-specified functions are set up when power is first supplied or after the release of the reset state. The option bytes cannot be set up by any user program.

The option bytes can exercise the controls listed below. They must be set up without fail before the microcomputer is to be used.

User option bytes

- Makes settings related to the watchdog timer (000C0H/010C0H[*1]).
- Makes LVD-related settings (000C1H/010C1H[*2]).
- Sets up the HOCO and flash memory (000C2H/010C2H[*3]).

On-chip debugging option bytes (000C3H/010C3H[*4])

Notes: 1. 010C0H must also set to be the same value as 000C0H because the contents of 000C0H and 010C0H are swapped at boot swap time.

2. 010C1H must also set to be the same value as 000C1H because the contents of 000C1H and 010C1H are swapped at boot swap time.

3. 010C2H must also set to be the same value as 000C2H because the contents of 000C2H and 010C2H are swapped at boot swap time.

4. 010C3H must also set to be the same value as000C3H because the contents of 000C3H and 010C3H are swapped at boot swap time.

The option bytes can be specified in vector_table.c.

5.2.1 000C0H / 010C0H* (watchdog timer related settings)

7	6	5	4	3	2	1	0
WDTINT	WINDOW1	WINDOW0	WDTON	WDCS2	WDCS1	WDCS0	WDSTBON
0	**1**	**1**	**0**	**1**	**1**	**1**	**0**

Bit 0

WDSTBYON	Control of watchdog timer counter
0	**Disables counter operation in HALT/STOP mode.**
1	Enables counter operation in HALT/STOP mode.

Bits 3 to 1

WDCS2-0	Watchdog timer overflow time
000	$2^{6}/f_{IL}$
001	$2^{7}/f_{IL}$
010	$2^{8}/f_{IL}$
011	$2^{9}/f_{IL}$
100	$2^{11}/f_{IL}$
101	$2^{13}f_{IL}$
110	$2^{14}/f_{IL}$
111	$\mathbf{2^{16}/f_{IL}}$

Bit 4

WDTON	Control of watchdog timer counter
0	**Disables counter operation.** **(Stops counter after the release of reset sequence.)**
1	Enables counter operation. (Starts counter after the release of reset sequence.)

Bits 6 to 5

WINDOW1 WINDOW0	Watchdog timer window open period
00	Setting prohibited
01	50%
10	75%
11	**100**%

Bit 7

WDTINT	Use of interval interrupts
0	**Interval interrupt is not used.**
1	An interval interrupt is generated when 75% is reached.

Note: 010C0H must also set to be the same value as 000C0H because the contents of 000C0H and 010C0H are swapped at boot swap time.

5.2.2 000C1H / 010C1H* (LVD-related settings)

7	6	5	4	3	2	1	0
VPOC2	VPOC1	VPOC0	1	LVIS1	LVIS0	LVIMDS1	LVIMDS0
0	1	1	1	1	1	1	1

When use as interrupt & reset mode

Detection Voltage			Option Byte Setting Value						
V_{LVIH}		V_{LVIL}	LVIMDS1	LVIMDS0	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge	Falling edge							
1.77 V	1.73 V	1.63 V	1	0	0	0	0	1	0
1.88 V	1.84 V							0	1
2.92 V	2.86 V							0	0
1.98 V	1.94 V	1.84 V			0	0	1	1	0
2.09 V	2.04 V							0	1
3.13 V	3.06 V							0	0
2.61 V	2.55 V	2.45 V			0	1	0	1	0
2.71 V	2.65 V							0	1
3.75 V	3.67 V							0	0
2.92 V	2.86 V	2.75 V			0	1	1	1	0
3.02 V	2.96 V							0	1
4.06 V	3.98 V							0	0
Other than above			Setting prohibited						

When used as reset mode

Detection Voltage		Option Byte Setting Value						
V_{LVIH}	V_{LVIL}	LVIMDS1	LVIMDS0	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge							
1.67 V	1.63 V	**1**	**1**	0	0	0	1	1
1.77 V	1.73 V			0	0	0	1	0
1.88 V	1.84 V			0	0	1	1	1
1.98 V	1.94 V			0	0	1	1	0
2.09 V	2.04 V			0	0	1	0	1
2.50 V	2.45 V			0	1	0	1	1
2.61 V	2.55 V			0	1	0	1	0
2.71 V	2.65 V			0	1	0	0	1
2.81 V	**2.75 V**			**0**	**1**	**1**	**1**	**1**
2.92 V	2.86 V			0	1	1	1	0
3.02 V	2.96 V			0	1	1	0	1
3.13 V	3.06 V			0	0	1	0	0
3.75 V	3.67 V			0	1	0	0	0
4.06 V	3.98 V			0	1	1	0	0
Other than above		Setting prohibited						

Note: 010C1H must also set to be the same value as 000C1H because the contents of 000C1H and 010C1H are swapped at boot swap time.

When used as interrupt mode

Detection Voltage		Option Byte Setting Value						
V_{LVIH}	V_{LVIL}	LVIMDS1	LVIMDS0	VPOC2	VPOC1	VPOC0	LVIS1	LVIS0
Rising edge	Falling edge							
1.67 V	1.63 V	1	1	0	0	0	1	1
1.77 V	1.73 V			0	0	0	1	0
1.88 V	1.84 V			0	0	1	1	1
1.98 V	1.94 V			0	0	1	1	0
2.09 V	2.04 V			0	0	1	0	1
2.50 V	2.45 V			0	1	0	1	1
2.61 V	2.55 V			0	1	0	1	0
2.71 V	2.65 V			0	1	0	0	1
2.81 V	2.75 V			0	1	1	1	1
2.92 V	2.86 V			0	1	1	1	0
3.02 V	2.96 V			0	1	1	0	1
3.13 V	3.06 V			0	0	1	0	0
3.75 V	3.67 V			0	1	0	0	0
4.06 V	3.98 V			0	1	1	0	0
Other than above		Setting prohibited						

When LVD is off

Detection Voltage		**Option Byte Setting Value**						
V_{LVIH}	**V_{LVIL}**	**LVIMDS1**	**LVIMDS0**	**VPOC2**	**VPOC1**	**VPOC0**	**LVIS1**	**LVIS0**
Rising edge	**Falling edge**							
—	—	0/1	1	1	×	×	×	×
Other than above		Setting prohibited						

Remarks: × = don’t care

5.2.3 000C2H / 010C2H* (HOCO and flash memory operation settings)

7	6	5	4	3	2	1	0
CMODE1	CMODE0	1	0	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0
1	**1**	**1**	**0**	**1**	**0**	**0**	**0**

Bits 7 and 6

CMODE1	CMODE0	Setting of Flash Memory Operating Mode		
			Operating Frequency Range	Operating Voltage Range
0	0	LV (low voltage main) mode	1 MHz to 4 MHz	1.6 V to 5.5 V
1	0	LS (low speed main) mode	1 MHz to 8 MHz	1.8 V to 5.5 V
1	**1**	**HS (high speed main) mode**	1 MHz to 16 MHz	2.4 V to 5.5 V
			1 MHz to 32 MHz	**2.7 V** to **5.5 V**
Other than above		Setting prohibited		

Bits 3 to 0

FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0	HOCO Frequency
1	**0**	**0**	**0**	**32 MHz**
0	0	0	0	24 MHz
1	0	0	1	16 MHz
0	0	0	1	12 MHz
1	0	1	0	8 MHz
1	0	1	1	4 MHz
1	1	0	1	1 MHz
Other than above				Setting prohibited

Note: 010C2H must also set to be the same value as 000C2H because the contents of 000C2H and 010C2H are swapped at boot swap time.

5.2.4 000C3H / 010C3H* (On-chip debugging option bytes)

7	6	5	4	3	2	1	0
OCDENSET	0	0	0	0	1	0	OCDERSD
1	**0**	**0**	**0**	**0**	**1**	**0**	**1**

Bits 7 and 0

OCDENSET	OCDERSD	Control of On-chip Debugging Operation
0	0	Disables on-chip debugging.
0	1	Setting prohibited
1	0	Enables operation and erases flash memory data when authentication of security ID fails.
1	**1**	**Enables operation but does not erase flash memory data when authentication of security ID fails.**

Note: 010C3H must also set to be the same value as 000C3H because the contents of 000C3H and 010C3H are swapped at boot swap time.

5.3 List of Functions

Table 5.3 lists the functions that are used by this sample program.

Table 5.3 Functions

Function Name	Outline
__low_level_init()	Initializes the hardware settings.
R_Systeminit	Calls the hardware initialization functions.
R_PORT_Create	Initializes the I/O ports.
R_CGC_Create	Initializes the clock generator.
main	Main function

5.4 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] __low_level_init

Synopsis	Initialize hardware settings.
Header	r_cg_macrodriver.h r_cg_cgc.h r_cg_port.h r_cg_userdefine.h
Declaration	int __low_level_init (void)
Explanation	Performs the following operations: (1) Executes the DI instruction. (2) Executes the function R_Systeminit(). (3) Executes the EI instruction.
Arguments	None
Return value	1
Remarks	This function is called by the startup routine.

[Function Name] R_Systeminit

Synopsis	Call hardware initialization functions.
Header	r_cg_macrodriver.h r_cg_cgc.h r_cg_port.h r_cg_userdefine.h
Declaration	void R_Systeminit(void)
Explanation	Performs the following operations: (1) Sets the initial value of the peripheral I/O redirection register (PIOR). (2) Executes the function R_PORT_Create(). (3) Executes the function R_CGC_Create(). (4) Sets the initial value of the flash memory CRC control register (CRC0CTL). (5) Sets the initial value of the invalid memory access detection control register (IAWCTL).
Arguments	None
Return value	None
Remarks	

[Function Name] R_PORT_Create

Synopsis	Initialize I/O ports.
Header	r_cg_macrodriver.h r_cg_port.h r_cg_userdefine.h
Declaration	void R_PORT_Create(void)
Explanation	Configures P50 and P51 for input (enabling the on-chip pull-up resistor) and P53, P62, and P63 for output (high-level output). Configures the other ports except pin P40 for output (low-level output).
Arguments	None
Return value	None
Remarks	

[Function Name] R_CGC_Create

Synopsis Initialize the clock generator.

Header r_cg_macrodriver.h
r_cg_cgc.h
r_cg_userdefine.h

Declaration void R_CGC_Create(void)

Explanation Initializes the registers related to the clock generator.

Arguments None

Return value None

Remarks

[Function Name] main

Synopsis Main function

Header r_cg_macrodriver.h
r_cg_cgc.h
r_cg_port.h
r_cg_userdefine.h

Declaration void main(void)

Explanation main function of the C language

Places the following outputs on the LEDs according to the values of SW1 (P50) and SW2 (P51):

SW2:SW1	: LED Binary Value
0:0	: 0b00000011
0:1	: 0b00000101
1:0	: 0b00000110
1:1	: 0b00000111

Arguments None

Return value None

Remarks

5.5 Flowcharts

Shown below is the overall flow of the sample program described in this application note.

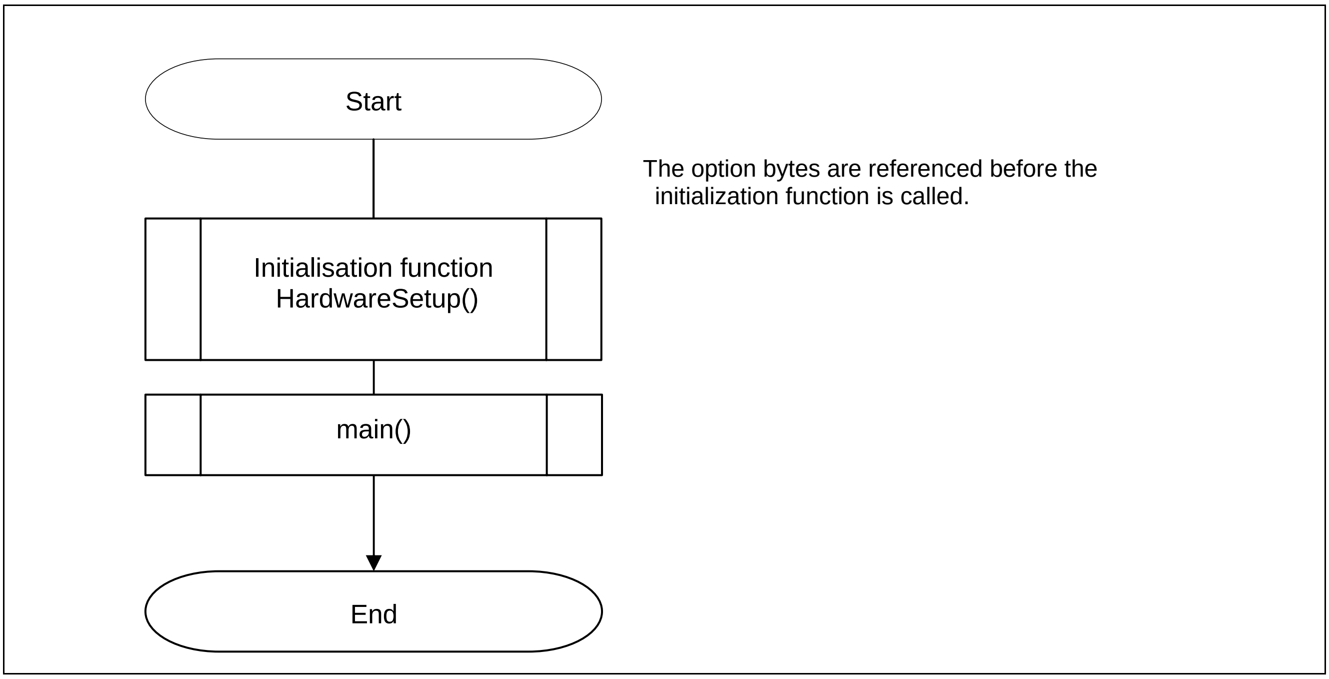

Start
Initialisation function
HardwareSetup()
main()
End
The option bytes are referenced before the
initialization function is called.

Figure 5.1 Overall Flow

5.5.1 Initialization Function

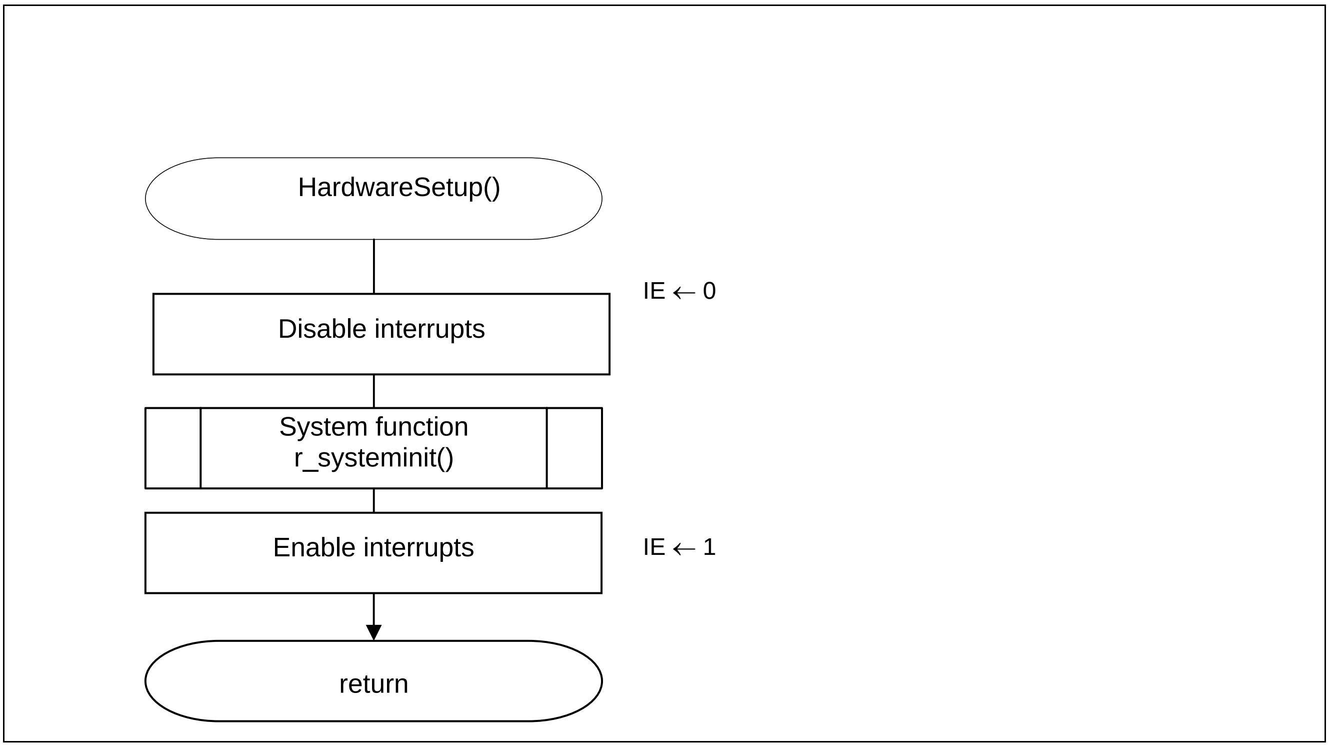


Figure 5.2 Initialization Function

5.5.2 System function

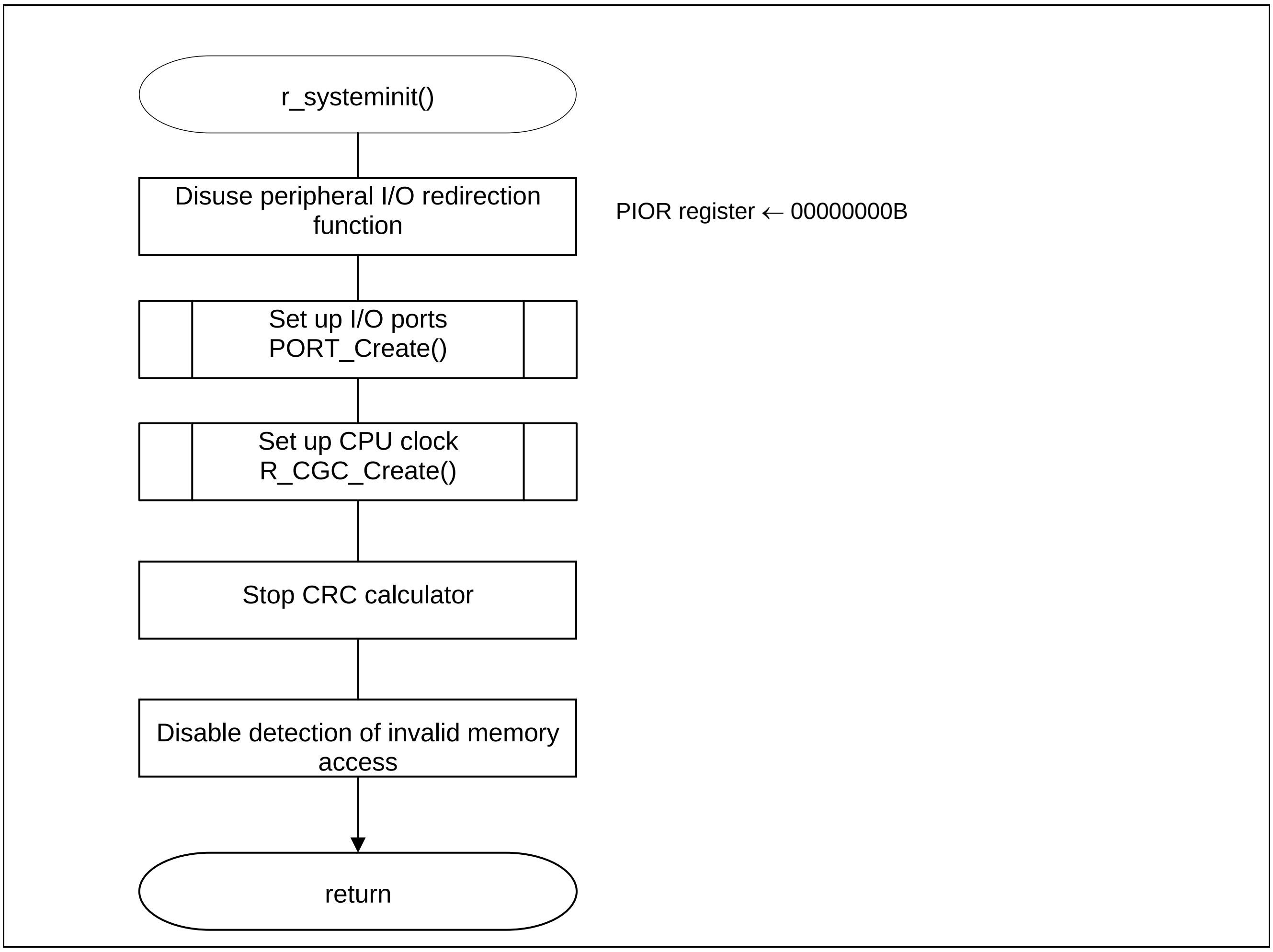

r_systeminit()
Disuse peripheral I/O redirection function
PIOR register ← 00000000B
Set up I/O ports
PORT_Create()
Set up CPU clock
R_CGC_Create()
Stop CRC calculator
Disable detection of invalid memory access
return

Figure 5.3 System Function

5.5.3 Setting up the I/O Ports

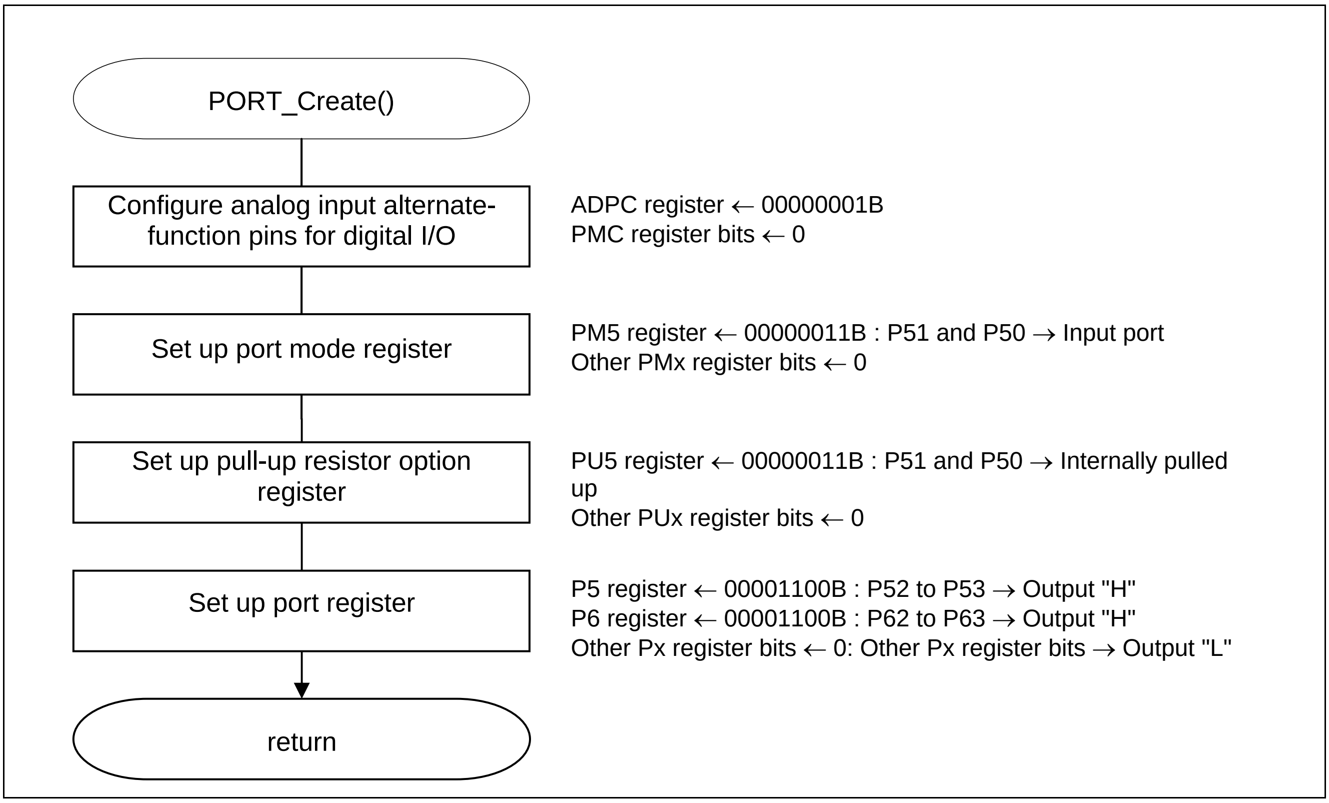

PORT_Create()
Configure analog input alternate-function pins for digital I/O
ADPC register ← 00000001B
PMC register bits ← 0
Set up port mode register
PM5 register ← 00000011B : P51 and P50 → Input port
Other PMx register bits ← 0
Set up pull-up resistor option register
PU5 register ← 00000011B : P51 and P50 → Internally pulled up
Other PUx register bits ← 0
Set up port register
P5 register ← 00001100B : P52 to P53 → Output "H"
P6 register ← 00001100B : P62 to P63 → Output "H"
Other Px register bits ← 0: Other Px register bits → Output "L"
return

Figure 5.4 I/O Port Setup

Outline of I/O port setup

The RL78/G13 is equipped with digital I/O ports so that it can provide a variety of controls.

The I/O ports serve multiple pin functions in addition to serving as digital I/O ports.

The I/O ports are controlled by the registers listed below. They must be set up during the system initialization routine that is executed when power is first supplied or after the release of the reset state.

Registers that are used to manipulate ports:

- Port mode register (PMxx)
- Port register (Pxx)
- Pull-up resistor option register (PUxx)
- Port input mode register (PIMx)
- Port output mode register (POMx)
- Port mode control register (PMCxx)*
- A/D port configuration register (ADPC)*
- Peripheral I/O redirection register (PIOR)
- Global digital input disable register (GDIDIS)

Note: A register used to place port pins in digital I/O or analog input mode. Since the port pins are configured for analog input when a reset signal occurs, the pins that are to be used for digital I/O must always be set up with this register after the release of the reset state. For the sample program described in this application note, all port pins are configured for digital I/O.

Notes 1. Refer to RL78/G13 User's Manual: Hardware for the procedure to set up registers to configure ports as alternate-function pins for peripheral functions.

2. Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a resistor.

3. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.

Given below is an example of manipulating ports that are used in this sample code.

Setting up ports for LEDs

- Port mode register 5 (PM5), Port mode register 6 (PM6)
  P52: LED0
  P53: LED1
  P62: LED2
  P63: LED3

Symbol: PM5

7	6	5	4	3	2	1	0
PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50
0	0	0	0	**0**	**0**	1 (See SW2)	1 (See SW1)

PM5n	PM5n pin I/O mode selection.
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Symbol: PM6

7	6	5	4	3	2	1	0
PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60
0	0	0	0	**0**	**0**	0	0

PM6n	PM6n pin I/O mode selection.
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Notes 1. This sample code configures any unused ports for output to minimize the adverse influence of through current.

2. For details on the procedure for setting up the registers, refer to RL78/G13 User's Manual: Hardware.

Setting up ports for switches

- Port mode register 5 (PM5)
- Pull-up resistor option register 0 (PU0)
  P50: SW1 P51: SW2
- Port mode control register 0 (PMC0)
  Digital input

Symbol: PM5

7	6	5	4	3	2	1	0
PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50
0	0	0	0	**0** **(See LED1)**	**0** **(See LED0)**	**1**	**1**

PM5n	PM5n pin I/O mode selection.
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Symbol: PU5

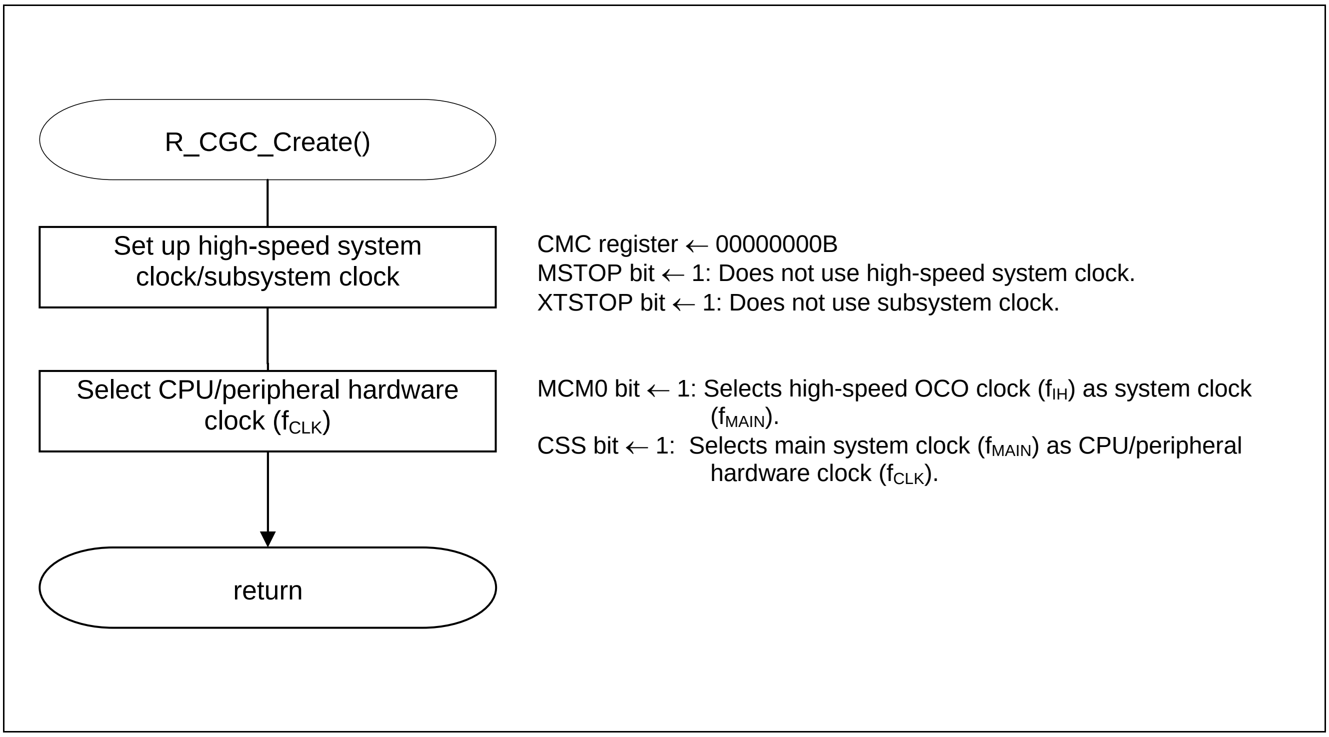
7	6	5	4	3	2	1	0
0	PU56	PU55	PU54	PU53	PU52	PU51	PU50
0	**0**	**0**	**0**	**0**	**0**	**1**	**1**

PU0n	Selection of on-chip pull-up resistor for P0n pin.
0	On-chip pull-up resistor not connected.
1	**On-chip pull-up resistor connected.**

Notes 1. This sample code configures any unused ports for output to minimize the adverse influence of through current.

2. For details on the procedure for setting up the registers, refer to RL78/G13 User's Manual: Hardware.

5.5.4 CPU Clock Setup


R_CGC_Create()
Set up high-speed system clock/subsystem clock
Select CPU/peripheral hardware clock (f_{CLK})
return

CMC register ← 00000000B
MSTOP bit ← 1: Does not use high-speed system clock.
XTSTOP bit ← 1: Does not use subsystem clock.

MCM0 bit ← 1: Selects high-speed OCO clock (f_{IH}) as system clock (f_{MAIN}).
CSS bit ← 1: Selects main system clock (f_{MAIN}) as CPU/peripheral hardware clock (f_{CLK}).

Figure 5.5 CPU Clock Setup

Outline of CPU clock setup

The RL78/G13 allows the user to select the system clock source from the high-speed on-chip oscillator (HOCO), main system clock oscillator/external clock input, and subsystem clock oscillator/external clock input*1.

The system clock is controlled by the registers listed below.

The CPU clock must be initialized during the system initialization routine that is executed when power is first supplied or after the release of the reset state.

Registers that are used to initialize the CPU clock:

- Clock operation mode control register (CMC)
- Clock operation status control register (CSC)
- System clock control register (CKC)
- Peripheral enable register 0 (PER0)
- Operation speed mode control register (OSMC)

Note: Selectable only for 40-, 44-, 48-, 52-, 64-, 80-, 100-, and 128-pin products.

Given below is an example of setting up the CPU clock for this sample code.

Setting up the clock operating mode

- Clock operation mode control register (CMC)
  High-speed system clock pin's operating mode: Input port mode
  Subsystem clock pin's operating mode: Input port mode
  XT1 oscillator oscillation mode: Low power consumption oscillation
  X1 clock oscillation frequency control: 1 MHz ≤ fMX ≤ 10 MHz

Symbol: CMC

7	6	5	4	3	2	1	0
EXCLK	OSCSEL	EXCLKS	OSCSELS	0	AMPHS1	AMPHS0	AMPH
0	**0**	**0**	**0**	0	**0**	**0**	**0**

Bit 0

AMPH	Control of X1 clock oscillation frequency
0	**1 MHz ≤ fMX ≤ 10 MHz**
1	10 MHz < fMX ≤ 20 MHz

Bits 2 and 1

AMPHS1	AMPHS0	Selection of oscillation mode for XT1 oscillator
0	**0**	**Low power consumption oscillation (default)**
0	1	Normal oscillation
1	×	Ultra-low power consumption oscillation

Bits 5 and 4

EXCLKS	OSCSELS	Subsystem Clock Pin Operating Mode	XT1/P123 Pin	XT2/EXCLKS/P124 Pin
0	**0**	**Input port mode**	**Input port**	
0	1	XT1 oscillation mode	Connected to crystal oscillator	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

Bits 7 and 6

EXCLK	OSCSEL	High-speed System Clock Pin Operating Mode	X1/P121 Pin	X2/EXCLK/P122 Pin
0	**0**	**Input port mode**	**Input port**	
0	1	X1 oscillation mode	Connected to crystal/ceramic oscillator	
1	0	Input port mode	Input port	
1	1	External clock input mode	Input port	External clock input

Note: For details on the procedure for setting up the registers, refer to RL78/G13 User's Manual: Hardware.

Controlling clock operations

- Clock operation status control register (CSC)
  High-speed system clock operation control: Stop X1 oscillator.
  Subsystem clock operation control: Stop XT1 oscillator.
  HOCO clock operation control: HOCO operation

Symbol: CSC

7	6	5	4	3	2	1	0
MSTOP	XTSTOP	0	0	0	0	0	HIOSTOP
1	**1**	0	0	0	0	0	**0**

Bit 0

HIOSTOP	Control of HOCO clock operation
0	**Runs HOCO.**
1	Stops HOCO.

Bit 6

XTSTOP	Control of Subsystem Clock Operation		
	XT1 Oscillation Mode	External Clock Input Mode	Input Port Mode
0	Runs XT1 oscillator.	Enables external clock from the EXCLKS pin.	Input port
1	**Stops XT1 oscillator.**	**Disables external clock from the EXCLK pin.**	

Bit 7

MSTOP	Control of High-speed System Clock Operation		
	X1 Oscillation Mode	External Clock Input Mode	Input Port Mode
0	Runs X1 oscillator.	Enables external clock from the EXCLKS pin.	Input port
1	**Stops X1 oscillator.**	**Disables external clock from the EXCLK pin.**	

Note: For details on the procedure for setting up the registers, refer to RL78/G13 User's Manual: Hardware.

Setting up the CPU/peripheral hardware clock (f_{CLK})

- System clock control register (CKC)
  f_{CLK} status: Main system clock
  f_{CLK} selection: HOCO clock (f_{IH})

Symbol: CKC

7	6	5	4	3	2	1	0
CLS	CSS	MCS	MCM0	0	0	0	0
0	**0**	**0**	**0**	0	0	0	0

Bit 4

MCM0	Control of main system clock (f_{MAIN}) operation
0	**Selects HOCO clock (f_{IH}) as the main system cock (f_{MAIN}).**
1	Selects high-speed system clock (f_{MX}) as the main system clock (f_{MAIN}).

Bit 5

MCS	Main system clock (f_{MAIN}) state
0	**HOCO clock (f_{IH})**
1	High-speed system clock (f_{MX})

Bit 6

CSS	Selection of CPU/peripheral hardware clock(f_{CLK})
0	**Main system clock (f_{MAIN})**
1	Subsystem clock (f_{SUB})

Bit 7

CLS	CPU/peripheral hardware clock (f_{CLK}) state
0	**Main system clock (f_{MAIN})**
1	Subsystem clock (f_{SUB})

Note: For details on the procedure for setting up the registers, refer to RL78/G13 User's Manual: Hardware.

Setting use/disuse of peripheral hardware macros

- Peripheral enable register 0 (PER0)
  Hardware input clock control: Stop input clocks.
  Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN *1	ADCEN	IICA0EN *2	SAU1EN *3	SAU0EN	TAU1EN *1	TAU0EN
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bits 1 and 0

TAUmEN	Control of timer array unit m input clock
0	**Stops supply of input clock.** **• SFR for timer array unit m cannot be written.** **• Timer array unit m is in the reset state.**
1	Supplies input clock. SFR for timer array unit m can be read and written.

Bits 3 and 2

SAUmEN	Control of serial array unit m input clock
0	**Stops supply of input clock.** **• SFR for serial array unit m cannot be written.** **• Serial array unit m is in the reset state.**
1	Supplies input clock. SFR for serial array unit m can be read and written.

Bits 6 and 4

IICAmEN	Control of serial interface IICAm input clock
0	**Stops supply of input clock.** **• SFR for IICAm cannot be written.** **• IICAm is in the reset state.**
1	Supplies input clock. SFR for IICAm can be read and written.

Bit 5

ADCEN	Control of A/D converter input clock
0	**Stops supply of input clock.** **• SFR for A/D converter cannot be written.** **• A/D converter is in the reset state.**
1	Supplies input clock. SFR for A/D converter can be read and written.

Bit 7

RTCEN	Control of realtime clock (RTC) input clock
0	**Stops supply of input clock.** **• SFR for RT cannot be written.** **• RTC is in the reset state.**
1	Supplies input clock. SFR for RTC can be read and written.

Notes: 1. For 80-, 100-, and 128-pin products only.
2. Not installed in 20-pin products.
3. Not installed in 20-, 24-, and 25-pin products.

Note: Power saving and noise reduction are achieved by stopping the supply of clocks to any unused hardware macros.

Controlling the operation speed mode

- Operation speed mode control register (OSMC)
  Setting in STOP mode or HALT mode while subsystem clock is selected as CPU clock
: Enables supply of subsystem clock to peripheral functions.
  Selection of operation clock for realtime clock and interval timer
: Subsystem clock

Symbol: OSMC

7	6	5	4	3	2	1	0
RTCLPC	0	0	WUTMMCK0	0	0	0	0
0	0	0	**0**	0	0	0	0

Bit 4

WUTMMCK0	Selection of operation clock for realtime clock and interval timer
0	**Subsystem clock (f_{SUB})**
1	Internal low-speed oscillator (LOCO) clock

Bit 7

RTCLPC	Setting in STOP Mode or HALT Mode while subsystem clock is selected as CPU clock
0	Enables supply of subsystem clock to peripheral functions
1	Stops supply of subsystem clock to peripheral functions except the realtime clock and interval timer.

Note: The OSMC register is designed to reduce the operating current, for low power operation, in STOP mode and in HALT mode in which the CPU is running on the subsystem clock. For details on its configuration procedure, refer to RL78/G13 User's Manual: Hardware.

5.5.5 Main Processing

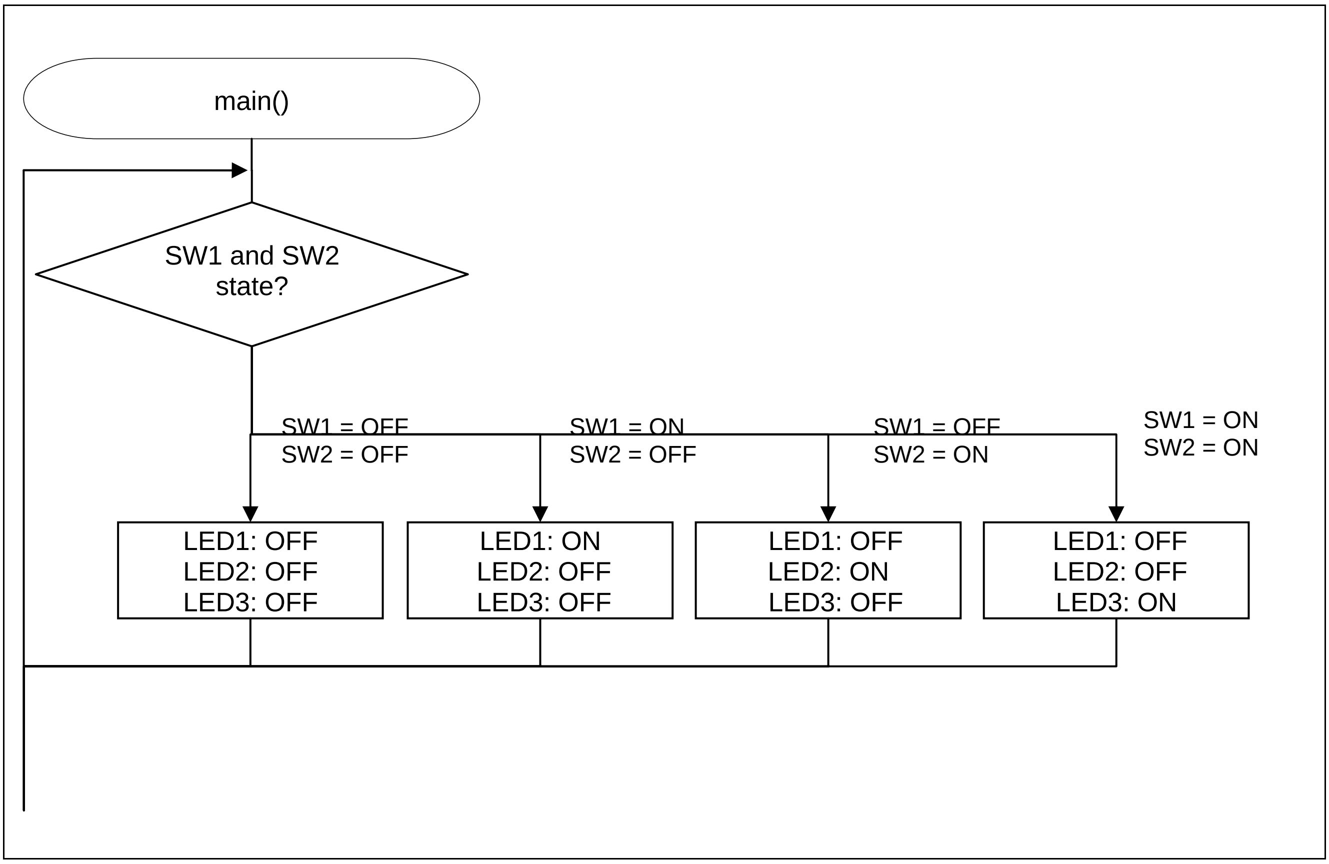
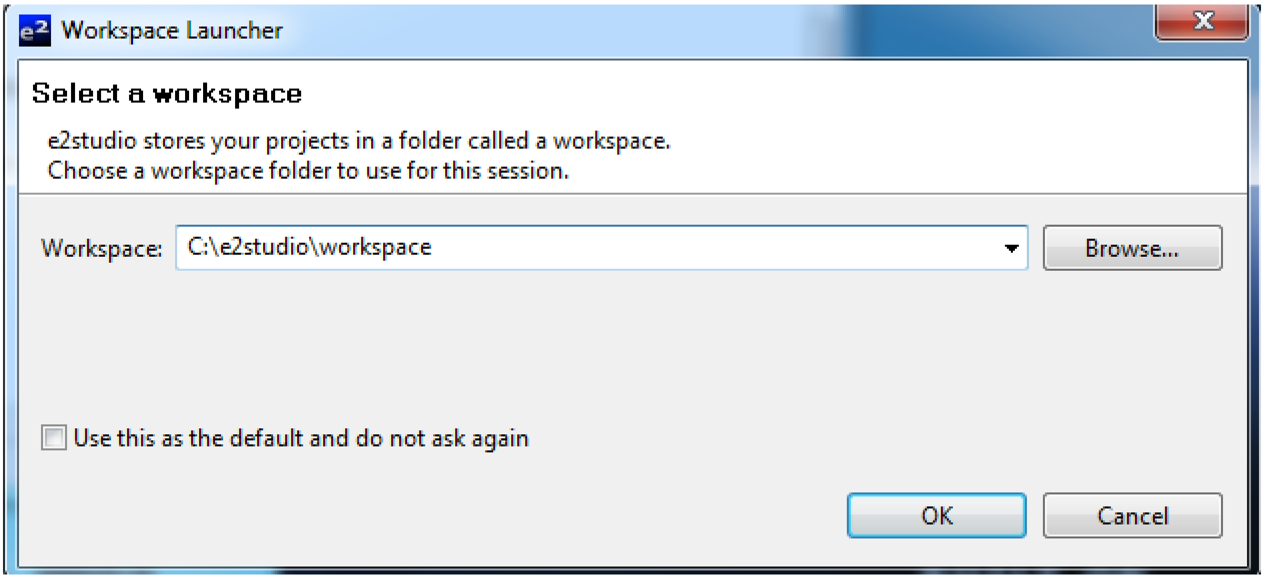


Figure 5.6 Main Processing

6. Creating the Project Workspace

Run e^{2}studio by clicking the Windows Start button, select All Programs > Renesas Electronics e2studio > Renesas e2studio. Choose a workspace folder.



Workspace Launcher

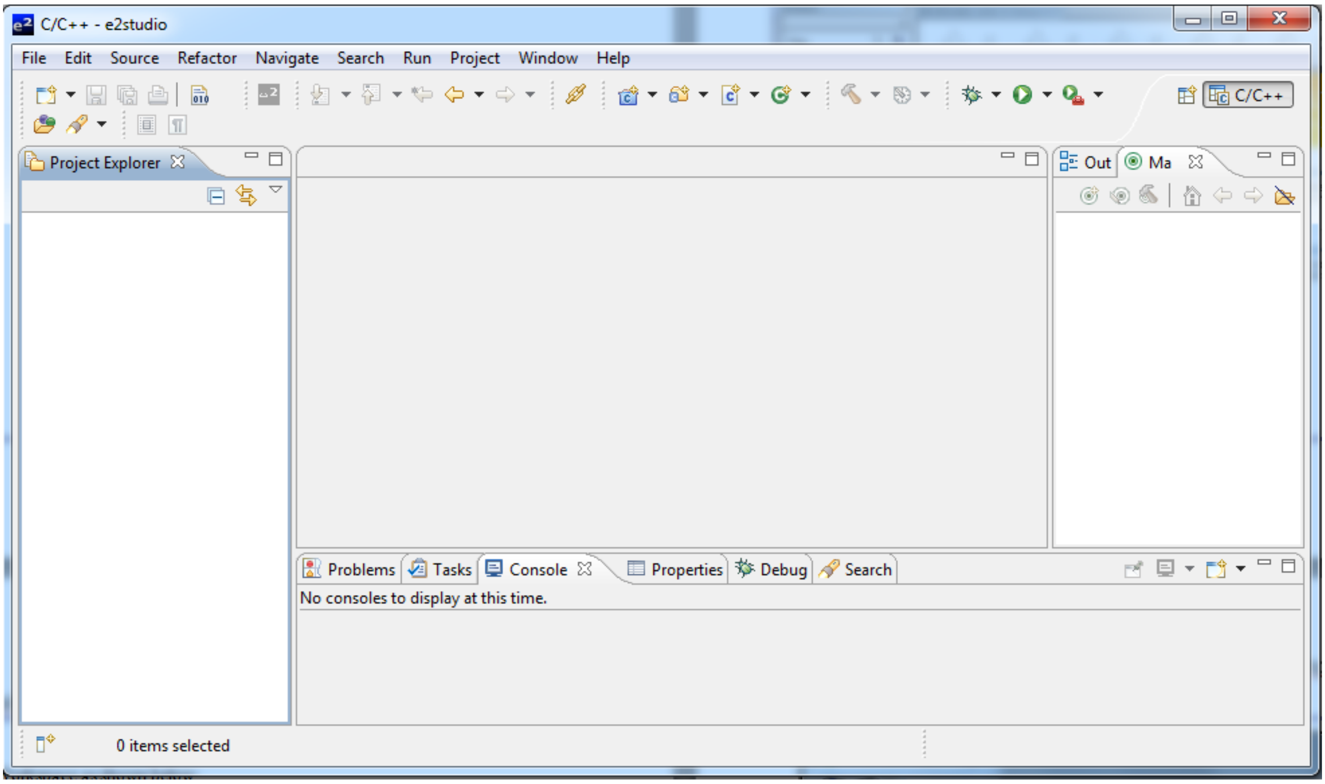
Select a workspace

e2studio stores your projects in a folder called a workspace.
Choose a workspace folder to use for this session.

Workspace: C:\e2studio\workspace

□ Use this as the default and do not ask again

This will automatically open e^{2}studio IDE with an empty workspace.

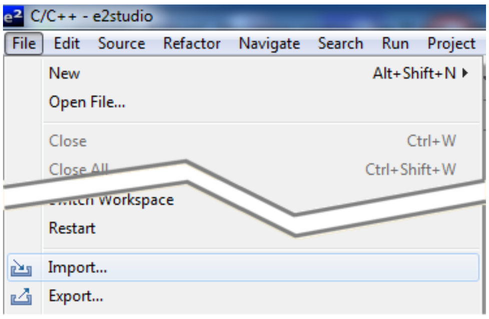


C/C++ - e2studio

No consoles to display at this time.

0 items selected

To add the sample code select from the menu bar File > Import as shown:



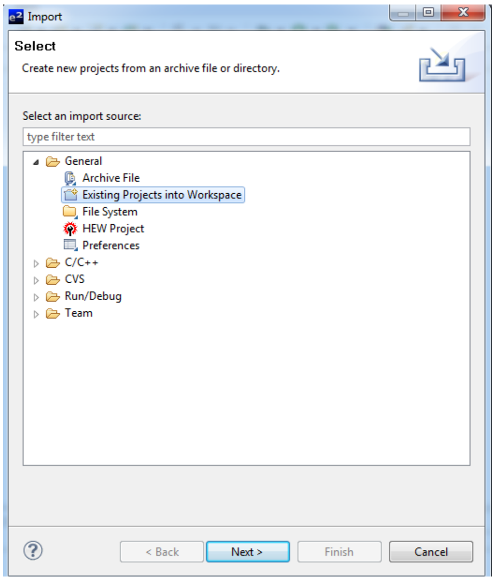
Choose 'Existing Projects into Workspace'as shown:

Click Next >, a new window will appear. Navigate to the RSKRL78G13_Workspace folder and select the Application folder.

Make sure that 'Copy projects into workspace' is checked.

Single-click the project file to select it.

Click < Finish > to add the project to the workspace.



7. Opening Sample Code and Source Files

Once the project has been added, the source code and all dependant files can be opened in the editor by expanding the folders in the Project Explorer window and double clicking the files in the folders. Each source file listed in Workspace window in e^{2}studio can be expanded to reveal its dependant files; as well as the output files.

In the Project Explorer sidebar, right-click on the project's name and select Build Configurations > Set Active > HardwareDebug. This ensures that the best debug experience will be made available when trying this sample.

8. Sample Code

The source code project is specifically written to run on the appropriate RSK. However this source code can be useful as an example even without the RSK.

The project was written using source files containing API functions generated using Applilet. The project will contain a C source file 'r_main.c'. This source file will include the C function main(). All source files and dependant files whose filenames are prefixed with 'r_' were generated using Applilet.

9. Code Execution

1. Compile and download the Application code. From the debugging perspective, click the 'Resume' button to start the software.
2. Hold down combinations of SW1 and SW2 to view the LEDs illuminate as listed in Figure 2.1 Overview of Sample Code Operation

10. Documents for Reference

RL78/G13 User's Manual: Hardware Rev.1.00 (R01UH0146EJ0100)

RL78 Family User's Manual: Software Rev.1.00 (R01US0015EJ0100)

RL78/G13 Renesas Starter Kit Users’s Manual Rev.1.00 (R20UT0459EG0100)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

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Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Jun 7, 2013		Original document updated for e^{2}studio IDE and GNURL78 v13.01 toolchain

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

- Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

—

2. Processing at Power-on

- The state of the product is undefined at the moment when power is supplied.
  - — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
  - In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
  - In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

- Access to reserved addresses is prohibited.
  - — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

- After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
  - — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

- Before changing from one product to another, i.e. to one with a different type number, confirm that

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Colophon 2.2