Description

The IEEE 1588-2008 Precision Time Protocol (PTP) is a packet-based synchronization mechanism used in packet-switched networks. PTP synchronizes the clocks of different devices with the most accurate clock on the network – usually a precise, grandmaster clock such as one using a Primary Reference Time Clock (PRTC) time signal.

The 82P33913-x is a software and hardware system that can operate as a PTP slave or PTP master. As a PTP slave, the 82P33913-x recovers accurate and stable electrical synchronization signals from a packet-based reference generated by a PTP master. As a PTP master, the 82P33913-x can lock to a stable electrical clock source and generate packet based PTP references for downstream PTP slaves.

The 82P33913-x is available with the two software options listed in Table 1.

Table 1. Software Options by Part Number

Part Number	Included Software
82P33913	Renesas Clock Recovery Servo Software
82P33913-1	Renesas Clock Recovery Servo Software IEEE 1588 Protocol Stack

Typical Applications

- Access routers, edge routers, core routers
- Carrier Ethernet switches
- Multiservice access platforms
- PON OLT
- LTE eNodeB
- ITU-T G.8265.1 and G.8275.1 Telecom Profile clock synthesizer
- ITU-T G.8273.2 Telecom Boundary Clock (T-BC) and Telecom
- Time Slave Clock (T-TSC)
- ITU-T G.8264 Synchronous Equipment Timing Source (SETS)
- ITU-T G.8263 Packet-based Equipment Clock (PEC)
- ITU-T G.8262 Synchronous Ethernet Equipment Clock (EEC) and G.8262.1 Enhanced Synchronous Ethernet Equipment Clock (eEEC)
- ITU-T G.813 Synchronous Equipment Clock (SEC)
- Telcordia GR-253-CORE Stratum 3 Clock (S3) and SONET Minimum Clock (SMC)

Features

- System implements ITU-T telecom profiles
- Composed of Renesas' IEEE 1588 software and Renesas' Synchronization Management Unit (SMU) hardware
- Operates as IEEE 1588 / PTP slave
- Recovers accurate and stable synchronization signals from packet based IEEE 1588 / PTP master
- Provides integrated physical layer frequency support
- Operates as an IEEE 1588 / PTP master

Software

- C99 source code distribution, supporting POSIX-based Operating Systems (OSs) such as Linux
- IEEE 1588 compliant Precision Time Protocol (PTP) stack
- Abstraction interface supports user-supplied IEEE 1588 compliant Precision Time Protocol (PTP) stack
- Reference trackers filter packet synchronization noise from IEEE 1588 unaware networks

Hardware

- Synchronization Management Unit (SMU) provides tools to manage physical layer and packet based synchronous clocks for IEEE 1588 Telecom Profile applications
- Supports independent IEEE 1588 and Synchronous Ethernet (SyncE) timing paths
- Combo mode provides SyncE physical layer frequency support for IEEE 1588 Telecom Boundary Clocks (T-BC) and Telecom Time Slave Clocks (T-TSC) per G.8273.2
- Digital PLLs can be configured as Digitally Controlled Oscillators (DCOs) for IEEE 1588 clock synthesis
- Generates G.8262 and G.8262.1 compliant SyncE clocks
- Fractional-N input dividers support a wide range of reference frequencies
- Locks to 1 pulse per second (PPS) references from GPS based sources
- Loads configuration from an external EPROM after reset

System Component Documentation

The detailed characteristics of the 82P33913-x software and hardware components are described in other documents as shown in Table 2 and Table 3.

Table 2. Software Documentation

Software System Component	Reference
82P33913-x IEEE 1588 Software	Please contact Renesas

Table 3. SMU Hardware Documentation

Part Number	Reference
82P33913 82P33913-1	82P33813 Datasheet

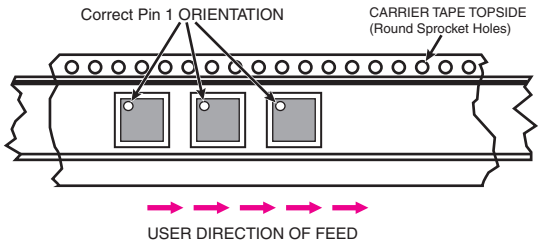
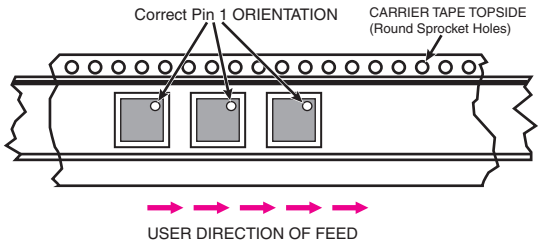
Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Ordering Information

Orderable Part Number	Package	Shipping Packaging	Temperature
82P33913NLG	10 × 10 × 0.9 mm 72-VFQFPN	Tray	-40° to +85°C
82P33913NLG8	10 × 10 × 0.9 mm 72-VFQFPN	Tape & Reel, Pin 1 Orientation: EIA-481-C	-40° to +85°C
82P33913NLG/W	10 × 10 × 0.9 mm 72-VFQFPN	Tape & Reel, Pin 1 Orientation: EIA-481-D	-40° to +85°C
82P33913-1NLG	10 × 10 × 0.9 mm 72-VFQFPN	Tray	-40° to +85°C
82P33913-1NLG8	10 × 10 × 0.9 mm 72-VFQFPN	Tape & Reel, Pin 1 Orientation: EIA-481-C	-40° to +85°C
82P33913-1NLG/W	10 × 10 × 0.9 mm 72-VFQFPN	Tape & Reel, Pin 1 Orientation: EIA-481-D	-40° to +85°C

Table 4. Pin 1 Orientation in Tape and Reel Packaging

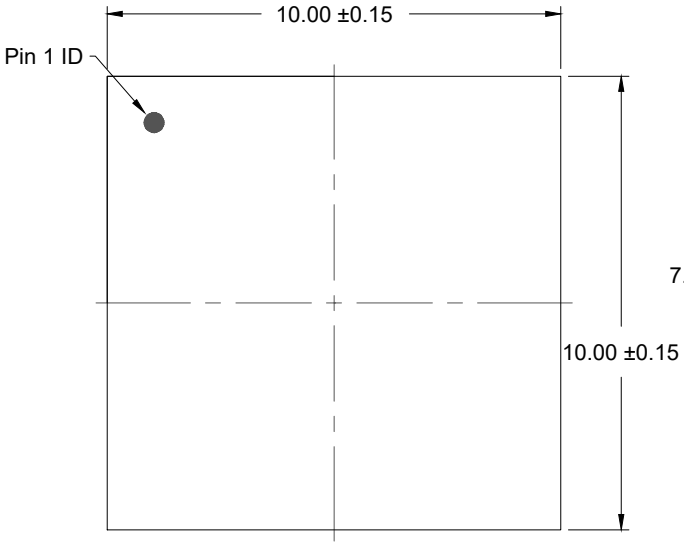
Part Number Suffix	Pin 1 Orientation	Illustration
NLG8 BAG8	Quadrant 1 (EIA-481-C)	
NLG/W	Quadrant 2 (EIA-481-D)	

Revision History

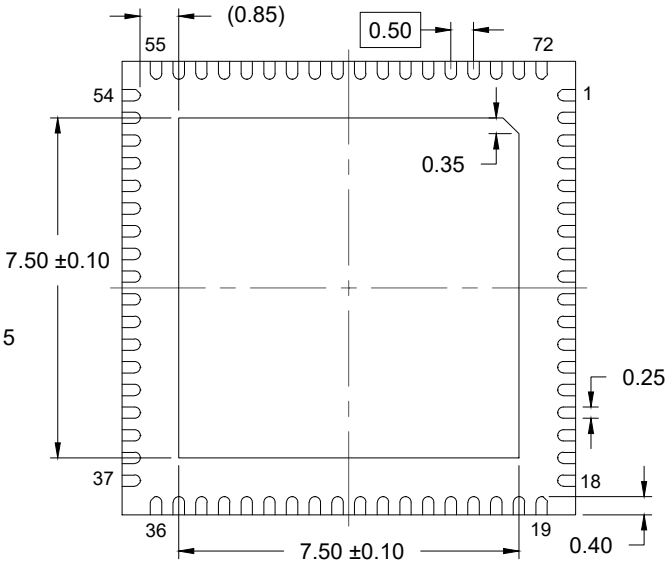
Revision Date	Description of Change
November 18, 2021	▪ Added “G.8262.1” information to *ITU-T G.8262 Synchronous Ethernet Equipment Clock (EEC)* bullet in Typical Applications and Features/Hardware sections on front page. ▪ Added Package Outline Drawings section.
December 5, 2017	Initial release of stand-alone 82P33913 / 82P33913-1 Datasheet.

Package Outline Drawing

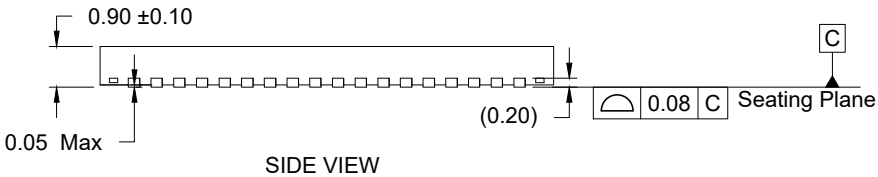
Package Code:NLG72P2
72-VFQFPN 10.0 x 10.0 x 0.90 mm Body, 0.50 mm Pitch
PSC-4208-02, Revision: 02, Date Created: Jul 27, 2023



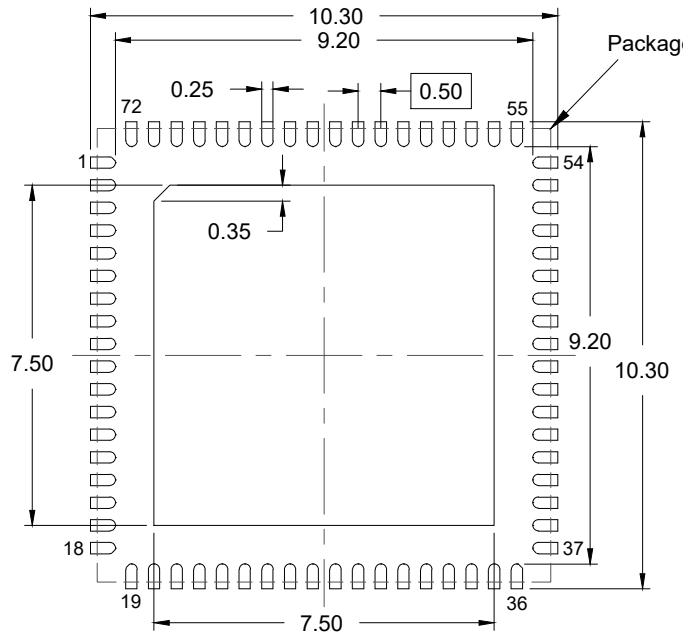
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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