Description

The 9ZXL0851 is a low-power 8-output differential buffer that meets all the performance requirements of the Intel DB1200ZL specification. It is suitable for PCI-Express Gen1–3 or QP/UPI applications, and uses a fixed external feedback to maintain low drift for critical QPI/UPI applications.

Applications

Buffer for Romley, Grantley and Purley Servers, SSD drives and PCIe

Output Features

- 8 LP-HCSL Output Pairs w/integrated terminations (Zo = 85Ω)

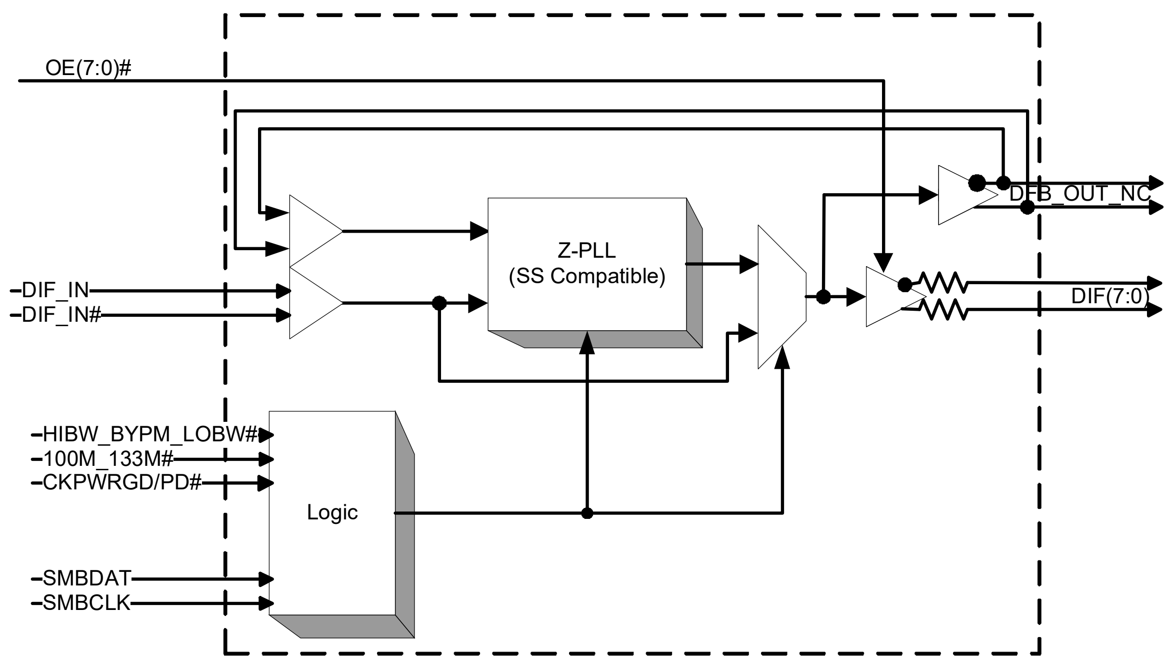
Features

- LP-HCSL outputs with Zo = 85Ω; save power and board space - no termination resistors required.
- Space-saving 48-pin VFQFPN package
- Fixed feedback path for 0ps input-to-output delay
- 8 OE# pins; hardware control of each output
- PLL or bypass mode; PLL can dejitter incoming clock
- 100MHz or 133MHz PLL mode operation; supports PCIe and QPI applications
- Selectable PLL bandwidth; minimizes jitter peaking in downstream PLLs
- Spread spectrum compatible; tracks spreading input clock for low EMI
- 25MHz PFT clock delay management

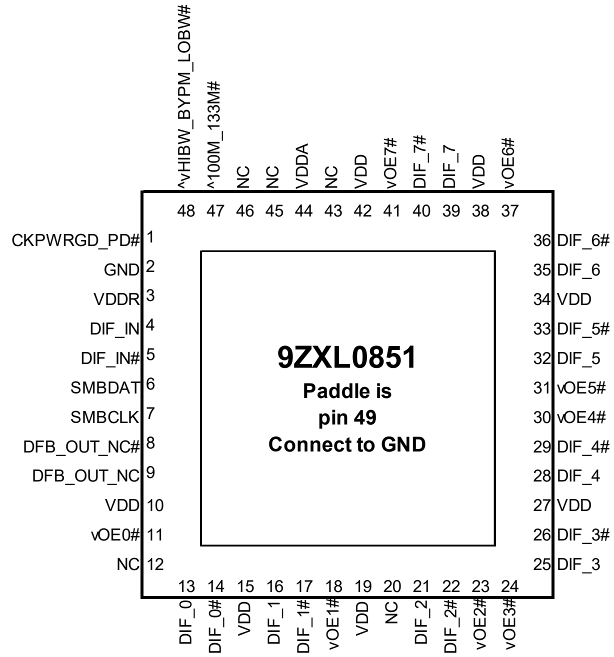
Key Specifications

- Cycle-to-cycle jitter < 50ps
- Output-to-output skew < 65ps
- Input-to-output delay variation < 50ps
- PCIe Gen3 phase jitter < 1.0ps RMS
- QPI/UPI 9.6GT/s 12UI phase jitter < 0.2ps RMS

Block Diagram



Pin Configuration



48-pin VFQFPN, 6x6 mm, 0.4mm pitch

Note: Pins with ^ prefix have internal 120kOhm pull-up
Pins with v prefix have internal 120kOhm pull-down
Pins with ^v prefix have internal 120kOhm pull-up/pull-down (biased to VDD/2)

Power Management Table

CKPWRGD_PD#	DIF_IN/ DIF_IN#	SMBus EN bit	DIF(7:0)/ DIF(7:0)#	PLL STATE IF NOT IN BYPASS MODE
0	X	X	Low/Low	OFF
1	Running	0	Low/Low	ON
		1	Running	ON

Functionality at Power-up (PLL mode)

100M_133M#	DIF_IN MHz	DIF(7:0)
1	100.00	DIF_IN
0	133.33	DIF_IN

PLL Operating Mode Readback Table

HiBW_BypM_LoBW#	Byte0, bit 7	Byte 0, bit 6
Low (Low BW)	0	0
Mid (Bypass)	0	1
High (High BW)	1	1

Power Connections

Pin Number		Description
VDD	GND	
44	49	Analog PLL
3	2	Analog Input
10,15,19, 27,34,38, 42	49	DIF clocks

Tri-Level Input Thresholds

Level	Voltage
Low	<0.8V
Mid	1.2<Vin<1.8V
High	Vin > 2.2V

SMBus Address

Address	+ Read/Write bit
1101100	x

PLL Operating Mode

HiBW_BypM_LoBW#	MODE
Low	PLL Lo BW
Mid	Bypass
High	PLL Hi BW

NOTE: PLL is OFF in Bypass Mode

Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	CKPWRGD_PD#	IN	3.3V Input notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.
2	GND	GND	Ground pin.
3	VDDR	PWR	3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.
4	DIF_IN	IN	0.7 V Differential True input
5	DIF_IN#	IN	0.7 V Differential Complementary Input
6	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
7	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
8	DFB_OUT_NC#	OUT	Complementary half of differential feedback output, provides feedback signal to the PLL for synchronization with input clock to eliminate phase error. This pin should NOT be connected on the circuit board, the feedback is internal to the package.
9	DFB_OUT_NC	OUT	True half of differential feedback output, provides feedback signal to the PLL for synchronization with the input clock to eliminate phase error. This pin should NOT be connected on the circuit board, the feedback is internal to the package.
10	VDD	PWR	Power supply, nominal 3.3V
11	vOE0#	IN	Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
12	NC	N/A	No Connection.
13	DIF_0	OUT	0.7V differential true clock output
14	DIF_0#	OUT	0.7V differential Complementary clock output
15	VDD	PWR	Power supply, nominal 3.3V
16	DIF_1	OUT	0.7V differential true clock output
17	DIF_1#	OUT	0.7V differential Complementary clock output
18	vOE1#	IN	Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
19	VDD	PWR	Power supply, nominal 3.3V
20	NC	N/A	No Connection.
21	DIF_2	OUT	0.7V differential true clock output
22	DIF_2#	OUT	0.7V differential Complementary clock output
23	vOE2#	IN	Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
24	vOE3#	IN	Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
25	DIF_3	OUT	0.7V differential true clock output
26	DIF_3#	OUT	0.7V differential Complementary clock output
27	VDD	PWR	Power supply, nominal 3.3V
28	DIF_4	OUT	0.7V differential true clock output
29	DIF_4#	OUT	0.7V differential Complementary clock output
30	vOE4#	IN	Active low input for enabling DIF pair 4. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
31	vOE5#	IN	Active low input for enabling DIF pair 5. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs

Pin Descriptions (cont.)

PIN #	PIN NAME	TYPE	DESCRIPTION
32	DIF_5	OUT	0.7V differential true clock output
33	DIF_5#	OUT	0.7V differential Complementary clock output
34	VDD	PWR	Power supply, nominal 3.3V
35	DIF_6	OUT	0.7V differential true clock output
36	DIF_6#	OUT	0.7V differential Complementary clock output
37	vOE6#	IN	Active low input for enabling DIF pair 6. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
38	VDD	PWR	Power supply, nominal 3.3V
39	DIF_7	OUT	0.7V differential true clock output
40	DIF_7#	OUT	0.7V differential Complementary clock output
41	vOE7#	IN	Active low input for enabling DIF pair 7. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
42	VDD	PWR	Power supply, nominal 3.3V
43	NC	N/A	No Connection.
44	VDDA	PWR	3.3V power for the PLL core.
45	NC	N/A	No Connection.
46	NC	N/A	No Connection.
47	^100M_133M#	IN	3.3V Input to select operating frequency. This pin has an internal pull-up resistor. See Functionality Table for Definition
48	^vHIBW_BYPM_LOBW#	LATCHED IN	Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details.
49	GND	PWR	Ground

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZXL0851. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Supply Voltage	VDD, VDDA, VDDR	VDD for core logic and PLL			4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5V	V	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics–DIF_IN Clock Input Parameters

T_A = T_{COM}; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Crossover Voltage - DIF_IN	V_{CROSS}	Crossover Voltage	150		900	mV	1
Input Swing - DIF_IN	V_{SWING}	Differential value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	V_{IN} = V_{DD} , V_{IN} = GND	-5		5	uA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through +/-75mV window centered around differential zero.

Electrical Characteristics–Input/Supply/Common Parameters

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	T_{COM}	Commercial range	0		70	°C	1
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND - 0.3		0.8	V	1
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	1
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	1
Input Frequency	F_{ibyp}	V_{DD} = 3.3 V, Bypass mode	25		150	MHz	2
	F_{ipll}	V_{DD} = 3.3 V, 100MHz PLL mode	25	100.00	110	MHz	2
	F_{ipll}	V_{DD} = 3.3 V, 133.33MHz PLL mode	120	133.33	147	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.250	1	ms	1,2
Input SS Modulation Frequency	f_{MODIN}	Allowable Frequency (Triangular Modulation)	30		33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	4		12	cycles	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t_F	Fall time of control inputs			10	ns	1,2
Trise	t_R	Rise time of control inputs			10	ns	1,2
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	1
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	1
SMBus Output Low Voltage	V_{OLSMB}	At I_{PULLUP}			0.4	V	1
SMBus Sink Current	I_{PULLUP}	At V_{OL}	4			mA	1
Nominal Bus Voltage	V_{DDSMB}	3V to 5V +/- 10%	2.7		5.5	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			100	kHz	1,5

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] DIF_IN input.

[5] The differential input clock must be running for the SMBus to be active.

Electrical Characteristics–DIF 0.7V Low Power Differential Outputs

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on	1		4	V/ns	1, 2, 3
Slew rate matching	ΔTrf	Slew rate matching, Scope averaging on			20	%	1, 2, 4
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660		850	mV	1
Voltage Low	VLow		-150		150		1
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)			1150	mV	1
Min Voltage	Vmin		-300				1
Vswing	Vswing	Scope averaging off	300			mV	1, 2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	300		550	mV	1, 5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off			140	mV	1, 6

[1]Guaranteed by design and characterization, not 100% tested in production. C_L = 2pF with R_S = 27Ω for Zo = 85Ω differential trace impedance).

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage t

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

Electrical Characteristics–Current Consumption

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I_{DDVDD}	133MHz, VDD rail			135	mA	1
	I_{DDVDDA}	133MHz, VDDA + VDDR rail, PLL Mode			20	mA	1
Powerdown Current	$I_{DDVDDPD}$	Power Down, VDD Rail			1.2	mA	1
	$I_{DDVDDAPD}$	Power Down, VDDA Rail			5	mA	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] C_L = 2pF with R_S = 27Ω for Zo = 85Ω differential trace impedance

Electrical Characteristics–Skew and Differential Jitter Parameters

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
CLK_IN, DIF[x:0]	t_{SPO_PLL}	Input-to-Output Skew in PLL mode nominal value @ 25°C, 3.3V	-100		100	ps	1,2,4,5,8
CLK_IN, DIF[x:0]	t_{PD_BYP}	Input-to-Output Skew in Bypass mode nominal value @ 25°C, 3.3V	2.5		4.5	ns	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSPO_PLL}	Input-to-Output Skew Variation in PLL mode across voltage and temperature	-50		50	ps	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSPO_BYP}	Input-to-Output Skew Variation in Bypass mode across voltage and temperature	-250		250	ps	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DTE}	Random Differential Tracking error between two 9ZX devices in Hi BW Mode			5	ps (rms)	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSSTE}	Random Differential Spread Spectrum Tracking error between two 9ZX devices in Hi BW Mode			75	ps	1,2,3,5,8
DIF{x:0]	t_{SKEW_ALL}	Output-to-Output Skew across all outputs (Common to Bypass and PLL mode)			65	ps	1,2,3,8
PLL Jitter Peaking	$j_{peak-hibw}$	LOBW#_BYPASS_HIBW = 1	0		2.5	dB	7,8
PLL Jitter Peaking	$j_{peak-lobw}$	LOBW#_BYPASS_HIBW = 0	0		2	dB	7,8
PLL Bandwidth	pll_{HIBW}	LOBW#_BYPASS_HIBW = 1	2		4	MHz	8,9
PLL Bandwidth	pll_{LOBW}	LOBW#_BYPASS_HIBW = 0	0.7		1.4	MHz	8,9
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45		55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode @100MHz	-2		2	%	1,10
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode			50	ps	1,11
		Additive Jitter in Bypass Mode			50	ps	1,11

Notes for preceding table:

[1] C_L = 2pF with RS = 27Ω for Zo = 85Ω differential trace impedance. Input to output skew is measured at the first output edge following the corresponding input.

[2] Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

[3] All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

[4] This parameter is deterministic for a given device.

[5] Measured with scope averaging on to find mean value.

[6] t is the period of the input clock.

[7] Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

[8]. Guaranteed by design and characterization, not 100% tested in production.

[9] Measured at 3 db down or half power point.

[10] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[11] Measured from differential waveform.

Electrical Characteristics–Phase Jitter Parameters

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1}$	PCIe Gen 1			86	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz			3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)			3.1	ps (rms)	1,2
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)			1	ps (rms)	1,2,4
	t_{jphQPI_SMI}	QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)			0.5	ps (rms)	1,5
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)			0.3	ps (rms)	1,5
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)			0.2	ps (rms)	1,5
Additive Phase Jitter, Bypass mode	$t_{jphPCIeG1}$	PCIe Gen 1			10	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz			0.3	ps (rms)	1,2,6
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)			0.6	ps (rms)	1,2,6
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, 2-5MHz, CDR = 10MHz)			0.2	ps (rms)	1,2,4,6
	t_{jphQPI_SMI}	QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)			0.2	ps (rms)	1,5,6
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)			0.1	ps (rms)	1,5,6
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)			0.1	ps (rms)	1,5,6

[1] Applies to all outputs.

[2] See http://www.pcisig.com for complete specs.

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

[4] Subject to final ratification by PCI SIG.

[5] Calculated from Intel-supplied clock jitter tool v1.6.3.

[6] For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)^2 = (total jitter)^2 - (input jitter)^2.

Clock Periods–Differential Outputs with Spread Spectrum Disabled

SSC OFF	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2,3
	133.33	7.44925		7.49925	7.50000	7.50075		7.55075	ns	1,2,4

Clock Periods–Differential Outputs with Spread Spectrum Enabled

SSC ON	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2,3
	133.00	7.44930	7.49930	7.51805	7.51880	7.51955	7.53830	7.58830	ns	1,2,4

Notes:

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements (+/-100ppm). The 9ZXL0851 itself does not contribute to ppm error.

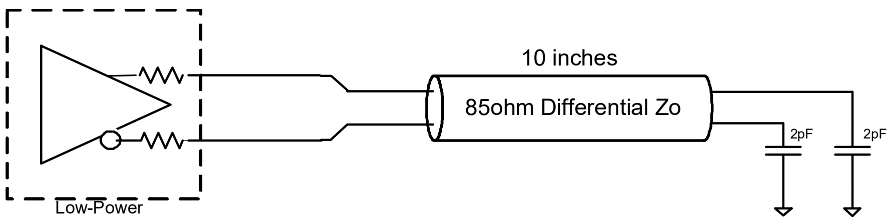
[3] Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode

[4] Driven by CPU output of main clock, 133 MHz PLL Mode or Bypass mode

Test Loads

Differential Output Terminations

DIF Zo (Ω)	Rs (Ω)
100	7
85	0



General SMBus Serial Interface Information for 9ZXL0851

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			Renesas (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)			Renesas
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBusTable: PLL Mode, and Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	48	PLL Mode 1	PLL Operating Mode Rd back 1	R	See PLL Operating Mode Readback Table		Latch
Bit 6	48	PLL Mode 0	PLL Operating Mode Rd back 0	R			Latch
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		PLL_SW_EN	Enable S/W control of PLL BW	RW	HW Latch	SMBus Control	0
Bit 2		PLL Mode 1	PLL Operating Mode 1	RW	See PLL Operating Mode Readback Table		1
Bit 1		PLL Mode 0	PLL Operating Mode 0	RW			1
Bit 0	47	100M_133M#	Frequency Select Readback	R	133MHz	100MHz	Latch

Note: Setting bit 3 to '1' allows the user to override the Latch value from pin 5 via use of bits 2 and 1. Use the values from the PLL Operating Mode Readback Table. Note that Bits 7 and 6 will keep the value originally latched on pin 5. A warm reset of

SMBusTable: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	32/33	DIF_5_En	Output Control - '0' overrides OE# pin	RW	Low/Low	Enable	1
Bit 6	28/29	DIF_4_En	Output Control - '0' overrides OE# pin	RW			1
Bit 5	25/26	DIF_3_En	Output Control - '0' overrides OE# pin	RW			1
Bit 4	21/22	DIF_2_En	Output Control - '0' overrides OE# pin	RW			1
Bit 3		Reserved					1
Bit 2	16/17	DIF_1_En	Output Control - '0' overrides OE# pin	RW	Low/Low	Enable	1
Bit 1	13/14	DIF_0_En	Output Control - '0' overrides OE# pin	RW			1
Bit 0		Reserved					1

SMBusTable: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					1
Bit 2	39/40	DIF_7_En	Output Control - '0' overrides OE# pin	RW	Low/Low	Enable	1
Bit 1		Reserved					1
Bit 0	35/36	DIF_6_En	Output Control - '0' overrides OE# pin	RW	Low/Low	Enable	1

SMBusTable: Reserved Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

SMBusTable: Reserved Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

SMBusTable: Vendor & Revision ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	A rev = 0000		X
Bit 6	-	RID2		R			X
Bit 5	-	RID1		R			X
Bit 4	-	RID0		R			X
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBusTable: DEVICE ID

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Device ID 7 (MSB)		R	0851 is 184 Decimal or 8B Hex		1
Bit 6	-	Device ID 6		R			0
Bit 5	-	Device ID 5		R			0
Bit 4	-	Device ID 4		R			0
Bit 3	-	Device ID 3		R			1
Bit 2	-	Device ID 2		R			0
Bit 1	-	Device ID 1		R			1
Bit 0	-	Device ID 0		R			1

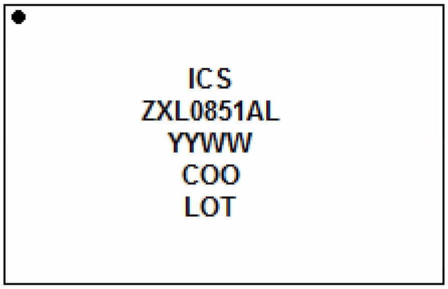
SMBusTable: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4	-	BC4	Writing to this register configures how many bytes will be read back.	RW	Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default.		0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			0
Bit 0	-	BC0		RW			0

SMBusTable: Reserved Register

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

Marking Diagram



- Line 2: truncated part number.
  - "L" denotes RoHS compliant package.
- Line 3: "YYWW" is the last two digits of the year and week that the part was assembled.
- Line 4: "COO" denotes country of origin.
- Line 5: "LOT" denotes the lot number.

Package Outline Drawings

The package outline drawings are appended at the end of this document and accessible from the link below. The package information is the most current data available.

www.renesas.com/us/en/document/psc/package-outline-drawing-package-code-ndg48p1-48-vfqfpn-60-x-60-x-09-mm-body-04-mm

Ordering Information

Part / Order Number	Shipping Package	Package	Temperature
9ZXL0851AKLF	Trays	48-VFQFPN	0 to +70°C
9ZXL0851AKLFT	Tape and Reel	48-VFQFPN	0 to +70°C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

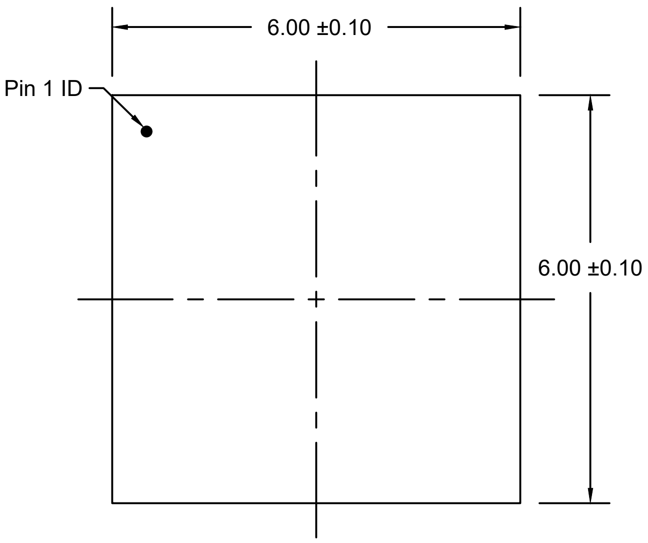
"A" is the device revision designator (will not correlate with the datasheet revision).

Revision History

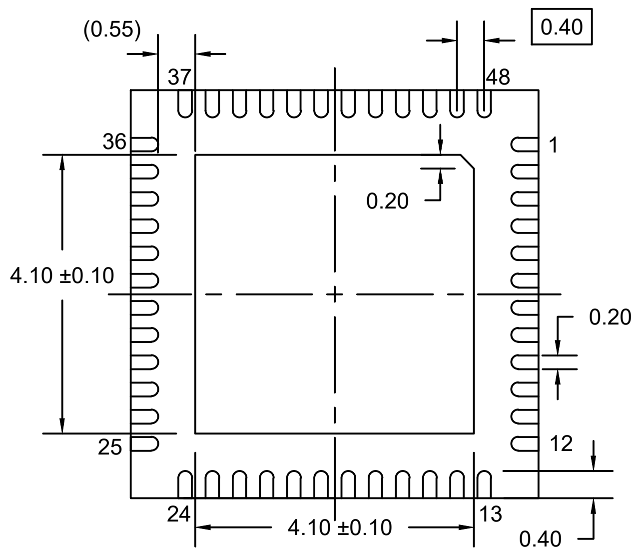
Revision Date	Description
March 28, 2013	Initial release
November 20, 2015	1. Updated QPI references to QPI/UPI 2. Updated DIF_IN table to match PCI SIG specification, no silicon change
March 10, 2021	1. Updated input frequency minimum values from 33MHz to 25MHz. 2. Added "25MHz PFT clock delay management" bullet to Features section on cover page. 3. Reformatted headers and footers to Renesas. 4. Updated Marking Diagram and Package Outline Drawings sections.
February 6, 2023	Updated POD link.

Package Outline Drawing

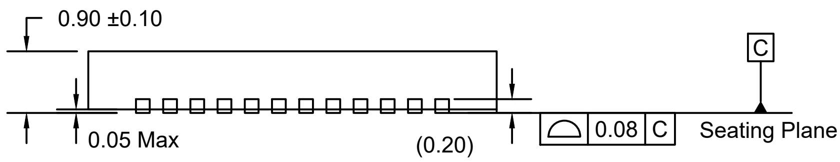
Package Code: NDG48P1
48-VFQFPN 6.0 x 6.0 x 0.9 mm Body, 0.4 mm Pitch
PSC-4212-01, Revision: 02, Date Created: Nov 18, 2022



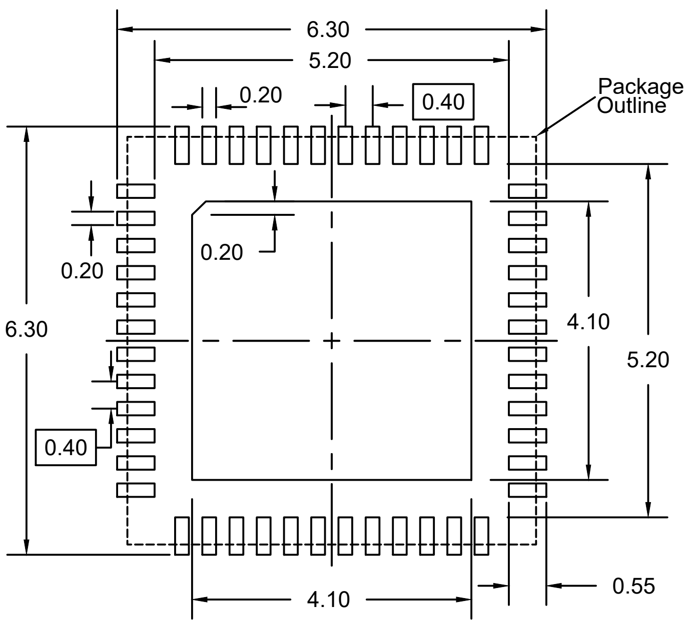
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.50 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

IMPORTANT NOTICE AND DISCLAIMER

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