High-Efficiency, 10 A, High-Voltage Direct Charger

General Description

DA9318L/M is a direct charger using a high-efficiency current doubler with integrated Analog to Digital Converter (ADC) for system monitoring. The device is especially optimized to handle high charging currents and at the same time ensure the safety of the battery and the system. It operates together with a main charger, which handles the pre-charge and constant voltage charging duties.

The current doubling is achieved with a high-efficiency capacitive divider that provides an output voltage of $V_{IN}/2$, which allows the use of standard Type-C™ cables for charging currents up to 6 A. The peak efficiency of DA9318L/M is 98 %.

Available as two variants, the DA9318L provides a maximum 8 A charging current and 35 W of charging power, whereas DA9318M provides 10 A output current and 44 W of charging power.

An integrated reverse protection feature blocks current flow in both directions while the device is not operational. Additionally, the battery is protected by DA9318L/M by six hardware based safety functions for any over- or under-voltage condition. All safety triggered events lead to an automatic shutdown and are reported via interrupt to the system.

DA9318L/M features an 8-bit ADC for input and output current and voltage, and junction temperature monitoring which ensures safety during direct charging. For software supervision a programmable watchdog timer, and for battery overload protection a safety timer, are included.

An I^2C compatible 2-wire interface is provided for the device control.

The DA9318L/M is available in a small WLCSP 3.62 mm × 3.78 mm package.

Key Features

- 8 A output current (DA9318L)
- 10 A output current (DA9318M)
- 98 % efficiency at 2 A
- 5 % current sense accuracy (DA9318L)
- 10 % current sense accuracy (DA9318M)
- Reverse and forward current protection in IDLE mode
- I^2C compatible 2-wire interface
- 8-bit ADC to measure voltage and current at the input and output as well as junction temperature
- Safety timer and watchdog
- Automatic shutdown in fault condition
- Travel adaptor detection
- No inductors
- WLCSP package: 3.62 mm × 3.78 mm

Applications

- Direct charging in smartphones and tablets, battery packs, and Li-ion powered devices

Contents

Figures

Tables

1 Terms and Definitions

ADC	Analog to digital converter
DC	Direct current
ESD	Electrostatic discharge
FET	Field effect transistor
HBM	Human body model
I^2C	Inter-integrated circuit (bus)
MSB	Most significant bit
OTP	One-time programable
PCB	Printed circuit board
PMIC	Power management integrated circuit
POR	Power on reset
RCP	Reverse current protection
WLCSP	Wafer level chip scale package

2 References

[1] NXP Semiconductors, I^2C Bus Specification and User Manual

[2] Universal Serial Bus Power Delivery Specification, Revision 2.0, V1.2. Mar. 2016

3 Block Diagram

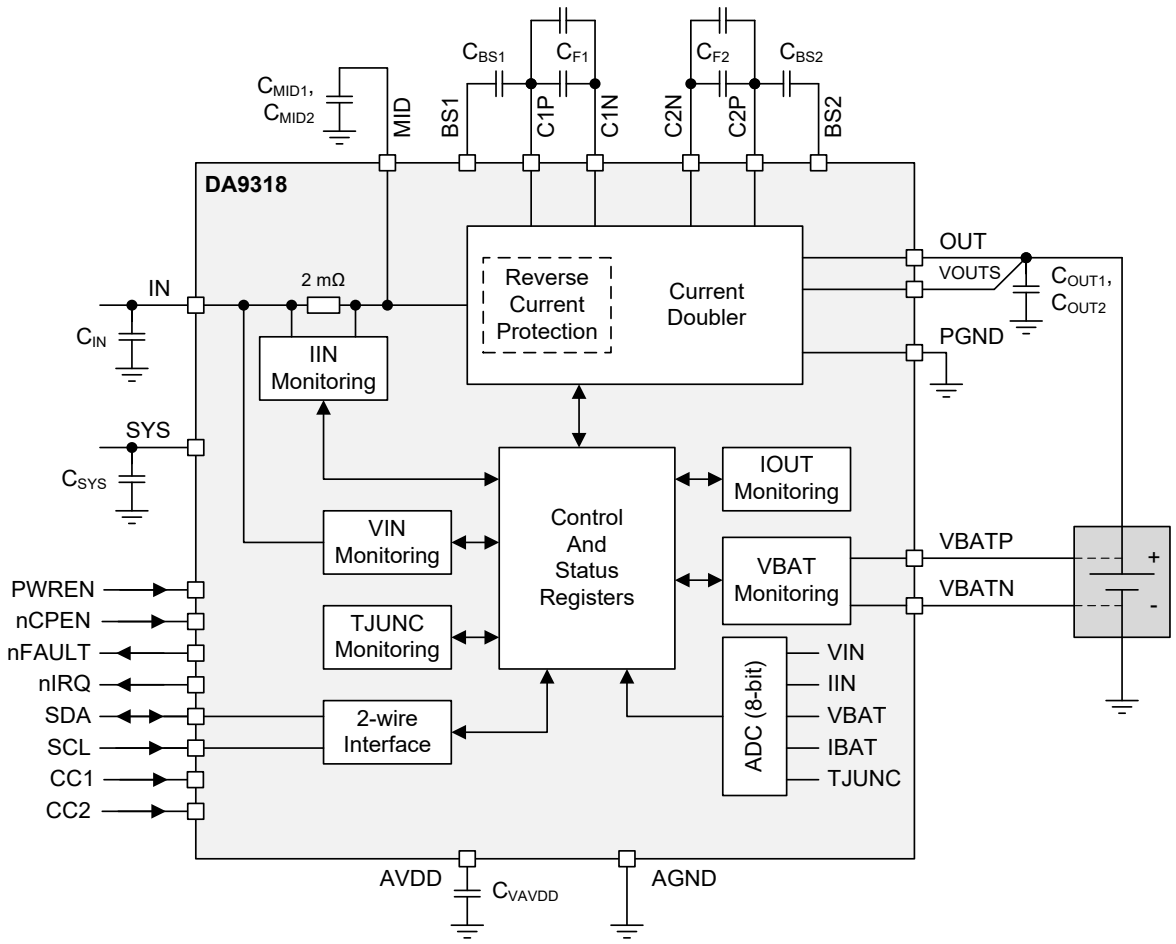

Figure 1: Block Diagram

The two instances of CMID, CBS, CF, and COUT are placed on opposite sides of the die. See Figure 24 for details.

4 Ballout

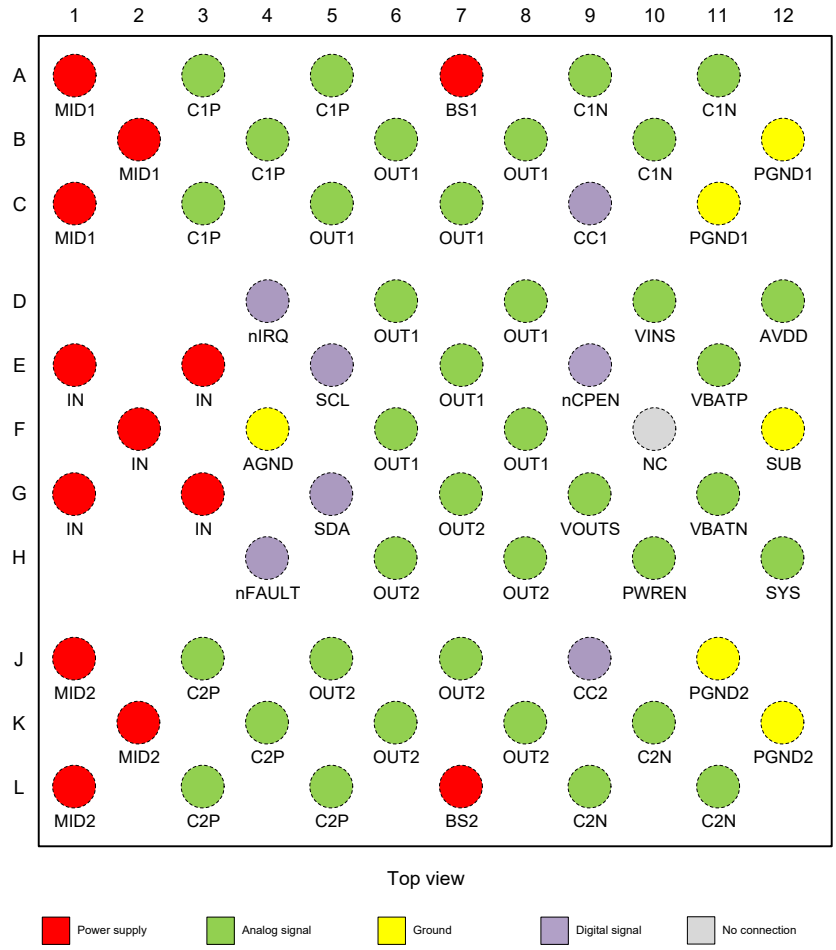

Figure 2: Ballout Diagram

Table 1: Ball Description

Ball No.	Ball Name	Type (Table 2)	Description
E1, E3, F2, G1, G3	IN	PS	Input supply, bypass to power ground with CIN
A1, B2, C1	MID1	PS	Input to the current doubler, bypass to power ground with CMID1
J1, K2, L1	MID2	PS	Input to the current doubler, bypass to power ground with CMID2
A3, A5, B4, C3	C1P	AIO	CF positive terminal
A9, A11, B10	C1N	AIO	CF negative terminal
J3, K4, L3, L5	C2P	AIO	CF positive terminal
K10, L9, L11	C2N	AIO	CF negative terminal
A7	BS1	PS	Gate driver supply of the current doubler, bypass to C1P with CBS1
L7	BS2	PS	Gate driver supply of the current doubler, bypass to C2P with CBS2

Ball No.	Ball Name	Type (Table 2)	Description
B6, B8, C5, C7, D6, D8, E7, F6, F8	OUT1	AO	Output of current doubler, bypass to power ground with COUT1
G7, H6, H8, J5, J7, K6, K8	OUT2	AO	Output of current doubler, bypass to power ground with COUT2
B12, C11	PGND1	GND	Power ground
J11, K12	PGND2	GND	Power ground
F4	AGND	GND	Analog ground
F12	SUB	GND	Substrate ground connection
G9	VOUTS	AI	Output voltage sense
D10	VINS	AI	Input voltage sense
E11	VBATP	AI	Positive battery voltage sense
G11	VBATN	AI	Negative battery voltage sense
H12	SYS	AI	Secondary power supply of the AVDD, bypass to analog ground with CSYS
D12	AVDD	AIO	Internal supply, bypass to analog ground with CAVDD
H10	PWREN	DI	Power enable, tie to AVDD if not used
D4	nIRQ	DO	Interrupt request, open-drain, active low, connect to an IO supply via pull-up R_{PU}
E9	nCPEN	DI	Current doubler enable, active low
H4	nFAULT	DO	Fault status, open-drain, active low, connect to an IO supply via pull-up R_{PU}
G5	SDA	DIO	2-wire data
E5	SCL	DI	2-wire clock
C9	CC1	DI	USB Type-C configuration channel, connect to ground if not used
J9	CC2	DI	USB Type-C configuration channel, connect to ground if not used
F10	NC	N/A	Not connected. Connect to GND PCB plane (not directly to power ground)

Table 2: Ball Type Definition

Ball Type	Description	Ball Type	Description
DI	Digital Input	AI	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input/Output	AIO	Analog Input/Output
PS	Power Supply	GND	Ground

5 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions (Note 1)	Min	Max	Unit
T_S	Storage temperature		-60	+150	°C
V_{IN}	Input voltage (Note 2)	Referenced to PGND	-0.3	20	V
V_{INS}	Input voltage sense pin (Note 2)		-0.3	20	V
V_{MID}	Voltage on pin MID		V_{IN} – 0.025	V_{IN}	V
V_{C1P}	Maximum voltage across C1P		V_{C1N} - 0.3	V_{C1N} + 5.5	V
V_{C2P}	Maximum voltage across C2P		V_{C2N} - 0.3	V_{C2N} + 5.5	V
V_{C1N}	Maximum voltage across C1N		-0.3	V_{OUT} +0.3	V
V_{C2N}	Maximum voltage across C2N		-0.3	V_{OUT} + 0.3	V
V_{BS1}	Maximum voltage across BS1		V_{C1P} - 0.3	V_{C1P} + 5.5	V
V_{BS2}	Maximum voltage across BS2		V_{C2P} - 0.3	V_{C2P} + 5.5	V
V_{OUT}	Output voltage		-0.3	6	V
V_{BATP}	Voltage on battery positive terminal	Referenced to VBATN	-0.3	6	V
V_{BATN}	Voltage on battery negative terminal	Referenced to AGND	-0.3	0.3	V
V_{OUTS}	Output voltage sense pin		-0.3	6	V
V_{SYS}	System voltage		-0.3	6	V
V_{PWREN}	Power enable voltage limit		-0.3	V_{AVDD} + 0.3	V
V_{PIN}	All other pins		-0.3	V_{AVDD} + 0.3	V
V_{ESD_HBM}	Electrostatic discharge (ESD) protection	Human Body Model (HBM)	2000		V

Note 1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2 dV_{IN}/dt must be slower than 1 V/µs. The device is not operational (charging) above V_{OV_ACT}.

6 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating temperature		-40		85	°C
V_{IN_ACT}	Input supply voltage	In ACTIVE mode	5.5		10.5	V
V_{IN_IDLE}		In IDLE mode	4.5		13.5	V
V_{BAT}	Battery voltage		2.4		5.5	V
V_{SYS}	System voltage		2.5		5.5	V

7 Electrical Characteristics

Electrical characteristics table limits are guaranteed by production testing, design, or correlation using standard statistical quality control methods unless otherwise stated. Typical (Typ) specifications are mean or average values at 25 ºC and are not guaranteed. Unless otherwise noted, the parameters listed in Table 5 to Table 16 are valid for T_A = -40 ºC to +85 ºC, V_{IN} = 4.5 V to 13.5 V.

7.1 Current Consumption

Table 5: Current Consumption Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{Q_SHIP}	Current drawn from OUT1, OUT2, VOUTS, and VBATP (combined) in SHIP mode (Note 1)	SHIP mode, VBAT = 3.8 V, VIN = 0 V, VSYS = 0 V		3		µA
$I_{Q\_NO\_PWR}$	Current drawn from SYS in NO-POWER mode	NO-POWER mode, V_{BAT} = 3.8 V		25		µA
$I_{Q\_IDLE\_LP}$	Current drawn from SYS in IDLE_LP mode	IDLE_LP mode, V_{SYS} = 3.8 V		110		µA
I_{Q_IDLE}	Current draw from VINS in IDLE mode	IDLE mode, V_{INS} = 8 V		1.4		mA

Note 1 In SHIP mode the battery is connected but the system rail and input rails are not powered (= 0 V).

7.2 Travel Adaptor Detection

Table 6: Travel Adaptor Detection Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{THR_RISE}	Adaptor detection rising threshold	Rising threshold in IDLE mode (Note 1)	4.07	4.29	4.5	V
$V_{THR\_RISE\_ACC}$	Adaptor detection rising threshold accuracy		-5		+5	%
$t_{DEGLITCH}$	Adaptor detection deglitch time			1.25		ms
V_{THR_HYS}	Adaptor detection hysteresis			300		mV

Note 1 The device is only operational when V_{IN} is within the range defined by V_{IN2OUT_MIN} and V_{IN2OUT_MAX}, see Table 9.

7.3 Voltage Protection

7.3.1 Input Voltage Protection

Table 7: Input Voltage Protection Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OV_IDLE}	V_{IN} over-voltage threshold	Rising threshold in IDLE mode (Note 1)	13.5		14.2	V
V_{OV_ACT}		Rising threshold during current doubler operation (ACTIVE mode) (Note 1)	10.5			V
$t_{DEGLITCH\_OV}$	V_{IN} over-voltage deglitch time			10		µs
V_{UV_RISE}	V_{IN} under-voltage threshold	Rising threshold, during current doubler operation (ACTIVE mode) (Note 1)		5.5		V
V_{UV_FALL}		Falling threshold, during current doubler operation (ACTIVE mode) (Note 1)		5.1		V
$t_{DEGLITCH\_UV}$	V_{IN} under-voltage deglitch time			10		µs
V_{PROT_HYS}	V_{IN} protection hysteresis (applies to V_{OV_IDLE} and V_{OV_ACT})			2		%
R_{PD}	IN pull-down			20		kΩ

Note 1 The device is only operational when V_{IN} is within the range defined by V_{IN2OUT_MIN} and V_{IN2OUT_MAX}, see Table 9.

7.3.2 Battery Voltage Protection

Table 8: Battery Protection Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OV_HI}	Over-voltage threshold	Rising threshold VBAT_OV_THRSH = 0x3C		5.5		V
V_{OV_LO}		Rising threshold VBAT_OV_THRSH = 0x0		4.0		V
$t_{DEGLITCH\_OV}$	Battery over-voltage protection deglitch delay			5		µs
V_{UV_HI}	Under voltage threshold	Falling threshold VBAT_UV_THRSH = 11		3.0		V
V_{UV_LO}		Falling threshold VBAT_UV_THRSH = 00		2.4		V
$V_{BAT\_PROT\_HYS}$	V_{BAT} protection hysteresis			2		%
$V_{BAT\_PROT\_ACC}$	V_{BAT} protection accuracy	VBAT_OV (4 V to 5.5 V)	-2		+2	%
		VBAT_UV (2.4 V to 3 V)	-4		+4	%
$t_{DEGLITCH\_UV}$	Battery under-voltage protection deglitch delay			5		µs
V_{WARN_HI}	V_{BAT} warning threshold	VBAT_WARN_THRSH = 0XF0		5.5		V
V_{WARN_LO}		VBAT_WARN_THRSH = 0X10		2.4		V

7.3.3 Input to Output Voltage Protection

Table 9: Input to Output Voltage Protection Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IN2OUT_MIN}	Minimum input-to-output voltage	$V_{IN}/2$ to V_{OUT} falling threshold		5		mV
V_{IN2OUT_MAX}	Maximum input-to-output voltage	$V_{IN}/2$ to V_{OUT} rising threshold		200		mV
$V_{IN2OUT\_MAX\_ACC}$	Protection accuracy		-20		+20	mV
V_{IN2OUT_HYS}	V_{IN2OUT} hysteresis			20		%

7.4 Current Sensing

Table 10: Current Sensing Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
DA9318L						
$I_{IN\_OC\_HI}$	I_{IN} over-current threshold	IIN_OC_THRSH = 0xF0		4.1		A
$I_{IN\_OC\_LO}$		IIN_OC_THRSH = 0x10		500		mA
$I_{IN\_ACC\_HI}$	I_{IN} current sensing accuracy	I_{IN} = 2 A to 4 A	-5		+5	%
$I_{IN\_ACC\_LO}$		I_{IN} = 500 mA to 2 A	-100		+100	mA
$I_{OUT\_ACC\_HI}$	I_{OUT} current sensing accuracy	I_{OUT} = 4 A to 8 A	-5		+5	%
$I_{OUT\_ACC\_LO}$		I_{OUT} = 1 A to 4 A	-200		+200	mA
DA9318M						
$I_{IN\_OC\_HI}$	I_{IN} over-current threshold	IIN_OC_THRSH = 0xF0		5.1		A
$I_{IN\_OC\_LO}$		IIN_OC_THRSH = 0x10		500		mA
$I_{IN\_ACC\_HI}$	I_{IN} current sensing accuracy	I_{IN} = 2 A to 5 A	-10		+10	%
$I_{IN\_ACC\_LO}$		I_{IN} = 500 mA to 2 A	-100		+100	mA
$I_{OUT\_ACC\_HI}$	I_{OUT} current sensing accuracy	I_{OUT} = 4 A to 10 A	-10		+10	%
$I_{OUT\_ACC\_LO}$		I_{OUT} = 1 A to 4 A	-200		+200	mA

7.5 Junction Temperature Monitoring

Table 11: Junction Temperature Monitoring Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_{POR}	Power on reset (POR) temperature threshold	Rising threshold		150		°C
T_{POR_HYS}	POR temperature hysteresis			5		°C
T_{CRIT}	Critical temperature threshold	Rising threshold		140		°C
T_{CRIT_HYS}	Critical temperature hysteresis			5		°C
T_{WARN_HI}	Warning temperature threshold	Rising threshold TJUNC_WARN_THRSH = 11		120		°C
T_{WARN_LO}		Rising threshold TJUNC_WARN_THRSH = 00		70		°C

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_{WARN_HYS}	Warning temperature hysteresis			2		°C
$t_{DEGLITCH}$	Junction temperature monitoring deglitch delay	Applies to T_{POR} and T_{CRIT}		2.8		µs

7.6 Current Doubler

The parameters listed in Table 13 are valid with the following external component values, unless otherwise noted.

Table 12: Current Doubler External Components

Parameter	Description	Conditions	Min	Typ	Max	Unit
C_{FLY}	Flying capacitors			2×47		µF
C_{OUT}	Output capacitors			4.7		µF
C_{LOAD}	Load capacitor				470	µF
C_{BS}	Bootstrap capacitors			10		nF
C_{MID}	Input capacitor			4.7		µF
C_{IN}	Input capacitor			4.7		µF

Table 13: Current Doubler Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IN_IDLE}	Supply voltage	In IDLE mode	4.5		13.5	V
V_{IN_ACTIVE}		In ACTIVE mode	5.5		10.5	V
V_{OUT}	Output voltage	I_{OUT} = 0 A		0.5 * V_{IN}		V
I_{OUT_MAX}	Max output current DA9318L	Continuous output current	8			A
	Max output current DA9318M	Continuous output current	10			A
I_{LIM_PK}	Cycle-by-cycle peak current limit of individual switching FETs	Programmable in 450 mA steps (CP_ILIM)	4.8		11.55	A
$t_{DEGLITCH\_ILIM\_PK}$	Deglitch time for the peak current limit			10		µs
I_{LIM_ACC}	Peak current limit accuracy	C_{F1} ≥ 30 µF, C_{F2} ≥ 30 µF C_{F1} = C_{F2}	-20		+20	%
f_{SW}	Switching frequency	CP_FREQ = 11		1500		kHz
		CP_FREQ = 10		1000		kHz
		CP_FREQ = 01 (default)		500		kHz
		CP_FREQ = 00		250		kHz
η	Current doubler efficiency	V_{OUT} = 4.2 V I_{OUT} = 2 A fixed frequency mode fsw = 500 kHz		98		%

Parameter	Description	Conditions	Min	Typ	Max	Unit
η	Current doubler efficiency	V_{OUT} = 4.2 V I_{OUT} = 6 A fixed frequency mode fsw = 500 kHz		97		%
$R_{DS\_ON\_HS}$	High-side NMOS switch on-resistance	Including pin and routing V_{IN} = 7.4 V		20		mΩ
$R_{DS\_ON\_LS}$	Low-side NMOS switch on-resistance	Including pin and routing V_{IN} = 7.4 V		10		mΩ
t_{RCP}	Response time of the reverse current protection (RCP)			3		µs

7.7 Safety Timer and Watchdog

Table 14: Safety Timer and Watchdog Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{WD}	Watchdog period	Controlled by writing a timeout value to WD_TIMER_LOAD	0		255	s
t_{SFTY_HI}	Safety timer period	SAFETY_TIMER_LOAD = 0xC		18		h
t_{SFTY_LO}		SAFETY_TIMER_LOAD = 0x0		0.25		h
t_{ACC}	Timer accuracy		-10		+10	%

7.8 Digital I/O

Table 15: Digital I/O Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high voltage		1.26			V
V_{IL}	Input low voltage				0.4	V
V_{OL}	Output low voltage	Sink current 5 mA			0.3	V
C_{IN}	Input capacitance				10	pF
$t_{DEGLITCH}$	Deglitch time for inputs			1.25		ms
t_{FLT_MIN}	Minimum pulse width of nFAULT			2		ms

7.9 Interface Timing

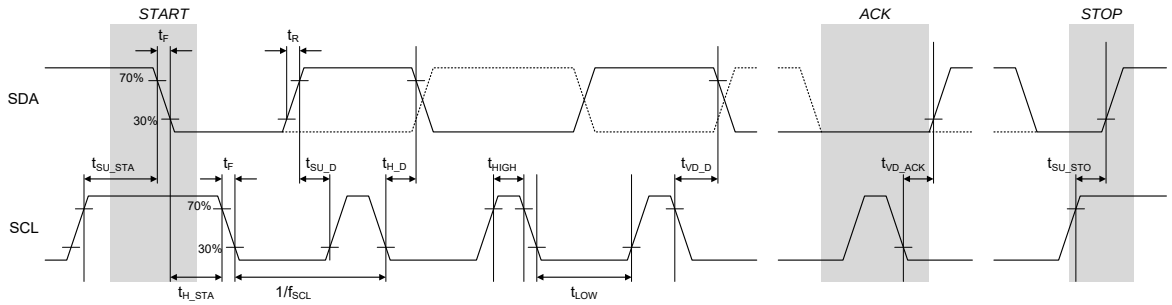

Figure 3: Interface Timing

Unless otherwise noted, the following is valid for T_A = -40 ºC to +85 ºC, V_{IN} = 4.3 V to 11 V, V_{BAT} = 2.6 V to 4.4 V.

Table 16: Interface Timing Characteristics

Parameter	Description	Test conditions	Min	Max	Unit
t_{BUF}	Bus free time from STOP to START condition		0.5		µs
Standard, Fast, and Fast-Plus Modes					
C_B	Bus line capacitive load			150	pF
f_{SCL}	SCL clock frequency	Note 1	0	400	kHz
t_{SU_STA}	Start condition setup time		0.26		µs
t_{H_STA}	Start condition hold time		0.26		µs
t_{W_CL}	SCL low time		0.5		µs
t_{W_CH}	SCL high time		0.26		µs
t_R	2-wire SCL and SDA rise time			120	ns
t_F	2-wire SCL and SDA fall time			120	ns
t_{SU_D}	Data setup time		50		ns
t_{H_D}	Data hold-time		0		ns
t_{SU_STO}	Stop condition setup time		0.26		µs
t_{VD_D}	Data valid time			0.45	µs
t_{VD_ACK}	Data valid acknowledge time			0.45	µs
t_{SP}	Spike suppression (SCL, SDA)	Fast/Fast+ mode		50	ns
High-Speed Mode					
C_B	Bus line capacitive load			100	pF
f_{SCL}	SCL clock frequency	Note 1	0	3400	kHz
t_{SU_STA}	Start condition setup time		160		ns
t_{H_STA}	Start condition hold time		160		ns
t_{SCL_LO}	SCL low time		160		ns
t_{SCL_HI}	SCL high time		60		ns

Parameter	Description	Test conditions	Min	Max	Unit
t_R	2-wire SCL and SDA rise time			80	ns
t_F	2-wire SCL and SDA fall time			80	ns
t_{SU_D}	Data setup time		10		ns
t_{H_D}	Data hold-time		0		ns
t_{SU_STO}	Stop condition setup time		160		ns
t_{SP}	Spike suppression (SCL, SDA)			10	ns

Note 1 Minimum clock frequency is 10 kHz if I2C_TO_EN = 1.

7.10 Internal Supplies

7.10.1 AVDD

The parameters listed in Table 18 are valid with the following external component values, unless otherwise noted.

Table 17: AVDD External Components

Parameter	Description	Conditions	Min	Typ	Max	Unit
C_{AVDD}	Output capacitors			4.7		µF

Table 18: AVDD Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{AVDD}	Internal supply	V_{IN_MAX}, V_{SYS_MAX} > 4.15 V		4.0		V
		V_{SYS} < V_{IN} < 4.15 V		V_{IN} - 0.02		V
		V_{IN} < V_{SYS} < 4.15 V		V_{SYS} - 0.02		V
V_{POR_RISE}	POR threshold	Rising threshold of V_{AVDD}		2.4	2.5	V
V_{POR_FALL}		Falling threshold of V_{AVDD}	2.20	2.33		V

7.11 Thermal Characteristics

Table 19: WLCSP Thermal Ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
Θ_{JA}	Junction-to-ambient thermal resistance	Ambient temperature of 27 °C Device with uniform power dissipation of 1 W Device mounted on 4L Jedec PCB		32.18		°C/W

8 Typical Characteristics

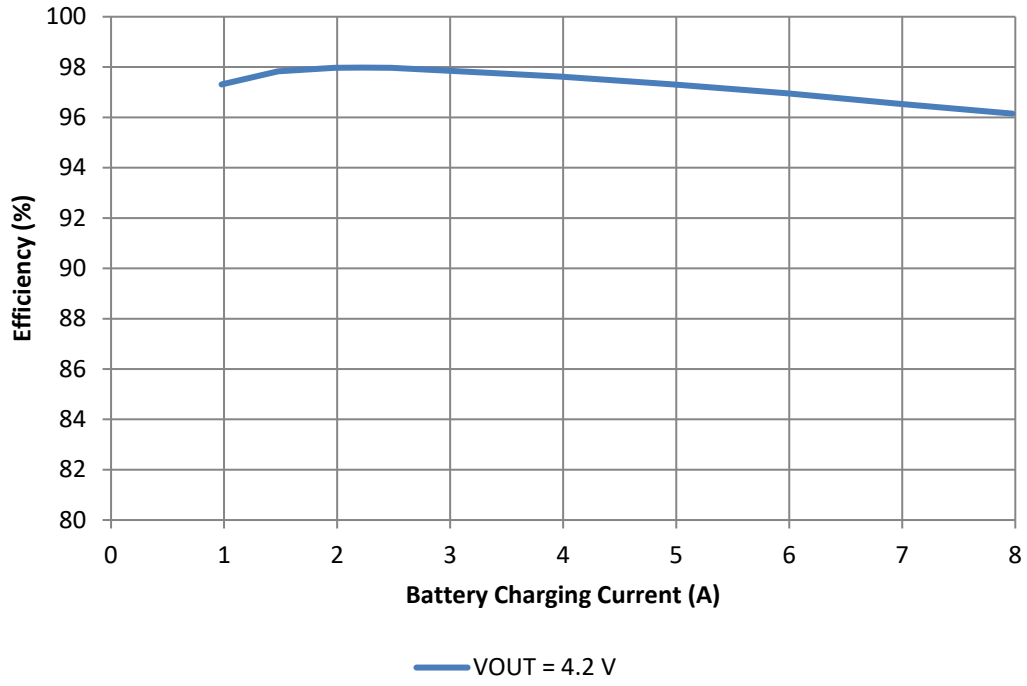

Figure 4: DA9318L Efficiency

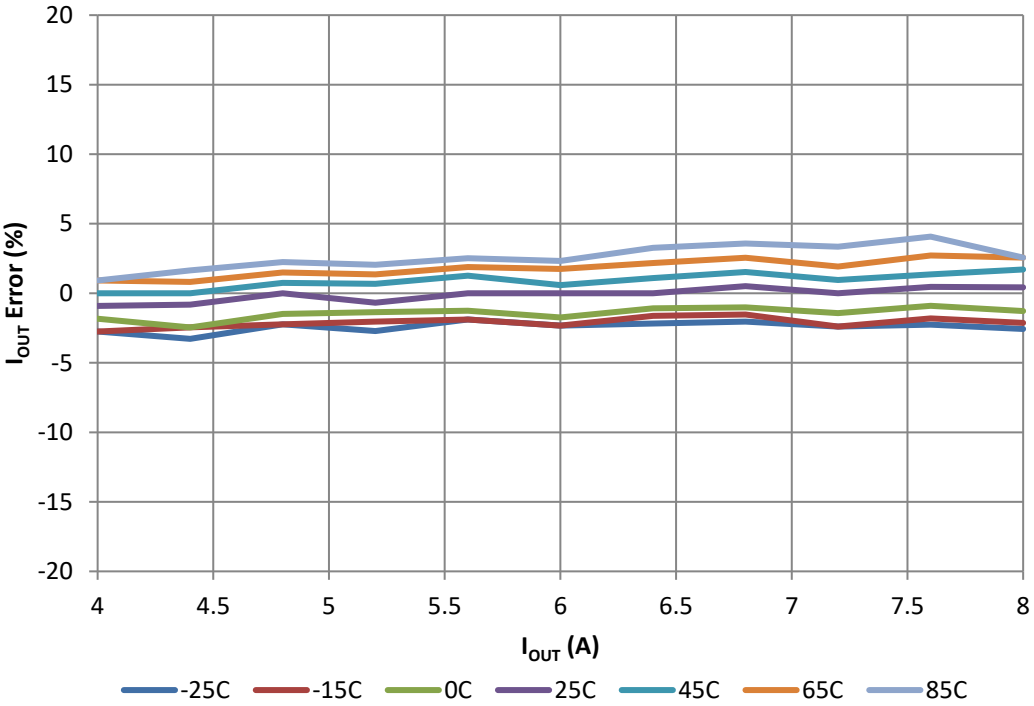

Figure 5: DA9318L I_{OUT} ADC Error vs. I_{OUT} vs. Temperature

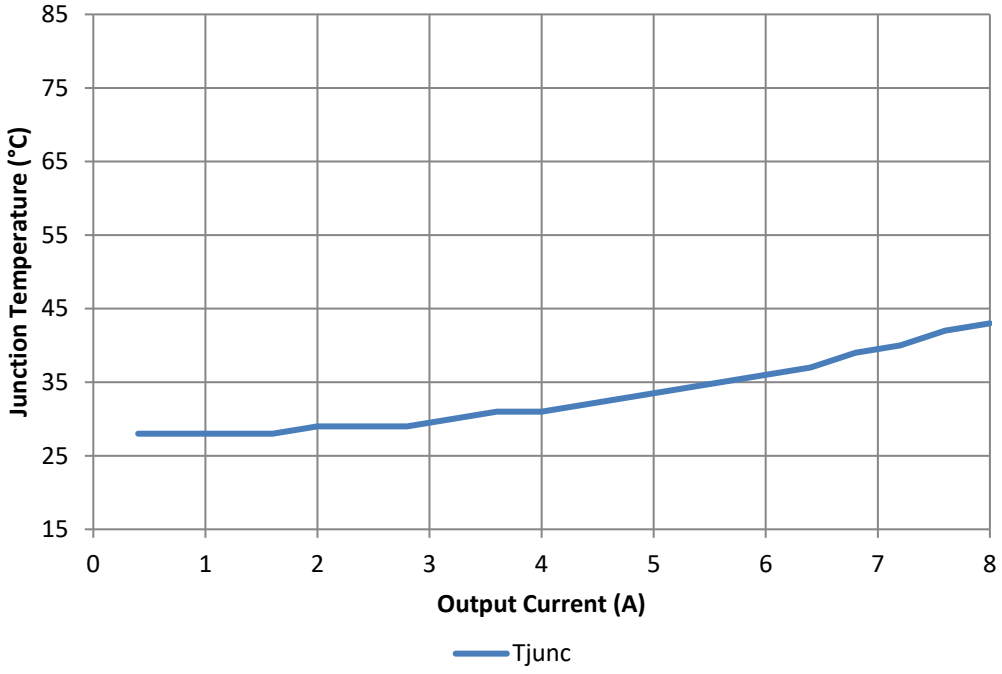

Figure 6: DA9318L Junction Temperature vs. Output Current

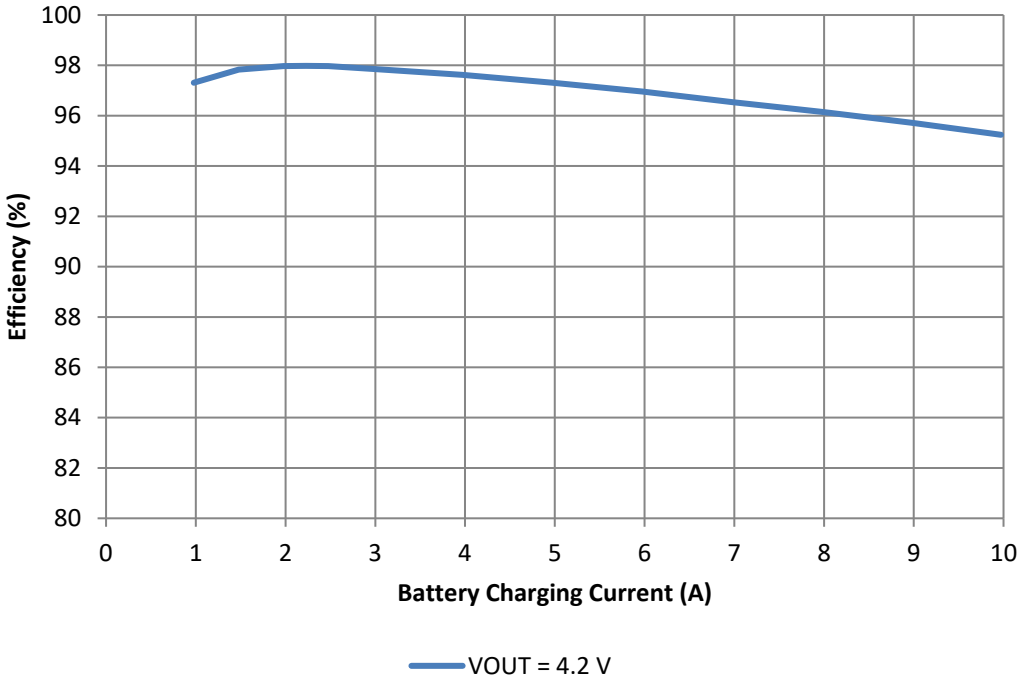

Figure 7: DA9318M Efficiency

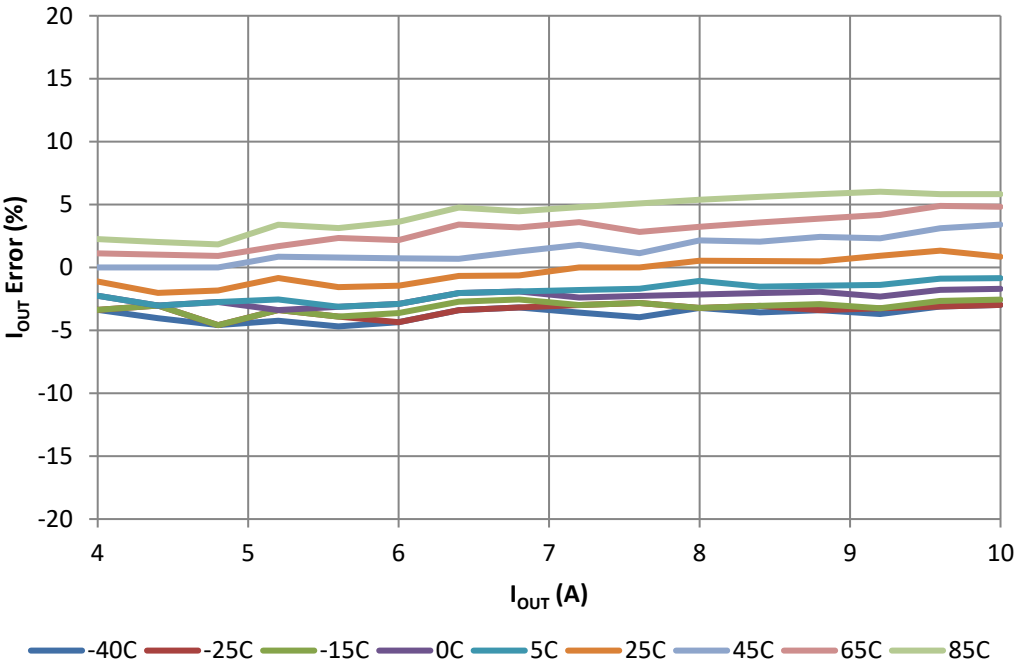

Figure 8: DA9318M I_{OUT} ADC Error vs. I_{OUT} vs. Temperature

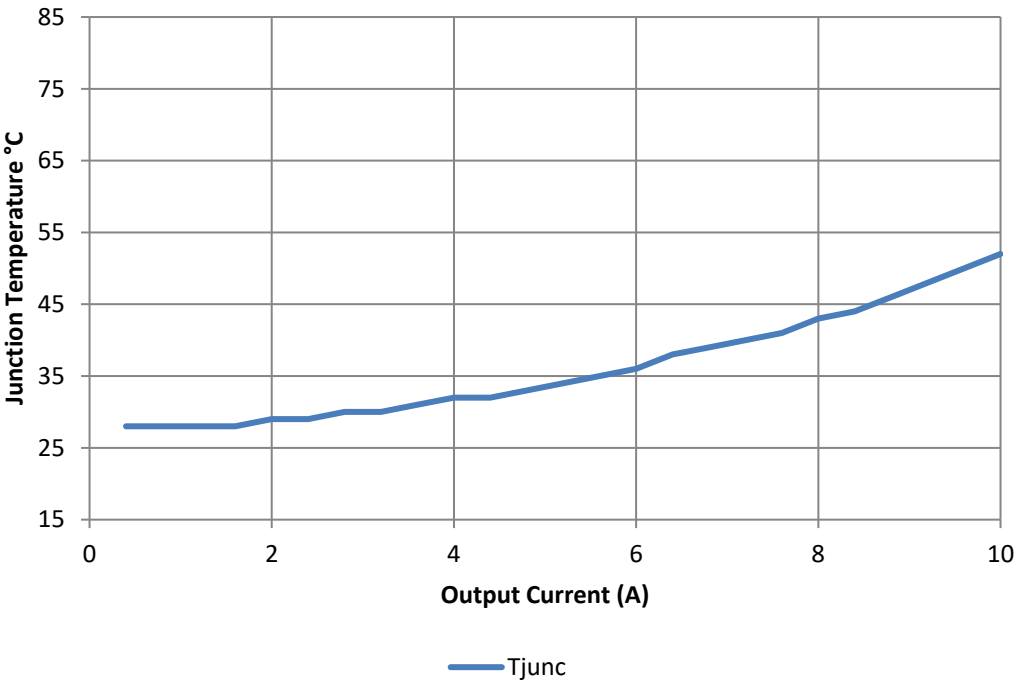

Figure 9: DA9318M Junction Temperature vs. Output Current

9 Functional Description

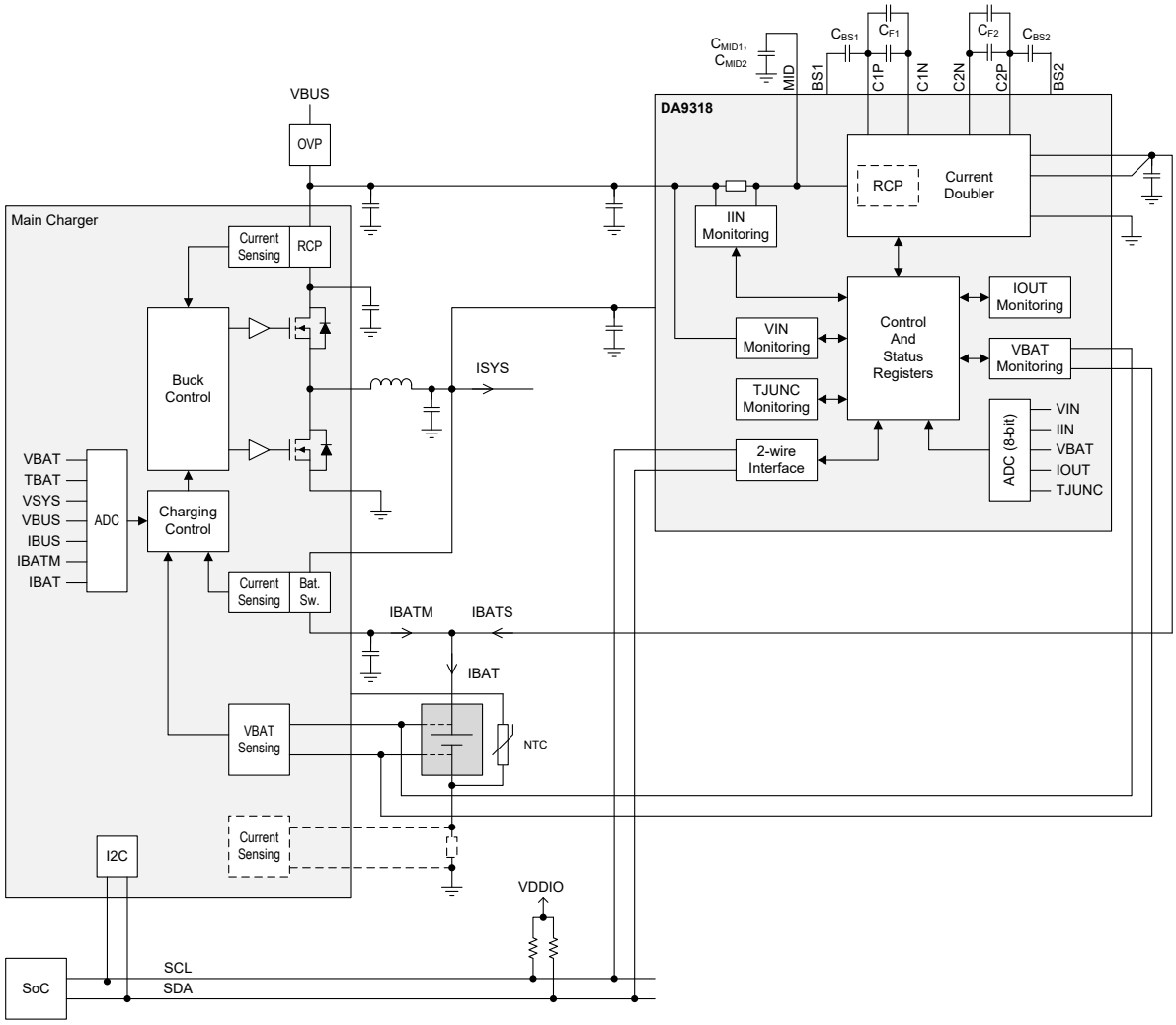

Figure 10: System Level Block Diagram

9.1 Current Doubler

The current doubler operates with a fixed duty cycle. Under no-load condition, the output voltage is half of the input voltage. When a current I_{OUT} is drawn at the V_{OUT} node and the current doubler is switching at an f_{SW} frequency, the output voltage is determined as:

$$V_{OUT} = \frac{V_{IN}}{2} - R_{EQ} * I_{OUT}$$

R_{EQ} is a function of the sum of all resistances in the input/output power path (including the power device's on-resistance and the PCB routing resistance) as well as the switching frequency, CFLY and PCB parasitics.

The dual phase interleaved operation ensures an almost constant input current, thereby highly improving the application design against noise.

The voltage ripple at V_{OUT} can be first order approximated as the voltage drop due to the discharge of the C_{FLY} capacitor in half of the period at an f_{SW} switching frequency, plus the discharge voltage of the output V_{OUT} capacitor during a typical 5 ns short dead time for phase switch.

Selecting a good C_{FLY} capacitor is a key factor for a well performing current doubler. Increasing the switching frequency and the V_{OUT} capacitors to compensate for the DC bias degradation of C_{FLY} may both result in a worse efficiency. For a list of suggested external components see Table 12.

9.1.1 Reverse Current Protection

RCP is enabled whenever DA9318L/M is not in the ACTIVE mode. The current doubler blocks current flow from IN to OUT and from OUT to IN. In this mode, the C1P and C2P terminals are floating.

9.1.2 Switching Frequency

In normal conditions the switching frequency of the current doubler is static and it is defined by the CP_FREQ register bits.

9.1.3 Start-Up

The current doubler is capable of starting up when V_{IN} is within the accepted range defined by V_{IN2OUT_MIN} and V_{IN2OUT_MAX}. If V_{IN} is not within the accepted range during start-up, the start-up is aborted and an event is triggered (E_VIN2OUT_MIN or E_VIN2OUT_MAX).

Resuming normal operation after a start-up fault requires that V_{IN} is within the accepted range and the event is cleared.

9.1.4 Current Limit

The maximum continuous output current of the current doubler is I_{OUT_MAX}. In addition, individual switching FETs are protected with cycle-by-cycle peak current limit of I_{LIM_PK}. The configurable integrated current limit is aimed to protect DA9318L/M power stages and the external components from excessive current.

When hitting the current limit, a timer is started. If the current limit is exceeded for longer than $t_{DEGLITCH\_ILIM\_PK}$, the current doubler is disabled and an event E_ILIM_OC_CRIT is triggered.

9.1.5 Input-to-Output Voltage Protection

DA9318L/M features an input-to-output voltage protection described in section 9.3.3. The protection is used to automatically disable the current doubler when the input-to-output voltage ratio is out of the accepted range defined by V_{IN2OUT_MIN} and V_{IN2OUT_MAX}. When the either of these thresholds is crossed during current doubler operation an event, E_VIN2OUT_MIN or E_VIN2OUT_MAX, is triggered and the current doubler is automatically disabled.

9.2 Travel Adaptor Detection

The detection of a travel adaptor insertion is made based on rising V_{IN} voltage. The detection of a travel adaptor removal is made based on falling V_{IN} voltage.

When V_{IN} exceeds V_{THR_RISE} the travel adaptor status bit S_VIN_ADP_DET is asserted and the associated event (E_VIN_ADP_DET) is triggered. The travel adaptor status bit and the current doubler enable are de-asserted when V_{IN} falls below V_{THR_RISE}.

9.3 Voltage Protection

Figure 11 illustrates the voltage protection, including the V_{IN} and V_{BAT} voltage protection levels. All voltage protection functions have an event associated with them, which is triggered whenever the comparator trips.

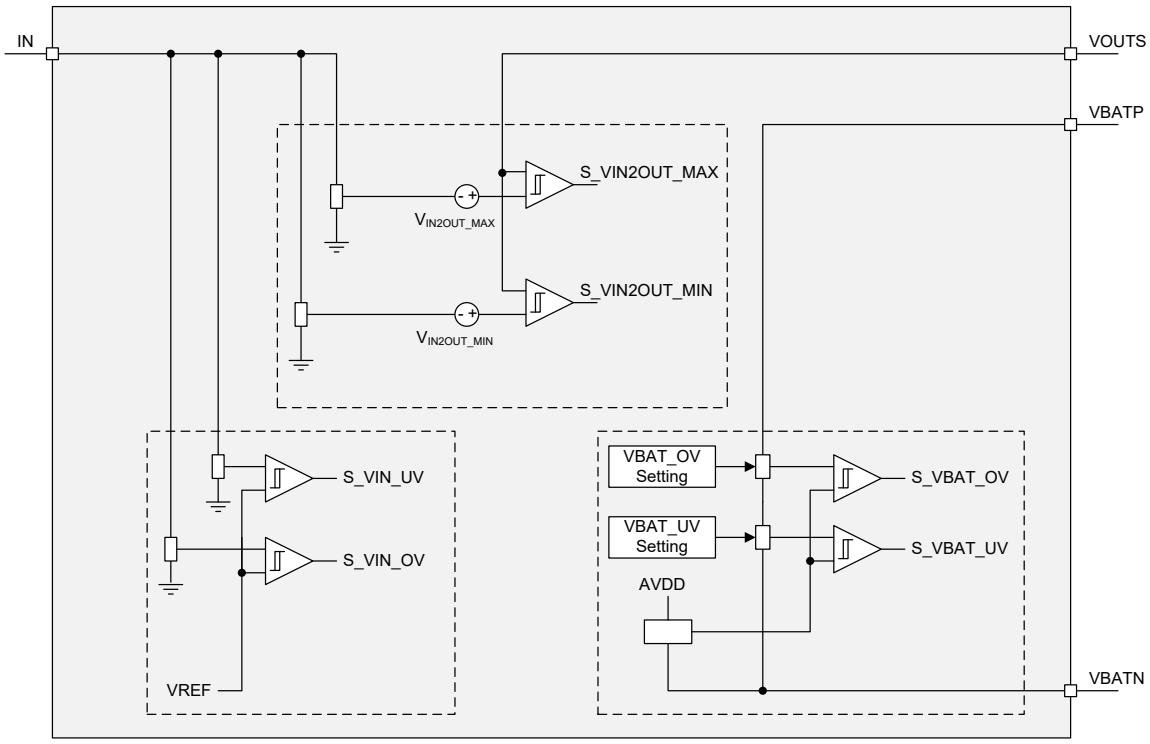

Figure 11: Voltage Protection

9.3.1 Input Voltage Protection

Input voltage (V_{IN}) protection is used for detecting the presence of an input supply and for disabling the current doubler when V_{IN} rises too high. Note that the current doubler is only operational when V_{IN} is within the range defined by V_{IN2OUT_MIN} and V_{IN2OUT_MAX}.

V_{IN} over-voltage conditions longer than $t_{DEGLITCH\_OV}$ will disable the current doubler by disabling CP_EN and will trigger the event E_VIN_OV. Resuming normal operation after the over-voltage event is triggered requires that the event is cleared and that the current doubler is re-enabled either by writing CP_EN or by asserting the nCPEN signal.

Under-voltage conditions longer than $t_{DEGLITCH\_UV}$ will disable the current doubler by disabling CP_EN and trigger the event E_VIN_UV. Resuming normal operation after the under-voltage event is triggered requires that the event is cleared and that the current doubler is re-enabled either by writing CP_EN or by asserting the nCPEN signal.

The adaptor detection is made by comparing V_{IN} to a threshold V_{THR_RISE}. If V_{IN} is above V_{THR_RISE}, a supply is assumed to be detected. When V_{IN} falls under the $V_{THR\_RISE} - V_{THR\_HYS}$, an event E_VIN_UV is triggered and a pull-down resistor (R_{PD}) is activated. Note that V_{THR_RISE} is not enough to start the current doubler, see section 9.1.3. Once the adaptor detection is successful, the threshold of the comparator is moved to V_{UV_RISE}.

9.3.2 Battery Voltage Protection

DA9318L/M features differential sense inputs for the battery voltage. The battery voltage is monitored before enabling the current doubler and during current doubler operation to detect over-voltage and under-voltage conditions.

Over-voltage conditions longer than $t_{DEGLITCH\_OV}$ will disable the current doubler by clearing the CP_EN register and trigger the event E_VBAT_OV. A 20 kΩ pull-down is applied on the OUT pin as long as the status bit S_VBAT_OV remains asserted. Resuming normal operation after the over-voltage event is triggered requires that the event is cleared and that the current doubler is re-enabled either by writing CP_EN or by asserting the nCPEN signal.

Under-voltage conditions longer than $t_{DEGLITCH\_UV}$ will disable the current doubler and trigger the event E_VBAT_UV. Starting the current doubler requires that the event is cleared and that the current doubler is re-enabled either by writing CP_EN or by asserting the nCPEN signal.

In addition to battery over-voltage and under-voltage, DA9318L/M features a battery voltage protection based on the ADC results. In the continuous mode of the ADC converter, the result on the VBAT channel (ADC_VBATT_RESULT) is compared against the threshold programmed in the VBAT_WARN_THRSH register bits. If the measurement exceeds the threshold, an event E_VBAT_WARN is triggered. The battery voltage warnings are only enabled in the continuous mode of the ADC and when the VBAT_WARN_THRSH register bits are programmed with a non-zero value.

9.3.3 Input to Output Voltage Protection

The purpose of the input to output voltage (V_{IN2OUT}) protection is to detect when the input-to-output voltage ratio is suitable for the current doubler operation, see section 9.1.5.

Fault conditions lasting longer than $t_{DEGLITCH}$ will disable the current doubler by clearing the CP_EN register bit and trigger the event E_VIN2OUT_MIN or E_VIN2OUT_MAX. Resuming normal operation after an event is triggered requires that the event is cleared and that the current doubler is re-enabled either by writing CP_EN or by asserting the nCPEN signal.

9.4 Current Sensing

DA9318L/M features input and output current reporting based on the internal current sense. The current sense information is sampled by the ADC and reported via registers ADC_IIN_RESULT and ADC_IOUT_RESULT. The input and output current sensing does not require an external shunt resistor. Table 10 defines the range and precision for current sensing.

9.4.1 Over-Current Monitoring

DA9318L/M features a programmable over-current monitoring that uses the ADC reading of the input current to detect an over-current condition. The monitoring value can be programmed in the IIN_OC_THRSH register bits. The conversion result (reported via the ADC_IIN_RESULT register bits) is compared to the IIN_OC_THRSH value and an over-current event (E_IIN_OC) is triggered if the measurement value exceeds the threshold. The over-current fault can be configured to either trigger the event, or to trigger the event and clear the current doubler enable (CP_EN). The over-current monitoring is only enabled in the continuous mode of the ADC (ADC_AUTO_CNVRT = 1) and if IIN_OC_THRSH is programmed with a non-zero value.

9.5 Junction Temperature Monitoring

To protect DA9318L/M from damage due to excessive power dissipation the junction temperature (T_{JUNC}) is monitored continuously. The monitoring is split into three temperature ranges T_{WARN} (programmable via TJUNC_WARN_THRSH from 70 °C to 125 °C), T_{CRIT} (140 °C), and T_{POR} (150 °C).

The first level monitoring (T_{WARN}) is implemented by using the ADC. If the junction temperature rises above the first threshold (T_{WARN}), the event E_TJUNC_WARN is asserted. If the event is not masked, this will trigger an interrupt. This first level of temperature supervision is intended for non-invasive temperature control, where the necessary measures for cooling the system down are left to the host software. The status of the T_{WARN} comparator can be read from S_TJUNC_WARN. An interrupt is generated when the temperature crosses the threshold from low to high, or from high to low. After the interrupt, the application processor can read out the comparator status to detect when the temperature drops below the threshold.

The second level monitoring (T_{CRIT}) is implemented with a comparator. If the junction temperature continues to rise and crosses the second threshold (T_{CRIT}), an event is triggered (E_TJUNC_CRIT) and DA9318L/M moves to the IDLE mode. Resuming normal operation requires that the junction temperature drops below T_{CRIT}.

The third level monitoring (T_{POR}) is implemented with a comparator. Crossing the third threshold causes DA9318L/M to enter SHUTDOWN mode. DA9318L/M stays in SHUTDOWN mode as long as the junction temperature is above T_{CRIT}.

9.6 ADC

DA9318L/M features an 8-bit ADC that can be used to monitor V_{IN}, I_{IN}, V_{BAT}, I_{OUT}, and T_{JUNC}. Table 20 summarizes the ADC channels. The ADC is enabled in IDLE and ACTIVE modes. It features two operational modes: continuous and single shot.

By default, the ADC runs in the continuous mode (ADC_AUTO_CNVRT = 1). In this mode, the ADC runs continuously through its channels and updates the results registers (ADC_RES_x). The number of conversions averaged for each result can be controlled using the ADC_AVERAGE register bits. An event (E_ADC_DONE) is triggered only once in the continuous mode, when the first results are ready after enabling the ADC or starting the continuous mode.

Measurements can also be taken in single shot mode (ADC_AUTO_CNVRT = 0) via the 2-wire interface by writing 1 to the ADC_SINGLE_CNVRT register bit. Once a conversion is initiated, the result register (ADC_RES_x) of each channel is updated using the averaging set in the ADC_AVERAGE register bits. Once the measurement is done, an event is triggered (E_ADC_DONE) and the measurement of each channel can be read out from the result registers.

Table 20: ADC Channels

Channel	Parameter	Description	Range	Equation
1	V_{IN}	Input voltage	5.5 V to 14 V	V_{IN} = (ADC_VIN_RESULT - 16) * (8.5 / 224) + 5.5
2	V_{BAT}	Battery voltage	2.4 V to 5.5 V	V_{BAT} = (ADC_VBATT_RESULT - 16) * (3.1 / 224) + 2.4
3	I_{IN}	Input current DA9318L	500 mA to 4.1 A	I_{IN} = (ADC_IIN_RESULT - 16) * (3.6 / 224) + 0.5
		Input current DA9318M	500 mA to 5.1 A	I_{IN} = (ADC_IIN_RESULT - 16) * (4.6 / 224) + 0.5
4	I_{OUT}	Output current DA9318L	1 A to 8.2 A	I_{OUT} = (ADC_IOUT_RESULT - 16) * (7.2 / 224) + 1
		Output current DA9318M	1 A to 10.2 A	I_{OUT} = (ADC_IOUT_RESULT - 16) * (9.2 / 224) + 1
5	V_{OUT}	Output voltage (V_{OUTS})	2.4 V to 5.5 V	V_{OUT} = (ADC_VOUT_RESULT - 16) * (3.1 / 224) + 2.4
6	T_{JUNC}	Junction temperature	0 °C to 255 °C	T_{JUNC} = ADC_TJUNC_RESULT

9.7 Safety Timer

A safety timer is running whenever DA9318L/M is in ACTIVE mode. The purpose of the safety timer is to detect a condition where the battery does not react to charging as expected. For example, if the voltage of the battery does not rise during constant current charging it is likely that the battery is damaged. This condition is detected by the safety timer.

The safety timer is automatically enabled whenever DA9318L/M moves to the ACTIVE mode. If the safety timer expires an event is triggered (E_SAFETY_TIMER) and CP_EN is cleared. Note that the safety timer count is only reset by writing the SAFETY_TIMER_LOAD register. The SAFETY_TIMER_LOAD register should be written before the start of a new charging cycle.

Restarting the current doubler after a safety timeout requires that the timeout event is cleared and that the CP_EN bit is asserted.

The following conditions will disable the safety timer:

- V_{IN} supply removal
- Other fault condition (V_{OV_ACT}, V_{UV_RISE}, VBAT_OV_THRSH, VBAT_UV_THRSH, T_{CRIT})

9.8 Watchdog Timer

DA9318L/M features a watchdog timer that is intended to monitor the host software during charging and disable the charger in the event of system malfunction. Some of the automatic charging features of DA9318L/M, such as battery temperature profiling, can be disabled and implemented in software instead. Moving the control to software requires tighter supervision than is provided by the charging timer, therefore a separate watchdog timer is provided.

Whenever the charger is enabled, the watchdog timer is loaded (via I^2C) with a pre-programmed value (WD_TIMER_LOAD) which starts decrementing. In normal operation the application processor should periodically re-initialize the safety timer by writing a new value to the WD_TIMER_LOAD register bits. The value of the counter can be read from the WD_TIMER_COUNT register bits. However, if the timer reaches zero an event (E_WD) is asserted and the charger is automatically disabled.

The following conditions will disable the watchdog timer:

- V_{IN} supply removal
- Other fault condition (V_{OV_ACT}, V_{UV_RISE}, VBAT_OV_THRSH, VBAT_UV_THRSH, T_{CRIT})

9.9 Control Interface

All the output signals of DA9318L/M are driven with an open drain stage. The signals have to be pulled up with external resistors to an IO supply. The inputs are compared to internally generated references V_{IH} and V_{IL} to detect the high and low levels of the signals, respectively. Figure 12 depicts the structure of the control signals.

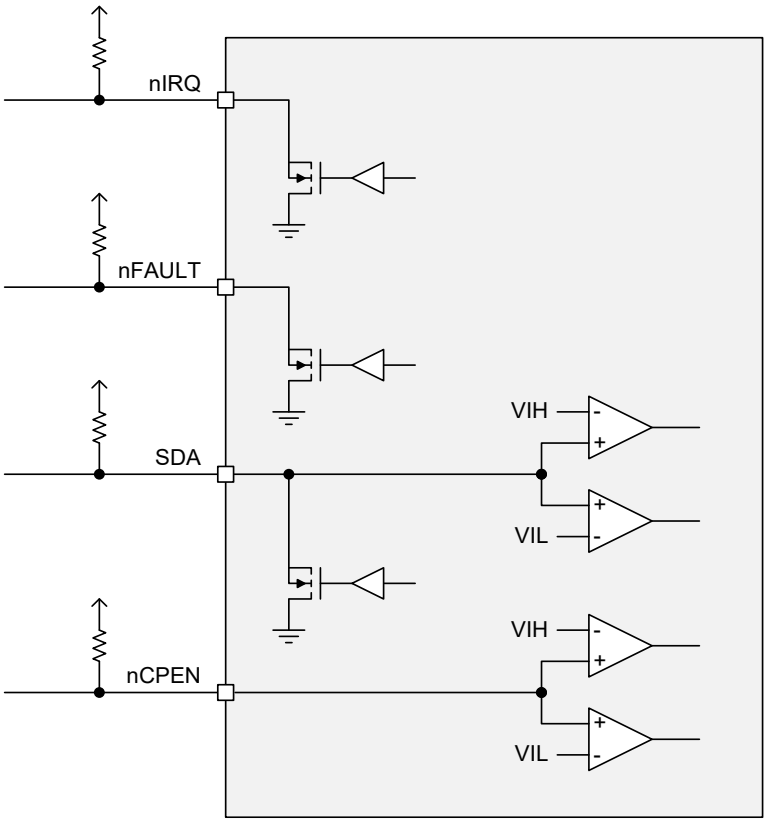

Figure 12: Control Signals

9.9.1 PWREN

PWREN is a master enable for the DA9318L/M internal blocks and 2-wire interface. It is used to minimize the power consumption of DA9318L/M during NO-POWER mode of the system. It can be tied to a supply rail driven by the PMIC to allow DA9318L/M enter NO-POWER mode whenever the PMIC powers down.

9.9.2 nCPEN

nCPEN is an edge sensitive, active low, chip enable signal. It works in conjunction with the CP_EN register bit. A falling edge of nCPEN sets the CP_EN register bit and a rising edge clears it. The current doubler can be started by asserting the nCPEN pin or by writing to CP_EN. The current doubler can be stopped by de-asserting the nCPEN pin or by writing to CP_EN.

9.9.3 nFAULT

nFAULT is an active low, open drain, status output. The assertion of any of the following status bits results in the assertion of nFAULT:

- S_VIN_OV
- S_VIN_UV
- S_VBAT_OV
- S_VBAT_UV
- S_VIN2OUT_MAX
- S_VIN2OUT_MIN
- S_TJUNC_CRIT

- S_IIN_OC
- S_VBAT_WARN

The removal of the fault condition results in the de-assertion of nFAULT. The minimum length of nFAULT assertion is t_{FLT_MIN}. This will ensure that the signal passes through the deglitch filter and synchronizer in the receiving end.

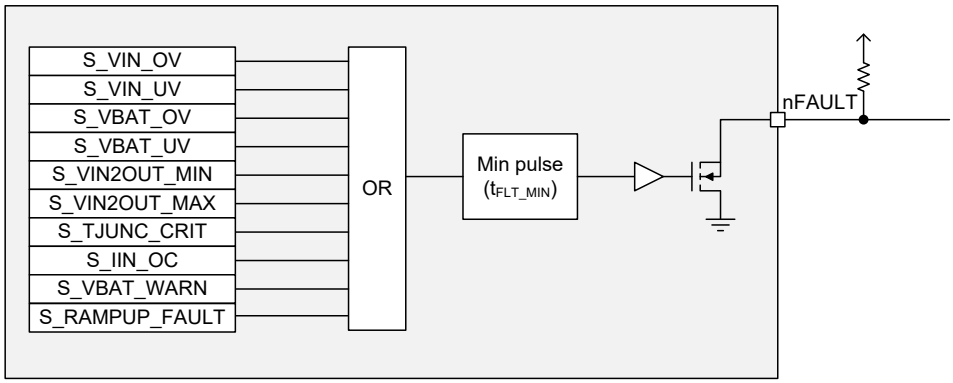

Figure 13: nFAULT Operation

9.9.4 nIRQ

nIRQ is a level sensitive, active low, interrupt signal. The assertion of an unmasked event results in the assertion of nIRQ. The nIRQ will not be released until all event registers have been cleared. New events that occur during an event register read will be held until the event register has been cleared, ensuring that the host processor does not miss them. By default all mask bits are asserted.

Several sources can generate some events, as depicted in Figure 14. After receiving an interrupt, the source can be detected by reading the associated status registers.

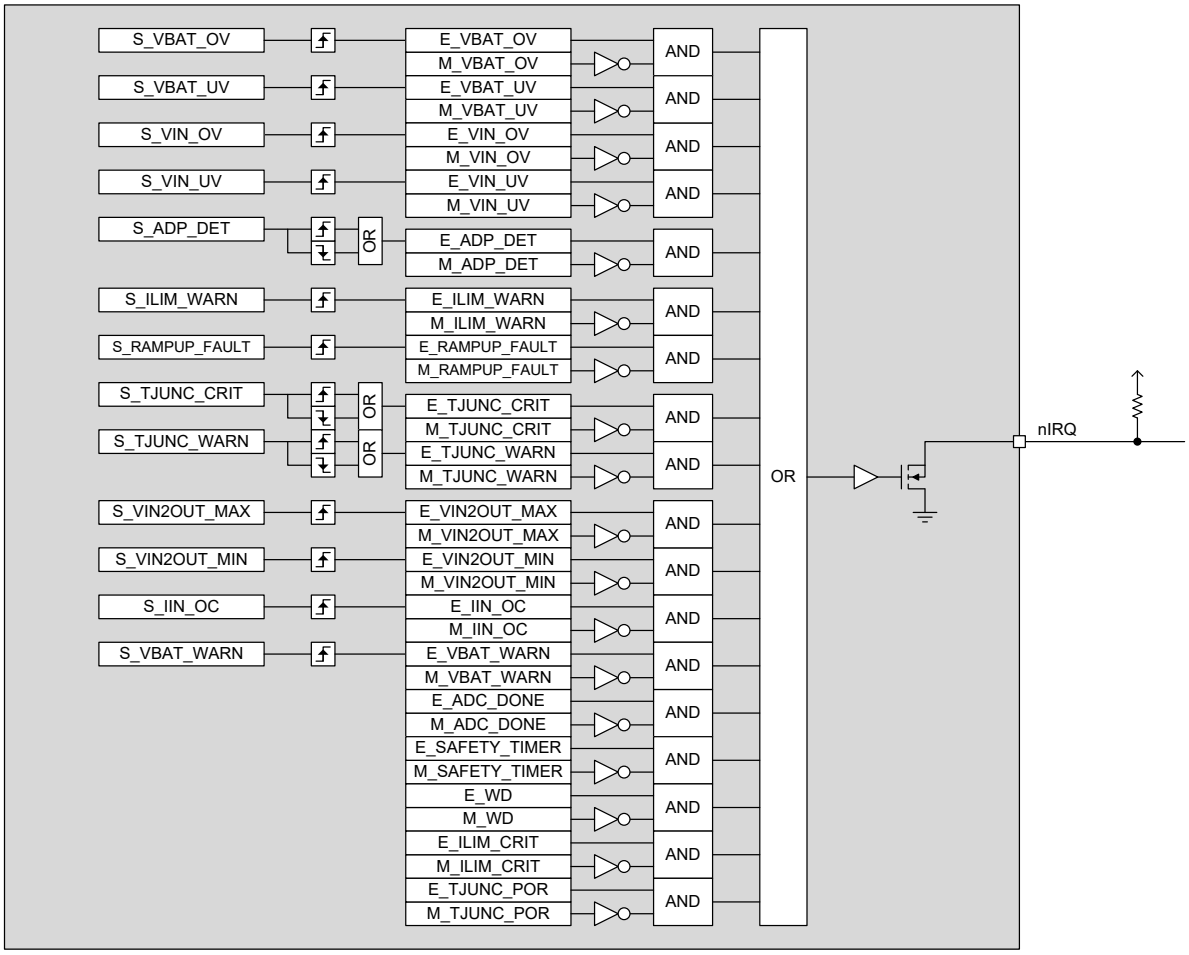

Figure 14: Interrupt Logic

9.10 2-Wire Interface

The 2-wire interface provides access to control and status registers. The interface supports operations compatible to Standard, Fast, Fast+ and High-speed mode of the I²C bus specification [6]. Table 21 lists the slave addresses of DA9318L/M.

Table 21: Interface Slave Address.

Device	7-bit Slave Address	8-bit Slave Address
DA9318L/M	0x59	0xB2 (write), 0xB3 (read)

Communication on the 2-wire bus is always between two devices, one acting as the master and the other as the slave. DA9318L/M will only operate as a slave.

SCL carries the 2-wire clock and SDA carries the bidirectional data. The 2-wire interface is open drain, supporting multiple devices on a single line. The bus lines have to be pulled high by external pull-up resistors (2 kΩ to 20 kΩ). These are often shared between multiple devices connected to the interface. The attached devices only drive the bus lines low by connecting them to ground. As a result, two devices cannot conflict if they drive the bus simultaneously.

In Standard/Fast mode the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and it does not have any relation to the DA9318L/M internal clock signals. DA9318L/M will follow the host clock speed within the described limitations and does not initiate any clock arbitration or slow down. An automatic interface reset can be triggered in case the clock signal ceases to toggle for > 35 ms (controlled in I2C_TO_EN).

Bus clear, if the SDA is stuck, is achieved after receiving nine clock pulses. Operation in High-speed mode at 3.4 MHz requires a minimum interface supply voltage of 1.8 V and a mode change in order to enable spike suppression and slope control characteristics compatible to the I^2C specification. The High-speed mode can be enabled on a transfer-by-transfer basis by sending the master code (0000 1XXX) at the beginning of the transfer. DA9318L/M does not make a use of clock stretching and delivers read data without additional delay up to 3.4 MHz.

Alternatively the interface can be configured to use High-speed mode continuously via I2C_IF_HSM, so that the master code is not required at the beginning of every transfer. This reduces communication overhead on the bus, but limits the attachable bus slaves to compatible devices.

9.10.1 Details of the 2-Wire Protocol

All data is transmitted across the 2-wire bus in 8-bit groups. To send a bit the SDA line is driven at the intended state while the SCL is low. Once the SDA has settled, the SCL line is brought high and then low. This pulse on SCL clocks the SDA bit into the receiver's shift register.

A two byte serial protocol is used containing one address byte and one data byte. Data and address transfer is transmitted MSB first for both read and write operations. All transmission begins with the START condition from the master during which the bus is in IDLE mode (the bus is free). It is initiated by a high-to-low transition on the SDA line, while the SCL is in the high state. A low-to-high transition on the SDA line, while the SCL is in the high state, indicates a STOP condition. Figure 15 illustrates the START and STOP conditions.

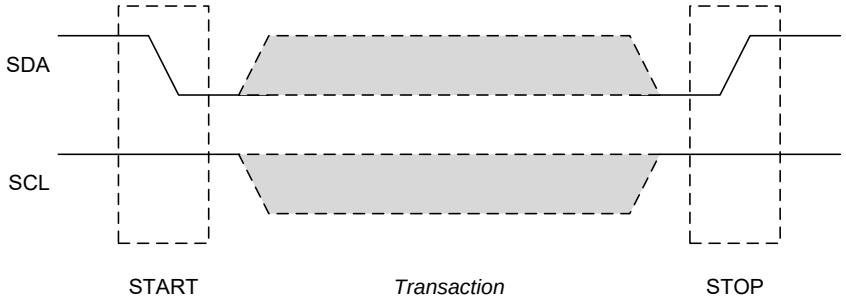

Figure 15: START and STOP Condition Timing

The 2-wire bus will be monitored by DA9318L/M for a valid slave address whenever the interface is enabled. It responds immediately when it receives its own slave address. This is acknowledged by pulling the SDA line low during the following clock cycle (white blocks marked with A in the following figures).

The protocol for a register write from master to slave consists of a START condition, a slave address, a read/write-bit, 8-bit address, 8-bit data, and a STOP condition. DA9318L/M responds to all bytes with an A. Figure 16 illustrates a register write operation.

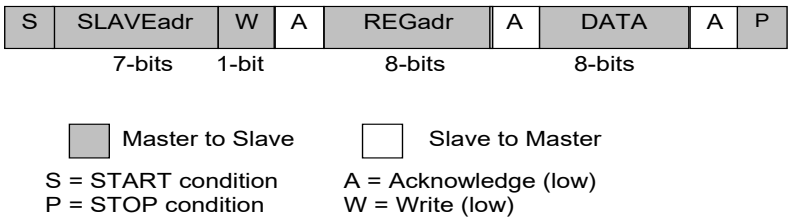

Figure 16: Byte Write

When the host reads data from a register it first has to write access DA9318L/M the target register address and then read access DA9318L/M with a Repeated START, or alternatively a second START, condition. After receiving the data, the host sends No Acknowledge and terminates the transmission with a STOP condition, see Figure 17.

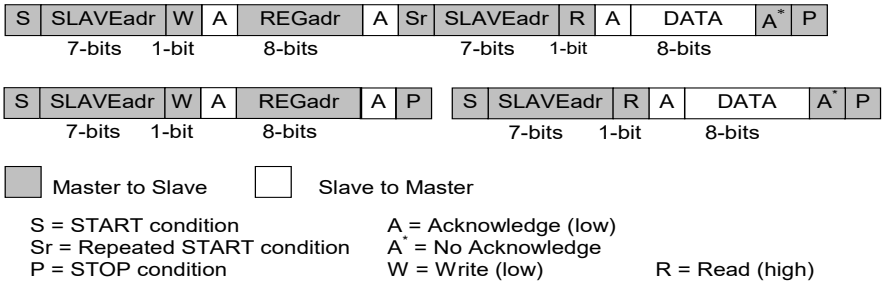

Figure 17: Byte Read

Consecutive (page) read-out mode is initiated from the master by sending an A instead of No Acknowledge after receiving a byte, see Figure 18. The 2-wire control block then increments the address pointer to the next register addresses and sends the data to the master. This enables an unlimited read of data bytes until the master sends No Acknowledge directly after receiving the data, followed by a subsequent STOP condition. If a non-existent 2-wire address is read out then DA9318L/M will return code zero.

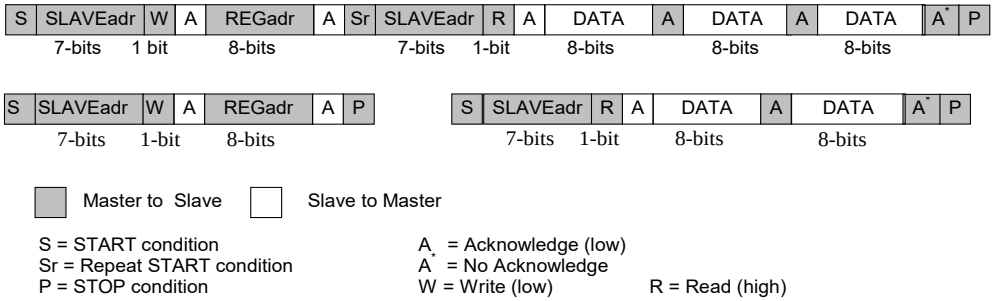

Figure 18: Page Read

The slave address after the Repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the master sends several data bytes following a slave register address. The 2-wire control block then increments the address pointer to the next 2-wire address, stores the received data, and sends an A until the master sends a STOP condition. Figure 19 illustrates the page write mode.

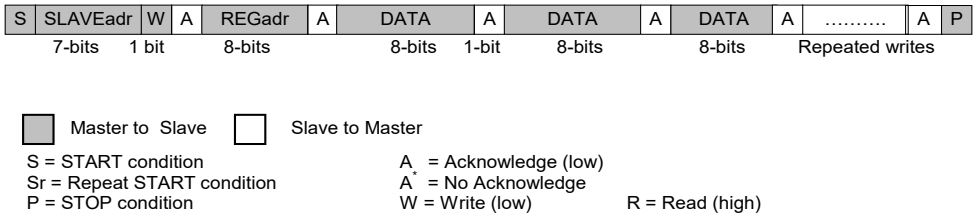

Figure 19: Page Write

Via control WRITE_MODE, a repeated write mode can be enabled. In this mode, the master can execute back-to-back write operations to non-consecutive addresses. This is achieved by transmitting register address and data pairs. The data will be stored in the address specified by the preceding byte. Figure 20 illustrates the repeated write mode.

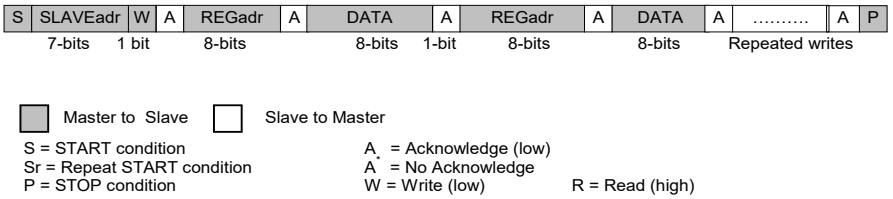

Figure 20: Repeated Write

If a new START or STOP condition occurs within a message, the bus will return to IDLE mode.

9.11 Internal Supplies

The internal supply of DA9318L/M is illustrated in Figure 21, the AVDD regulator is powered from IN and SYS.

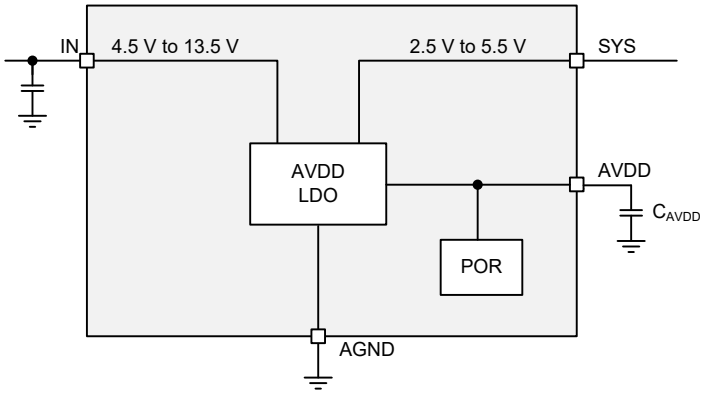

Figure 21: Internal Supply

9.11.1 AVDD

AVDD is an internal supply that is powered from the higher of IN and SYS. During current doubler operation the input supply to the AVDD regulator is IN and the output voltage is 4 V. If IN is not supplied, the input supply to the AVDD regulator is SYS. If V_{SYS} is not high enough to supply the normal 4 V, the pass device of the AVDD regulator operates as a switch. DA9318L/M remains operational as long as V_{AVDD} is above the POR threshold V_{POR_FALL}.

9.12 Internal Oscillator

The internal high-speed oscillator generates a signal at f_{OSC}, the internal 6 MHz clock reference. In the IDLE_LP mode the oscillator goes in to a low-power state and changes the frequency to 1 MHz.

9.13 Power Modes

Figure 22 illustrates the power modes of DA9318L/M. The following transitions are high priority and override other transitions in the diagram:

- Critical junction temperature ($T_{JUNC} > T_{CRIT}$)
- Transition to IDLE mode
- Missing supply ($V_{AVDD} < V_{POR\_FALL}$)
- Transition to NO-POWER mode

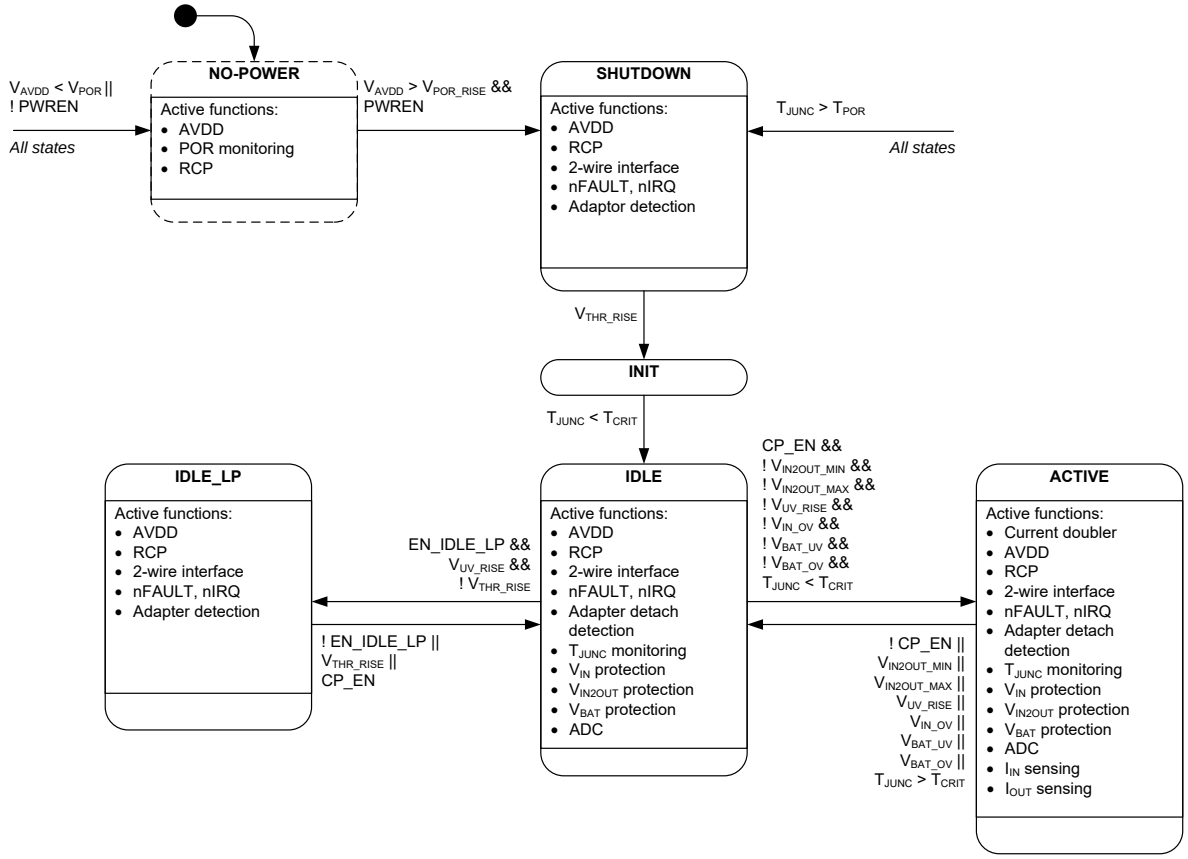

Figure 22: Power Modes

9.13.1 NO-POWER Mode

DA9318L/M is in NO-POWER mode when V_{AVDD} is below the V_{POR_RISE} threshold. RCP is active, as described in section 9.1.1. When IN or SYS is supplied and PWREN is de-asserted, the internal supply AVDD is automatically enabled and when V_{AVDD} rises above the V_{POR_RISE} threshold, DA9318L/M moves to the INIT (initialization) mode.

9.13.2 SHUTDOWN Mode

The SHUTDOWN mode activates the internal oscillator, adaptor detection, 2-wire interface, and output signals. The 2-wire interface is operational, but as the initialization is not completed, all registers will return their power-on-reset values. Transition to INIT mode is triggered when a travel adaptor is detected.

9.13.3 INITIALIZATION Mode

In the INIT mode, the internal reference, oscillator, and clock generator are enabled. RCP is active, as described in section 9.1.1. DA9318L/M goes through a full initialization including an OTP read. After the initialization is complete, the status registers and events are updated to match the status of the internal protections. The junction temperature is checked, and if it is below the critical level (T_{CRIT}), DA9318L/M moves automatically to the IDLE mode.

9.13.4 IDLE Mode

In the IDLE mode DA9318L/M is fully operational but the current doubler is not enabled. RCP is active, as described in section 9.1.1.

If the current doubler is enabled (CP_EN = 1), DA9318L/M enables monitoring features and evaluates the conditions for start-up:

- Junction over-temperature (junction temperature exceeds T_{CRIT})
- Output voltage (VBAT_UV_THRSH < V_{BAT} < VBAT_OV_THRSH)
- Input voltage (V_{UV_RISE} < V_{IN} < V_{OV_ACT})
- Input to output voltage (V_{IN2OUT_MIN}, V_{IN2OUT_MAX})

If the conditions are met, DA9318L/M soft-starts the current doubler and moves to the ACTIVE mode.

If IN is not supplied, the current doubler is disabled (EN_IDLE_LP = 1) and DA9318L/M moves to the LOW-POWER IDLE mode.

9.13.4.1 LOW-POWER IDLE Mode

The LOW-POWER IDLE (IDLE_LP) mode is a low power sub-mode of the IDLE mode. In IDLE mode DA9318L/M is fully operational but the current doubler is not enabled. RCP is active, as described in section 9.1.1. In IDLE-LP mode, most DA9318L/M features are disabled in order to minimize the quiescent current. The only active functions are the AVDD regulator, which ensures the preservation of the logic state, the V_{THR_RISE} monitoring which detects the assertion of a travel adaptor, and the 2-wire interface. RCP is active.

The reduced functionality has the consequence that the status bits in the register map are not automatically updated. Otherwise, IDLE-LP mode is transparent to the system. DA9318L/M reacts identically to register writes and external events in both modes.

A transition to IDLE mode is triggered if an input supply is attached and the current doubler is enabled.

The transition to IDLE-LP mode can be also controlled with the EN_IDLE_LP bit. By writing EN_IDLE_LP = 0, DA9318L/M never transitions to IDLE-LP mode. If already in IDLE-LP mode, writing EN_IDLE_LP = 0 triggers a transition to IDLE mode.

9.13.5 ACTIVE Mode

In ACTIVE mode the current doubler is enabled. DA9318L/M moves back to IDLE mode in any of the following circumstances:

- The current doubler is disabled (CP_EN = 0)
- The input supply is outside the supported range
- The junction temperature exceeds the critical threshold
- The battery voltage is outside the supported range

9.14 Status Flags

The status flags are listed Table 22.

Table 22: Status Flags

Flag	Description	Assert	De-assert
CHARGER_STATE	Mode of DA9318L/M: 000: SHUTDOWN and/or INIT 001: IDLE 010: IDLE_LP 011: Reserved 100: ACTIVE	Automatically updated whenever the state machine changes state. All lower-level states should be mapped to one of the four modes.	
S_VBAT_OV	V_{BAT} over-voltage comparator status	V_{BAT} exceeds VBAT_OV_THRSH for longer than $t_{DEGLITCH\_OV}$	V_{BAT} falls below VBAT_OV_THRSH - $V_{BAT\_PROT\_HYS}$
S_VBAT_UV	V_{BAT} under-voltage comparator status	V_{BAT} drops below VBAT_UV_THRSH for longer than $t_{DEGLITCH\_UV}$	V_{BAT} rises above VBAT_UV_THRSH + $V_{BAT\_PROT\_HYS}$
S_VIN_OV	V_{IN} over-voltage comparator status	V_{IN} exceeds V_{OV_IDLE} for longer than $t_{DEGLITCH\_OV}$	V_{IN} falls below V_{OV_IDLE} – V_{PROT_HYS}
S_VIN_UV	V_{IN} under-voltage comparator status	V_{IN} drops below $V_{UV\_FALL/RISE}$- V_{PROT_HYS} for longer than $t_{DEGLITCH\_UV}$	V_{IN} rises above $V_{UV\_FALL/RISE}$
S_VIN_ADP_DET	Adaptor detection comparator status	V_{IN} rises above V_{THR_RISE} for longer than $t_{DEGLITCH\_UV}$	V_{IN} drops below V_{THR_RISE} - V_{PROT_HYS}
S_TJUNC_CRIT	T_{CRIT} comparator status	T_{JUNC} rises above T_{CRIT}	T_{JUNC} drops below T_{CRIT} - T_{CRIT_HYS}
S_TJUNC_WARN	T_{WARN} comparator status	T_{JUNC} rises above TJUNC_WARN_THRSH	T_{JUNC} drops below TJUNC_WARN_THRSH - T_{WARN_HYS}
S_VIN2OUT_MAX	$V_{IN}/2$-V_{OUT} comparator status	$V_{IN}/2$ - V_{OUT} rises above V_{IN2OUT_MAX} for longer than $t_{DEGLITCH}$	$V_{IN}/2$-V_{OUT} drops below V_{IN2OUT_MAX} - V_{IN2OUT_HYS}
S_VIN2OUT_MIN	$V_{IN}/2$ - V_{OUT} comparator status	$V_{IN}/2$ - V_{OUT} falls below V_{IN2OUT_MIN} for longer than $t_{DEGLITCH}$	$V_{IN}/2$ - V_{OUT} rises above V_{IN2OUT_MIN} + V_{IN2OUT_HYS}
S_IIN_OC	I_{IN} over-current status	The ADC is in the continuous measurement mode, the value programmed in IIN_OC_THRSH is non-zero, and the ADC result of the IIN channel is greater than or equal to IIN_OC_THRSH	The ADC result of the IIN channel is less than IIN_OC_THRSH
S_VBAT_WARN	V_{BAT} monitoring status	The ADC is in the continuous measurement mode, the value programmed in VBAT_WARN_THRSH is non-zero, and the ADC result of the VBAT channel is greater than or equal to VBAT_WARN_THRSH	ADC result of the VBAT channel is greater or smaller than VBAT_WARN_THRSH
S_ILIM_OC_WARN	80 % of I_{LIM_PK} current protection warning status	The current exceeds 80 % of I_{LIM_PK} (set by CP_ILIM) for longer than $t_{DEGLITCH\_ILIM\_PK}$	The current decreases below 80 % of I_{LIM_PK} longer than $t_{DEGLITCH\_ILIM\_PK}$
S_RAMPUP_FAULT	Current doubler ramp-up was unsuccessful	Current doubler ramp-up time reached timeout	Current doubler ramped down and the system goes back to IDLE

10 Register Definition

Table 23: Register Overview

Status and Events										
Register	**Addr**	**POR**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
STATUS_A	0x00	0x00	S_VBAT_OV	S_VBAT_UV	S_VIN_OV	S_VIN_UV	S_VIN_ADP_DET	CHARGER_STATE<2:0>		
STATUS_B	0x01	0x00	S_ILIM_OC_WARN	S_RAMPUP_FAULT	S_TJUNC_CRIT	S_TJUNC_WARN	S_VIN2OUT_MAX	S_VIN2OUT_MIN	S_IIN_OC	S_VBAT_WARN
EVENT_A	0x02	0x00	E_VBAT_OV	E_VBAT_UV	E_VIN_OV	E_VIN_UV	E_VIN_ADP_DET	Reserved	Reserved	Reserved
EVENT_B	0x03	0x00	E_ILIM_OC_WARN	E_RAMPUP_FAULT	E_TJUNC_CRIT	E_TJUNC_WARN	E_VIN2OUT_MAX	E_VIN2OUT_MIN	E_IIN_OC	E_VBAT_WARN
EVENT_C	0x04	0x00	Reserved	Reserved	Reserved	E_ADC_DONE	E_SAFETY_TIMER	E_WD	E_ILIM_OC_CRIT	E_TJUNC_POR
MASK_A	0x05	0xF0	M_VBAT_OV	M_VBAT_UV	M_VIN_OV	M_VIN_UV	M_VIN_ADP_DET	Reserved	Reserved	Reserved
MASK_B	0x06	0xFF	M_ILIM_OC_WARN	M_RAMPUP_FAULT	M_TJUNC_CRIT	M_TJUNC_WARN	M_VIN2OUT_MAX	M_VIN2OUT_MIN	M_IIN_OC	M_VBAT_WARN
MASK_C	0x07	0x1F	Reserved	Reserved	Reserved	M_ADC_DONE	M_SAFETY_TIMER	M_WD	M_ILIM_OC_CRIT	M_TJUNC_POR
Voltage Protections										
Register	**Addr**	**POR**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VBAT_CTRL_A	0x08	0xF3	VBAT_OV_THRSH<5:0>						VBAT_UV_THRSH<1:0>	
Current and Voltage Monitoring (ADC)										
Register	**Addr**	**POR**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VBAT_CTRL_B	0x09	0xFF	VBAT_WARN_THRSH<7:0>							
IIN_CTRL_A	0x0A	0xD9	IIN_OC_THRSH<7:0>							
Current Doubler										
Register	**Addr**	**POR**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CP_CTRL_A	0x0B	0x10	Reserved	CP_SWITCHING	CP_FREQ<1:0>		Reserved	Reserved	Reserved	CP_EN
CP_CTRL_B	0x0C	0x0F	Reserved	Reserved	Reserved	Reserved	CP_ILIM<3:0>			
Junction Temperature Monitoring										
Register	**Add**	**POR**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TJUNC_CTRL_A	0x0D	0x01	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TJUNC_WARN_THRSH<1:0>	

ADC										
Register	**Addr**	**POR**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADC_CTRL_A	0x0E	0x0E	Reserved	Reserved	Reserved	Reserved	ADC_AVERAGE<1:0>		ADC_AUTO_CNVRT	ADC_SINGLE_CNVRT
ADC_RES_0	0x0F	0x00	ADC_VIN_RESULT<7:0>							
ADC_RES_1	0x10	0x00	ADC_VBATT_RESULT<7:0>							
ADC_RES_2	0x11	0x00	ADC_IIN_RESULT<7:0>							
ADC_RES_3	0x12	0x00	ADC_IOUT_RESULT<7:0>							
ADC_RES_4	0x13	0x00	ADC_TJUNC_RESULT<7:0>							
ADC_RES_5	0x14	0x00	ADC_VOUT_RESULT<7:0>							
Interface Control										
Register	**Addr**	**POR**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
I2C_CTRL_A	0x15	0x02	Reserved	Reserved	Reserved	WRITE_MODE	Reserved	Reserved	I2C_TO_EN	I2C_IF_HSM
I2C_CTRL_B	0x16	0xB2	IF_BASE_ADDR1<6:0>							Reserved
Watchdog and Safety Timers										
Register	**Addr**	**POR**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CONFIG_A	0x17	0x01	Reserved	Reserved	Reserved	Reserved	Reserved	WATCHDOG_TIMER_EN	SAFETY_TIMER_EN	EN_IDLE_LP
TIMER_CTRL_A	0x18	0x01	Reserved	Reserved	Reserved	Reserved	SAFETY_TIMER_LOAD<3:0>			
TIMER_CTRL_B	0x19	0xFF	WD_TIMER_LOAD<7:0>							
WD_TIMER_COUNT	0x1A	0x00	WD_TIMER_COUNT<7:0>							
SAFETY_TIMER_COUNT	0x1B	0x00	Reserved	SAFETY_TIMER_COUNT<6:0>						

10.1 Register Descriptions

10.1.1 Status and Event

Table 24: STATUS_A (0x00)

Bit	Register Bits	Description	Reset
7	S_VBAT_OV	V_{BAT} over-voltage comparator status	0x0
6	S_VBAT_UV	V_{BAT} under-voltage comparator status	0x0
5	S_VIN_OV	V_{IN} over-voltage comparator status	0x0
4	S_VIN_UV	V_{IN} under-voltage comparator status	0x0
3	S_VIN_ADP_DET	Adaptor detection status	0x0
2:0	CHARGER_STATE	Mode of DA9318L/M: 000: SHUTDOWN 001: IDLE 010: IDLE_LP 011: Reserved 100: ACTIVE	0x0

Table 25: STATUS_B (0x01)

Bit	Register Bits	Description	Reset
7	S_ILIM_OC_WARN	Current protection warning status	0x0
6	S_RAMPUP_FAULT	Current doubler ramp-up was unsuccessful	0x0
5	S_TJUNC_CRIT	T_{CRIT} comparator status	0x0
4	S_TJUNC_WARN	T_{WARN} comparator status	0x0
3	S_VIN2OUT_MAX	$V_{IN}/2$ - V_{OUT} comparator status	0x0
2	S_VIN2OUT_MIN	$V_{IN}/2$ - V_{OUT} comparator status	0x0
1	S_IIN_OC	I_{IN} over-current status	0x0
0	S_VBAT_WARN	V_{BAT} monitoring status	0x0

Table 26: EVENT_A (0x02)

Bit	Register Bits	Description	Reset
7	E_VBAT_OV	V_{BAT} over-voltage event (S_VBAT_OV)	0x0
6	E_VBAT_UV	V_{BAT} under-voltage event (S_VBAT_UV)	0x0
5	E_VIN_OV	V_{IN} over-voltage event (S_VIN_OV)	0x0
4	E_VIN_UV	V_{IN} under-voltage event (S_VIN_UV)	0x0
3	E_VIN_ADP_DET	Adaptor detection event (S_VIN_ADP_DET)	0x0
2:0	Reserved		0x0

Table 27: EVENT_B (0x03)

Bit	Register Bits	Description	Reset
7	E_ILIM_OC_WARN	Current protection warning event (S_ILIM_OC_WARN)	0x0
6	E_RAMPUP_FAULT	Current doubler ramp-up failure event (S_RAMPUP_FAULT)	0x0
5	E_TJUNC_CRIT	Junction temperature monitoring event (S_TJUNC_CRIT)	0x0
4	E_TJUNC_WARN	Junction temperature monitoring event (S_TJUNC_WARN)	0x0
3	E_VIN2OUT_MAX	Input-to-output voltage monitoring event (S_VIN2OUT_MAX)	0x0
2	E_VIN2OUT_MIN	Input-to-output voltage monitoring event (S_VIN2OUT_MIN)	0x0
1	E_IIN_OC	I_{IN} over-current event (S_IIN_OC)	0x0
0	E_VBAT_WARN	V_{BAT} monitoring event (S_VBAT_WARN)	0x0

Table 28: EVENT_C (0x04)

Bit	Register Bits	Description	Reset
7:5	Reserved		0x0
4	E_ADC_DONE	The ADC measurement was completed	0x0
3	E_SAFETY_TIMER	The safety timer expired	0x0
2	E_WD	The watchdog timer expired	0x0
1	E_ILIM_OC_CRIT	The peak current limit was exceeded for longer than $t_{DEGLITCH\_ILIM\_PK}$	0x0
0	E_TJUNC_POR	Junction temperature monitoring event. Reset only in NO-POWER mode ($V_{AVDD} < V_{POR\_RISE}$).	0x0

Table 29: MASK_A (0x05)

Bit	Register Bits	Description	Reset
7	M_VBAT_OV	Masks for interrupts in EVENT_A	0x1
6	M_VBAT_UV		0x1
5	M_VIN_OV		0x1
4	M_VIN_UV		0x1
3	M_VIN_ADP_DET		0x0
2:0	Reserved		

Table 30: MASK_B (0x06)

Bit	Register Bits	Description	Reset
7	M_ILIM_OC_WARN	Masks for interrupts in EVENT_B	0x1
6	M_RAMPUP_FAULT		0x1
5	M_TJUNC_CRIT		0x1
4	M_TJUNC_WARN		0x1
3	M_VIN2OUT_MAX		0x1
2	M_VIN2OUT_MIN		0x1
1	M_IIN_OC		0x1
0	M_VBAT_WARN		0x1

Table 31: MASK_C (0x07)

Bit	Register Bits	Description	Reset
7:5	Reserved	Masks for interrupts in EVENT_C	
4	M_ADC_DONE		0x1
3	M_SAFETY_TIMER		0x1
2	M_WD		0x1
1	M_ILIM_OC_CRIT		0x1
0	M_TJUNC_POR		0x1

10.1.2 Voltage Protection

Table 32: VBAT_CTRL_A (0x08)

Bit	Register Bits	Description	Reset
7:2	VBAT_OV_THRSH	Battery over-voltage threshold (4.0 V to 5.5 V). The maximum value is 5.5 V (0x3C). Any value greater than the maximum will be stored in the register but tied to the maximum internally. VBAT_OV_THRSH = 4.0 + N * 0.025 V Where N = the decimal number represented by the VBAT_OV_THRSH setting.	0x3C
1:0	VBAT_UV_THRSH	Battery under-voltage threshold (2.4 V to 3.0 V) : 00: 2.4 V 01: 2.6 V 10: 2.8 V 11: 3.0 V	0x3

10.1.3 Current and Voltage Monitoring

Table 33: VBAT_CTRL_B (0x09)

Bit	Register Bits	Description	Reset
7:0	VBAT_WARN_THRSH	Warning threshold for the battery voltage. A value 0x0 will disable the monitoring. VBAT_WARN_THRSH = 2.1784 + (N * 0.01385) V Where N = the decimal number represented by the VBAT_WARN_THRSH setting	0xFF

Table 34: IIN_CTRL_A (0x0A)

Bit	Register Bits	Description	Reset
7:0	IIN_OC_THRSH	Threshold for the input over-current. A value 0x0 will disable the monitoring.	0xD9

10.1.4 Current Doubler

Table 35: CP_CTRL_A (0x0B)

Bit	Register Bits	Description	Reset
7	Reserved		
6	CP_SWITCHING	Current doubler is switching	0X0
5:4	CP_FREQ	Switching frequency of the current doubler: 00: 250 kHz 01: 500 kHz 10: 1 MHz 11: 1.5 MHz	0X1
3:1	Reserved		
0	CP_EN	Main current doubler enable	0X0

Table 36: CP_CTRL_B (0x0C)

Bit	Register Bits	Description	Reset
7:4	Reserved		
3:0	CP_ILIM	Current doubler peak current limit (programmable in 450 mA steps): 0000: 4.8 A 1111: 11.55 A	0xF

10.1.5 Junction Temperature

Table 37: TJUNC_CTRL_A (0x0D)

Bit	Register Bits	Description	Reset
7:2	Reserved		
1:0	TJUNC_WARN_THRSH	Threshold for junction temperature warning: 00: 70 ºC 01: 80 ºC 10: 100 ºC 11: 120 ºC	0x1

10.1.6 ADC

Table 38: ADC_CTRL_A (0x0E)

Bit	Register Bits	Description	Reset
7:4	Reserved		
3:2	ADC_AVERAGE	Defines the number of measurements that are averaged for each ADC result. ADC_AVERAGE = 2^N.	0x3
1	ADC_AUTO_CNVRT	Enables the continuous ADC measurements	0x1
0	ADC_SINGLE_CNVRT	Triggers the ADC measurement. When this bit is set during a write access, the MSBs are ignored. When the measurement is done (E_ADC_DONE) the results can be read from ADC_RES_x.	0x0

Table 39: ADC_RES_0 (0x0F)

Bit	Register Bits	Description	Reset
7:0	ADC_VIN_RESULT	ADC V_{IN} measurement result	0x0

Table 40: ADC_RES_1 (0x10)

Bit	Register Bits	Description	Reset
7:0	ADC_VBATT_RESULT	ADC V_{BAT} measurement result	0x0

Table 41: ADC_RES_2 (0x11)

Bit	Register Bits	Description	Reset
7:0	ADC_IIN_RESULT	ADC I_{IN} measurement result	0x0

Table 42: ADC_RES_3 (0x12)

Bit	Register Bits	Description	Reset
7:0	ADC_IOUT_RESULT	ADC I_{OUT} measurement result	0x0

Table 43: ADC_RES_4 (0x13)

Bit	Register Bits	Description	Reset
7:0	ADC_TJUNC_RESULT	ADC T_{JUNC} measurement result	0x0

Table 44: ADC_RES_5 (0x14)

Bit	Register Bits	Description	Reset
7:0	ADC_VOUT_RESULT	ADC V_{OUT} measurement result	0x0

10.1.7 Interface Control

Table 45: I2C_CTRL_A (0x15)

Bit	Register Bits	Description	Reset
7:5	Reserved		
4	WRITE_MODE	Write mode of the 2-wire interface: 0: Consecutive write mode 1: Repeated write mode	0x0
3:2	Reserved		

Bit	Register Bits	Description	Reset
1	I2C_TO_EN	Automatic interface reset	0x1
0	I2C_IF_HSM	Interface operates continuously in High-speed mode	0x0

Table 46: I2C_CTRL_B (0x16)

Bit	Register Bits	Description	Reset
7:1	IF_BASE_ADDR1	Slave address of the device	0x59
0:0	Reserved		

10.1.8 Watchdog and Safety Timers

Table 47: CONFIG_A (0x17)

Bit	Register Bits	Description	Reset
7:3	Reserved		
2	WATCHDOG_TIMER_EN	Enables the watchdog timer	0x0
1	SAFETY_TIMER_EN	Enables the pre-charge / CCCV timer	0x0
0	EN_IDLE_LP	Disables the LOW-POWER IDLE mode	0x1

Table 48: TIMER_CTRL_A (0x18)

Bit	Register Bits	Description	Reset
7:4	Reserved		
3:0	SAFETY_TIMER_LOAD	Defines safety timer duration (tSFTY)	0x1

Table 49: TIMER_CTRL_B (0x19)

Bit	Register Bits	Description	Reset
7:0	WD_TIMER_LOAD	Watchdog timer pre-load and re-load. Writing the register when the charger is not enabled sets the pre-load value. The pre-load value is automatically loaded in to WD_TIMER_COUNT the next time the charger starts. Writing the register during charging loads the written value in to WD_TIMER_COUNT.	0xFF

Table 50: WD_TIMER_COUNT (0x1A)

Bit	Register Bits	Description	Reset
7:0	WD_TIMER_COUNT	Count value of the watchdog timer. Decremented at 1 s intervals when charging is enabled. Reading the register gives the current timer value. Writing the register has no affect.	0x0

Table 51: SAFETY_TIMER_COUNT (0x1B)

Bit	Register Bits	Description	Reset
7	Reserved		
6:0	SAFETY_TIMER_COUNT	Count value of the safety timer. Incremented at 15 min intervals when charging is enabled. Reading the register gives the current timer value. Writing the register has no affect.	0x0

11 Package Information

11.1 Package Outline

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOM.	MAX.
Total Thickness	A	0.471	0.511	0.551
Stand Off	A1	0.162	–	0.222
Wafer Thickness	A2		0.279	±0.025
Body Size	D	3.590	3.620	3.650
	E	3.750	3.780	3.810
Ball Diameter (Size)			0.250	
Ball/Bump Width	b	0.240	0.270	0.300
Ball/Bump Pitch	eD		0.403	
	eE		0.403	
Ball/Bump Count	n		64	
Edge Ball Center to Center	D1		3.080	BSC
	E1		3.300	BSC
Package Edge Tolerance	aaa		0.03	
Coplanarity (whole wafer)	ccc		0.03	
Ball/Bump Offset (Package)	ddd		0.05	
Ball/Bump Offset (Ball)	eee		0.015	

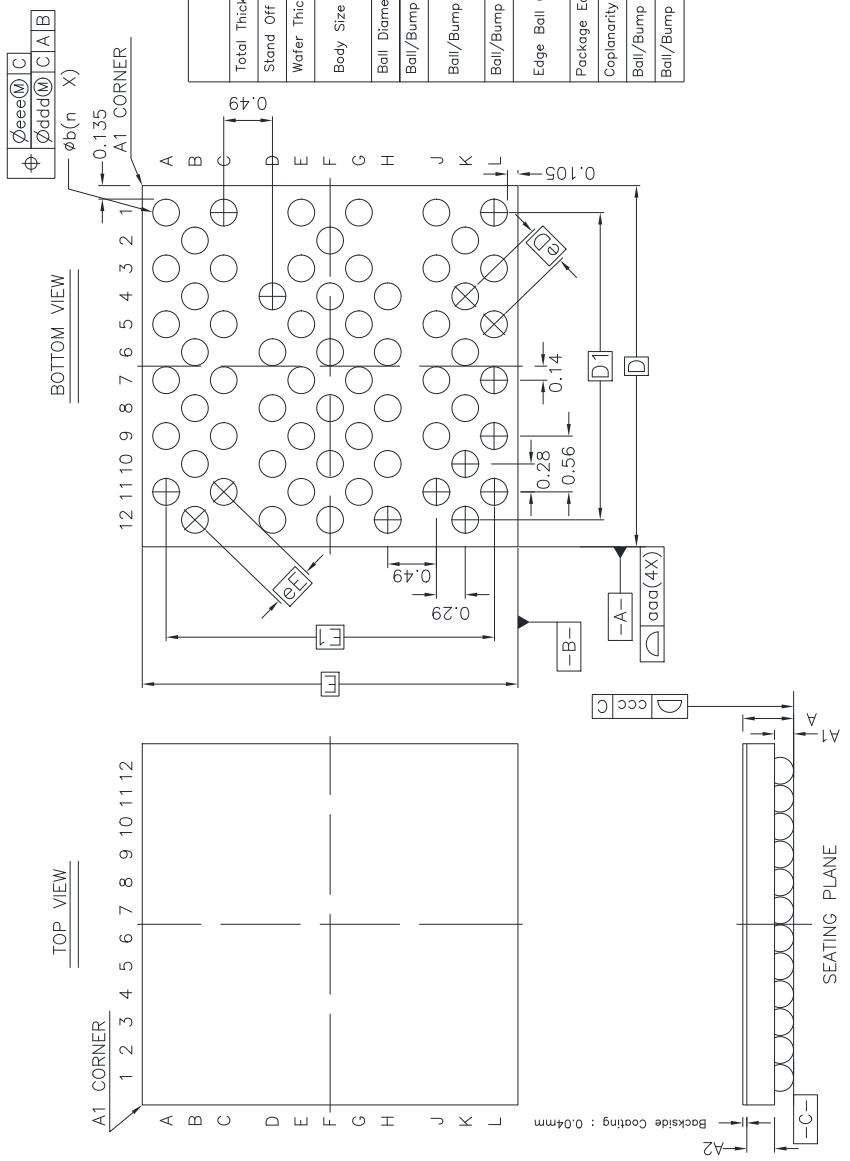

Figure 23: Package Outline Drawing

11.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. Table 52 defines the MSL classification.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The WLCSP package is qualified for MSL 1.

Table 52: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	unlimited	30 °C / 85 % RH

11.3 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of a WLCSP package will cause damage to the solder balls. Therefore a removed sample cannot be reused.

WLCSP packages are sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

11.4 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

12 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's customer portal or your local sales representative.

Table 53: Ordering Information

Part Number	Comment	Package	Size (mm)	Shipment Form	Pack Quantity
DA9318L-06UF2	8 A output current	64 WLCSP	3.62 mm x 3.78 mm	Tape and reel	7,500
DA9318M-07UF2	10 A output current	64 WLCSP	3.62 mm x 3.78 mm	Tape and reel	7,500

Appendix A Application Information

A.1 Suggested PCB Layout

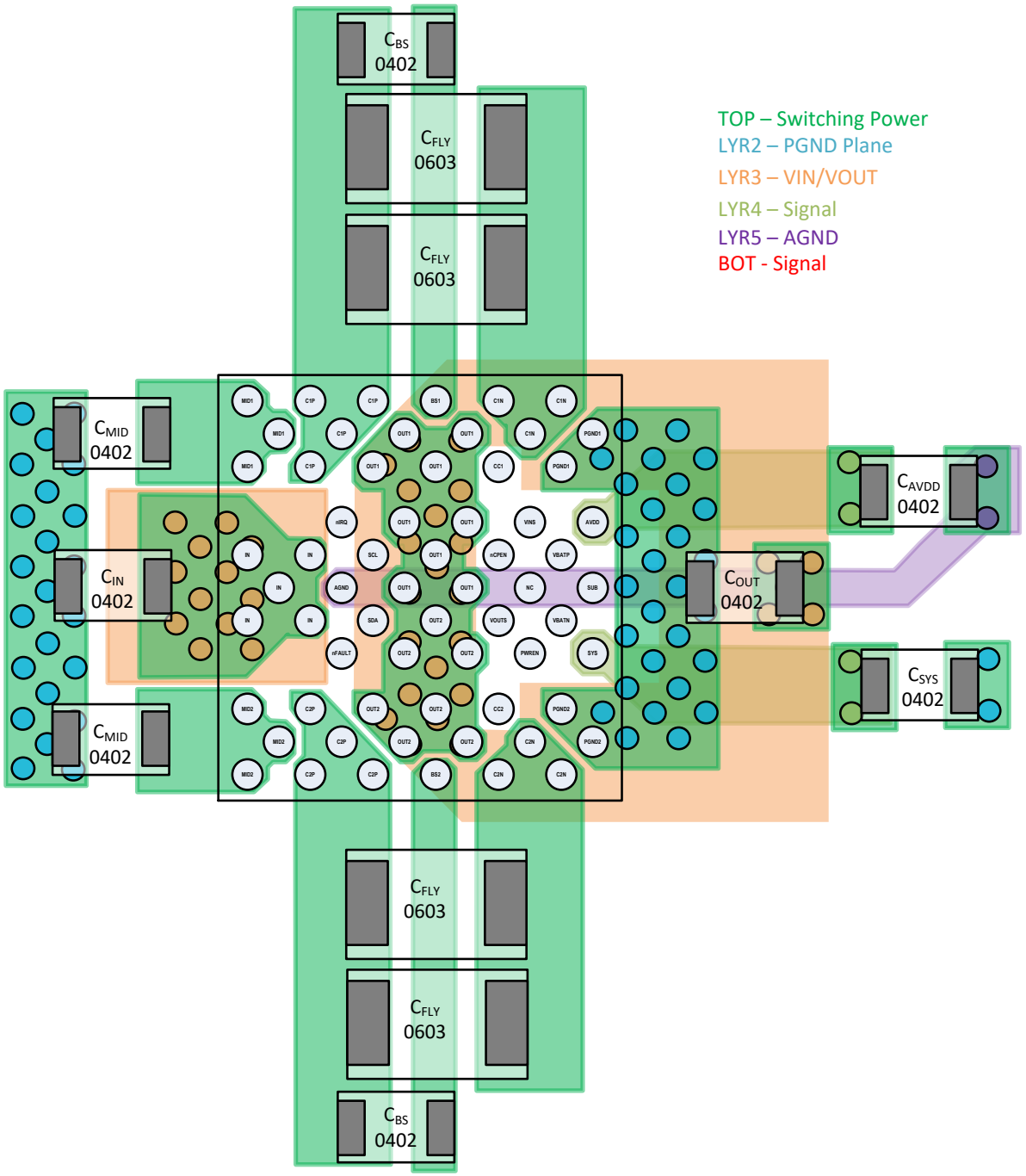

Figure 24: Suggested PCB Layout

Revision History

Revision	Date	Description
3.2	14-Feb-2022	Document rebranded to Renesas.
● Change Details: ○ Ordering information table: – Changed DA9318L-05UF2 to DA9318L-06UF2 – Changed DA9318M-06UF2 to DA9318M-07UF2		
3.1	21-Apr-2021	Production datasheet.
● Change Details: ○ Table 20: Added "Equation" column ○ Removed Watermark ○ Removed NDA Confidential in Header		
3.0	25-Jul-2018	Production datasheet.
● Change Details: ○ Table 1: Added "connect to ground if not used" to description for balls C9 and J9 ○ Chapter 7: Electrical Characteristics – Additional text in guarantee statement – Removal of references to OTP and "nominal" from conditions in all EC tables – Table 5: Added IQ_SHIP parameter and table note – Table 9: $V_{IN2OUT\_MAX\_ACC}$ was ± 5 % now ±20 mV – Table 12: Removal of "maximum" in conditions – Table 13: t_{RCP}: removal of "Guaranteed by design" from conditions – Table 17: C_{AVDD} was typ 1 µF now typ 4.7 µF ○ Section 9.3.2: Battery Voltage Protection – Removed text ""this feature can be removed by OTP)" ○ Section 9.14 Status Flags – Removed reference to OTP		
2.1	22-Dec-2017	Post evaluation phase changes.
2.0	23-Aug-2017	Changed datasheet status to Preliminary, no other changes.
1.6	20-Jul-2017	Added VINS to Absolute Maximum Ratings table, standard variants codes to part numbers in Ordering Information, and POR values to Register tables.
1.5	16-Jun-2017	Changes to device for AB silicon and post AA silicon evaluation. Changes listed in Rev 1.5.
1.4	08-May-2017	Updated Absolute Maximum Ratings max values for VOUT, VOUTS and VSYS,from 5.5 V to 6 V and added ratings for VBATP and VBATN.
1.3	08-Feb-2017	Post first silicon evaluation changes to VPWREN_LIM, IQ_IDLE, IQ_IDLE_LP, Current doubler efficiency test conditions, SAFETY_TIMER increment interval.
1.2	13-Jan-2017	Reviewed and updated.
1.1	15-Dec-2016	Updated ballout and pin description.
1.0	08-Dec-2016	Initial version.

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com.
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

Important Notice and Disclaimer

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu

Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

https://www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.