Description

The F2971 is a high reliability, low insertion loss, 75Ω absorptive SP2T RF switch designed for a multitude of cable systems and RF applications. This device covers a broad frequency range from 5MHz to 3000MHz. In addition to providing low insertion loss, the F2971 also delivers excellent linearity and isolation performance while providing a 75Ω termination for the unselected port.

The F2971 uses a single positive supply voltage and supports 3.3V logic.

Competitive Advantage

The F2971 provides broadband RF performance to support the CATV market along with high power handling and high isolation.

- Low insertion loss
- High isolation
- Excellent linearity
- Extended temperature: -40°C to +105°C

Typical Applications

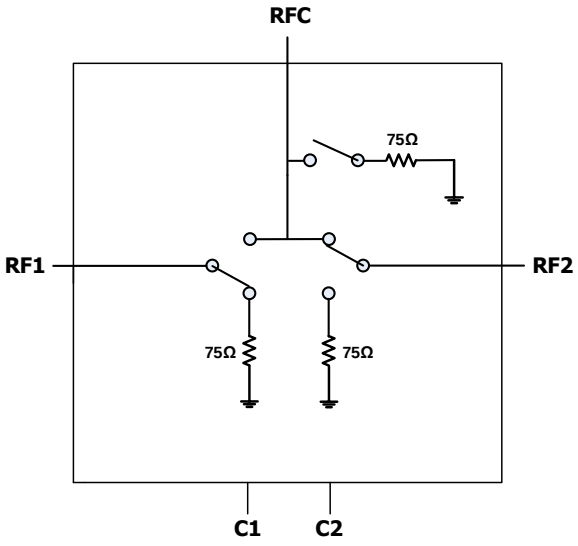
- CATV/Broadband applications
  - Headend
  - Fiber/HFC distribution nodes
  - Distribution amplifiers
  - Switch matrix
  - DTV tuner input select
  - DVR/PVR/Set-top box
- CATV test equipment

Features

- Low insertion loss: 0.31dB at 1200MHz
- High Isolation: 71dB at 1200MHz (RF1/RF2 to RFC)
- High IIP3: 67dBm at 5MHz
- Operating Temperature: -40°C to +105°C
- 4mm x 4mm, 20-pin LQFN package

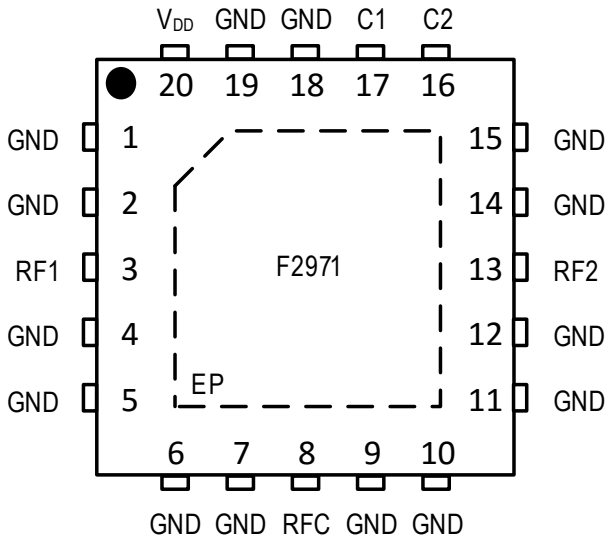
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 4mm x 4mm x 0.75mm 20-pin LQFN, NCG20P1 – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1, 2, 4, 5, 6, 7, 9, 10, 11, 12, 14, 15, 18, 19	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to the pin with thru-hole vias.
3	RF1	RF1 Port. Matched to 75Ω. If this pin is not 0V DC, then an external coupling capacitor must be used.
8	RFC	RFC Port. Matched to 75Ω. If this pin is not 0V DC, then an external coupling capacitor must be used.
13	RF2	RF2 Port. Matched to 75Ω. If this pin is not 0V DC, then an external coupling capacitor must be used.
16	C2	Control pin to set switch state. See Table 8.
17	C1	Control pin to set switch state. See Table 8.
20	V_{DD}	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit (see Figure 34) as close as possible to pin.
	EP	Exposed Paddle. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Symbol	Minimum	Maximum	Units
V_{DD} to GND		V_{DD}	-0.3	4.0	V
C1, C2 to GND		V_{CTRL}	-0.3	Lower of (V_{DD}+0.3, 3.9)	V
RF1, RF2, RFC to GND		V_{RFIN}	-0.3	+0.3	V
Maximum Input CW Power [a]	RF1 or RF2 as an input (connected to RFC). No RF power applied to unused RF1 or RF2 port.	P_{MAX-IN}		30	dBm
	RFC as an input (connected to RF1 or RF2). No RF power applied to terminated RF1 or RF2 port.			30	
	RF1 or RF2 port as an input (terminated states). Applied to only one port.			26	
	RFC as an input (terminated states). No RF drive applied to RF1 or RF2 ports.			30	
Maximum Junction Temperature		T_{JMAX}		140	°C
Storage Temperature Range		T_{STOR}	-65	150	°C
Lead Temperature (soldering, 10s)				260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)				1500 (Class 2)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)				1500 (Class C3)	V

a. Levels based on V_{DD} = 2.7V to 3.6V, 5MHz ≤ f_{RF} ≤ 3000MHz, T_{EP} = 105°C, Z_S = Z_L = 75Ω.

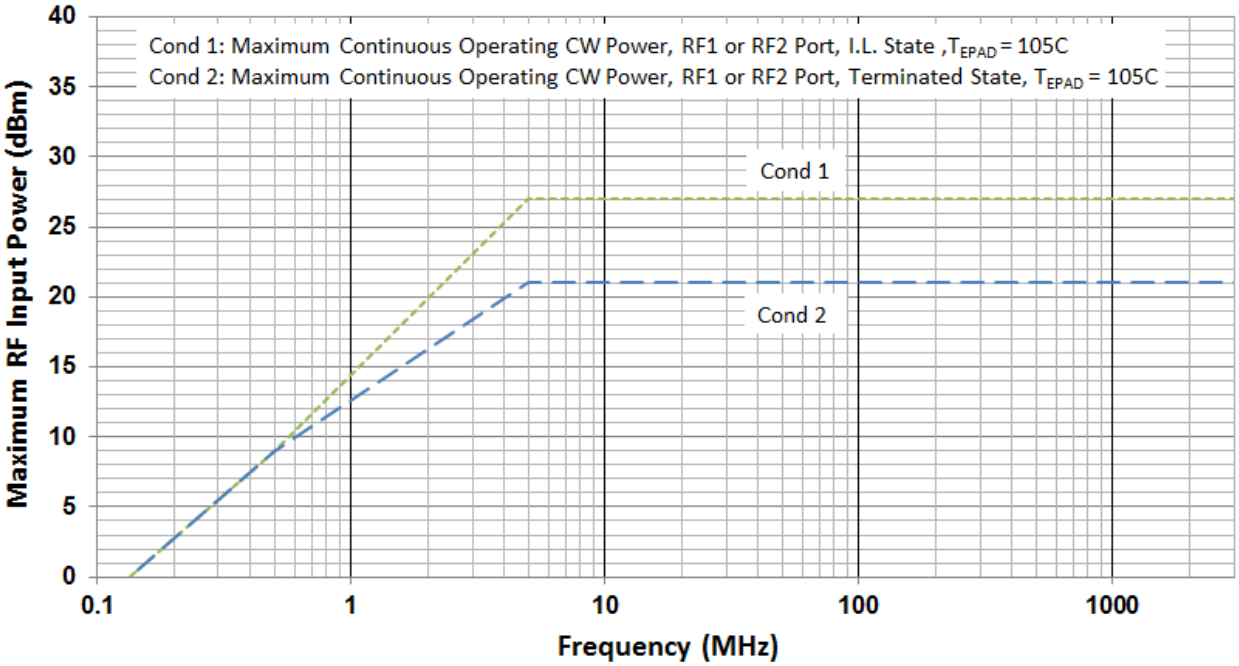
Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Supply Voltage	V_{DD}			2.7		3.6	V
Operating Temperature Range	T_{EP}	Exposed Paddle		-40		+105	°C
RF Frequency Range	f_{RF}			5		3000	MHz
RF Continuous Input CW Power (Non-Switched) [a]	P_{RF}	RFC connected to RF1 or RF2	T_{EP} = 85°C			27	dBm
			T_{EP} = 105°C			27	
		RF1 / RF2 Input, Terminated State	T_{EP} = 85°C			24	
			T_{EP} = 105°C			21	
RF Continuous Input Power (RF Hot Switching CW) [a]	P_{RFSW}	RFC Input switching between RF1 and RF2	T_{EP} = 85°C			21	dBm
			T_{EP} = 105°C			21	
		RF1 or RF2 as input, switched between RFC and Terminated State	T_{EP} = 85°C			17	
			T_{EP} = 105°C			17	
RF1 Port Impedance	Z_{RF1}	Single-ended			75		Ω
RF2 Port Impedance	Z_{RF2}	Single-ended			75		Ω
RFC Port Impedance	Z_{RFC}	Single-ended			75		Ω

a. Levels based on V_{DD} = 2.7V to 3.6V, 5MHz ≤ f_{RF} ≤ 3000MHz, Z_S = Z_L = 75Ω. See Figure 3 for power handling de-rating vs. RF frequency.

Figure 3. Maximum RF Input Operating Power vs. RF Frequency



Electrical Characteristics

Table 4. Electrical Characteristics

See the Typical Application Circuit in Figure 34. V_{DD} = 3.0V, T_{EP} = +25°C, f_{RF} = 1200MHz, driven port = RF1 or RF2, P_{IN} = 0dBm, Z_S = Z_L = 75Ω. PCB board trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input HIGH [a]	V_{IH}	2.7V ≤ V_{DD} ≤ 3.6V	0.7 x V_{DD} [b]		V_{DD}	V
Logic Input LOW [a]	V_{IL}		-0.3		0.3 x V_{DD}	V
Logic Current	I_{IH}, I_{IL}	For each control pin		5	***500*** [c]	nA
V_{DD} DC Current [a]	I_{DD}	Logic inputs at GND or V_{DD}		20	***30***	µA
Insertion Loss	IL	5MHz ≤ f_{RF} ≤ 250MHz		0.22		dB
		250MHz < f_{RF} ≤ 750MHz		0.26		
		750MHz < f_{RF} ≤ 1000MHz		0.29		
		1000MHz < f_{RF} ≤ 1200MHz [d]		0.31	***0.51***	
		1200MHz < f_{RF} ≤ 2000MHz		0.47		
		2000MHz < f_{RF} ≤ 3000MHz		0.64		
Isolation (RF1/RF2 to RFC)	ISO_{RFC}	5MHz ≤ f_{RF} ≤ 250MHz	76	81		dB
		250MHz < f_{RF} ≤ 750MHz	68	73		
		750MHz < f_{RF} ≤ 1000MHz	67	72		
		1000MHz < f_{RF} ≤ 1200MHz	66	71		
		1200MHz < f_{RF} ≤ 2000MHz	60	65		
		2000MHz < f_{RF} ≤ 3000MHz		57		
Isolation (RF1 to RF2 or RF2 to RF1)	ISO_{R12}	5MHz ≤ f_{RF} ≤ 250MHz	77	84		dB
		250MHz < f_{RF} ≤ 750MHz	69	74		
		750MHz < f_{RF} ≤ 1000MHz	66	71		
		1000MHz < f_{RF} ≤ 1200MHz	64	69		
		1200MHz < f_{RF} ≤ 2000MHz	56	61		
		2000MHz < f_{RF} ≤ 3000MHz		52		
RF1, RF2, RFC Return Loss (Insertion Loss State)	RL_{IL}	5MHz ≤ f_{RF} ≤ 250MHz		30		dB
		250MHz < f_{RF} ≤ 750MHz		22		
		750MHz < f_{RF} ≤ 1000MHz		20		
		1000MHz < f_{RF} ≤ 1200MHz		18		
		1200MHz < f_{RF} ≤ 2000MHz		14		
		2000MHz < f_{RF} ≤ 3000MHz		12		

a. Increased I_{DD} current will result if logic LOW level is above ground and up to V_{IL} max. Similarly, increased I_{DD} current will result if the logic HIGH level is below V_{DD} and down to V_{IH} min.
b. Items in min/max columns that are not bold italics are guaranteed by design characterization.
c. Items in min/max columns in ***bold italics*** are guaranteed by test.
d. Minimum or maximum specification guaranteed by test at 1200MHz and by design characterization over the full frequency range.

Electrical Characteristics

Table 5. Electrical Characteristics

See the Typical Application Circuit in Figure 34. V_{DD} = 3.0V, T_{EP} = +25°C, f_{RF} = 1200MHz, driven port = RF1 or RF2, P_{IN} = 0dBm, Z_S = Z_L = 75Ω. PCB board trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
RF1, RF2, RFC Return Loss (Terminated State)	RL_{TERM}	5MHz ≤ f_{RF} ≤ 250MHz			28		dB
		250MHz < f_{RF} ≤ 750MHz			24		
		750MHz < f_{RF} ≤ 1000MHz			22		
		1000MHz < f_{RF} ≤ 1200MHz			21		
		1200MHz < f_{RF} ≤ 2000MHz			17		
		2000MHz < f_{RF} ≤ 3000MHz			13		
Input 1dB Compression [c]	IP_{1dB}	5MHz ≤ f_{RF} ≤ 250MHz			31		dBm
		250MHz < f_{RF} ≤ 2000MHz			32		
Input IP2 (Insertion Loss State)	IIP2	P_{IN} = +13dBm/tone (f_1 + f_2 frequency)	f_1 = 5MHz f_2 = 6MHz		95		dBm
			f_1 = 185MHz f_2 = 190MHz		111		
			f_1 = 895MHz f_2 = 900MHz		124		
Input IP3 (Insertion Loss State)	IIP3	P_{IN} = +13dBm/tone	f_1 = 5MHz f_2 = 6MHz		67		dBm
			f_1 = 185MHz f_2 = 190MHz		75		
			f_1 = 1790MHz f_2 = 1795MHz		70		
CTB / CSO		77 and 110 channels, P_{OUT} = 44dBmV			-90		dBc
Non-RF Driven Spurious [d]	$Spur_{MAX}$	Out any RF port when externally terminated into 75Ω			-122		dBm
Switching Time [e]	T_{SW}	50% control to 90% RF			2.6		µs
		50% control to 10% RF			1.7		
Maximum Switching Rate [f]	SW_{RATE}					25	kHz
Maximum Video Feed-through on RF Ports	VID_{FT}	Peak transient during switching measured with 20ns rise time, 0V to 3.3V control pulse	Rise		1.1		mV_{pp}
			Fall		2.0		

a. Items in min/max columns in ***bold italics*** are guaranteed by test.
b. Items in min/max columns that are not bold italics are guaranteed by design characterization.
c. The input 1dB compression point is a linearity figure of merit. Refer to the “Recommended Operating Conditions” section and Figure 3 for the maximum operating power levels.
d. Spurious due to on-chip negative voltage generator. Spurious fundamental = approximately 2.2MHz.
e. f_{RF} = 1000MHz.
f. Minimum time required between switching of states = 1/ (Maximum Switching Rate).

Thermal Characteristics

Table 6. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	θ_{JA}	53	°C/W
Junction to Case Thermal Resistance (Case is defined as the exposed paddle)	θ_{JC}	13.8	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions (TOCs)

Unless otherwise noted:

- V_{DD} = +3.0V
- $Z_S = Z_L$ = 75Ω
- T_{EP} = 25°C
- f_{RF} = 1200MHz
- Small signal parameters measured with P_{IN} = 0dBm.
- Driven port is RF1 or RF2.
- All temperatures are referenced to the exposed paddle.
- Evaluation Kit traces and connector losses are de-embedded.

Typical Performance Characteristics [1]

Figure 4. Insertion Loss vs. Frequency over Temperature and V_{DD} [RF1]

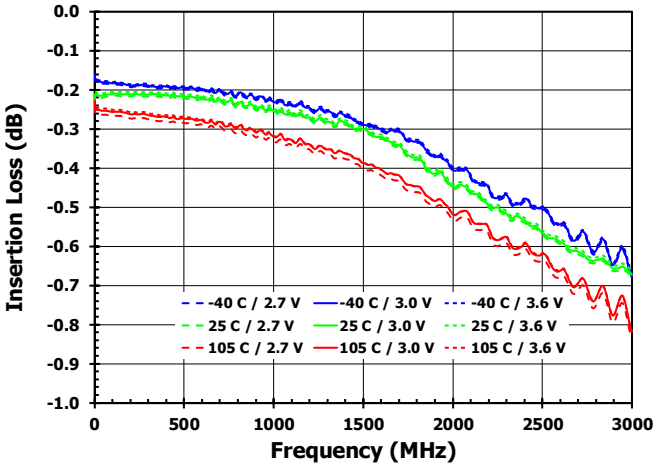


Figure 5. Insertion Loss vs. Frequency over Temperature and V_{DD} [RF2]

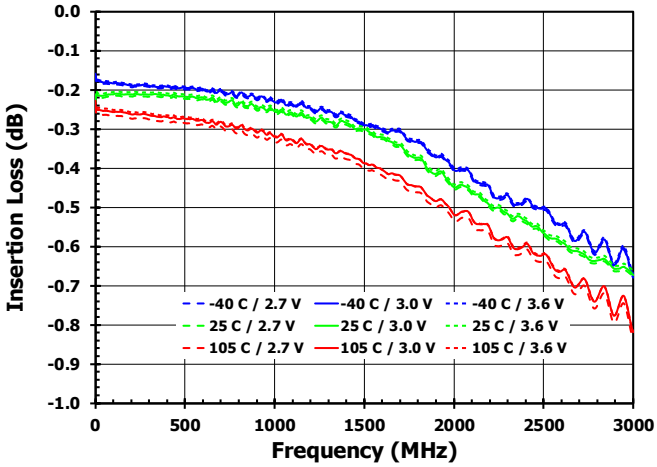


Figure 6. Isolation vs. Frequency over Temp. and V_{DD} [RF1 to RF2, RF1 Selected]

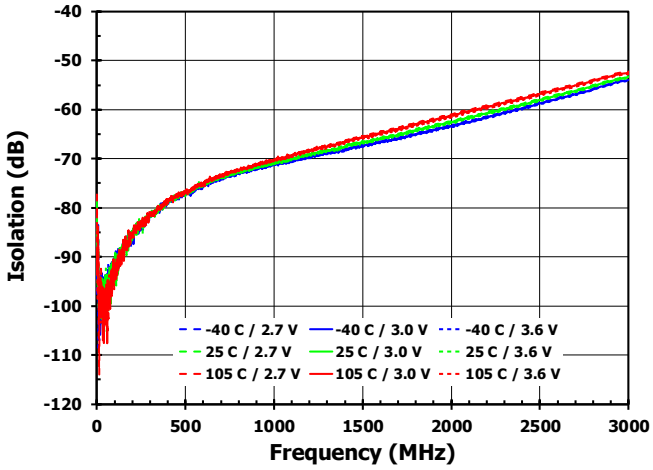


Figure 7. Isolation vs. Frequency over Temp. and V_{DD} [RF2 to RF1, RF2 Selected]

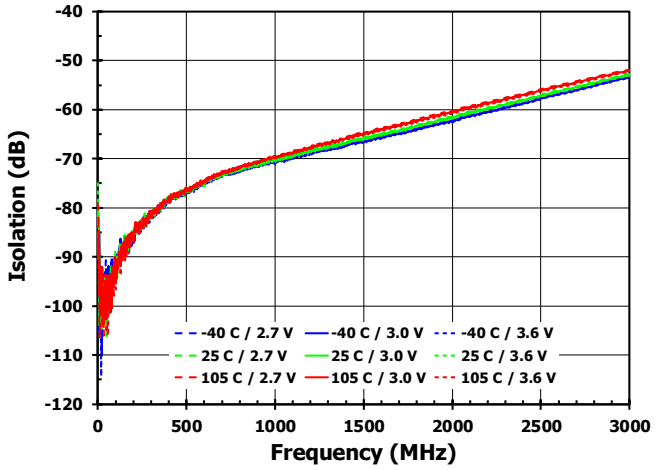


Figure 8. Isolation vs. Frequency over Temp. and V_{DD} [RF2 to RFC, RF1 Selected]

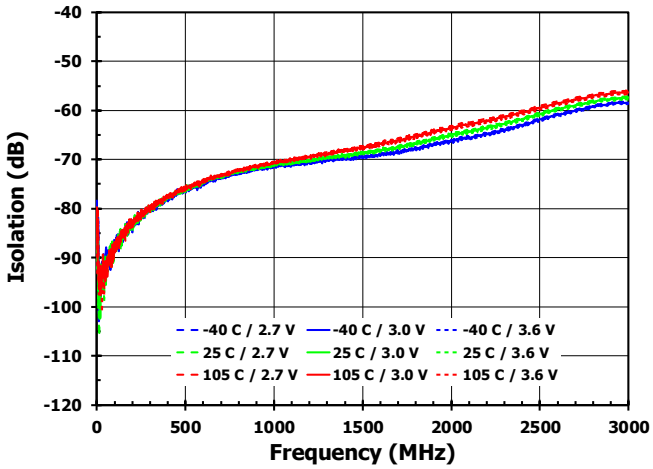
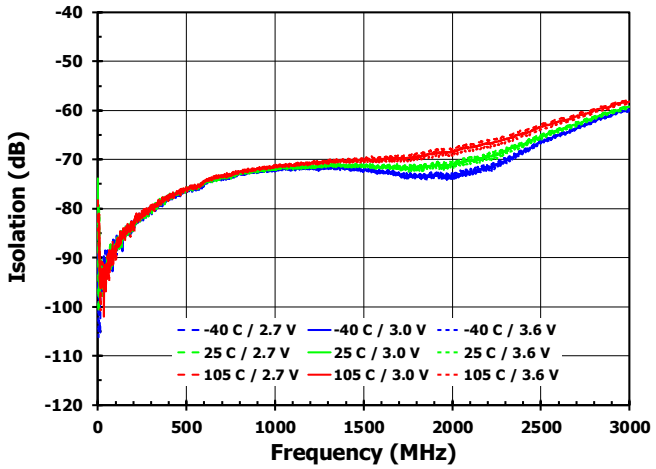


Figure 9. Isolation vs. Frequency over Temp. and V_{DD} [RF1 to RFC, RF2 Selected]



Typical Performance Characteristics [2]

Figure 10. Isolation vs. Frequency over Temp. and V_{DD} [RF1 to RFC, All Off]

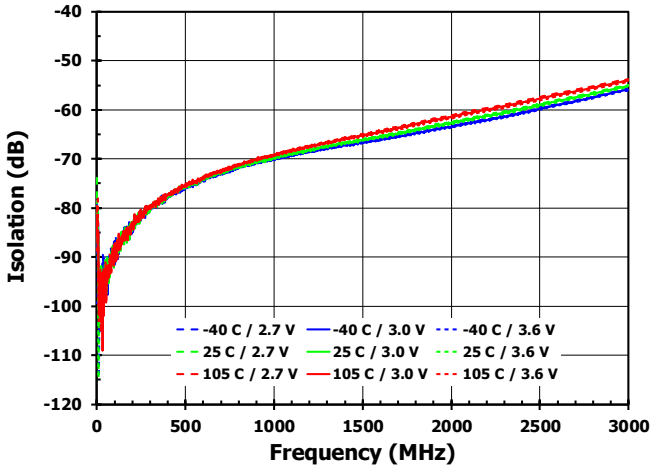


Figure 11. Isolation vs. Frequency over Temp. and V_{DD} [RF2 to RFC, All Off]

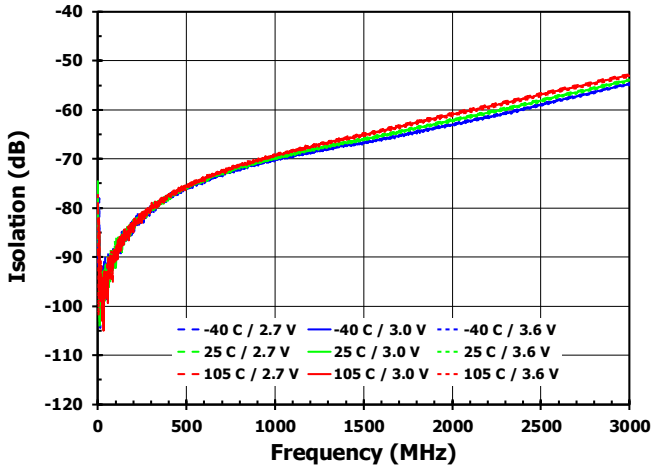


Figure 12. Isolation vs. Frequency over Temp. and V_{DD} [RF1 to RF2, All Off]

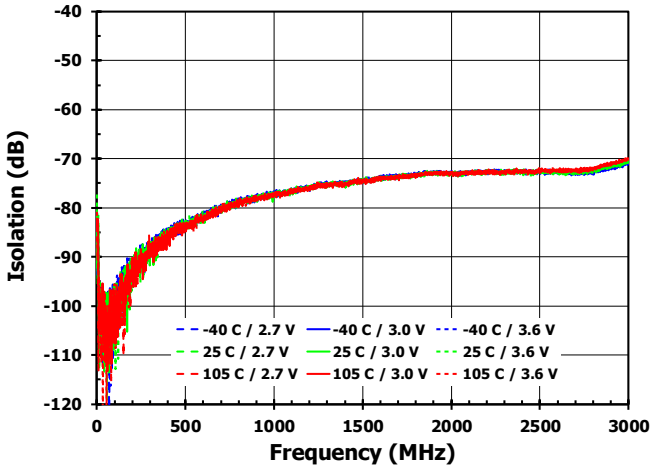


Figure 13. RFC Return Loss vs. Frequency over Temperature and V_{DD} [All Off]

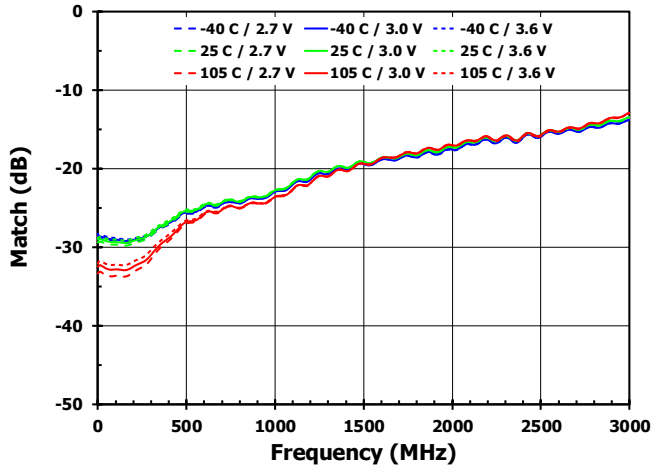


Figure 14. RF1 Return Loss vs. Frequency over Temperature and V_{DD} [All Off]

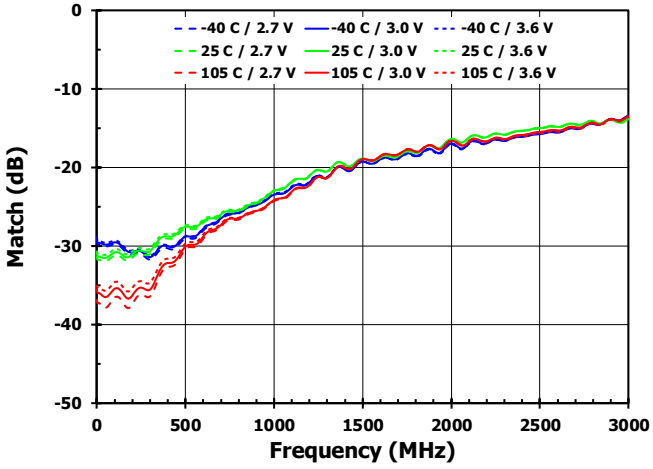
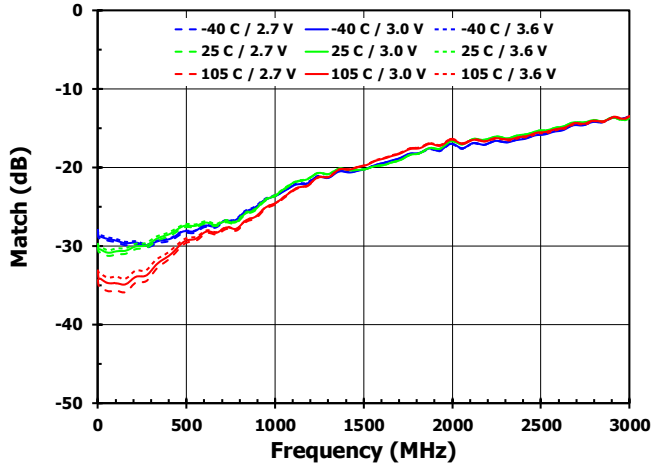


Figure 15. RF2 Return Loss vs. Frequency over Temperature and V_{DD} [All Off]



Typical Performance Characteristics [3]

Figure 16. RF1 Return Loss vs. Frequency over Temperature and V_{DD} [RF1 Selected]

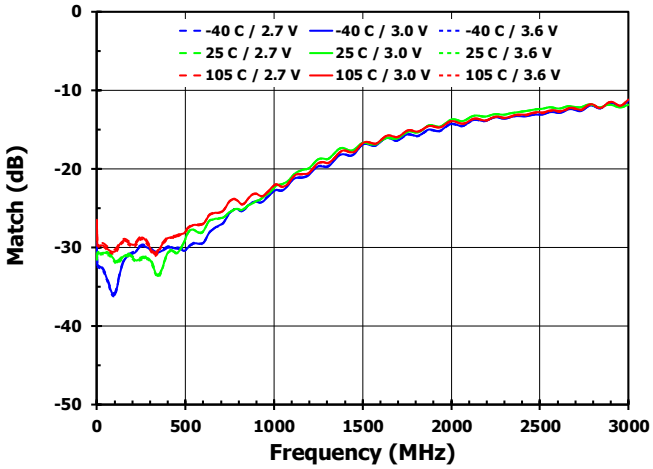


Figure 17. RF2 Return Loss vs. Frequency over Temperature and V_{DD} [RF2 Selected]

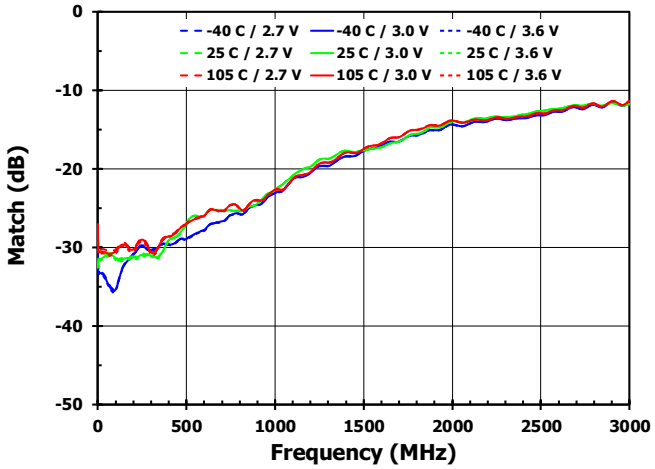


Figure 18. RF1 Return Loss vs. Frequency over Temperature and V_{DD} [RF2 Selected]

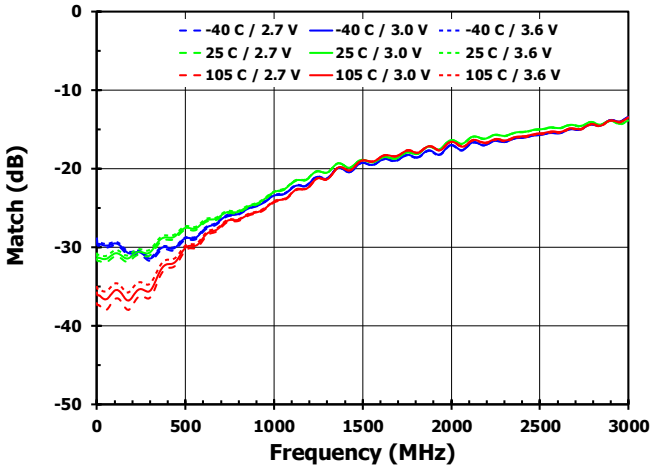


Figure 19. RF2 Return Loss vs. Frequency over Temperature and V_{DD} [RF1 Selected]

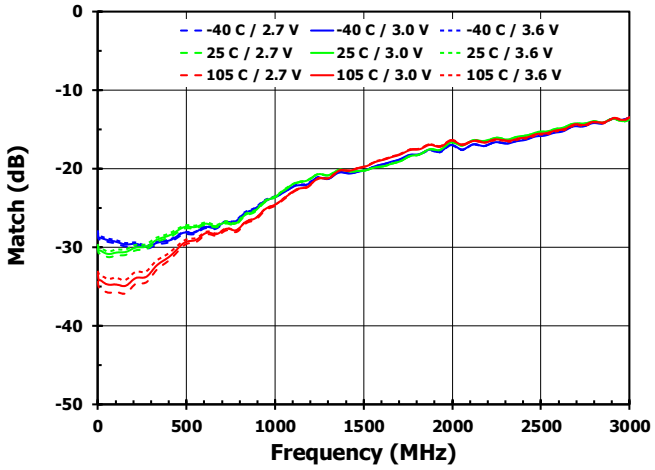


Figure 20. RFC Return Loss vs. Frequency over Temperature and V_{DD} [RF1 Selected]

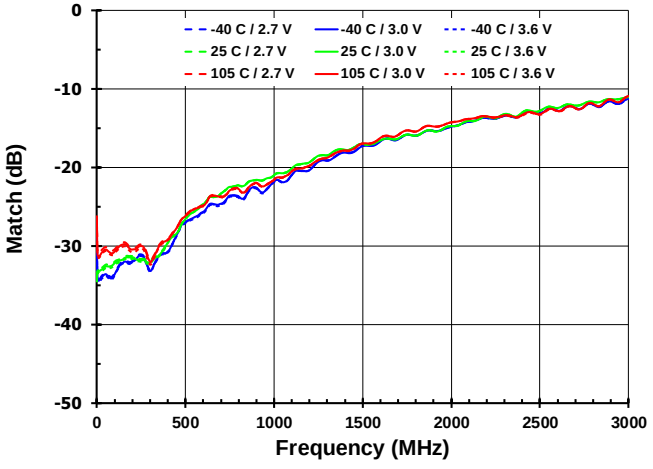
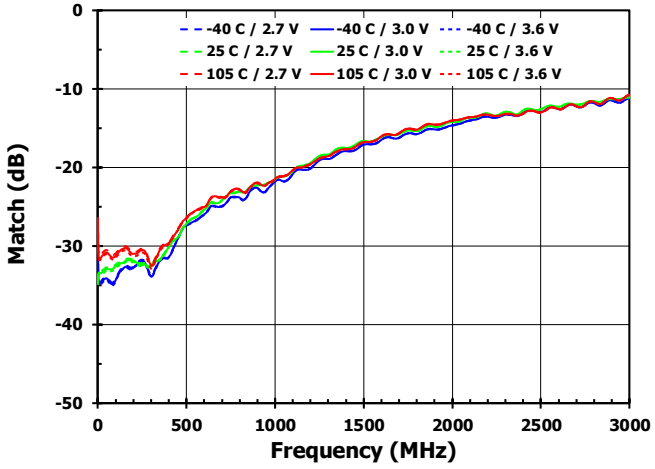


Figure 21. RFC Return Loss vs. Frequency over Temperature and V_{DD} [RF2 Selected]



Typical Performance Characteristics [4]

Figure 22. Evaluation Board Through-Line Loss vs. Frequency over Temperature

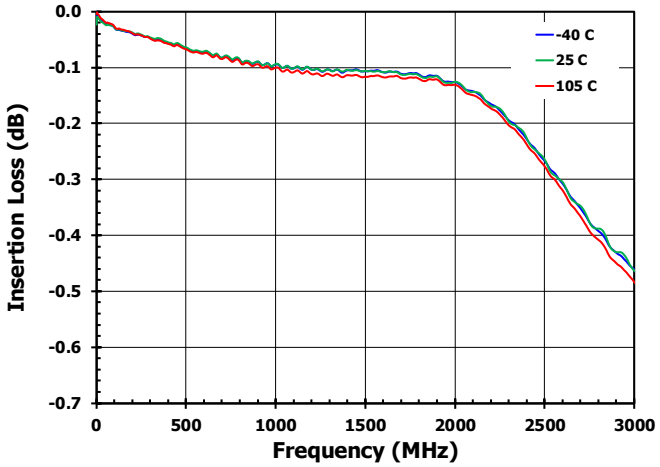


Figure 23. Evaluation Board Through-Line Return Loss vs. Freq. over Temp.

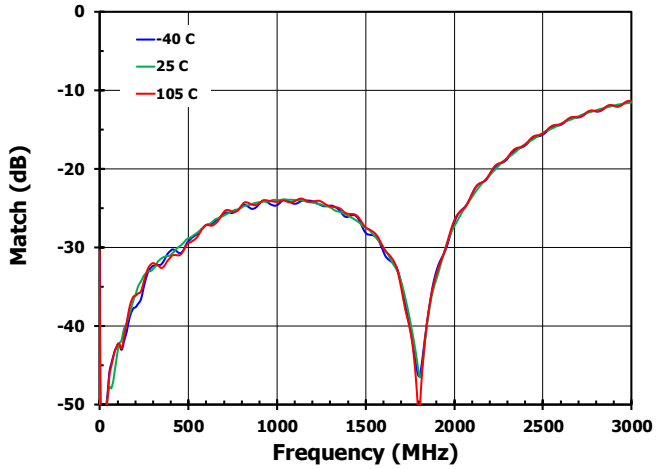


Figure 24. Switching Time Insertion Loss to Isolation

Figure 25. Switching Time Isolation to Insertion Loss

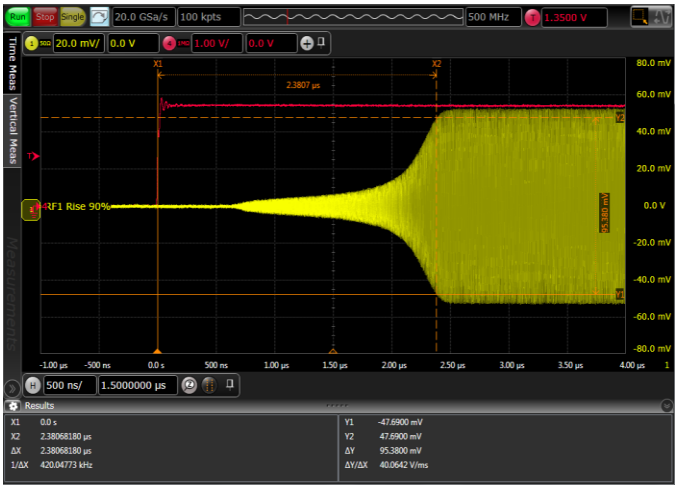


Figure 26. I_{DD} vs. Control Voltage; V_{DD} = 2.7V (C1 set to GND and V_{DD})

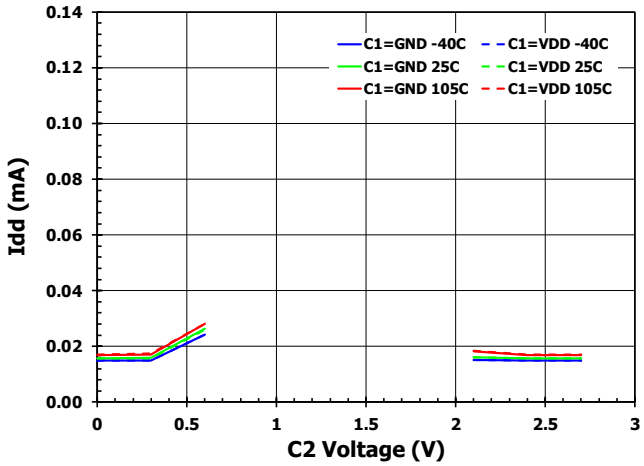
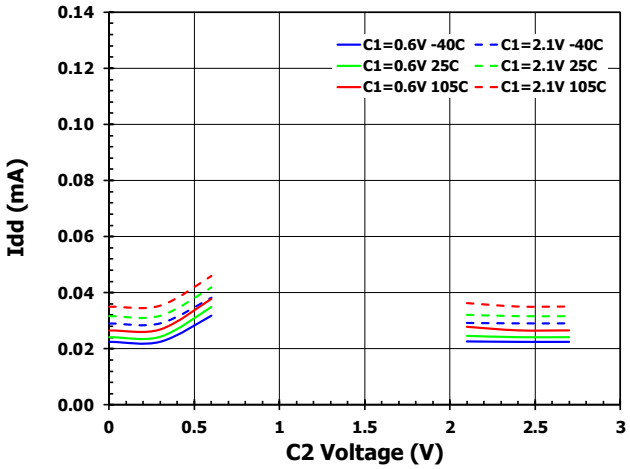


Figure 27. I_{DD} vs. Control Voltage; V_{DD} = 2.7V (C1 set to 0.6V and 2.1V)



Typical Performance Characteristics [5]

Figure 28. I_{DD} vs. Control Voltage; V_{DD} = 3.0V (C1 set to GND and V_{DD})

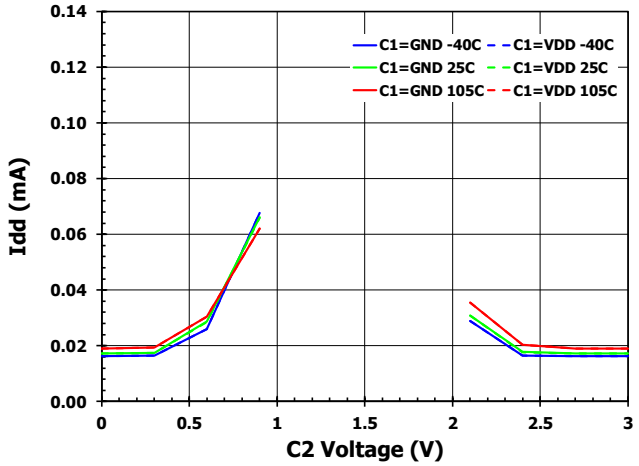


Figure 29. I_{DD} vs. Control Voltage; V_{DD} = 3.0V (C1 set to 0.9V and 2.1V)

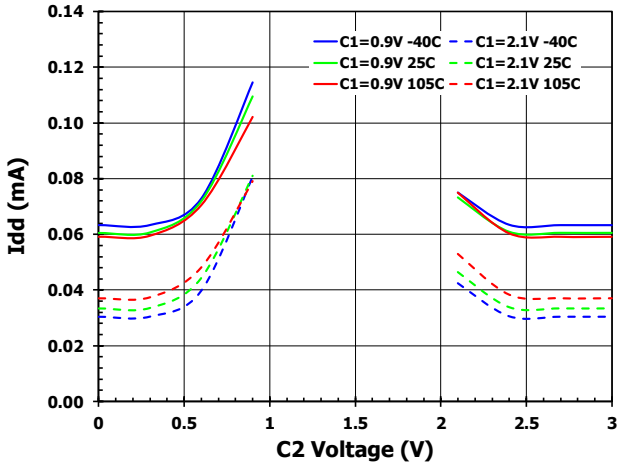


Figure 30. I_{DD} vs. Control Voltage; V_{DD} = 3.6V (C1 set to GND and V_{DD})

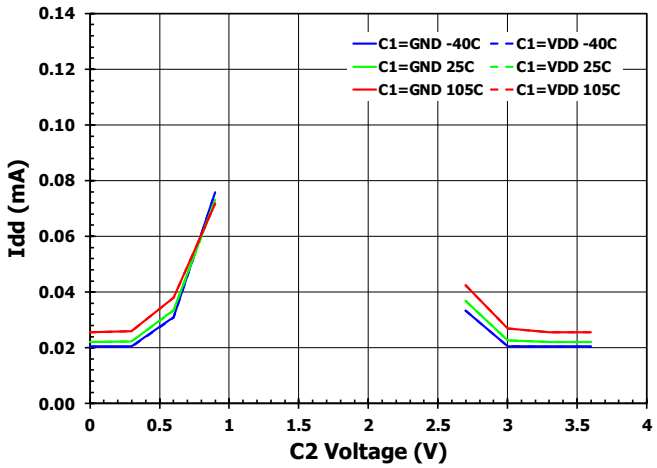
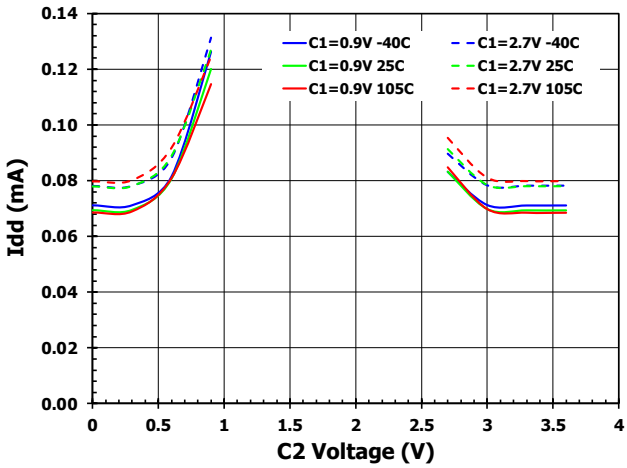


Figure 31. I_{DD} vs. Control Voltage; V_{DD} = 3.6V (C1 set to 0.9V and 2.7V)



Evaluation Kit Picture

Figure 32. Top View

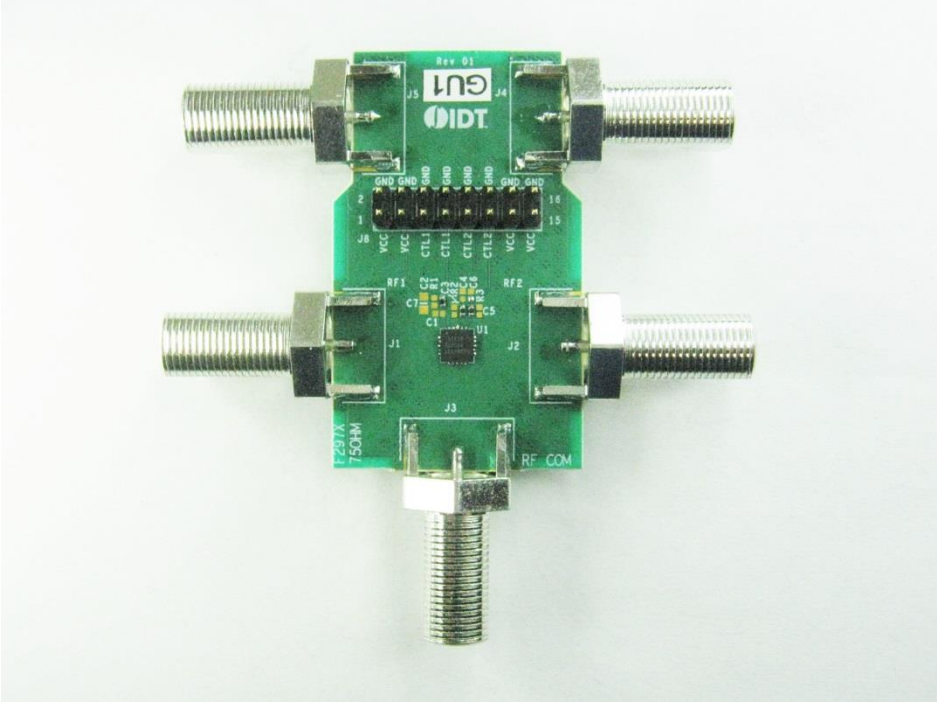
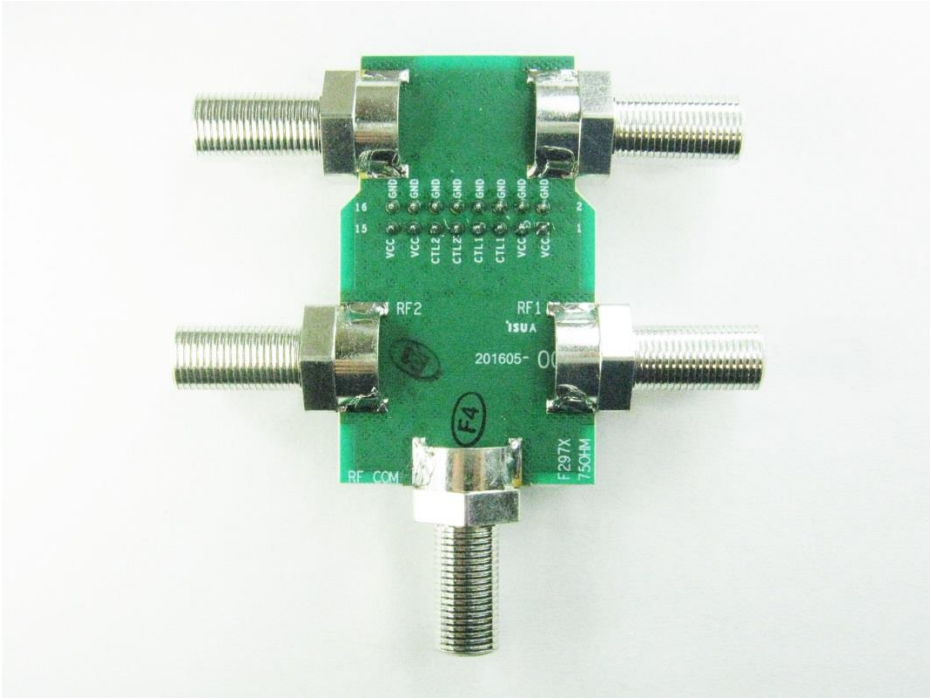


Figure 33. Bottom View



Evaluation Kit / Applications Circuit

Figure 34. Electrical Schematic

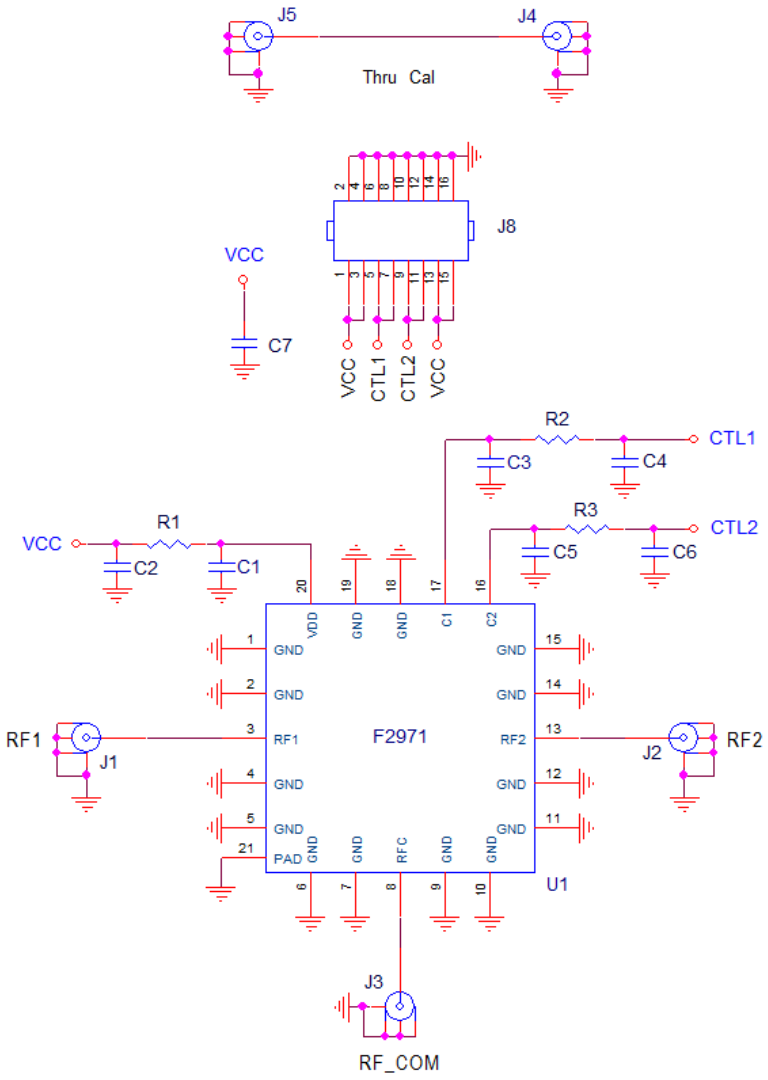


Table 7. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1 – C6	0	Not Installed		
C7	1	1000pF ±5%, 50V, C0G Ceramic Capacitor (0603)	GRM1885C1H102J	Murata
R1 – R3	3	100Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	Panasonic
J1 – J5	5	Connector Type F	222181	Amphenol RF
J8	1	Conn Header Vert 8x2 Pos Gold	961216-6404-AR	3M
U1	1	SP2T Switch 4mm x 4mm LQFN	F2971NCGK	IDT
	1	Printed Circuit Board	F297X EVKIT REV 01	IDT

Control Mode

Table 8. Switch Control Truth Table

C1	C2	RFC – RF1	RFC – RF2	75Ω Terminated Ports
LOW	LOW	OFF	OFF	RFC, RF1, RF2
LOW	HIGH	OFF	ON	RF1
HIGH	LOW	ON	OFF	RF2
HIGH	HIGH	N/A	N/A	N/A

Application Information

Default Start-up

Control pins do not include internal pull-down resistors to logic LOW or pull-up resistors to logic HIGH.

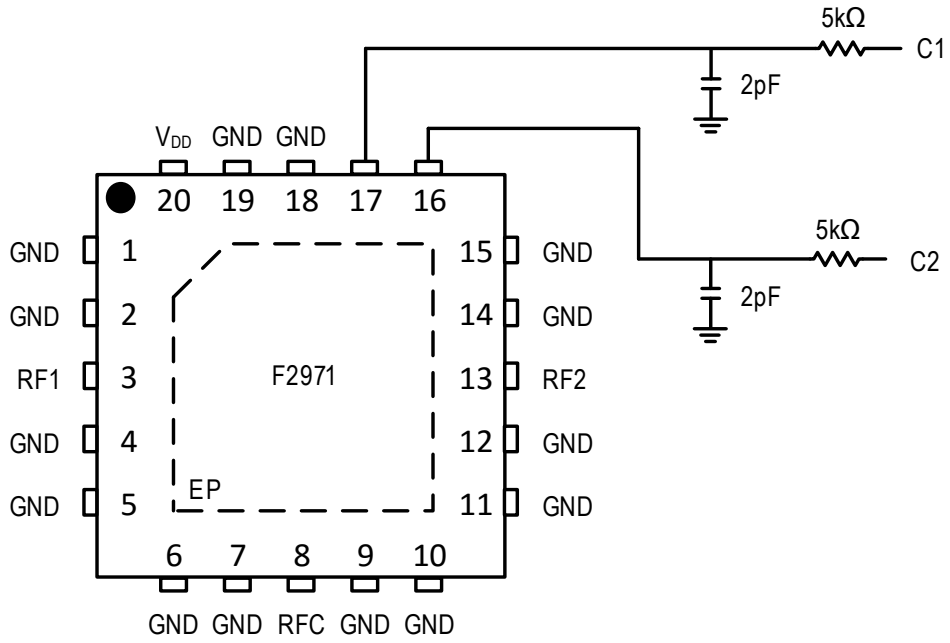
Power Supplies

A common V_{cc} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade the noise figure, and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V / 20µs. In addition, all control pins should remain at 0V (±0.3V) while the supply voltage ramps or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 16 and 17 as shown below.

Figure 35. Control Pin Interface Schematic



Evaluation Kit (EVKit) Operation

External Supply Setup

Set up a V_{CC} power supply in the voltage range of 2.7V to 3.6V with the power supply output disabled.

Logic Control Setup

External logic control is applied to J8 CTL1 (pins 5 and 7) and CTL2 (pins 9 and 11). See Table 8 for the logic truth table.

Turn On Procedure

Setup the supplies and EVKIT as noted in the “External Supply Setup” and “Logic Control Setup” sections above.

Enable the V_{CC} supply.

Set the desired logic setting to achieve the desired configuration (see Table 8). Note that external control logic should not be applied without V_{CC} being present.

Turn Off Procedure

Set the logic control to 0V.

Disable the V_{CC} supply.

Package Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available and is subject to change without notice or revision of this document.

www.idt.com/document/psc/20-qfn-package-outline-drawing-40-x-40-x-075-mm-body-05mm-pitch-epad-206-x-206-mm-ncg20p1

Marking Diagram

Line 1 and 2 are the part number.
Line 3 - “ZE” is for the die version.
Line 3 - “YWW” is the last digit of the year plus the work week.
Line 3 - “PBG” denotes the production process.

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Operating Temperature
F2971NCGK	4mm x 4mm x 0.75mm 20-LQFN (NCG20P1)	MSL1	Tray	-40°C to +105°C
F2971NCGK8	4mm x 4mm x 0.75mm 20-LQFN (NCG20P1)	MSL1	Reel	-40°C to +105°C
F2971EVBI	Evaluation Board			

Revision History

Revision	Revision Date	Description of Change
O	2018-April-24	Initial release.

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