

F6932

Dual-Channel Low Noise Amplifier 17.7GHz – 21.2GHz

The F6932 is an ultra-low power consumption, dual-channel, silicon on insulator (SOI) low noise amplifier (LNA) RFIC designed for application in Ka-Band SATCOM planar phased array antennas. The exceptional combination of low power consumption, low noise, high gain, and compact size, maximizes the antenna array G/T while minimizing overall system power dissipation.

The F6932 includes two LNA channels in a compact 23-pin, 0.5mm pitch BGA package. All inputs and outputs are single-ended and 50Ω matched for ease of integration on to phased array antenna panels.

Features

- Frequency: 17.7GHz – 21.2GHz
- Gain: 22dB
- Noise Figure: 1.2dB
- Output P1dB: -2dBm
- Power Consumption: 15mW/ch
- Supply Voltage: 1.2V nominal
- Compact size for planar integration on $\lambda/2$ grid
- 2.7 × 2.7 × 0.9 mm, 23-pin BGA
- -40°C to +85°C ambient operating temperature range

Applications

- Electronically Steered Phased Array Antennas (ESAs)
- Aerospace, Maritime, and Satcom-on-the-move (SOTM)
- Ka-Band SATCOM Terminals
- Communication, Electronic Warfare (EW) and Radar Systems

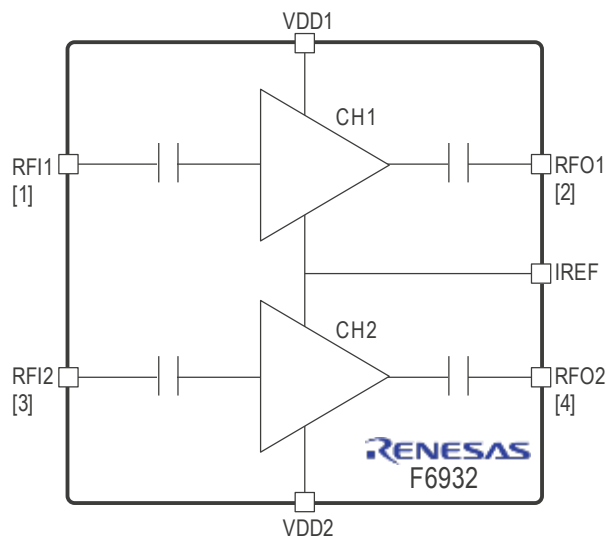


Figure 1. Block Diagram

Contents

1. Pin Information	3
1.1 Pin Assignments	3
1.2 Pin Descriptions.....	3
2. Specifications	4
2.1 Absolute Maximum Ratings	4
2.2 Recommended Operating Conditions.....	4
2.3 Thermal Specifications	4
2.4 Electrical Specifications	5
2.4.1 DC Electrical Specifications.....	5
2.4.2 RF Electrical Specifications.....	5
3. Typical Application Circuit	6
4. Typical Performance Graphs	7
5. Evaluation Board	10
5.1 Evaluation Board Photos	10
5.2 Evaluation Board Schematic.....	11
6. Package Outline Drawings	12
7. Marking Diagram	12
8. Ordering Information	12
9. Revision History	12

Figures

Figure 1. Block Diagram	1
Figure 2. Pin Assignments – Top View.....	3
Figure 3. Typical Application Circuits.....	6
Figure 4. Gain.....	7
Figure 5. Noise Figure	7
Figure 6. Input Match.....	7
Figure 7. Output Match.....	7
Figure 8. Output 1dB Compression	7
Figure 9. Output 3 rd Order Intercept	7
Figure 10. Reverse Isolation.....	8
Figure 11. Supply Current, Per Channel.....	8
Figure 12. I _{REF} Pin Voltage vs Current.....	8
Figure 13. Gain vs Bias	8
Figure 14. NF vs Bias	8
Figure 15. Supply Current vs Bias, Per Channel	8
Figure 16. Channel-Channel Isolation	9
Figure 17. Evaluation Board – Top View	10
Figure 18. Evaluation Board – Bottom View	10
Figure 19. Evaluation Board – Schematic	11

1. Pin Information

1.1 Pin Assignments

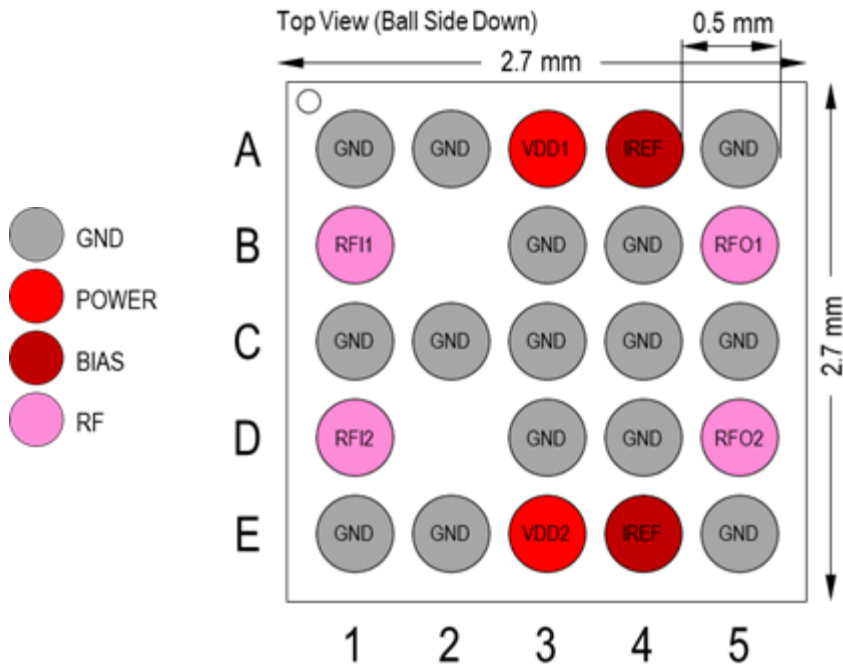


Figure 2. Pin Assignments – Top View

1.2 Pin Descriptions

Pin Number	Name	Type	I/O	Description
A1, A2, A5, B3, B4, C1, C2, C3, C4, C5, D3, D4, E1, E2, E5	GND	Ground	–	DC and RF ground.
A3	VDD1	Power	Input	Positive supply voltage input for channel 1.
E3	VDD2	Power	Input	Positive supply voltage input for channel 2. VDD1 must also be powered for channel 2 to be operable.
A4, E4	IREF	Power	Input	Reference bias current input, tied to a common node shared by channels 1 and 2. Connect directly to a current source, voltage source through a resistor, or to the IBx pin of the F612x beamforming IC.
B1	RFI1	Analog	Input	Channel 1 RF input port.
D1	RFI2	Analog	Input	Channel 2 RF input port.
B5	RFO1	Analog	Output	Channel 1 RF output port.
D5	RFO2	Analog	Output	Channel 2 RF output port.

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Exposure of the device to parameter values outside of the range listed below may reduce the operating lifetime and adversely and permanently alter the device characteristics. Furthermore, functional operation at or near absolute maximum ratings is not implied.

Parameter	Symbol	Conditions	Minimum	Maximum	Unit
Supply Voltage	V_{DD1} V_{DD2}	-	-0.3	1.4	V
IREF Pin Input Current	I_{REF}	-	0	70	μ A
IREF Pin Voltage	V_{REF}	-	0	0.75	V
RF Input Power	P_{IN}	VSWR \leq 2.1. 30s CW	-	0	dBm
Junction Temperature	T_J	-	-	125	$^{\circ}$ C
Lead Temperature (soldering)	T_{LEAD}	Not to exceed 30s at Max temperature per J-STD-020E	-	260	$^{\circ}$ C
Human Body Model, VHBM (Tested per JS-001-2012)	-	-	-	1000	V
Charged Device Model, VCDM (Tested per JESD22-C101)	-	-	-	150	V

2.2 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
RF Frequency Range	f_{RF}	17.7	-	21.2	GHz
Power Supply Voltage	V_{DD1} V_{DD2}	1.1	1.2	1.3	V
Reference Bias Current	I_{REF}	35	45	55	μ A
Ambient Temperature	T_A	-40	-	85	$^{\circ}$ C
RF Pin Load Impedance	Z_{RF}	-	50	-	Ω

2.3 Thermal Specifications

Parameter	Symbol	Value	Unit
Theta JB. Junction to board	θ_{JB}	14	$^{\circ}$ C/W
Theta JC. Junction to case (case top)	θ_{JC}	108	$^{\circ}$ C/W
Theta JA. Junction to ambient	θ_{JA}	47	$^{\circ}$ C/W
Storage Temperature	T_{STOR}	-40 to +150	$^{\circ}$ C

2.4 Electrical Specifications

2.4.1 DC Electrical Specifications

$V_{DD} = 1.2V$, $T_A = 25^\circ C$, unless otherwise specified.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Supply Current, Per Channel	I_{DD}	$I_{REF} = 45\mu A$, $T_A = 25^\circ C$	-	12.4	17.5	mA
		$I_{REF} = 45\mu A$, $T_A = 85^\circ C$	-	13.1	-	mA
Supply Current, Idle-state ^[1]	I_{DD_IDLE}	$I_{REF} = 0\mu A$	-	2	-	mA

1. I_{REF} pin may be grounded or left floating for idle state.

2.4.2 RF Electrical Specifications

$V_{DD} = 1.2V$, $I_{REF} = 45\mu A$, $T_A = 25^\circ C$, $Z_S = Z_L = 50\Omega$, $f_{RF} = 17.7 - 21.2$ GHz, unless otherwise specified.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain	G	$T_A = 25^\circ C$	18	22	-	dB
		$T_A = 85^\circ C$	-	21	-	dB
Gain Flatness vs. Frequency	G_{VAR_FREQ}	$f_{RF} = 17.7 - 21.2$ GHz	-	2.9	-	dB
		Within any 250MHz	-	0.3	-	dB
Noise Figure	NF	$T_A = 25^\circ C$	-	1.2	-	dB
		$T_A = 85^\circ C$	-	2.0	-	dB
Output 1dB Compression Point	OP1dB	-	-	-2	-	dBm
Output 3 rd Order Intercept Point	OIP3	Pin = -35 dBm/tone, $\Delta f = 1$ MHz	-	7	-	dBm
Input Return Loss	IRL	-	-	12	-	dB
Output Return Loss	ORL	-	-	13	-	dB
Reverse Isolation	ISO	-	-	45	-	dB
Channel-to-Channel Isolation	ISO_{CH-CH}	-	-	37	-	dB

3. Typical Application Circuit

Figure 3 shows two typical application circuits for biasing the F6932 supplying V_{DD1} and V_{DD2} from a single common V_{DD} supply.

The top circuit uses a voltage source V_{REF} to supply the bias reference current I_{REF} through an external resistor R_{REF} . V_{REF} should be set to achieve the recommended I_{REF} bias currents per the indicated formula. For $V_{REF} = 1.2V$, a value of $R_{REF} = 13.7k\Omega$ will produce the recommended typical I_{REF} bias condition.

The bottom circuit uses the programmable IDAC of the Renesas F612X beamforming IC to provide the reference current directly to the F6932.

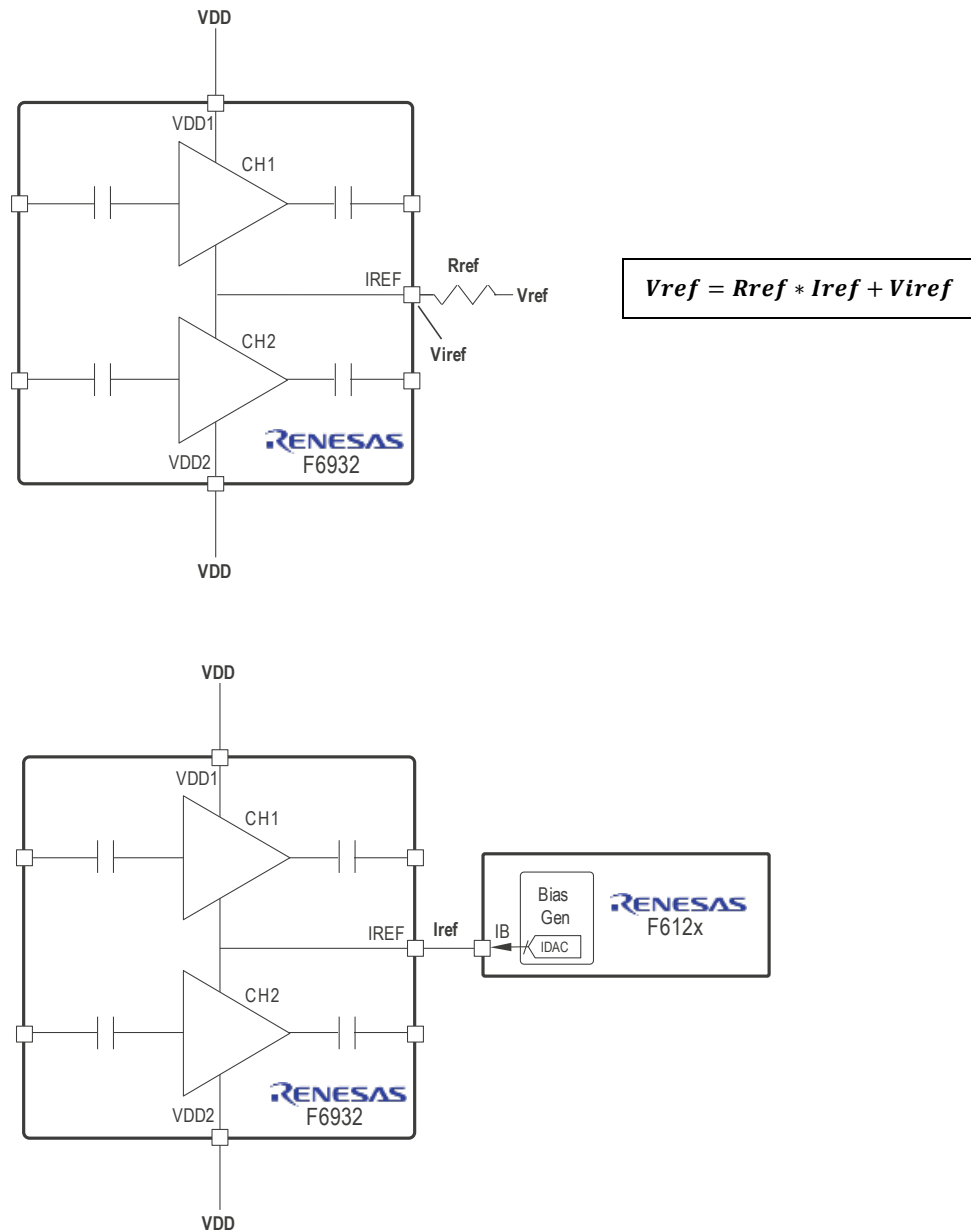


Figure 3. Typical Application Circuits

4. Typical Performance Graphs

$V_{DD} = 1.2V$, $I_{REF} = 45\mu A$, $T_A = 25^\circ C$, $Z_S = Z_L = 50\Omega$, $f_{RF} = 19.5GHz$ unless otherwise stated.

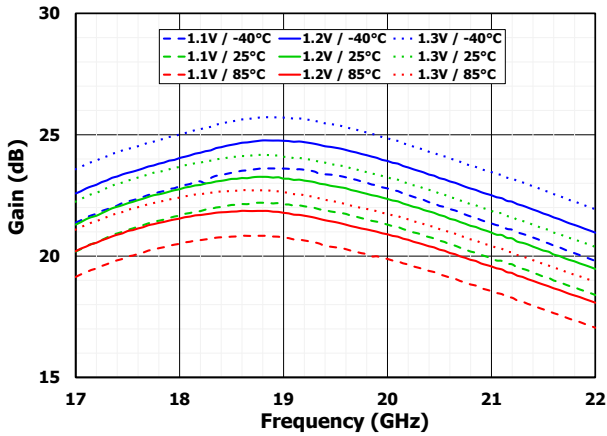


Figure 4. Gain

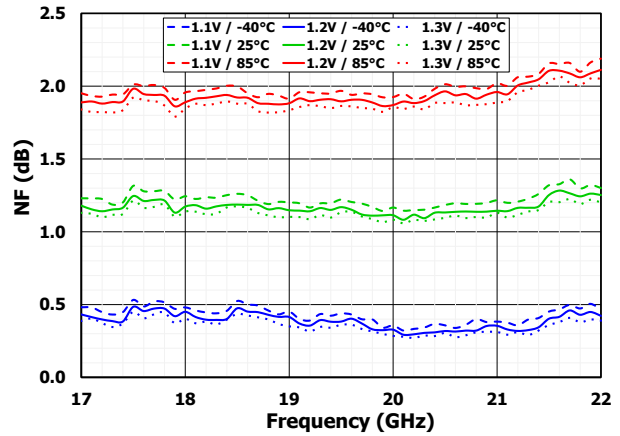


Figure 5. Noise Figure

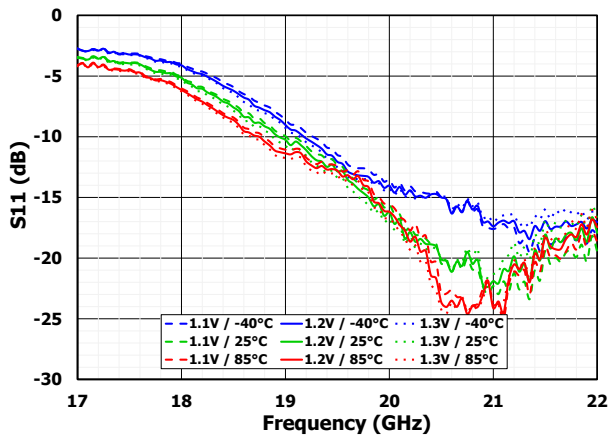


Figure 6. Input Match

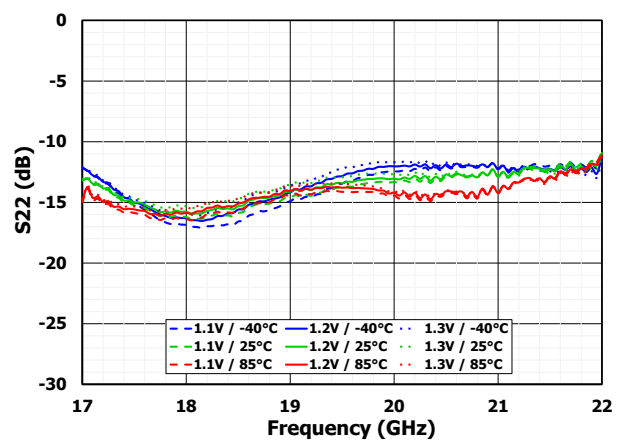


Figure 7. Output Match

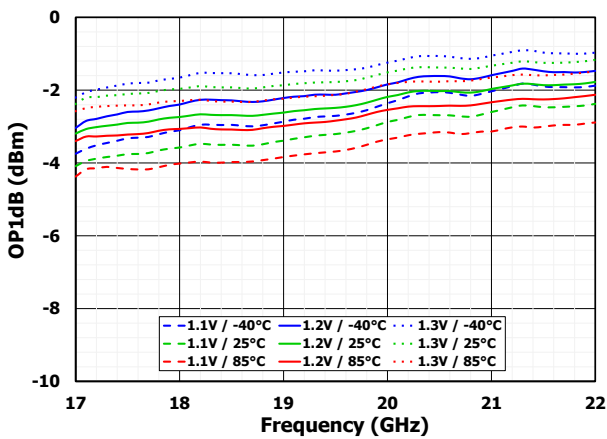


Figure 8. Output 1dB Compression

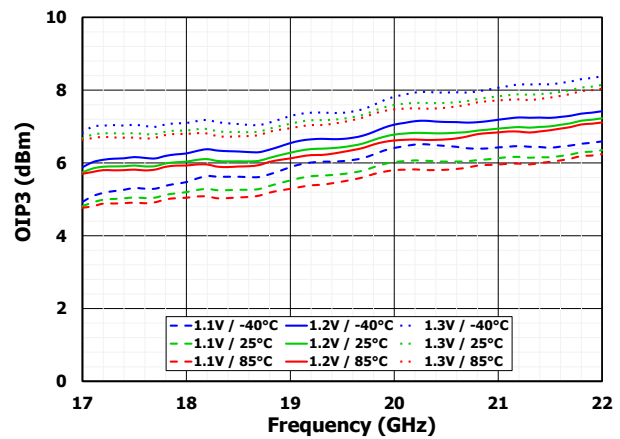


Figure 9. Output 3rd Order Intercept

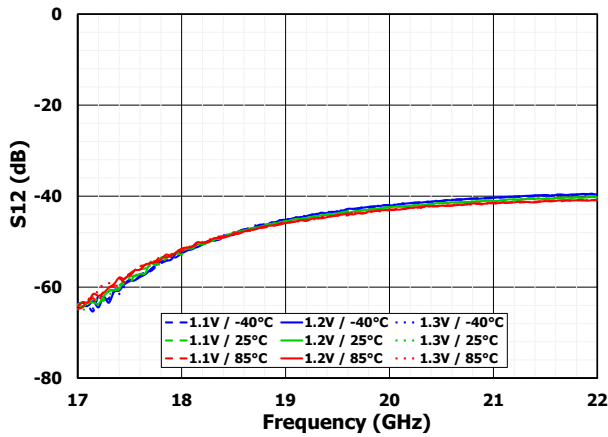


Figure 10. Reverse Isolation

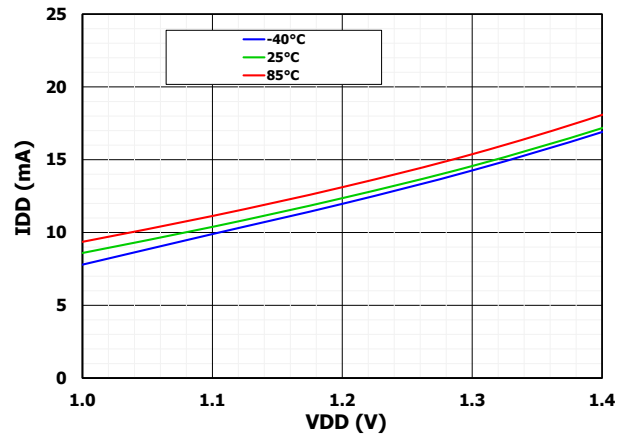


Figure 11. Supply Current, Per Channel

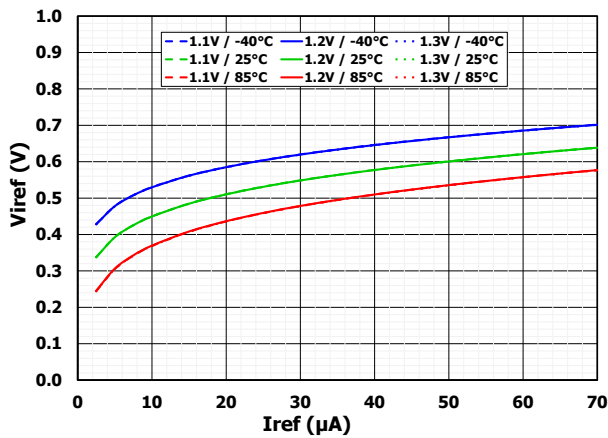


Figure 12. IREF Pin Voltage vs Current

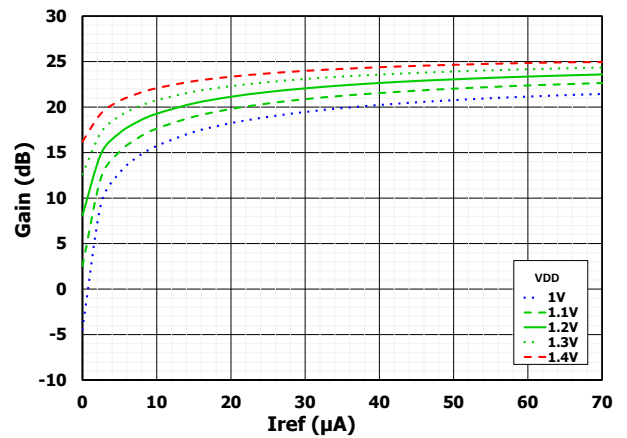


Figure 13. Gain vs Bias

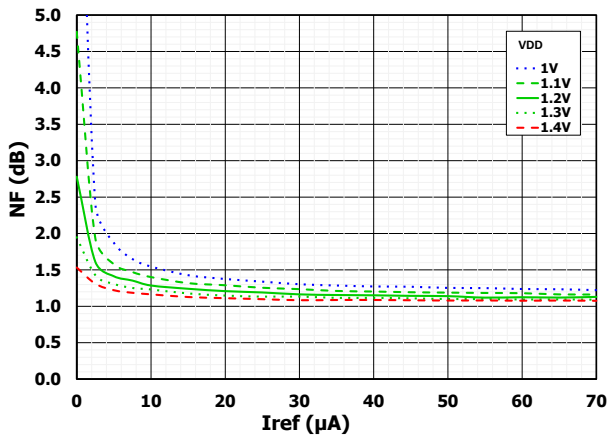


Figure 14. NF vs Bias

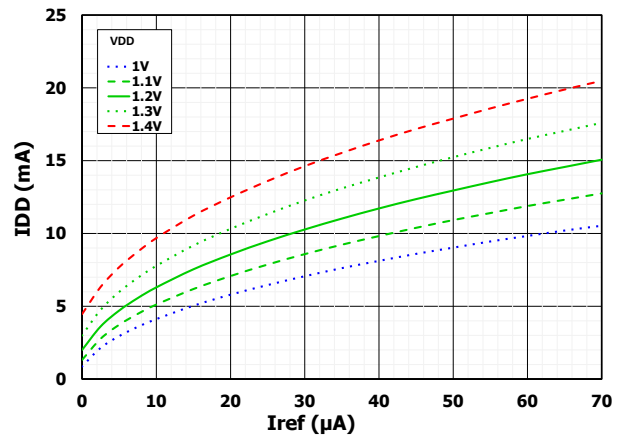


Figure 15. Supply Current vs Bias, Per Channel

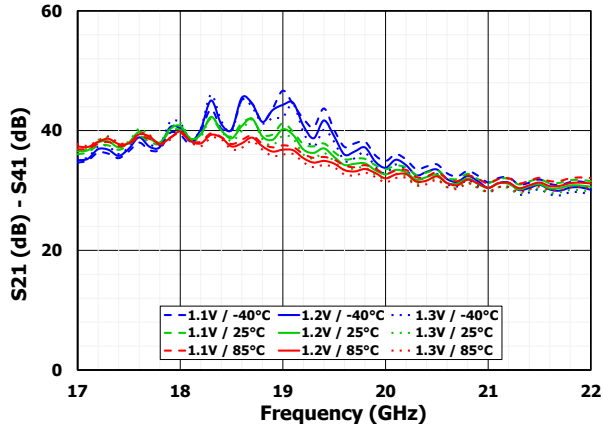


Figure 16. Channel-Channel Isolation

5. Evaluation Board

5.1 Evaluation Board Photos

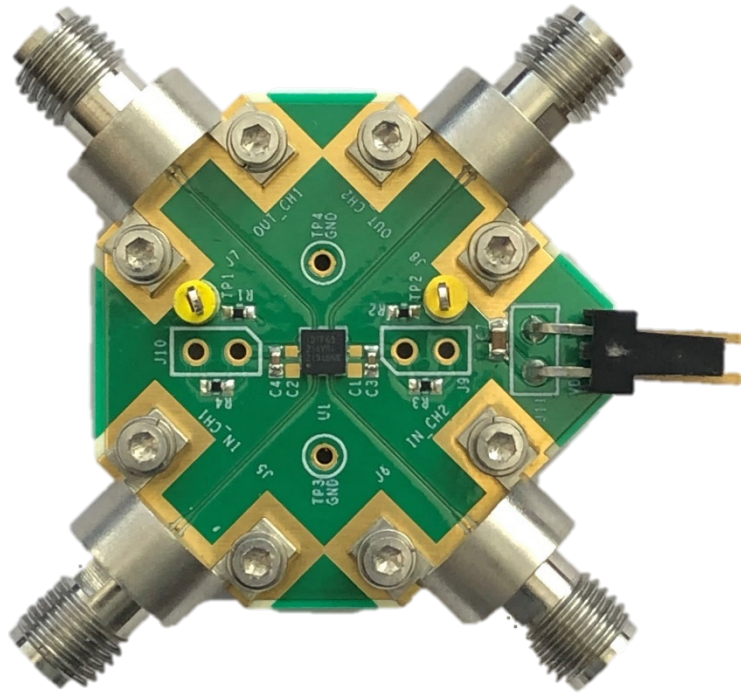


Figure 17. Evaluation Board – Top View

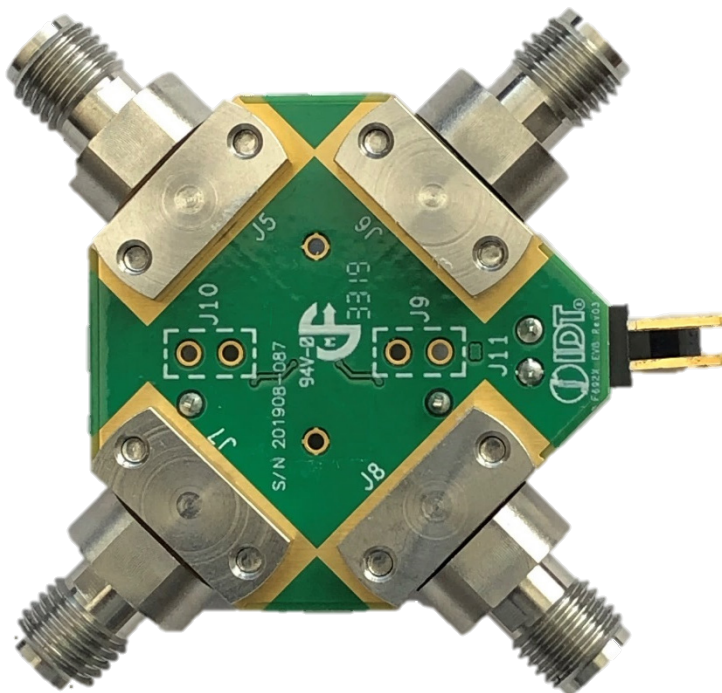


Figure 18. Evaluation Board – Bottom View

5.2 Evaluation Board Schematic

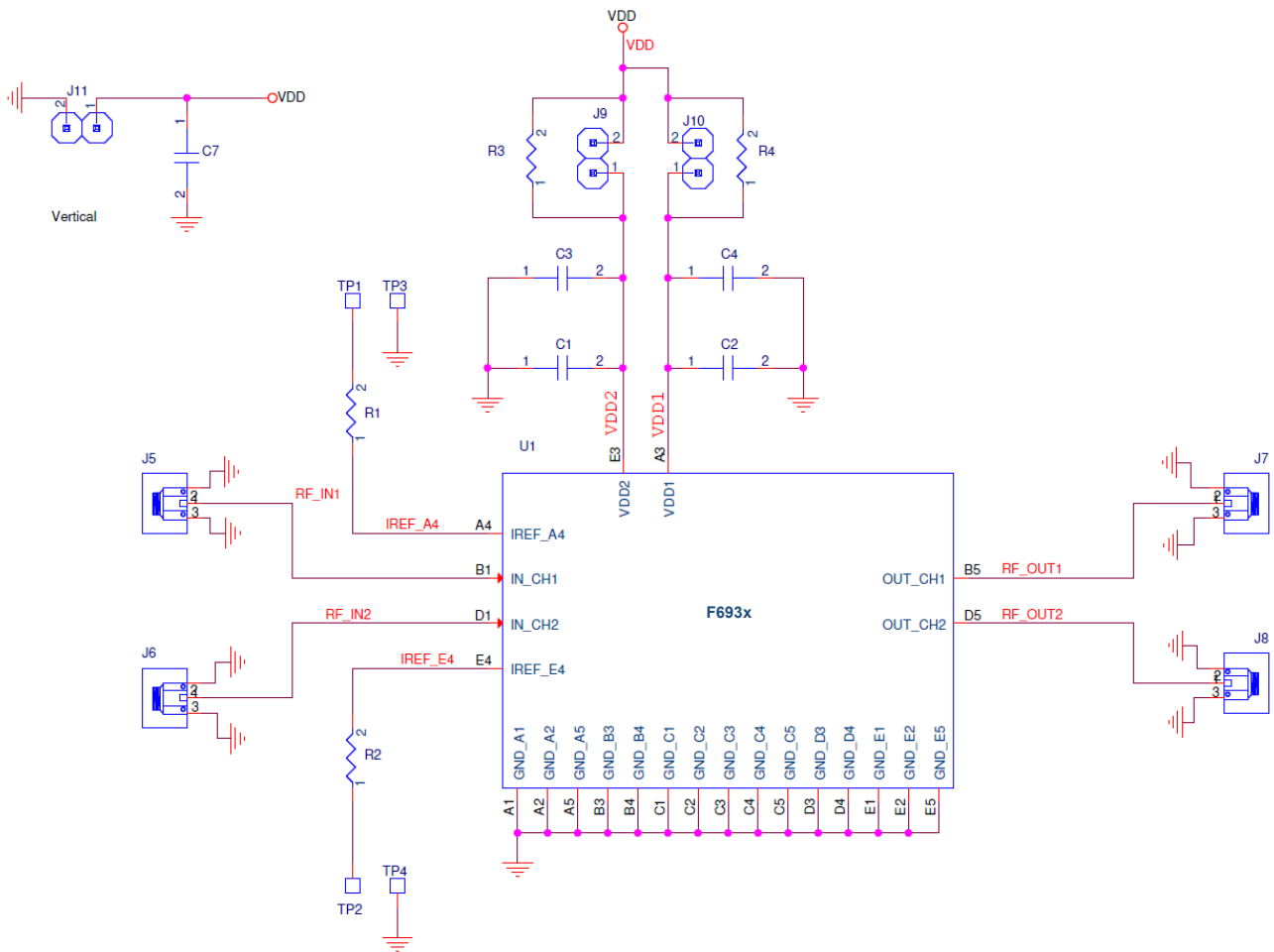


Figure 19. Evaluation Board – Schematic

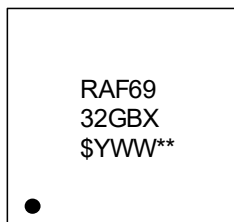
Table 1. Bill of Materials (BOM)

Part Reference	QTY	Description	Part Number	Manufacturer
C1, C2	2	33pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H330J	MURATA
C3, C4	2	1µF ±10%, 16V, X6S Ceramic Capacitor (0402)	GRM155C81C105K	MURATA
C7	1	10µF ±20%, 16V, X6S Ceramic Capacitor (0603)	GRM188C81C106M	MURATA
R1, R2	2	13.7kΩ ±1%, 1/16W, Resistor (0402)	RC0402FR-0713K7L	Yageo
R3, R4	2	0Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
J5–J8	4	Edge Launch 2.92mm 40GHz	ELF-40-002	SIGNAL MICROWAVE
J9, J10	2	DNI	DNI	DNI
J11	1	CONN HEADER R/A 2POS 2.54MM	1718571002	MOLEX
TP1, TP2, TP3, TP4	4	Test Point Yellow	5004	Keystone Electronics
U1	1	Dual-Channel Low Noise Amplifier 17.7GHZ to 21.2GHZ	F6932	Renesas

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

7. Marking Diagram



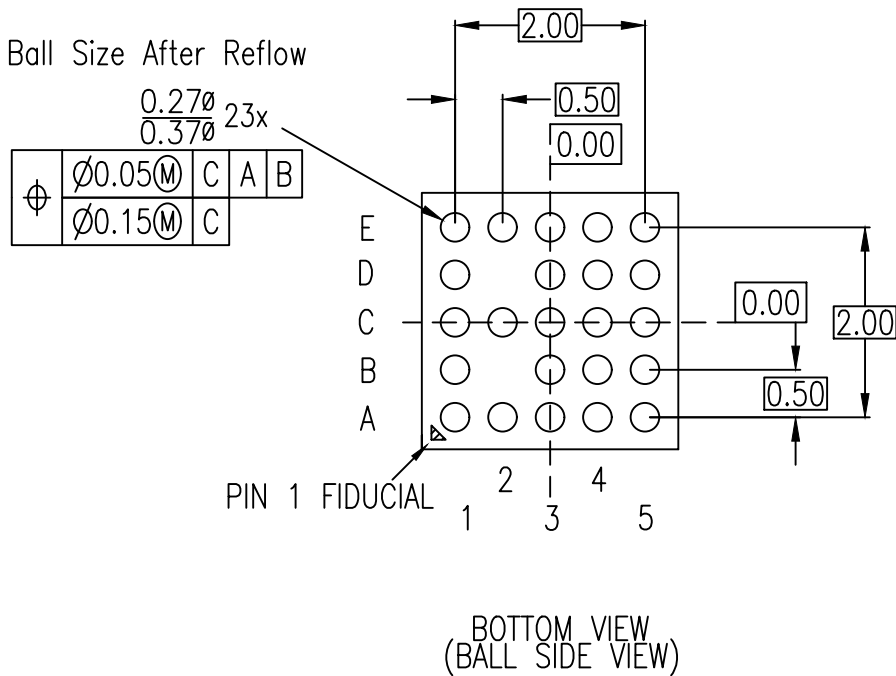
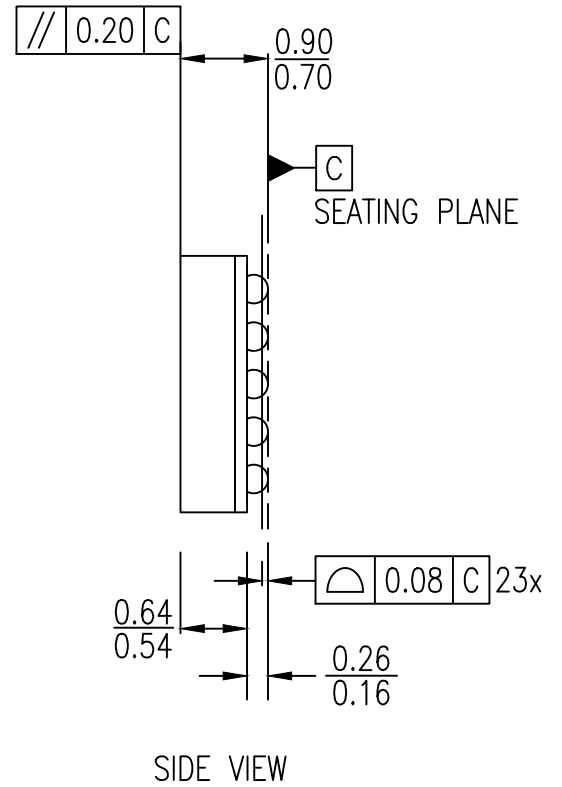
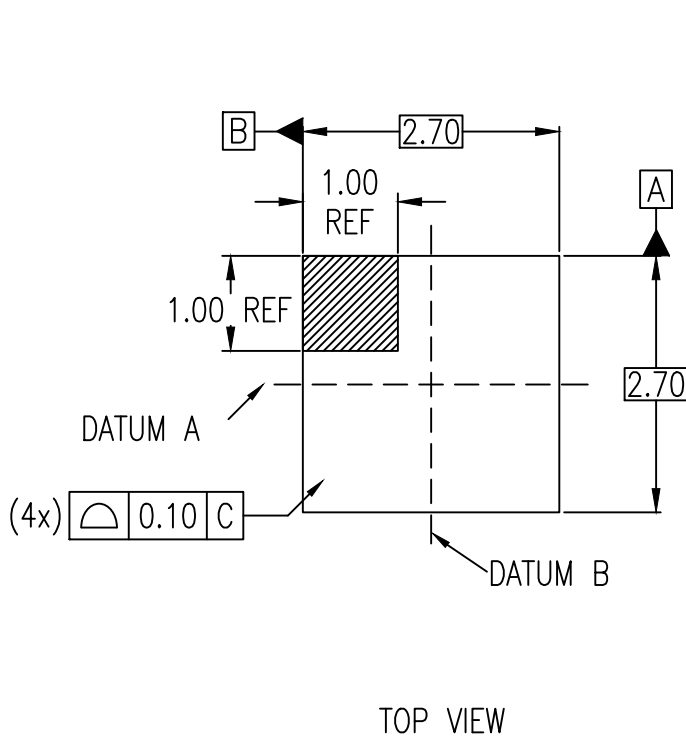
- Lines 1 and 2: part number
- Line 3:
 - “\$” is the mark location code
 - “Y” is the last digit of the assembly year
 - “WW” is the assembly workweek
 - “**” is the lot sequential code

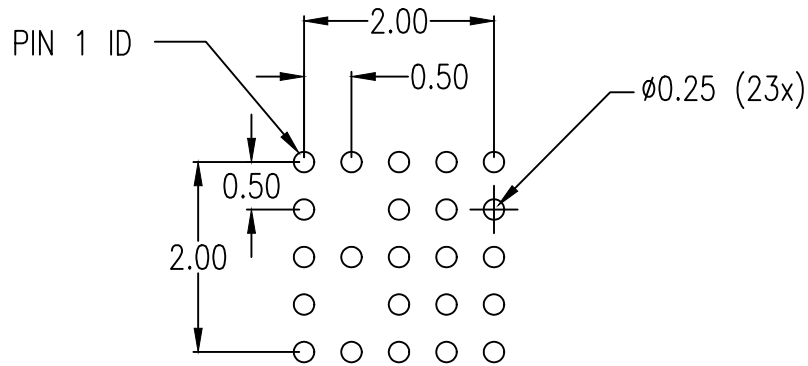
8. Ordering Information

Part Number	Package Description	MSL Rating	Carrier Type	Temperature Range
RA81F6932GBX#BC0	2.7 × 2.7 × 0.9 mm 23-FCCSP	3	Tray	-40°C to +85°C
RA81F6932GBX#HC0		3	Reel	
RTKA81F6932000RU	F6932 Evaluation Board			

9. Revision History

Revision	Date	Description
1.00	Feb 23, 2024	Initial release.





RECOMMENDED LAND PATTERN DIMENSION
(TOP VIEW)

NOTES:

1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Dec. 6, 2018	Rev 00	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.