## General Description

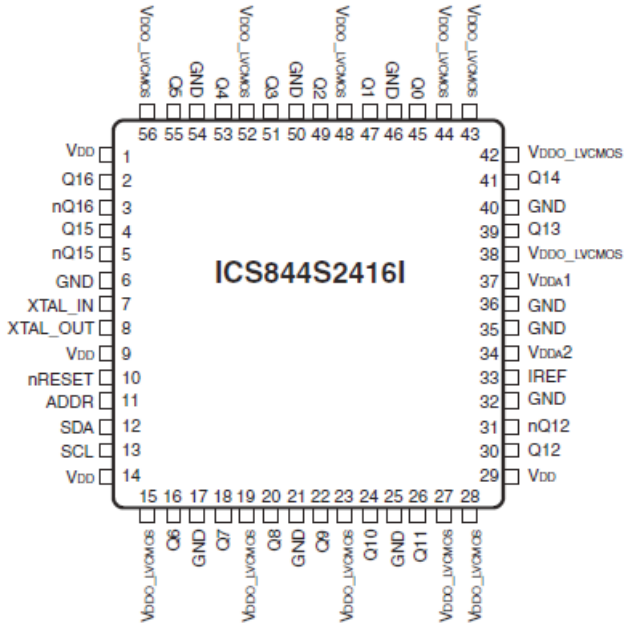
The 844S2416 is a 17 output, dual-PLL frequency synthesizer optimized to generate a variety of clocks for Ethernet, USB and other interfaces. Using a 25MHz 18pF parallel resonant crystal, the device will generate 24MHz, 25MHz, 100MHz and 200MHz clocks withmixed HCSL and LVCMOS/LVTTL levels.

The 844S2416 is packaged in a 56-pin VFQFN package that is optimum for applications with space limitations.

## Features

- Two LVCMOS/LVTTL single-ended outputs at 24MHz
  Twelve LVCMOS/LVTTL single-ended outputs at 25MHz
  Two differential HCSL output pairs at 100MHz
  One differential HCSL output pair at 100MHz or 200MHz
- Crystal oscillator interface: 25MHz
- PLL1 – VCO: 2.4GHz
- PLL2 – VCO range: 1.8GHz - 2.2GHz
  ±10% frequency margining in 1.25% steps
  Selectable spread spectrum – downspread at -0.5%
- I²C control interface with address configuration pin and with default loading on release of active low reset
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Pin Assignment




**56-Lead VFQFN**
8mm x 8mm x 0.925mm package body
**K Package**
Top View

## Block Diagram

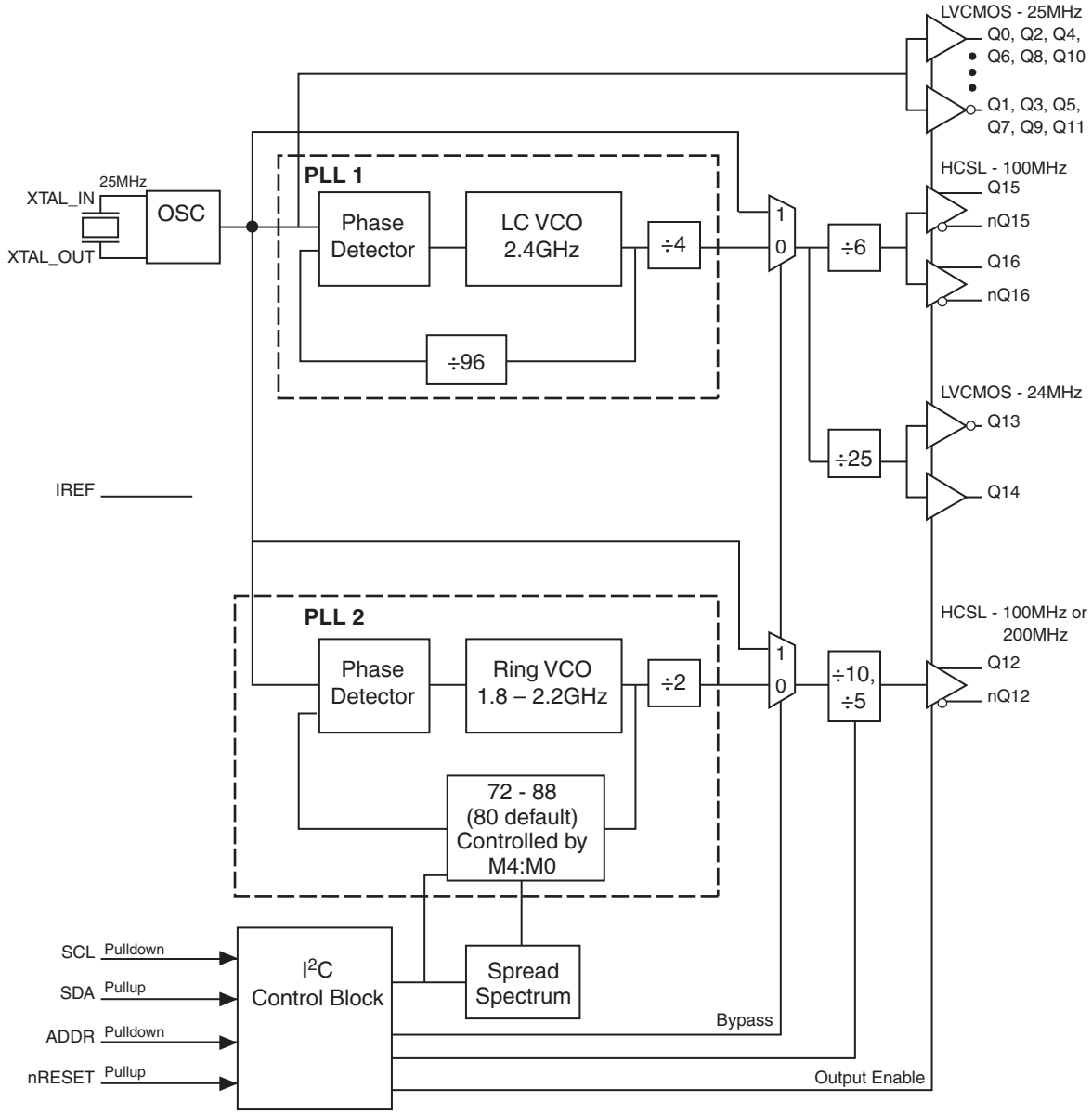


**Table 1. Pin Descriptions**

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1, 9, 14, 29 | $V_{DD}$ | Power | | Core supply pins. |
| 2, 3 | Q16, nQ16 | Output | | Differential clock outputs. HCSL interface levels. |
| 4, 5 | Q15, nQ15 | Output | | Differential clock outputs. HCSL interface levels. |
| 6, 17, 21, 25, 32, 35, 36, 40, 46, 50, 54 | GND | Power | | Power supply ground. |
| 7, 8 | XTAL_IN, XTAL_OUT | Input | | Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output. |
| 10 | nRESET | Input | Pullup | nRESET signal resets all the output dividers, default setting of PLL1 and I²C registers. nRESET signal also puts Q0:Q11 outputs in the Hi-Z state for power sequencing. LVCMOS/LVTTL interface levels. |
| 11 | ADDR | Input | Pulldown | Serial address select pin. LVCMOS/ LVTTL interface levels. |
| 12 | SDA | I/O | Pullup | I²C serial data input. LVCMOS/ LVTTL interface levels. |
| 13 | SCL | Input | Pulldown | I²C serial clock input. LVCMOS/ LVTTL interface levels. |
| 15, 19, 23, 27, 28, 38, 42, 43, 44, 48, 52, 56 | $V_{DDO\_LVCMOS}$ | Power | | Output supply pins for LVCMOS/LVTTL outputs. |
| 16, 20, 24, 41, 45, 49, 53 | Q6, Q8, Q10, Q14, Q0, Q2, Q4 | Output | | Single-ended non-inverted clock outputs. LVCMOS/LVTTL interface levels. |
| 18, 22, 26, 39, 47, 51, 55 | Q7, Q9, Q11, Q13, Q1, Q3, Q5 | | | Single-ended inverted clock outputs. LVCMOS/LVTTL interface levels. |
| 30, 31 | Q12, nQ12 | Output | | Differential clock outputs. HCSL interface levels. |
| 33 | IREF | | | HCSL current reference resistor output. An external fixed precision resistor (475Ω) from this output to ground provides a reference current used for differential current mode outputs Q12/nQ12, Q15/nQ15 and Q16/nQ16. |
| 34 | $V_{DDA2}$ | Power | | Analog supply pin for PLL2. |
| 37 | $V_{DDA1}$ | Power | | Analog supply pin for PLL1. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 5, Pin Characteristics, for typical values.

**Table 2. Pin Characteristics**

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | | 2 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | | 51 | | kΩ |
| $R_{OUT}$ | Output Impedance | Q0:Q11, Q13:Q14 | | | 21 | | Ω |

The 844S2416 uses an industry standard I²C interface to control the programming of the output enables of every output, the feedback divider value for PLL2, spread spectrum enabling for PLL2, and output divider clock source selection. The I²C control registers and default settings are shown below:

**Output Enable Control Bits:** Q0:Q11, Q13:Q14, Q15:Q16/nQ15:nQ16 outputs are enabled, Q12/nQ12 is disabled

**PLL2 M Divider Value:** 80

**SSC:** Off

**BYPASS:** Output divider clock source is the PLL

**Q12 Frequency (*ƒ*):** 200MHz

## I²C Register Summary

**Data Byte 0**

| Control Bit | Q16_EN | Q15_EN | Q14_EN | Q13_EN | Q12_EN | Q11_EN | Q10_EN | Q9_EN |
|---|---|---|---|---|---|---|---|---|
| Power-up Default Value | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |

**Data Byte 1**

| Control Bit | Q8_EN | Q7_EN | Q6_EN | Q5_EN | Q4_EN | Q3_EN | Q2_EN | Q1_EN |
|---|---|---|---|---|---|---|---|---|
| Power-up Default Value | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Data Byte 2**

| Control Bit | Q0_EN | M4 | M3 | M2 | M1 | M0 | SSC | BYPASS |
|---|---|---|---|---|---|---|---|---|
| Power-up Default Value | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

**Data Byte 3**

| Control Bit | *ƒ* (Q12) | Revision | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
|---|---|---|---|---|---|---|---|---|
| Power-up Default Value | 0 | 1 | X | X | X | X | X | X |

# Function Tables

### Table 3A. Output States Function Table

| Outputs | Output Levels | Disable State |
|---|---|---|
| Q0:Q11 | LVCMOS | Hi-Z |
| Q12/nQ12 | HCSL | Hi-Z |
| Q13:Q14 | LVCMOS | Hi-Z |
| Q15/nQ15 | HCSL | Hi-Z |
| Q16/nQ16 | HCSL | Hi-Z |

### Table 3B. PLL2 Feedback Divider Function Table (Q12/nQ12, ÷10 Mode)

| VCO Frequency (MHz) | Q12/nQ12 Frequency (MHz) | Feedback Divide | M4 | M3 | M2 | M1 | M0 |
|---|---|---|---|---|---|---|---|
| 1800 | 90 | 72 | 0 | 0 | 0 | 0 | 0 |
| 1825 | 91.25 | 73 | 0 | 0 | 0 | 0 | 1 |
| 1850 | 92.5 | 74 | 0 | 0 | 0 | 1 | 0 |
| 1875 | 93.75 | 75 | 0 | 0 | 0 | 1 | 1 |
| 1900 | 95 | 76 | 0 | 0 | 1 | 0 | 0 |
| 1925 | 96.25 | 77 | 0 | 0 | 1 | 0 | 1 |
| 1950 | 97.5 | 78 | 0 | 0 | 1 | 1 | 0 |
| 1975 | 98.75 | 79 | 0 | 0 | 1 | 1 | 1 |
| 2000 | 100 | 80 (default) | 0 | 1 | 0 | 0 | 0 |
| 2025 | 101.25 | 81 | 0 | 1 | 0 | 0 | 1 |
| 2050 | 102.5 | 82 | 0 | 1 | 0 | 1 | 0 |
| 2075 | 103.75 | 83 | 0 | 1 | 0 | 1 | 1 |
| 2100 | 105 | 84 | 0 | 1 | 1 | 0 | 0 |
| 2125 | 106.25 | 85 | 0 | 1 | 1 | 0 | 1 |
| 2150 | 107.5 | 86 | 0 | 1 | 1 | 1 | 0 |
| 2175 | 108.75 | 87 | 0 | 1 | 1 | 1 | 1 |
| 2200 | 110 | 88 | 1 | 0 | 0 | 0 | 0 |
| Not Used | Not Used | Not Used | 1 | 0 | 0 | 0 | 1 |
| | | | • • • | | | | |
| | | | 1 | 1 | 1 | 1 | 1 |

### Table 3C. PLL2, SSC Mode Function Table

| Register Bit | |
|---|---|
| SSC | SS Mode |
| 0 | |
| 1 | |

### Table 3D. Bypass Clock Selection Table

| Register Bit | |
|---|---|
| Bypass | Clock Source |
| 0 (default) | |
| 1 | |

### Table 3E. Q12 Frequency Selection Table

| Register Bit | |
|---|---|
| Q12 Frequency | Output Frequency |
| 0 (default) | 200MHz |
| 1 | 100MHz |

### Table 3F. Revision Description Table

| Register Bit | |
|---|---|
| Revision | Part Revision |
| 0 | Revision B |
| 1 | Revision C |

## I²C Addressing

The 844S2416 can be set to decode one of two addresses to minimize the chance of address conflict on the I²C bus. The address that is decoded is controlled by the setting of the ADDR pin as shown below.

**ADDR = 0**

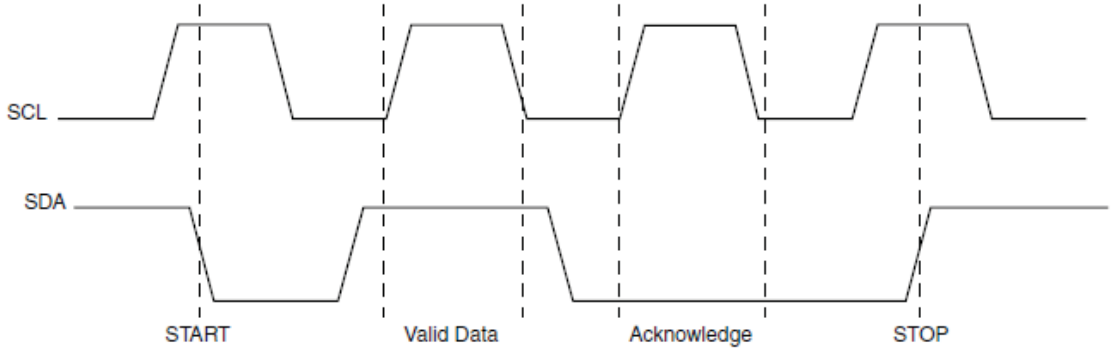
| ADDR = 0 Default | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | R/W |

**ADDR = 1**

| ADDR = 1 | | | | | | | |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | R/W |

## I²C Interface - Protocol

The 844S2416 is a slave-only device and uses the standard I²C protocol as shown in the below diagrams. The maximum SCL frequency is greater than 10MHz which is more than sufficient for standard I²C clock speeds.




**START (ST)** – defined as high-to-low transition on SDA while holding SCL HIGH.

**DATA** - Between START and STOP cycles, SDA is synchronous with SCL.
Data may change only when SCL is LOW and must be stable when SCL is HIGH.

**ACKNOWLEDGE (AK)** – SDA is driven LOW before the SCL rising edge and held LOW until the SCL falling edge.

**STOP (SP)** – defined as low-to-high transition on SDA while holding SCL HIGH.

## I²C Interface - A Write Example

A serial transfer to the 844S2416 always consists of an address cycle followed by 4 data bytes. Once the 4 data bytes are loaded and the master generates a stop condition, the values in the serial control register are latched into the M divider and control bits, and the device will move to the new frequency and any changes to the state of the control bits will take effect.

| ST | Slave Address: 7 Bits | R/W | AK |
|---|---|---|---|
| 1 Bit | Refer to I²C Addressing section for address choices based on ADDR pin setting | 1 Bit | 1 Bit |

| Data Byte 0: 8 Bits | | | | | | | | AK |
|---|---|---|---|---|---|---|---|---|
| Q16_EN | Q15_EN | Q14_EN | Q13_EN | Q12_EN | Q11_EN | Q10_EN | Q9_EN | 1 Bit |

| Data Byte 1: 8 Bits | | | | | | | | AK |
|---|---|---|---|---|---|---|---|---|
| Q8_EN | Q7_EN | Q6_EN | Q5_EN | Q4_EN | Q3_EN | Q2_EN | Q1_EN | 1 Bit |

| Data Byte 2: 8 Bits | | | | | | | | AK |
|---|---|---|---|---|---|---|---|---|
| Q0_EN | M4 | M3 | M2 | M1 | M0 | SSC | BYPASS | 1 Bit |

| Data Byte 3: 8 Bits | | | | | | | | AK | SP |
|---|---|---|---|---|---|---|---|---|---|
| ƒ (Q12) | Revision | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | 1 Bit | 1 Bit |

Data Byte values latched into control registers here.

### Absolute Maximum Ratings

| | |
|---|---|
| Supply Voltage, $V_{DD}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{DD}$ + 0.5 V |
| Outputs, $V_O$ (LVCMOS & HCSL) | -0.5V to $V_{DDO\_LVCMOS}$ + 0.5V |
| Package Thermal Impedance, $\theta_{JA}$ | 31.4°C/W (0 mps) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**Table 4A. Power Supply DC Characteristics,** $V_{DD}$ = $V_{DDO\_LVCMOS}$ = 3.3V±5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{DDA1}$, $V_{DDA2}$ | Analog Supply Voltage | | $V_{DD}$ – 0.31 | 3.3 | $V_{DD}$ | V |
| $V_{DDO\_LVCMOS}$ | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{DD}$ | Power Supply Current | No Load | | | 170 | mA |
| $I_{DDA1}$ | PLL1 Analog Supply Current | | | | 9 | mA |
| $I_{DDA2}$ | PLL2 Analog Supply Current | | | | 22 | mA |
| $I_{DDO\_LVCMOS}$ | Output Supply Current | No Load<br>Q[0:11] at 25MHz,<br>Q13, Q14 at 24MHz | | | 16 | mA |

**Table 4B. LVCMOS / LVTTL DC Characteristics,** $V_{DD}$ = $V_{DDO\_LVCMOS}$ = 3.3V±5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | ADDR, SCL | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 150 | µA |
| | | SDA, nRESET | $V_{DD}$ = $V_{IN}$ = 3.465V | | | 10 | µA |
| $I_{IL}$ | Input Low Current | ADDR, SCL | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -10 | | | µA |
| | | SDA, nRESET | $V_{DD}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |
| $V_{OH}$ | Output High Voltage | | $I_{OH}$ = -12mA | 2.6 | | | V |
| $V_{OL}$ | Output Low Voltage | | $I_{OL}$ = 12mA | | | 0.5 | V |

**Table 5. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Drive Level | | | | 100 | µW |

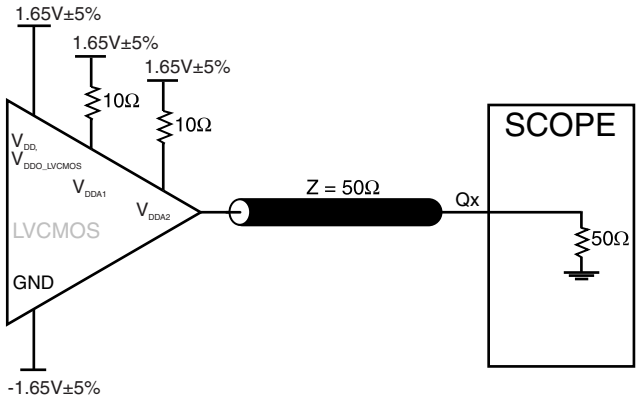
**TABLE 6. AC CHARACTERISTICS,** $V_{DD} = V_{DDO\_LVCMOS} = 3.3V \pm 5\%$, $T_A$ = -40°C TO 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | Q0:Q11 | | | 25 | | MHz |
| | | Q12/nQ12 | | | 100 | | MHz |
| | | Q13, Q14 | | | 24 | | MHz |
| | | Q15:Q16/nQ15:nQ16 | | | 100 | | MHz |
| $t_{jit(per)}$ | Period Jitter, Peak-to-Peak | Q12/nQ12 | BER = 10E-12, 100MHz | | | 70 | ps |
| | | Q13, Q14 | BER = 10E-12, 24MHz | | | 95 | ps |
| | | Q15:Q16/nQ15:nQ16 | BER = 10E-12, 100MHz | | | 70 | ps |
| $t_{jit(cc)}$ | Cycle-to-Cycle Jitter; NOTE 1, 2 | Q0:Q11 | 25MHz | | | 30 | ps |
| | | Q12/nQ12 | 100MHz | | | 80 | ps |
| | | Q13, Q14 | 24MHz | | | 90 | ps |
| | | Q15:Q16/nQ15:nQ16 | 100MHz | | | 70 | ps |
| $t_{RESET}$ | Minimum Reset Time for nRESET | | | 1.6 | | | ns |
| $t_{OEPD}$ | Maximum Propagation Delay from OE Register to Clock | | | | | $10 + t_{PER}$ | ns |
| $t_L$ | PLL Lock Time | | | | | 50 | ms |
| $F_{xtal}$ | Crystal Input Range; NOTE 1 | | | | 25 | | MHz |
| $F_M$ | SSC Modulation Frequency; NOTE 3 | | | 29 | | 33.33 | kHz |
| $F_{MF}$ | SSC Modulation Factor; NOTE 3 | | | | -0.4 | -0.5 | % |
| $SSC_{red}$ | Spectral Reduction; NOTE 3 | | | 4 | 6 | | dB |
| $t_{STABLE}$ | Power-up to Stable Clock Output, NOTE 4, 5 | | | 500 | | | ps |
| $V_{MAX}$ | Absolue Maximum Output Voltage; NOTE 6, 7 | | HCSL Levels | | | 1150 | mV |
| $V_{MIN}$ | Absolute Minimum Output Voltage; NOTE 6, 8 | | HCSL Levels | -300 | | | mV |
| $V_{rb}$ | Ringback Voltage; NOTE 4, 5 | | HCSL Levels | -100 | | 100 | mV |
| $V_{CROSS}$ | Absolute Crossing Voltage; NOTE 6, 9, 10 | | HCSL Levels | 250 | | 550 | mV |
| $\Delta V_{CROSS}$ | Total Variation of $V_{CROSS}$; NOTE 6, 9, 11 | | HCSL Levels | | | 140 | mV |
| $t_R$ / $t_F$ | Output Rise/Fall Time | Q[0:11], Q13, Q14 | 20% - 80% | 150 | | 350 | ps |
| | Rise/Fall Edge Rate; NOTE 4, 12 | | | 0.6 | | 5 | V/ns |
| odc | Output Duty Cycle; NOTE 4 | Q[0:11] | | 42 | | 58 | % |
| | | Q13, Q14 | | 49 | | 51 | % |
| | | Q12/nQ12, Q15/nQ15, Q16/nQ16 | | 49 | | 51 | % |

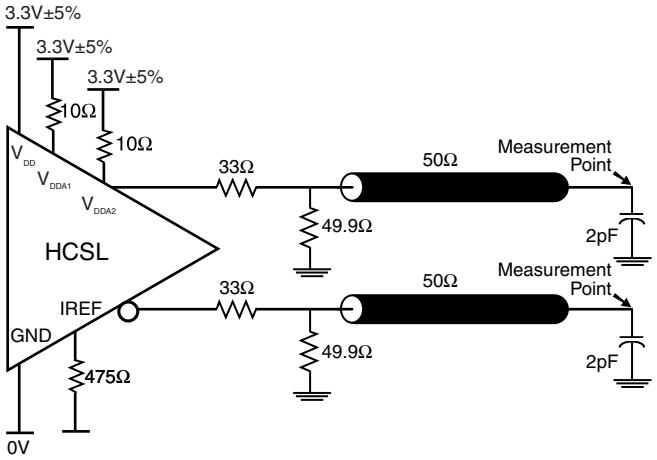
NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 2: Only valid within the VCO operating range.
NOTE 3: Spread Spectrum clocking enabled.
NOTE 4: Measurement taken from differential waveform.
NOTE 5: $T_{STABLE}$ is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to droop back into the $V_{RB}$ ±100mV differential range. See Parameter Measurement Information Section.
NOTE 6: Measurement taken from single-ended waveform.
NOTES continued on next page.

NOTE 7: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 8: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 9: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx. See Parameter Measurement Information Section.
NOTE 10: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.
NOTE 11: Defined as the total variation of all crossing voltage of Rising Qx and Falling nQx. This is the maximum allowed variance in the $V_{CROSS}$ for any particular system. See Parameter Measurement Information Section.
NOTE 12: Measured from -150mV to +150mV on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Parameter Measurement Information Section.

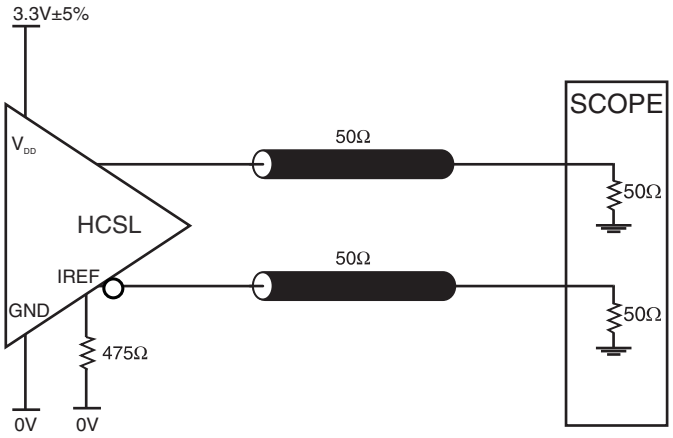
# Parameter Measurement Information




### 3.3V Core/3.3V LVCMOS Output Load AC Test Circuit

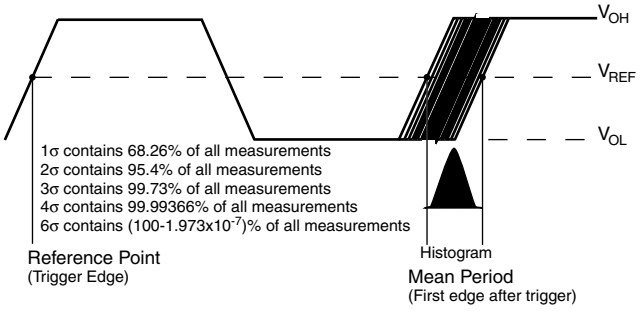



### 3.3V Core/3.3V HCSL Output Load AC Test Circuit

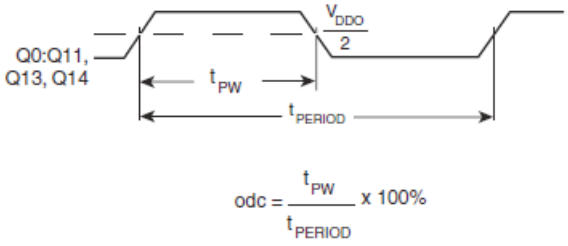



This load condition is used for $I_{DD}$, $I_{DDA1}$, $I_{DDA2}$ and *t*jit measurements.

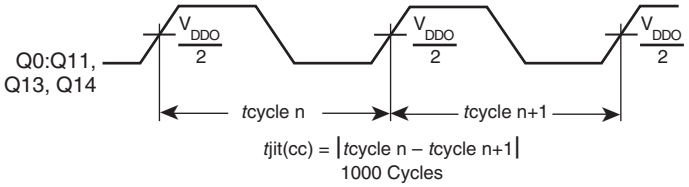
### HCSL Output Load AC Test Circuit




### Period Jitter

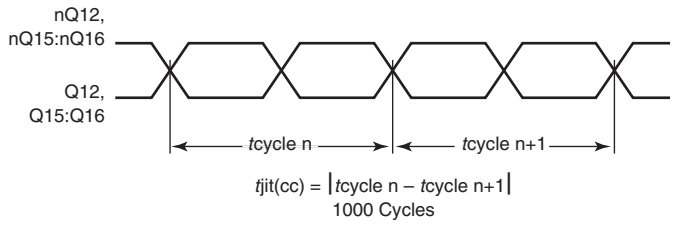



### LVCMOS Output Duty Cycle/Pulse Width/Period

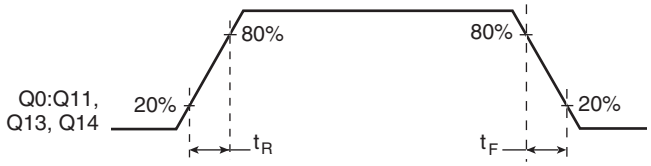



### LVCMOS Cycle-to-Cycle Jitter

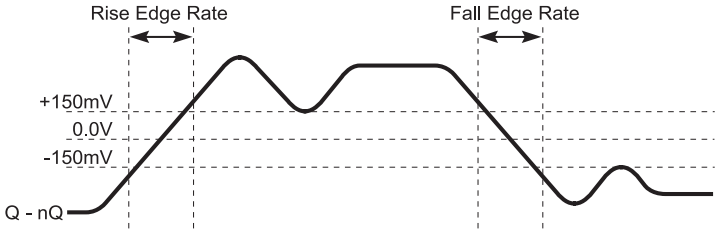
# PARAMETER MEASUREMENT INFORMATION, CONTINUED



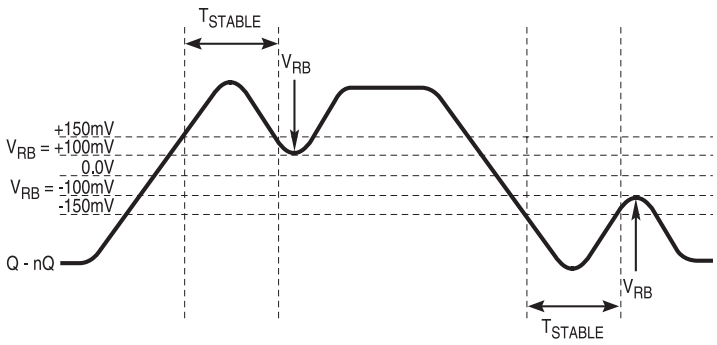

**HCSL CYCLE-TO-CYCLE JITTER**



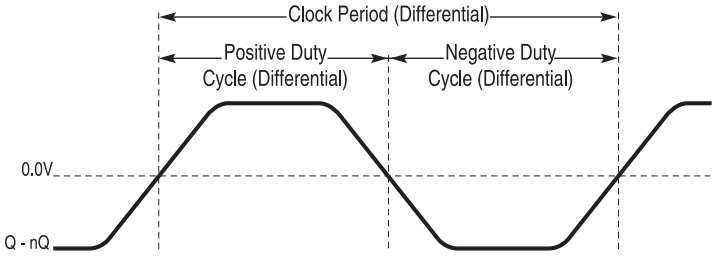

**LVCMOS OUTPUT RISE/FALL TIME**



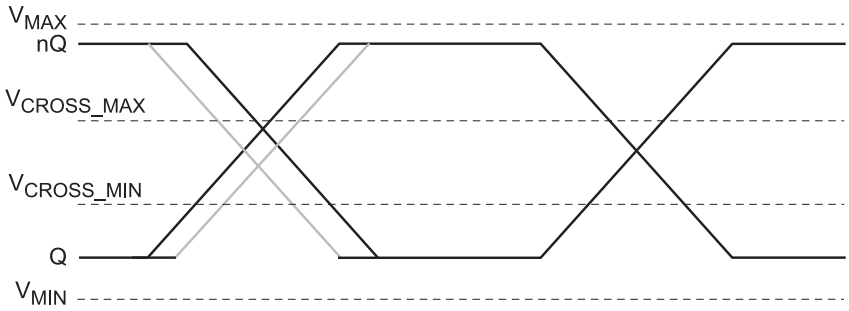

**DIFFERENTIAL HCSL MEASUREMENT POINTS FOR RISE/FALL EDGE RATE**




**DIFFERENTIAL MEASUREMENT POINTS FOR RINGBACK**




**HCSL DIFFERENTIAL MEASUREMENT POINTS FOR DUTY CYCLE/PERIOD**




**SINGLE-ENDED MEASUREMENT POINTS FOR ABSOLUTE CROSS POINT/SWING**

# APPLICATION INFORMATION

## POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 844S2416 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. $V_{DD}$, $V_{DDAX}$ and $V_{DDO\_LVCMOS}$ should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic $V_{DD}$ pin and also shows that $V_{DDA}$ requires that an additional10Ω resistor along with a 10µF bypass capacitor be connected to the $V_{DDA}$ pin.

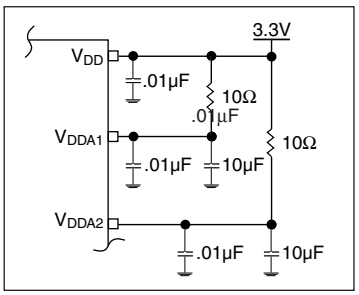



FIGURE 1. POWER SUPPLY FILTERING

## RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

### INPUTS:

#### LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### OUTPUTS:

#### LVCMOS OUTPUTS

All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

#### DIFFERENTIAL OUTPUTS

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Crystal Input Interface

The 844S2416 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The value can be varied for different board layouts.

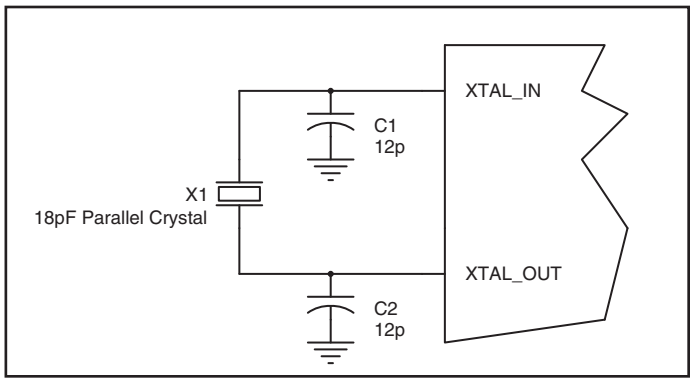



**Figure 2. Crystal Input Interface**

## LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

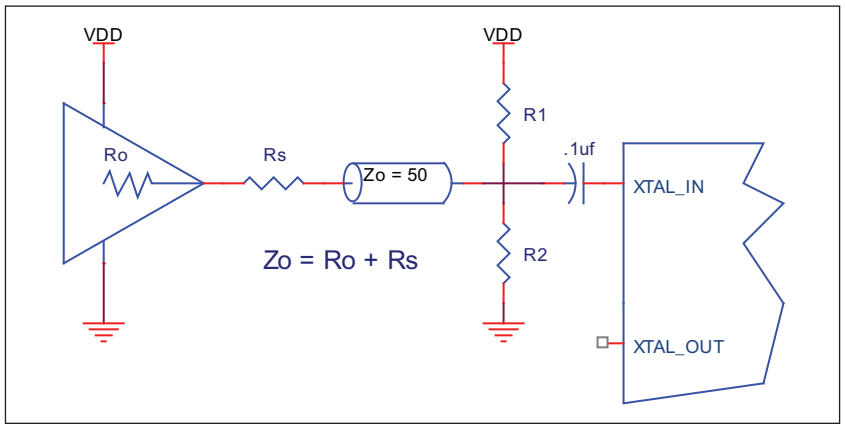



**Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface**

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor's Thermally/Electrically Enhance Leadfame Base Package, Amkor Technology.

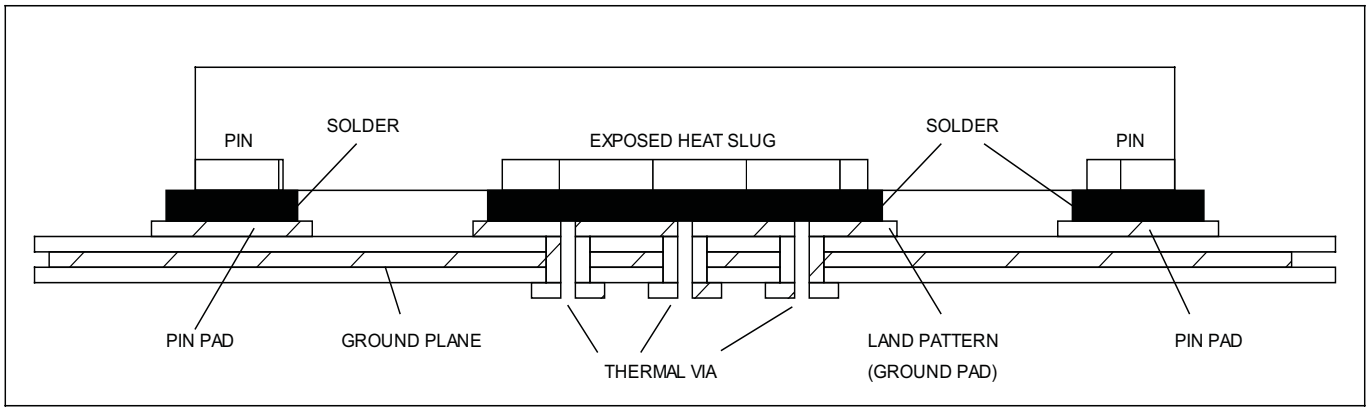



**Figure 4. P.C.Assembly for Exposed Pad Thermal Release Path –Side View (Drawing not to Scale)**

## Recommended Termination

*Figure 5A* is the recommended termination for applications which require the receiver and driver to be on a separate PCB. All traces should be 50Ω impedance.

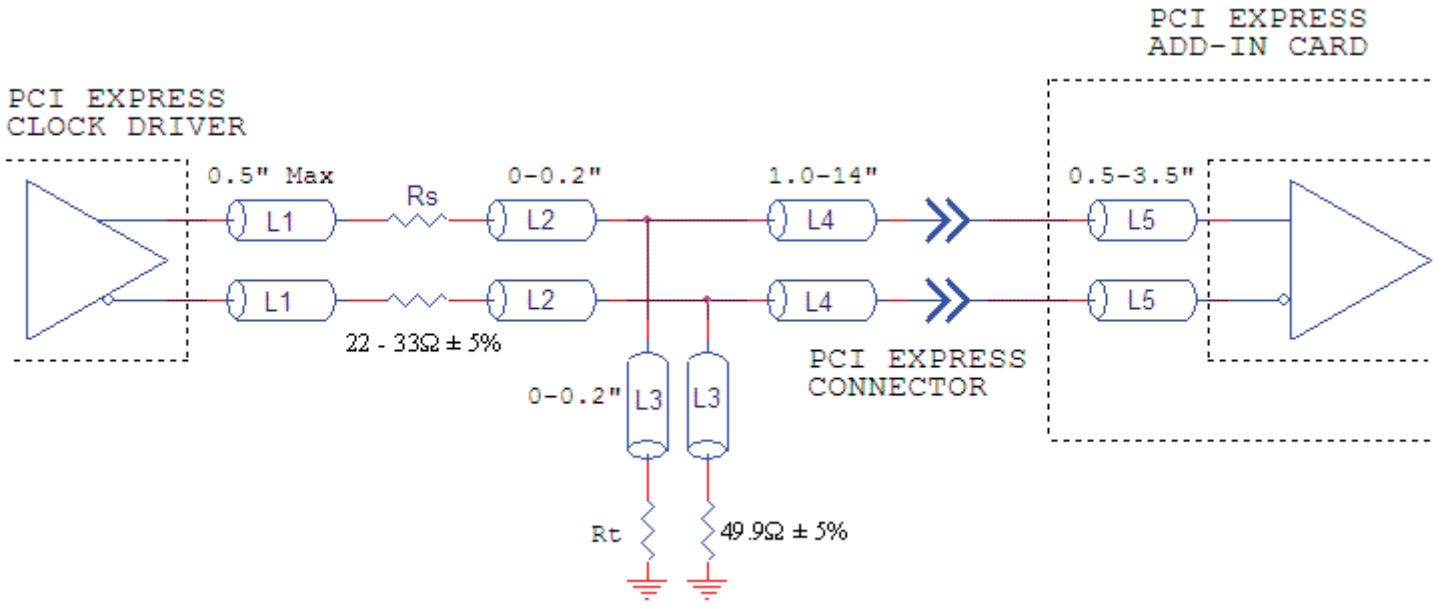



**Figure 5A. Recommended Termination**

*Figure 5B* is the recommended termination for applications which require a point to point connection and contain the driver and receiver on the same PCB. All traces should all be 50Ω impedance.

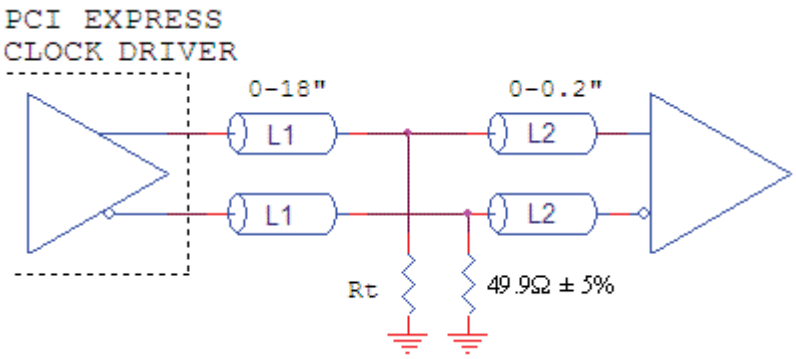



**Figure 5B. Recommended Termination**

# POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 844S2416.
Equations and example calculations are also provided.

*1. Power Dissipation.*

The total power dissipation for the 844S2416 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD}$ = 3.3V + 5% = 3.465V, which gives worst case results.

**Core and HCSL Output Power Dissipation**

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD} + I_{DDA1} + I_{DDA2})$ = 3.465V * (170 + 9mA + 22mA) = **696.5mW**
- Power $(HCSL)_{MAX}$ = **44.5mW/Loaded Output Pair**
  If all outputs are loaded, the total power is 3 * 44.5mW = **133.5mW**

**LVCMOS Output Power Dissipation**

- Output Impedance $R_{OUT}$ Power Dissipation due to Loading 50Ω to $V_{DDO}/2$
  Output Current $I_{OUT} = V_{DDO\_MAX} / [2 * (50Ω + R_{OUT})]$ = 3.465V / [2 * (50Ω + 21Ω)] = **24.4mA**

- Power Dissipation on the $R_{OUT}$ per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2$ = 21Ω * $(24.4mA)^2$ = **12.5mW per output**

- Total Power Dissipation on the $R_{OUT}$
  **Total Power ($R_{OUT}$)** = 12.5mW * 14 = **175mW**

- Dynamic Power Dissipation at 24MHz and 25MHz
  Power Dynamic = $V_{DDO\_LVCMOS\_MAX} * I_{DDO\_LVCMOS}$ = 3.465V * 16mA = **55.44mW**

**Total Power Dissipation**

- **Total Power**
  = Power (core) + Power (HCSL) + Total Power ($R_{OUT}$) + Total Power ($R_{OUT}$) + Total Power (Dynamic)
  = 696.5mW + 133.5mW + 175mW + 55.44mW
  **= 1060.4mW**

*2. Junction Temperature.*
Junction temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature
$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance
Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming air flow of 1 meter per second and a multi-layer board, the appropriate value is 27.5°C/W per Table 7.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.06W * 27.5°C/W = 114.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board.

**Table 7. Thermal Resistance $\theta_{JA}$ for 56-Lead VFQFN, Forced Convection**

| $\theta_{JA}$ vs. Air Flow (Meters per Second) | | | |
|---|---|---|---|
| | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 31.4°C/W | 27.5°C/W | 24.6°C/W |

*3. Calculations and Equations.*

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 6.*

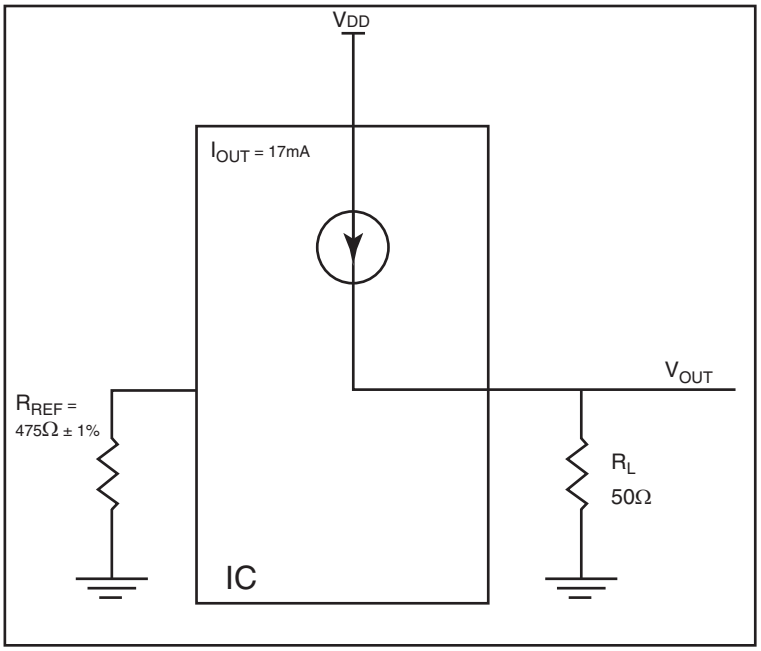



**FIGURE 6. HCSL DRIVER CIRCUIT AND TERMINATION**

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when $V_{DD}$ is HIGH.

Power $= (V_{DD\_HIGH} – V_{OUT}) * I_{OUT,}$ since $V_{OUT} = I_{OUT} * R_L$

$= (V_{DD\_HIGH} – I_{OUT} * R_L) * I_{OUT}$

$= (3.465V – 17mA * 50Ω) * 17mA$

Total Power Dissipation per output pair = **44.5mW**

# RELIABILITY INFORMATION

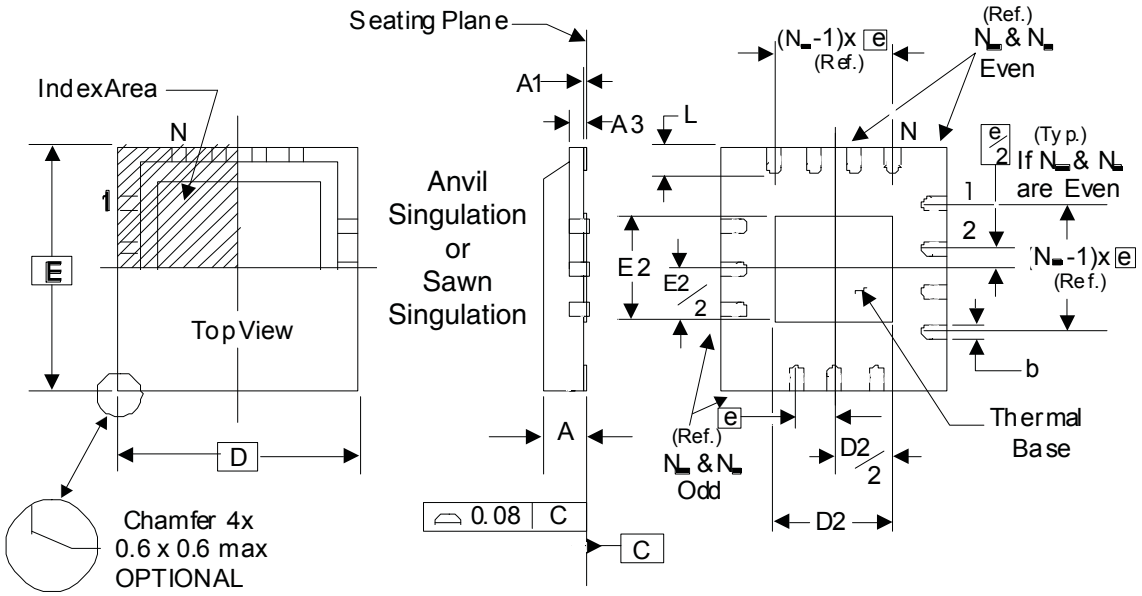
**TABLE 8. $\theta_{JA}$ VS. AIR FLOW TABLE FOR 56 LEAD VFQFN**

| $\theta_{JA}$ by Velocity (Meters per second) | | | |
|---|---|---|---|
| | **0** | **1** | **2.5** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 31.4°C/W | 27.5°C/W | 24.6°C/W |

**TRANSISTOR COUNT**

The transistor count for 844S2416 is: 13,890

## PACKAGE OUTLINE - K SUFFIX FOR 56 LEAD VFQFN




NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 8 below.

**TABLE 9. PACKAGE DIMENSIONS**

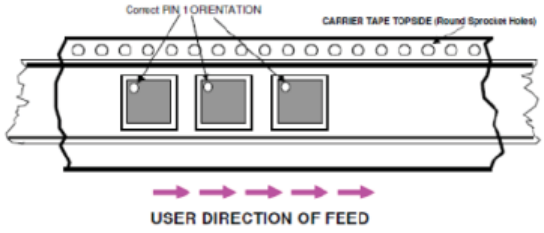
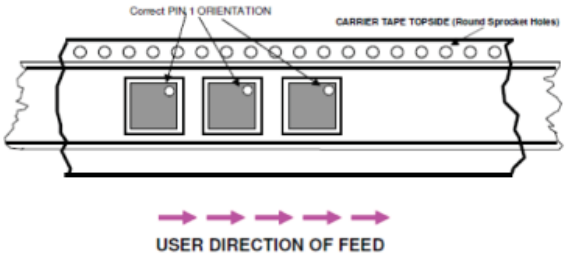
| JEDEC VARIATION<br>ALL DIMENSIONS IN MILLIMETERS | | |
|---|---|---|
| **SYMBOL** | **MINIMUM** | **MAXIMUM** |
| **N** | 56 | |
| **A** | 0.80 | 1.0 |
| **A1** | 0 | 0.05 |
| **A3** | 0.25 Reference | |
| **b** | 0.18 | 0.30 |
| **e** | 0.50 BASIC | |
| **$N_D$** | 14 | |
| **$N_E$** | 14 | |
| **D** | 8.0 | |
| **D2** | 4.35 | 4.65 |
| **E** | 8.0 | |
| **E2** | 5.05 | 5.35 |
| **L** | 0.3 | 0.55 |

Reference Document: JEDEC Publication 95, MO-220

**TABLE 10. ORDERING INFORMATION**

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 844S2416CKILF | ICS44S2416CIL | 56 lead “Lead Free” VFQFN | tray | -40°C to 85°C |
| 844S2416CKILFT | ICS44S2416CIL | 56 lead “Lead Free” VFQFN | tape & reel, Pin 1 orientation (EIA-481-C) | -40°C to 85°C |
| 844S2416CKILF/W | ICS44S2416CIL | 56 lead “Lead Free” VFQFN | tape & reel, Pin 1 orientation, (EIA-481-D) | -40°C to 85°C |

**TABLE 11. PIN 1 ORIENTATION IN TAPE AND REEL PACKAGING**

| Part Number Suffix | Pin 1 Orientation | Illustration |
|---|---|---|
| T | Quadrant 1 (EIA-481-C) |  |
| W | Quadrant 2 (EIA-481-D) |  |

| REVISION HISTORY SHEET | | | | |
|---|---|---|---|---|
| **Rev** | **Table** | **Page** | **Description of Change** | **Date** |
| A | | 1<br>17 | General Description - deleted HiperClocks logo. First sentence, deleted HiperClocks reference.Power Considerations - updated *Junction Temperature s*entence. | 12/2/13 |
| A | T10<br>T11 | 21<br>21 | Ordering Information - Added W part number.<br>Added Pin 1 orientation table. | 7/6/15 |
| A | T10 | 21 | Ordering Information - Deleted LF note below table.<br>Updated data sheet header and footer. | 4/29/16 |

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com


### Contact Information

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