R06PM0009EJ0110
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PLL Datasheet

Analog-PLL For Skew adjust

Key Features

- Including Loop-filter
- VCO operating range : 672MHz - 1400 MHz
- Output frequency range : 48MHz – 1400 MHz
- Input frequency range : 12MHz - 400MHz
- Multiplying (Output freq. / PFD freq.) : 14, 28 and 56
- Divider
  4bit feedback divider, 2bit input divider and 4bit output divider
- Power-down Mode
- SSC input is not available
- Power-on sequence is constraint-free
- STBY sequence is constraint-free

TECHNOLOGY

Process：TSMC 28nm HPC+
Available metallization technologies : 4X2Y2R and 5X2Y2R

OPERATING CONDITION

Parameter		Min	Max	Unit
Operating Voltage（AVDD)		1.62	1.98	V
Operating Voltage（VDD)		0.935	1.08	V
Junction Temperature		-40	125	℃
Input Clock	Duty	30	70	%
	Rise/Fall time	-	0.2	ns

**This IP is contract design IP. Please contact for detail.*

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