GPIO for TSMC 40nm N40EF2

Overview

The 3.3V general purpose(GPIO) I/O library with over-drive 2.5V device are provided for TSMC 40nm N40EF2 process. The 5V tolerant IO and I2C are supported.

Key Features

- Support 3.3V general purpose IO over-drive 2.5V device
- Support upto 120MHz Operating Frequency
- Programmable Output four drive strength
- CMOS Input and Schmitt trigger Input with programable pull-up or pull-down
- Staggered CUP(Circuit Under Pad) Bonding PAD Structure
- Minimized I/O size by optimized ESD structure
- High reliability of ESD protection with Dual diode & RC Triggered NMOS ESD structure

IO Lineup

IO	N40EF2	Feature
3.3V GPIO	●	• CMOS Input and Schmitt trigger Input with programable pull-up or pull-down • Programmable Output four drive strength
High Speed IO	●	• Support upto 120MHz@30pF operation • CMOS Input and Schmitt trigger Input with programable pull-up or pull-down • Programmable Output four drive strength
5V tolerant IO	●	• CMOS Input and Schmitt trigger Input with programable pull-up or pull-down • Programmable Output four drive strength
I2C IO (1 PAD)	●	• Supported I2C modes: Standard-mode, Fast-mode, Fast-mode+ • 5V input tolerant

● Available

ESD Robustness

- HBM : 2000V
- CDM : 500V

**This IP is contract design IP. Please contact for detail.*

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