ISL97649B

TFT-LCD Supply + DCP + VCOM Amplifier + Gate Pulse Modulator + RESET

FN7927
Rev 2.00
June 27, 2013

The ISL97649B is an integrated power management IC (PMIC) for TFT-LCDs used in notebooks, tablet PCs, and monitors. The device integrates a boost converter for generating A_{VDD}. V_{ON} and V_{OFF} are generated by a charge pump driven by the switching node of the boost. The ISL97649B also includes a V_{ON} slice circuit, reset function, and a high performance VCOM amplifier with DCP (Digitally Controlled Potentiometer) that is used as a VCOM calibrator.

The A_{VDD} boost converter features a 1.5A /0.18Ω boost FET with 600/1200kHz switching frequency. The gate pulse modulator can control gate voltage up to 30V, and both the rate and slew delay time are selectable. The supply monitor generates a reset signal when the system is powered down.

The ISL97649B provides a programmable VCOM with I^2C interface. One VCOM amplifier is also integrated in the chip. The output of VCOM is power-up with voltage at the last programmed 8-bit EEPROM setting.

Features

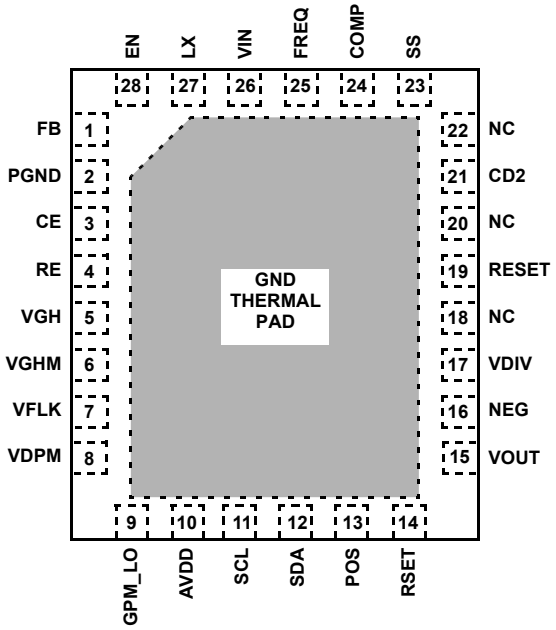
- 2.5V to 5.5V input
- 1.5A, 0.18Ω integrated boost FET
- V_{ON} /V_{OFF} supplies generated by charge pumps driven by boost switch node
- 600/1200kHz selectable switching frequency
- Integrated gate pulse modulator
- Reset signal generated by supply monitor
- Integrated VCOM amplifier
- DCP
  - I^2C serial interface, address:100111, msb left
  - Wiper position stored in 8-bit nonvolatile memory and recalled on power-up
  - Endurance, 1,000 data changes per bit
- UVLO, UVP, OVP, OCP, and OTP protection
- Pb-free (RoHS compliant)
- 28 Ld 4X5 QFN

Applications

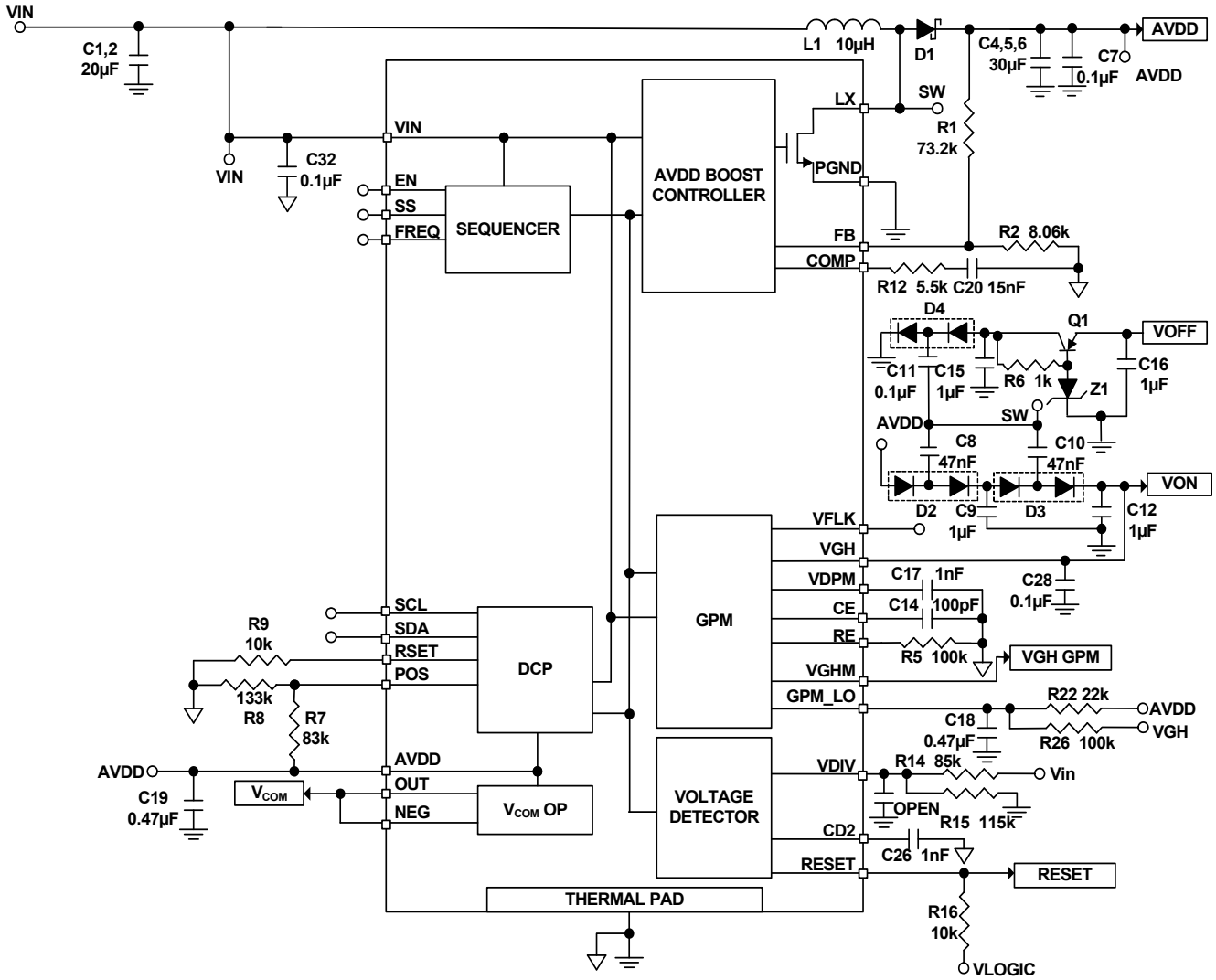
- LCD notebook, tablet, and monitor

Pin Configuration

ISL97649B
(28 LD 4X5 QFN)
TOP VIEW



Application Diagram



Pin Descriptions

PIN#	SYMBOL	DESCRIPTION
1	FB	AVDD boost converter feedback. Connect to the center of a voltage divider between AVDD and GND to set the AVDD voltage.
2	PGND	Power ground
3	CE	Gate Pulse Modulator delay control. Connect a capacitor between this pin and GND to set the delay time.
4	RE	Gate Pulse Modulator slew control. Connect a resistor between this pin and GND to set the falling slew rate.
5	VGH	Gate Pulse Modulator high voltage input. Place a 0.1µF decoupling capacitor close to VGH pin.
6	VGHM	Gate Pulse Modulator output for gate drive IC.
7	VFLK	Gate Pulse Modulator control input from T_{CON}.
8	VDPM	Gate Pulse Modulator enable. Connect a capacitor from VDPM to GND to set the delay time before GPM is enabled. A current source charges the capacitor on VDPM.
9	GPM_LO	Gate Pulse Modulator low voltage input. Place a 0.47µF decoupling capacitor close to GPM_LO pin.
10	AVDD	DCP and VCOM amplifier high voltage analog supply. Place a 0.47µF decoupling capacitor close to AVDD pin.
11	SCL	I^2C compatible clock input

Pin Descriptions (Continued)

PIN#	SYMBOL	DESCRIPTION
12	SDA	I^2C compatible serial bidirectional data line
13	POS	VCOM amplifier non-inverting input
14	RSET	DCP sink current adjustment pin. Connect a resistor between this pin and GND to set the resolution of DCP output voltage.
15	VOUT	VCOM amplifier output
16	NEG	VCOM amplifier inverting input
17	VDIV	Voltage detector threshold. Connect to the center of a resistive divider between V_{IN} and GND.
18	NC	Not connected
19	RESET	Voltage detector reset output
20	NC	Not connected
21	CD2	Voltage detector rising edge delay. Connect a capacitor between this pin and GND to set the rising edge delay.
22	NC	Not connected
23	SS	Boost converter soft-start. Connect a capacitor between this pin and GND to set the soft-start time.
24	COMP	Boost converter compensation pin. Connect a series resistor and capacitor between this pin and GND to optimize transient response and stability.
25	FREQ	Boost converter frequency select. Pull to logic high to operate boost at 1.2MHz. Connect this pin to GND to operate boost at 600kHz.
26	VIN	IC input supply. Connect a 0.1µF decoupling capacitor close to this pin.
27	LX	AVDD boost converter switching node
28	EN	AVDD enable pin

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{IN} RANGE (V)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL97649BIRZ	97649 BIRZ	2.5 to 5.5	-40 to +85	28 Ld 4x5 QFN	L28.4x5A
ISL97649BIRTZ-EVALZ	Evaluation Board				

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL97649B. For more information on MSL please see Tech Brief TB363.

Absolute Maximum Ratings

RE, VGHM, GPM_LO, and VGH to GND . . . . . -0.3 to +36V
LX, AVDD, POS, NEG, VOUT to GND . . . . . -0.3 to +18V
Voltage Between GND and PGND . . . . . ±0.5V
All Other Pins to GND . . . . . -0.3 to +6.0V
ESD Rating
Human Body Model (Tested per JESD22-A114E) 2kV
Machine Model (Tested per JESD22-A115-A) 200V
Charged Device Model (Tested per JESD22-C101) 1kV

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
4 x 5 QFN Package (Notes 4, 5)	38	4.5

Ambient Temperature . . . . . -40°C to +85°C
Functional Junction Temperature . . . . . -40°C to +150°C
Storage Temperature . . . . . -65°C to +150°C
Lead Temperature during Soldering . . . . . +260°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature . . . . . -40°C to +85°C
Supply Voltage . . . . . 2.5V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{IN} = ENABLE = 3.3V, A_{VDD} = 8V, V_{ON} = 24V, V_{OFF} = -6V. Boldface limits apply over the operating temperature range, -40°C to +85°C.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNITS
GENERAL						
VIN	V_{IN} Supply Voltage Range		**2.5**	3.3	**5.5**	V
I_{S_DIS}	V_{IN} Supply Currents when Disabled	VIN<UVLO		390	**500**	µA
I_S	V_{IN} Supply Currents	ENABLE = 3.3V, overdrive AVDD and VGH		0.7	**1.0**	mA
I_{ENABLE}	ENABLE Pin Current	ENABLE = 0V		0		µA
LOGIC INPUT CHARACTERISTICS - ENABLE, FLK, SCL, SDA, FREQ						
V_{IL}	Low Voltage Threshold				**0.65**	V
V_{IH}	High Voltage Threshold		**1.75**			V
R_{IL}	Pull-Down Resistor	Enable, FLK, FREQ	**0.85**	1.25	**1.65**	MΩ
INTERNAL OSCILLATOR						
F_{OSC}	Switching Frequencies	FREQ = low, T_A = 25°C	550	600	650	kHz
		FREQ = high, T_A = 25°C	1100	1200	1300	kHz
AVDD BOOST REGULATOR						
ΔAVDD/ ΔIOUT	AVDD Load Regulation	50mA < I_{LOAD} < 250mA		0.2		%
ΔAVDD/ ΔVIN	AVDD Line Regulation	I_{LOAD} = 150mA, 2.5V < V_{IN} < 5.5V		0.15		%
V_{FB}	Feedback Voltage (V_{FB})	I_{LOAD} = 100mA, T_A = +25°C	0.792	0.8	0.808	V
I_{FB}	FB Input Bias Current				**100**	nA
$r_{DS(ON)}$	Switch ON-resistance	T_A = +25°C		180	230	mΩ
I_{LIM}	Switch Current Limit		**1.125**	1.5	**1.875**	A
D_{MAX}	Max Duty Cycle	Freq = 1.2MHz	**80**	90		%
EFF		Freq = 1.2MHz, IAVDD = 100mA		91		%

Electrical Specifications V_{IN} = ENABLE = 3.3V, A_{VDD} = 8V, V_{ON} = 24V, V_{OFF} = -6V. Boldface limits apply over the operating temperature range, -40°C to +85°C. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNITS
GATE PULSE MODULATOR						
V_{GH}	VGH Voltage		**7**		**33**	V
V_{IH_VDPM}	V_{DPM} Enable Threshold		**1.13**	1.215	**1.30**	V
I_{VGH}	VGH Input Current	VFLK = 0		125		µA
		RE = 100kΩ, VFLK = VIN		27.5		µA
V_{GPM_LO}	GPM_LO Voltage		**2**		**VGH-2**	V
I_{GPM_LO}	VGPM_LO Input Current		**-2**	0.1	**2**	µA
VCE_{th1}	CE Threshold Voltage 1			0.6xVIN	**0.8xVIN**	V
VCE_{th2}	CE Threshold Voltage 2			1.215		V
I_{CE}	CE Current			100		µA
R_{VGHM_PD}	VGHM Pull-down Resistance			1.1		kΩ
R_{ONVGH}	VGH to VGHM On Resistance			23		Ω
IDPM	VDPM Charge Current			10		µA
SUPPLY MONITOR						
V_{IH_VDIV}	VDIV High Threshold	VDIV rising	**1.265**	1.280	**1.295**	V
V_{IL_VDIV}	VDIV Low Threshold	VDIV falling	**1.21**	1.222	**1.234**	V
Vth_{CD2}	CD2 Threshold Voltage		**1.200**	1.217	**1.234**	V
I_{CD2}	CD2 Charge Current			10		µA
R_{IL_RESET}	RESET Pull-down Resistance			650		Ω
t_{DELAY_RESET}	RESET Delay on Rising Edge			121.7k* CD		s
VCOM AMPLIFIER: R_{LOAD} = 10k, C_{LOAD} = 10pF, UNLESS OTHERWISE STATED						
I_{S_com}	VCOM Amplifier Supply Current			0.7	**1.08**	mA
V_{OS}	Offset Voltage			2.5	**15**	mV
I_B	Noninverting Input Bias Current			0		nA
CMIR	Common Mode Input Voltage Range		**0**		**AVDD**	V
CMRR	Common-mode Rejection Ratio		**60**	75		dB
PSRR	Power Supply Rejection Ratio		**70**	85		dB
V_{OH}	Output Voltage Swing High	I_{OUT}(source) = 0.1mA		AVDD - 1.39		mV
		I_{OUT}(source) = 75mA		AVDD - 1.27		V
V_{OL}	Output Voltage Swing Low	I_{OUT}(sink) = 0.1mA		1.2		mV
		I_{OUT}(sink) = 75mA		1		V
I_{SC}	Output Short Circuit Current	Pull-up	**150**	225		mA
		Pull-down	**150**	200		mA
SR	Slew Rate			25		V/µs
BW	Gain Bandwidth	-3dB gain point		20		MHz

Electrical Specifications

V_{IN} = ENABLE = 3.3V, A_{VDD} = 8V, V_{ON} = 24V, V_{OFF} = -6V. Boldface limits apply over the operating temperature range, -40°C to +85°C. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 6)	TYP (Note 7)	MAX (Note 6)	UNITS
DIGITAL CONTROLLED POTENTIOMETER						
SET_{VR}	SET Voltage Resolution (Note 12)			8		Bits
SET_{DNL}	SET Differential Nonlinearity (Notes 8, 9, 14)	T_A = +25°C	-	-	±1	LSB
SET_{ZSE}	SET Zero-Scale Error (Note 10, 14)	T_A = +25°C	-	-	±2	LSB
SET_{FSE}	SET Full-Scale Error (Note 11, 14)	T_A = +25°C	-	-	±8	LSB
I_{RSET}	RSET Current		-		**100**	µA
AVDD to SET	AVDD to SET Voltage Attenuation		-	1:20	-	V/V
FAULT DETECTION THRESHOLD						
V_{UVLO}	Undervoltage Lock-out Threshold	PV_{IN} rising	**2.25**	2.33	**2.41**	V
		PV_{IN} falling	**2.125**	2.20	**2.27**	V
OVP_{AVDD}	Boost Overvoltage Protection Off Threshold to Shut Down IC (Note 13)		**15.0**	15.5	**16.0**	V
T_{OFF}	Thermal Shut-Down all channels	Temperature rising		153		°C
POWER SEQUENCE TIMING						
I_{SS}	Boost Soft-start Current		**3**	5.5	**8**	µA

Serial Interface Specifications

For SCL and SDA, unless otherwise noted. Boldface limits apply over the operating temperature range, -40°C to +85°C.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP (Note 7)	MAX (Note 14)	UNITS
f_{SCL}	SCL Frequency (Note 6)				**400**	kHz
t_{iN}	Pulse Width Suppression Time at SDA and SCL Inputs (Note 6)	Any pulse narrower than the max spec is suppressed.			**50**	ns
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{IN}, until SDA exits the 30% to 70% of V_{IN} window.			480	ns
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{IN} during the following START condition.	480			ns
t_{LOW}	Clock LOW Time	Measured at 30% of V_{IN} crossing.	480			ns
t_{HIGH}	Clock HIGH Time	Measured at 70% of V_{IN} crossing.	400			ns
$t_{SU:STA}$	START Condition Set-up Time	SCL rising edge to SDA falling edge, both crossing 70% of V_{IN}.	480			ns
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{IN} to SCL falling edge crossing 70% of V_{IN}.	400			ns
$t_{SU:DAT}$	Input Data Set-up Time	From SDA exiting 30% to 70% of V_{IN} window to SCL rising edge crossing 30% of V_{IN}.	40			ns
$t_{HD:DAT}$	Input Data Hold Time	From SCL rising edge crossing 70% of V_{IN} to SDA entering 30% to 70% of V_{IN} window.	0			ns
$t_{SU:STO}$	STOP Condition Set-up Time	From SCL rising edge crossing 70% of V_{IN} to SDA rising edge crossing 30% of V_{IN}.	400			ns
$t_{HD:STO}$	STOP Condition Hold Time for Read, or Volatile Only Write	From SDA rising edge to SCL falling edge, both crossing 70% of V_{IN}.	400			ns
C_{SCL}	Capacitive on SCL			5		pF

Serial Interface Specifications

For SCL and SDA, unless otherwise noted. Boldface limits apply over the operating temperature range, -40°C to +85°C. **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP (Note 7)	MAX (Note 14)	UNITS
C_{SDA}	Capacitive on SDA			5		pF
t_{Wp}	Non-Volatile Write Cycle Time			25		ms
	EEPROM Endurance	T_A= +25°C		1		kCyc
	EEPROM Retention	T_A = +25°C		88		kHrs

NOTES:

6. Parameters with MIN and/or MAX limits are 100% tested at +25C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Typical values are for T_A = +25°C and V_{IN} = 3.3V.
8. LSB = I V_{255} - V_1 I / 254. V_{255} and V_1 are the measured voltages for the DCP register set to FF hex and 01 hex, respectively.
9. DNL = I V_{i+1} - V_i I / LSB-1, $i \in [1, 255]$
10. ZS error = (V_1- VMAX)/LSB. VMAX = (VAVDD * R2) * [1-2 * R1/(256 * 20 * RSET)]/(R1 + R2)
11. FS error = (V_{255} - VMIN)/LSB. VMIN = (VAVDD * R2) * [1-256 * R1/(256 * 20 * RSET)]/(R1 + R2)
12. Established by design. Not a parametric spec.
13. Boost will stop switching as soon as boost output reaches OVP threshold.
14. Compliance to limits is assured by characterization and design.

Typical Performance Curves

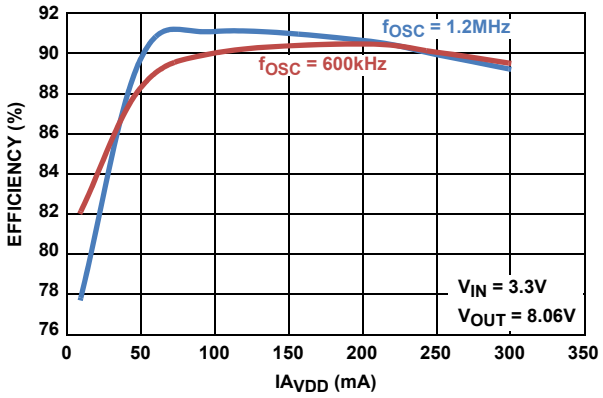


FIGURE 1. A_{VDD} EFFICIENCY vs IA_{VDD}

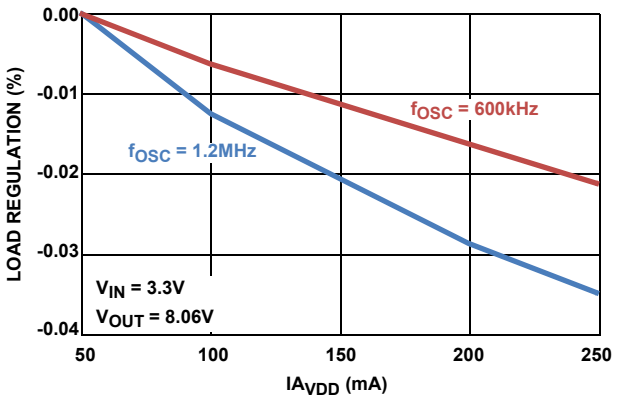


FIGURE 2. A_{VDD} LOAD REGULATION vs IA_{VDD}

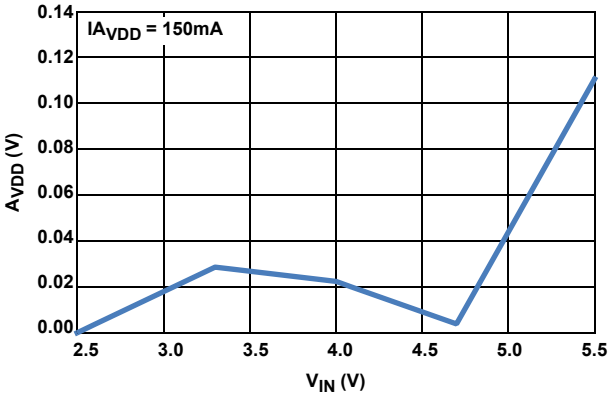


FIGURE 3. A_{VDD} LINE REGULATION vs V_{IN}

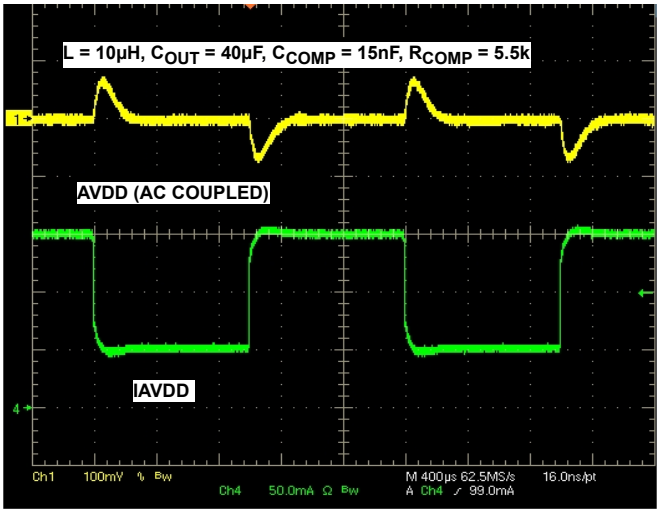


FIGURE 4. BOOST CONVERTER TRANSIENT RESPONSE

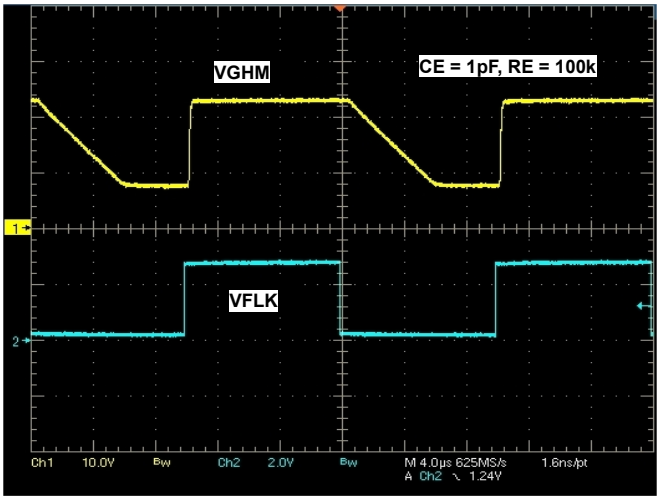


FIGURE 5. GPM CIRCUIT WAVEFORM

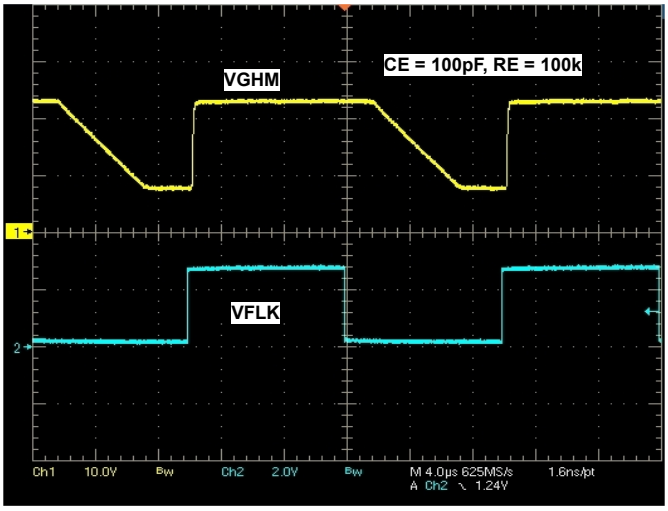


FIGURE 6. GPM CIRCUIT WAVEFORM

Typical Performance Curves (Continued)

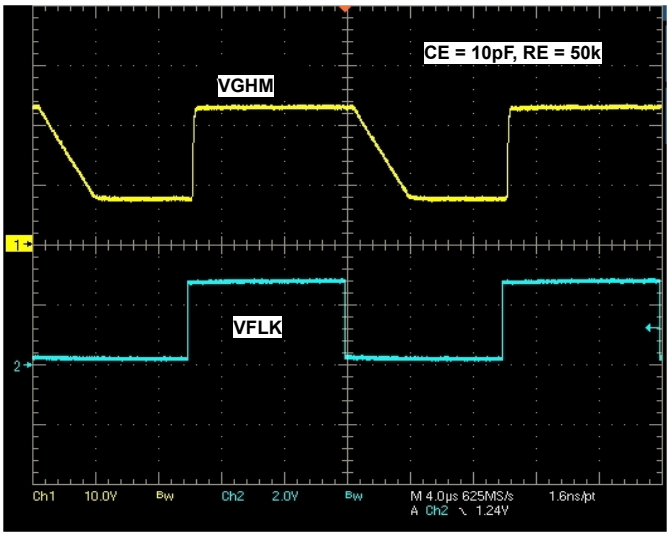


FIGURE 7. GPM CIRCUIT WAVEFORM

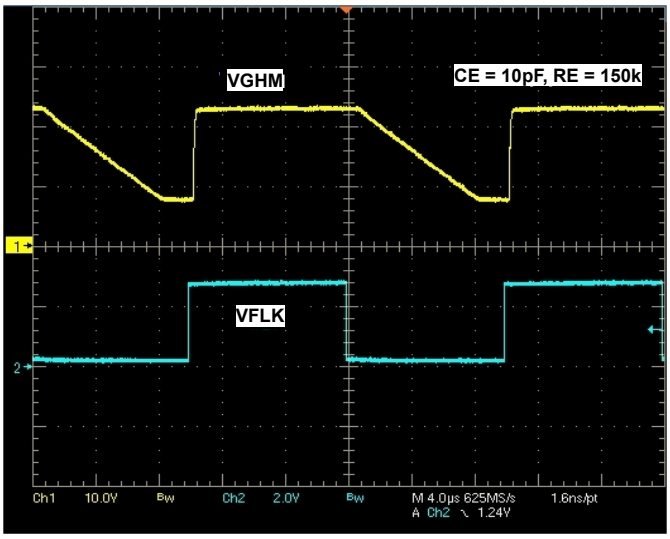


FIGURE 8. GPM CIRCUIT WAVEFORM

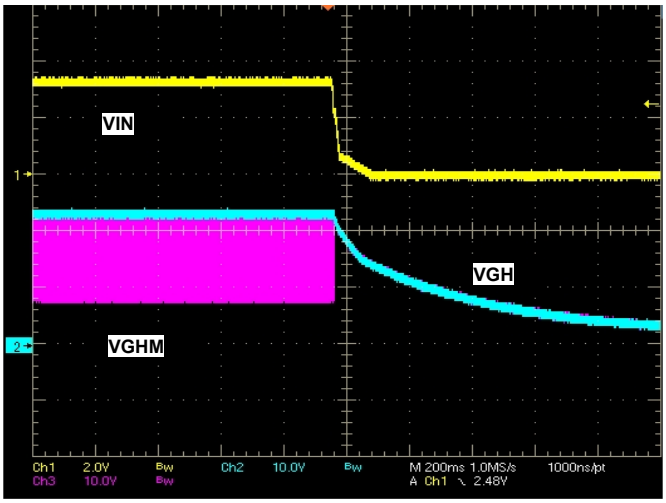


FIGURE 9. V_{GHM} FOLLOWS V_{GH} WHEN THE SYSTEM POWERS OFF

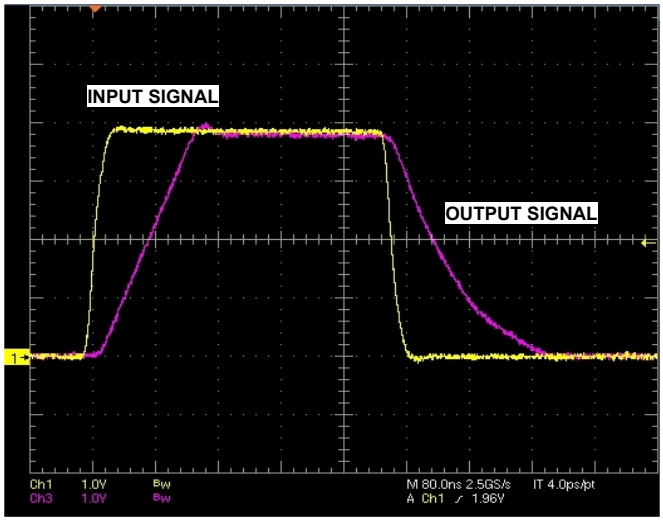


FIGURE 10. VCOM RISING SLEW RATE

Applications Information

Enable Control

With VIN > UVLO, all functions in ISL97649B are shut down when the Enable pin is pulling down. When the voltage at the Enable pin reaches H threshold, the whole ISL97649B is on.

Frequency Selection

The ISL97649B switching frequency can be user selected to operate at either a constant 600kHz or 1.2MHz. Lower switching frequency can save power dissipation when the boost load is very low and the device is operating in deep discontinuous mode. Higher switching frequency can allow the use of smaller external components like inductors and output capacitors. Higher switching frequency will get higher efficiency within some loading ranges, depending on V_{IN}, V_{OUT}, and external components, as shown in Figure 1. Connecting the FREQ pin to GND sets the PWM switching frequency to 600kHz. Connecting the FREQ pin to V_{IN} sets the PWM switching frequency to 1.2MHz.

Soft-Start

Soft-start is provided by an internal current source to charge the external soft-start capacitor. The ISL97649B ramps up the current limit from 0A to full value as voltage at the SS pin ramps from 0 to 0.8V. Hence, the soft-start time is 3.2ms when the soft-start capacitor is 22nF and is 6.8ms for 47nF and 14.5ms for 100nF.

Operation

The boost converter is a current mode PWM converter operating at either 600kHz or 1.2MHz. It can operate in both discontinuous conduction mode (DCM) at light load and in continuous conduction mode (CCM). In continuous conduction current mode, current flows continuously in the inductor during the entire switching cycle in steady-state operation. The voltage conversion ratio in continuous current mode is given by Equation 1:

$$\frac{V_{Boost}}{V_{IN}} = \frac{1}{1-D} \quad \text{(EQ. 1)}$$

where D is the duty cycle of the switching MOSFET.

The boost regulator uses a summing amplifier architecture consisting of gm stages for voltage feedback, current feedback, and slope compensation. A comparator looks at the peak inductor current, cycle by cycle, and terminates the PWM cycle if the current limit is reached.

An external resistor divider is required to divide the output voltage down to the nominal reference voltage. Current drawn by the resistor network should be limited to maintain the overall converter efficiency. The maximum value of the resistor network is limited by the feedback input bias current and the potential for noise being coupled into the feedback pin. A resistor network on the order of 60kΩ is recommended. The boost converter output voltage is determined by Equation 2:

$$V_{Boost} = \frac{R_1 + R_2}{R_2} \times V_{FB} \quad \text{(EQ. 2)}$$

The current through the MOSFET is limited to $1.5A_{PEAK}$. This restricts the maximum output current (average) based on Equation 3:

$$I_{OMAX} = \left(I_{LMT} - \frac{\Delta I_L}{2}\right) \times \frac{V_{IN}}{V_O} \quad \text{(EQ. 3)}$$

where ΔI_L is peak-to-peak inductor ripple current, which is set by Equation 4:

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f_s} \quad \text{(EQ. 4)}$$

where f_S is the switching frequency (600kHz or 1.2MHz).

Capacitor

An input capacitor is used to suppress the voltage ripple injected into the boost converter. A ceramic capacitor with capacitance larger than 10µF is recommended. The voltage rating of the input capacitor should be larger than the maximum input voltage. Table 1 shows some recommended input capacitors.

TABLE 1. BOOST CONVERTER INPUT CAPACITOR RECOMMENDATIONS

CAPACITOR	SIZE	MFG	PART NUMBER
10µF/6.3V	0603	TDK	C1608X5R0J106M
10µF/16V	1206	TDK	C3216X7R1C106M
10µF/10V	0805	Murata	GRM21BR61A106K
22µF/10V	1210	Murata	GRB32ER61A226K

Inductor

The boost inductor is a critical part that influences the output voltage ripple, transient response, and efficiency. Values of 3.3µH to 10µH are used to match the internal slope compensation. The inductor must be able to handle the average and peak currents shown in Equation 5:

$$I_{LAVG} = \frac{I_O}{1-D}$$
$$I_{LPK} = I_{LAVG} + \frac{\Delta I_L}{2} \quad \text{(EQ. 5)}$$

Table 2 shows some recommended inductors for different design considerations.

TABLE 2. BOOST INDUCTOR RECOMMENDATIONS

INDUCTOR	DIMENSIONS (mm)	MFG	PART NUMBER	DESIGN CONSIDERATION
10µH/ 4Apeak	8.3x8.3x4.5	Sumida	CDR8D43-100NC	Efficiency optimization
6.8µH/ 1.8Apeak	5.0x5.0x2.0	TDK	PLF5020T-6R8M1R8	
10µH/ 2.2Apeak	6.6x7.3x1.2	Cyntec	PCME061B-100MS	PCB space/profile optimization

Rectifier Diode

A high-speed diode is necessary due to the high switching frequency. Schottky diodes are recommended because of their fast recovery time and low forward voltage. The reverse voltage rating of this diode should be higher than the maximum output

voltage. The rectifier diode must meet the output current and peak inductor current requirements. Table 3 shows some recommendations for boost converter diode.

TABLE 3. BOOST CONVERTER RECTIFIER DIODE RECOMMENDATIONS

DIODE	V_R/I_{AVG} RATING	PACKAGE	MFG
PMEG2010ER	20V/1A	SOD123W	NXP
MSS1P2U	20V/1A	MicroSMP	VISHAY

Output Capacitor

The output capacitor supplies the load directly and reduces the ripple voltage at the output. Output ripple voltage consists of two components (Equation 6):

1. Voltage drop due to inductor ripple current flowing through the ESR of output capacitor.
2. Charging and discharging of output capacitor.

$$V_{RIPPLE} = I_{LPK} \times ESR + \frac{V_O - V_{IN}}{V_O} \times \frac{I_O}{C_{OUT}} \times \frac{1}{f_s} \quad \text{(EQ. 6)}$$

For low ESR ceramic capacitors, the output ripple is dominated by the charging and discharging of the output capacitor. The voltage rating of the output capacitor should be greater than the maximum output voltage.

NOTE: Capacitors have a voltage coefficient that makes their effective capacitance drop as the voltage across them increases. C_{OUT} in Equation 6 assumes the effective value of the capacitor at a particular voltage and not the manufacturer's stated value, measured at 0V.

Table 4 shows some recommendations for output capacitors.

TABLE 4. BOOST OUTPUT CAPACITOR RECOMMENDATIONS

CAPACITOR	SIZE	MFG	PART NUMBER
10µF/25V	1210	TDK	C3225X7R1E106M
10µF/25V	1210	Murata	GRM32DR61E106K

Compensation

The boost converter of ISL97649B can be compensated by an RC network connected from the COMP pin to ground. A 15nF and 5.5k RC network is used in the ISL97649BIRTZ-EVALZ evaluation board. The larger-value resistor and lower-value capacitor can lower the transient overshoot, but at the expense of loop stability.

Supply Monitor Circuit

The supply monitor circuit monitors the voltage on VDIV and sets the open-drain output RESET low when VDIV is below 1.28V (rising) or 1.22V (falling).

There is a delay on the rising edge, controlled by a capacitor on CD2. When VDIV exceeds 1.28V (rising), CD2 is charged up from 0V to 1.217V by a 10µA current source. When CD2 exceeds 1.217V, RESET goes tri-state. When VDIV falls below 1.22V, RESET becomes low, with a 650Ω pull-down resistance. Delay time is controlled, as shown in Equation 7:

$$t_{delay} = 121.7k \times CD2 \quad \text{(EQ. 7)}$$

For example, delay time is 12.17ms if CD2 = 100nF.

Figure 11 shows the supply monitor circuit timing diagram.

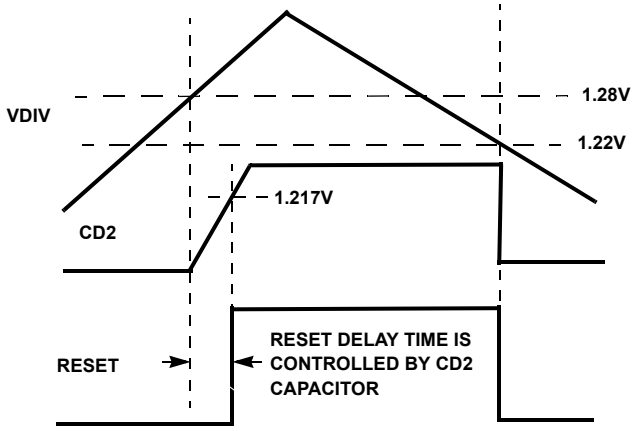


FIGURE 11. SUPPLY MONITOR CIRCUIT TIMING DIAGRAM

Gate Pulse Modulator Circuit

The gate pulse modulator circuit functions as a three-way multiplexer, switching VGHM between ground, GPM_LO, and VGH. Voltage selection is provided by digital inputs VDPM (enable) and VFLK (control). High-to-low delay and slew control are provided by external components on pins CE and RE, respectively.

When VDPM is LOW, the block is disabled, and VGHM is grounded. When the input voltage exceeds UVLO threshold, VDPM starts to drive an external capacitor. When VDPM exceeds 1.215V, the GPM circuit is enabled, and the output VGHM is determined by VFLK, RESET signal, and VGH voltage. If RESET signal is high and VFLK is high, VGHM is pulled to VGH. When VFLK goes low, there is a delay controlled by capacitor CE, following which VGHM is driven to GPM_LO, with a slew rate controlled by resistor RE. Note that GPM_LO is used only as a reference voltage for an amplifier, and thus does not have to source or sink a significant DC current.

Low-to-high transition is determined primarily by the switch resistance and the external capacitive load. High-to-low transition is more complex. Consider a case in which the block is already enabled (VDPM is H). When VFLK is H, if CE is not externally pulled above threshold voltage 1, Pin CE is pulled low. On the falling edge of VFLK, a current is passed into Pin CE to charge the external capacitor up to threshold voltage 2, providing a delay that is adjustable by varying the capacitor on CE. Once this threshold is reached, the output starts to be pulled down from VGH to GPM_LO. The maximum slew current is equal to 500/(RE + 40k), and the dv/dt slew rate is Isl/C_{LOAD}, where C_{LOAD} is the load capacitance applied to VGHM. The slew rate reduces as VGHM approaches GPM_LO.

If CE is always pulled up to a voltage above threshold 1, zero delay mode is selected; thus, there will be no delay from FLK falling to the point where VGHM starts to fall. Slew down currents will be identical to the previous case.

At power-down, when VIN falls to UVLO, VGHM is tied to VGH until the VGH voltage falls to 3V. Once the VGH voltage falls below 3V, VGHM is not actively driven until VIN is driven. Figure 12 shows the VGHM voltage based on V_{IN}, VGH, and RESET.

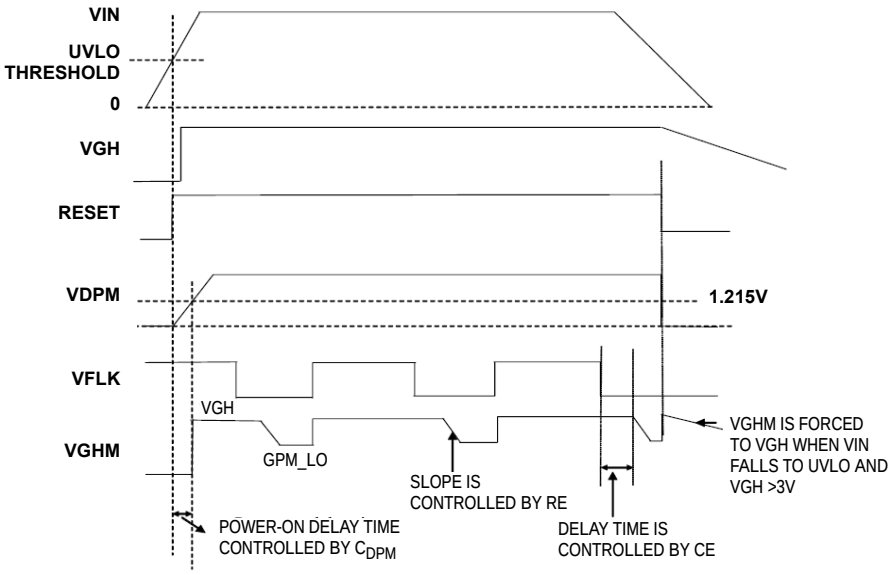


FIGURE 12. GATE PULSE MODULATOR TIMING DIAGRAM

VGH/VGL Charge Pump

To provide VGH and VGL rails for the application, two external charge pumps driven by AVDD and boost switching node can be used to generate the desired VGH and VGL, as shown in the "Application Diagram" on page 2.

The number of the charge pump stages can be calculated using the Equations 8 and 9.

$$VGL\_headroom = N*AVDD - 2*N*Vd - |VGL| > 0 \quad \text{(EQ. 8)}$$

$$VGH\_headroom = (N+1)*AVDD - 2*N*Vd - VGH > 0 \quad \text{(EQ. 9)}$$

Where N is the number of the charge pump stages and Vd is the forward voltage drop of one Schottky diode used in the charge pump. Vd is varied with forward current and ambient temperature, so it should be the maximum value in the diode datasheet according to max forward current and lowest temperature in the application condition.

Once the number of the charge pump stages is determined, the maximum current that the charge pump can deliver can be calculated using Equations 10 and 11 as follows:

$$VGL = N*(-AVDD + 2*Vd + |I_{VGL}|/(Freq*C\_fly)) \quad \text{(EQ. 10)}$$

$$VGH = AVDD + N*(AVDD - 2*Vd - |I_{VGH}|/(Freq*C\_fly)) \quad \text{(EQ. 11)}$$

Where Freq is the switching frequency of the AVDD boost, C_fly is the flying capacitance (C8, C10, C11 in the "Application Diagram"). I_{VGL} and I_{VGH} are the loadings of VGL and VGH. The relationships between minimum flying capacitance and VGL and VGH loadings are shown in Figures 13 and 14. The flying capacitance must be higher than the minimum value shown in Figure 13 and 14 for certain loadings on VGL and VGH.

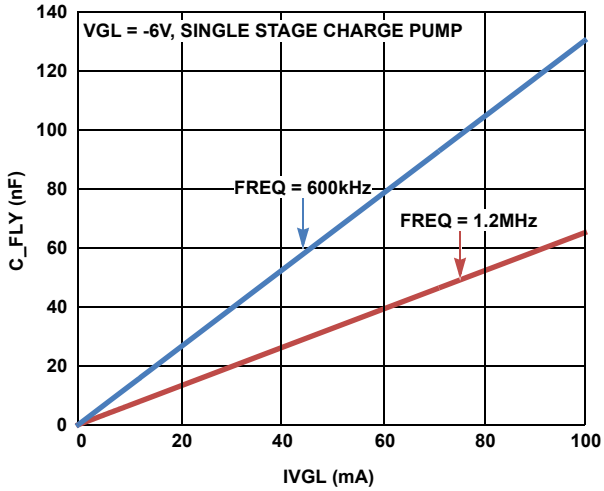


FIGURE 13. FLYING CAPACITANCE vs VGL LOADING

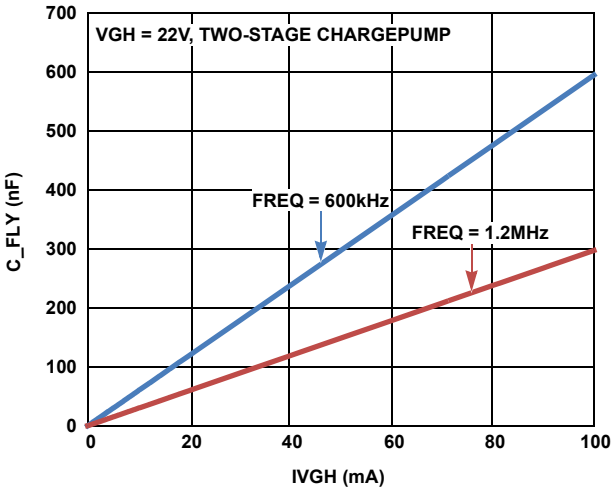


FIGURE 14. FLYING CAPACITANCE vs VGH LOADING

VCOM Amplifier

The VCOM amplifier is designed to control the voltage on the back plane of an LCD display. This plate is capacitively coupled to the pixel drive voltage, which alternately cycles positive and negative at the line rate for the display. Thus, the amplifier must be capable of sourcing and sinking pulses of current, which can occasionally be quite large (in the range of 100mA for typical applications).

The ISL97649B VCOM amplifier output current is limited to 225mA typical. This limit level, which is roughly the same for sourcing and sinking, is included to maintain reliable operation of the part. It does not necessarily prevent a large temperature rise if the current is maintained. (In this case, the whole chip may be shut down by the thermal trip to protect functionality.) If the display occasionally demands current pulses higher than this limit, the reservoir capacitor will provide the excess and the amplifier will top the reservoir capacitor back up once the pulse has stopped. This will happen in the µs time scale in practical systems and for pulses 2 or 3 times the current limit, the VCOM voltage will have settled again before the next line is processed.

DCP (Digitally Controlled Potentiometer)

Figure 15 shows the relationship between the register value and the resistor string of the DCP. Note that the register value of zero actually selects the first step of the resistor string. The output voltage of DCP is given by Equation 12:

$$V_{DCP} = \left(\frac{RegisterValue + 1}{256}\right)\left(\frac{A_{VDD}}{20}\right) \quad \text{(EQ. 12)}$$

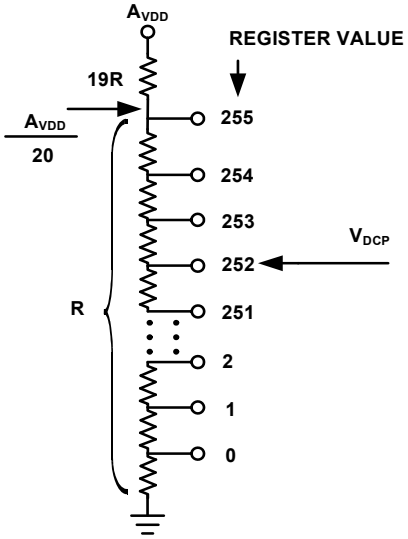


FIGURE 15. SIMPLIFIED SCHEMATIC OF DIGITALLY CONTROLLED POTENTIOMETER (DCP)

Current Sink

Figure 16 shows the schematic of the POS pin current sink. The circuit is made up of amplifier A1, transistor Q1, and resistor R_{SET}, which form a voltage controlled current source.

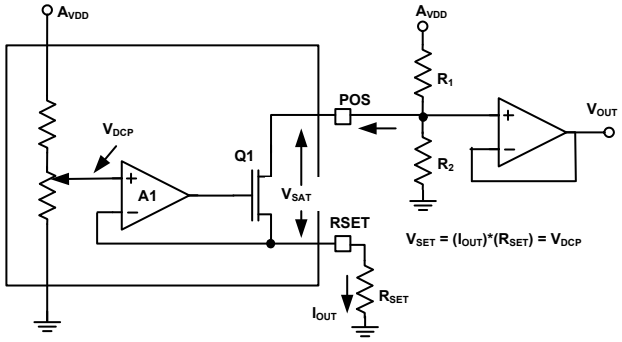


FIGURE 16. CURRENT SINK CIRCUIT

The external R_{SET} resistor sets the full-scale sink current that determines the lowest output voltage of the external voltage divider, R_1 and R_2. I_{OUT} is calculated as shown by Equation 13:

$$I_{OUT} = \frac{V_{DCP}}{R_{SET}} = \left(\frac{RegisterValue + 1}{256}\right)\left(\frac{A_{VDD}}{20}\right)\left(\frac{1}{R_{SET}}\right) \quad \text{(EQ. 13)}$$

The maximum value of I_{OUT} can be calculated by substituting the maximum register value of 255 into Equation 13, resulting in Equation 14:

$$I_{OUT}(MAX) = \frac{A_{VDD}}{20R_{SET}} \quad \text{(EQ. 14)}$$

Equation 13 can also be used to calculate the unit sink current step size by removing the Register Value term from it, as shown in Equation 15.

$$I_{STEP} = \frac{A_{VDD}}{(256)(20)(R_{SET})} \quad \text{(EQ. 15)}$$

The voltage difference between the POS and RSET pins, which are the drain and source, respectively, of the output transistor, should be greater than the minimum saturation voltage for the $I_{OUT}(MAX)$ being used. This difference keeps the output transistor in its saturation region. The maximum voltage on the RSET pin is $A_{VDD}/20$, and this voltage is added to the minimum voltage difference between the V_{OUT} and RSET pins to calculate the minimum V_{OUT} voltage, as shown in Equation 16.

$$V_{OUT}(MIN) \geq \frac{A_{VDD}}{20} + MinimumSaturationVoltage \quad \text{(EQ. 16)}$$

Output Voltage

The output voltage, V_{OUT}, can be calculated with Equation 17:

$$V_{OUT} = \frac{R_L \cdot V_{AVDD}}{(R_U + R_L)} \cdot \left(1 - \frac{RegisterValue + 1}{256} \times \frac{R_U}{20(RSET)}\right) \quad \text{(EQ. 17)}$$

Where R_L, R_U and RSET in Equation 15 correspond to the R_7, R_8 and R_9 in Application Diagram on page 2.

I²C Serial Interface

The ISL97649B supports a bidirectional, bus-oriented protocol. The protocol defines any device that sends data on to the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master, and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the DCP of the ISL97649B operates as a slave device in all applications. The fall and rise times of the SDA and SCL signals should be in the range listed in Table 5. Capacitive load on I²C bus is also specified in Table 5.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first.

TABLE 5. I²C INTERFACE SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
SDA and SCL Rise Time			1000	ns
SDA and SCL Fall Time			300	ns
I²C Bus Capacitive Load			400	pF

Programming Supply Voltage

To program EEPROM bits, VGH must be higher than 12V when AVDD is 8V. Outside these conditions, writing operations may not be successful.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (Figure 17). On power-up of the ISL97649B, the SDA pin is in input mode.

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The DCP continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (Figure 17). A START condition is ignored during the power-up sequence and during internal non-volatile write cycles.

All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is high (Figure 17). A STOP condition at the end of a read operation, or at the end of a write operation to volatile bytes only, places the device in standby mode. A STOP condition during a write operation to a non-volatile write byte initiates an internal non-volatile write cycle. The device enters standby mode when the internal non-volatile write cycle is completed.

An Acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge receipt of the eight bits of data (Figure 18).

The ISL97649B DCP responds with an ACK after recognizing a START condition followed by a valid identification byte (Byte 1). If a master-receiver is involved in a transfer, it must signal the end of data transmission to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The ISL97649B releases the dataline to allow the master to generate a STOP condition.

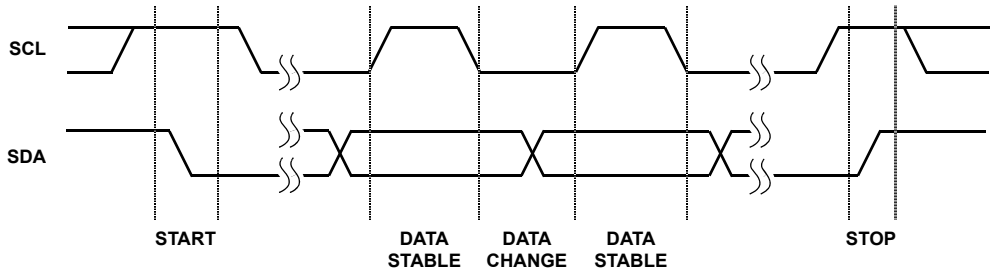


FIGURE 17. VALID DATA CHANGES, START, AND STOP CONDITIONS

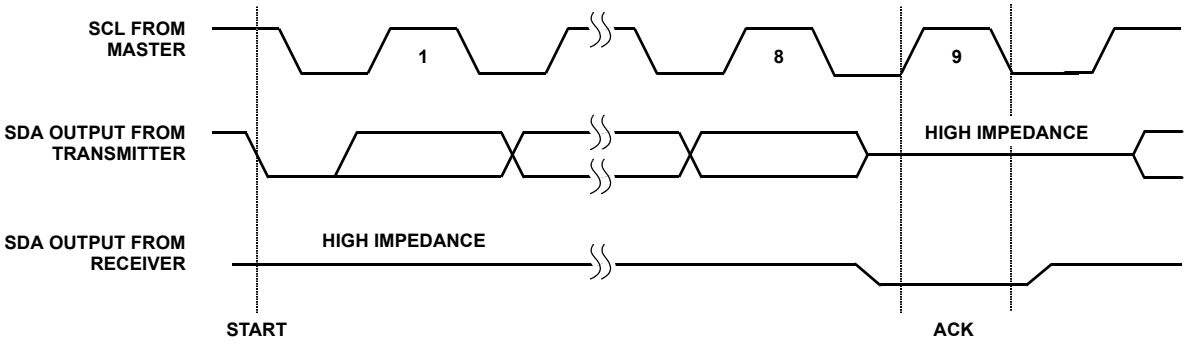


FIGURE 18. ACKNOWLEDGE RESPONSE FROM RECEIVER

A valid identification byte (Byte 1) contains 100111 as the six MSBs. The 7th bit could be either 0 or 1 in the read operation, while it is the data LSB (D0) in the write operation. The LSB is in the read/write bit. Its value is 1 for a read operation and 0 for a write operation (Figures 19 and 20).

Read Operation

A read operation consists of one instruction byte followed by one data byte (Figure 19). The master initiates a START and the identification byte with the R/W bit set to 1; the ISL97649B responds with an ACK; and then the ISL97649B transmits the data byte. The master terminates the read operation (issues a STOP condition) following the last bit of the data byte (Figure 19).

Write Operation

A write operation requires a START condition followed by a valid identification byte, a data byte, and a STOP condition (Figure 20). After each of the two bytes, the ISL97649B responds with an ACK. If the data byte is also to be written to non-volatile memory, the ISL97649B begins its internal write cycle to non-volatile memory. During the internal non-volatile write cycle, the device ignores transitions at the SDA and SCL pins (Figure 21), and the SDA output is at high impedance state. When the internal non-volatile write cycle is completed, the ISL97649B enters its standby state. The LSB in Byte 2 determines whether the data byte is to be written to volatile and/or non-volatile memory.

Data Protection

A STOP condition also acts as a protection of non-volatile memory. A valid identification byte, a data byte, and total number of SCL pulses act as a protection of both volatile and non-volatile registers. During a write sequence, the data byte is loaded into an internal shift register as it is received. If Byte 2 LSB is 1, the data byte is transferred to the register only. If Byte 2 LSB is 0, then the STOP condition initiates the internal write cycle to non-volatile memory.

ISL97649B Programming

Figure 19 shows the serial data format for reading the register. Figure 20 shows the serial data format for writing the register and Figure 21 for programming EEPROM.

The ISL97649B uses a 6-bit I2C address, which is 100111xx. The complete read and write protocol is shown in Figures 19 and 20.

I²C Read and Write Format

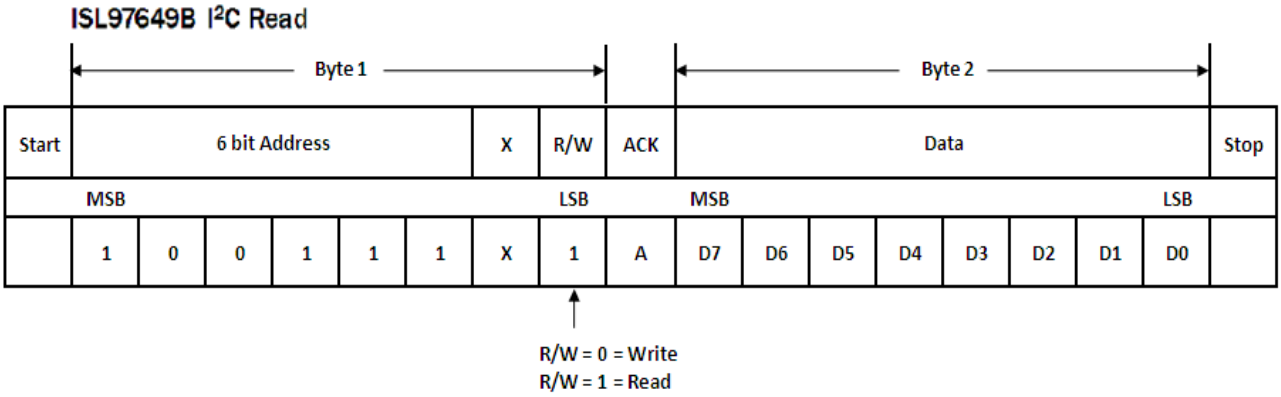


FIGURE 19. I²C READ FORMAT

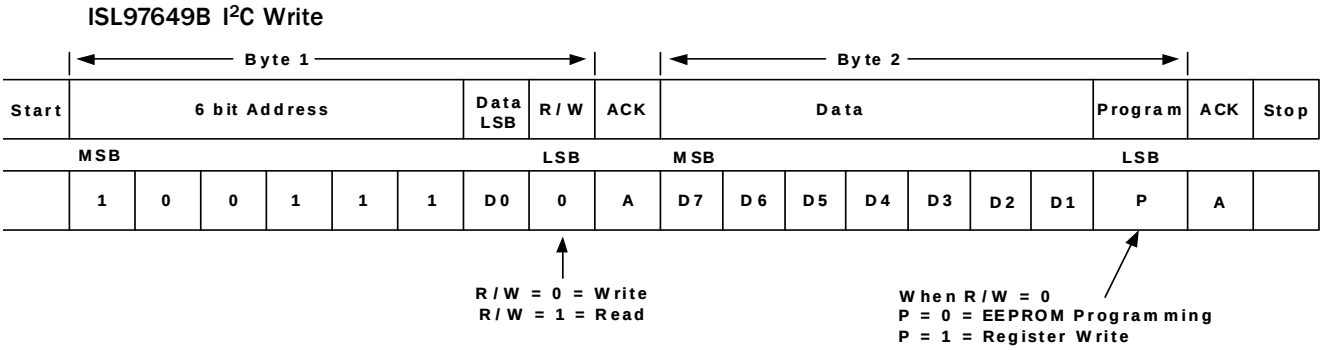


FIGURE 20. I²C WRITE FORMAT

Start-up Sequence

When VIN rising exceeds UVLO, it takes 120µs to read the settings stored in the chip in order to activate the chip correctly. When VIN is above UVLO and EN is high, the boost converter starts up. The gate pulse modulator output VGHM is held low until VDPM is charged to 1.215V. The detailed power-on sequence is shown in Figure 21.

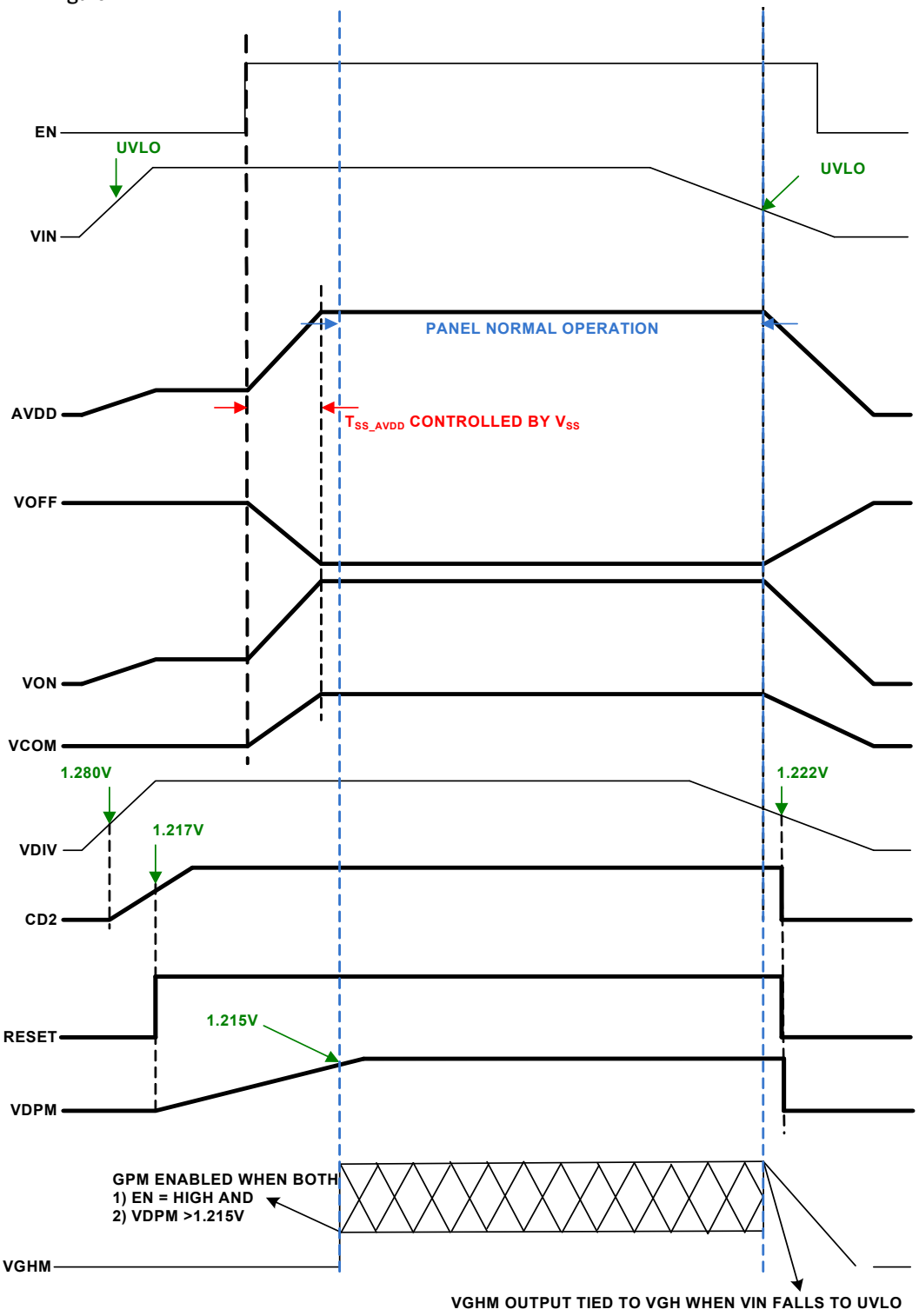


FIGURE 21. ISL97649B DETAILED POWER-ON/POWER-OFF SEQUENCE

Layout Recommendations

The device's performance, including efficiency, output noise, transient response and control loop stability, is dramatically affected by the PCB layout. PCB layout is critical, especially at high switching frequency.

Some general guidelines for layout:

1. Place the external power components (the input capacitors, output capacitors, boost inductor and output diodes, etc.) in close proximity to the device. Traces to these components should be kept as short and wide as possible to minimize parasitic inductance and resistance.
2. Place V_{DC} and V_{REF} bypass capacitors close to the pins.
3. Reduce the loop with large AC amplitudes and fast slew rate.
4. The feedback network should sense the output voltage directly from the point of load and should be as far away from the LX node as possible.
5. The power ground (PGND) and signal ground (SGND) pins should be connected at the ISL97649B exposed die plate area.
6. The exposed die plate, on the underside of the package, should be soldered to an equivalent area of metal on the PCB. This contact area should have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers, if available, to maximize thermal dissipation away from the IC.
7. To minimize thermal resistance of the package when soldered to a multi-layer PCB, the amount of copper track and ground plane area connected to the exposed die plate should be maximized and spread out as far as possible from the IC. The bottom and top PCB areas especially should be maximized to allow thermal dissipation to the surrounding air.
8. Minimize feedback input track lengths to avoid switching noise pick-up.

The ISL97649BIRTZ-EVALZ evaluation board is available to illustrate the proper layout implementation.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
June 14, 2013	FN7927.2	Added “VGH/VGL Charge Pump” on page 12. Made correction to Equation 9 From: VGH_headroom = (N + 1)*AVDD - N*Vd - VGH > 0 To: VGH_headroom = (N + 1)*AVDD - 2*N*Vd - VGH > 0
June 19, 2012	FN7927.1	Page 1, "Features" 1.5A Integrated Boost for Up to 15V AVDD changed to: 1.5A, 0.18Ω Integrated Boost FET
April 5, 2012		Changed pin 13, POS description in “Pin Descriptions” on page 2 from "VCOM Positive Amplifier Non-inverting input" to "VCOM Amplifier Non-inverting input" Changed pin 16, NEG description in “Pin Descriptions” on page 2 from "VCOM Negative Amplifier Non-inverting input" to "VCOM Amplifier inverting input" “Absolute Maximum Ratings” on page 4. Changed: LX, AVDD, POS, OUT to GND . . . . . -0.3 to +18V to: LX, AVDD, POS, NEG, VOUT to GND . . . . . -0.3 to +18V
October 7, 20011	FN7927.0	Initial Release

About Intersil

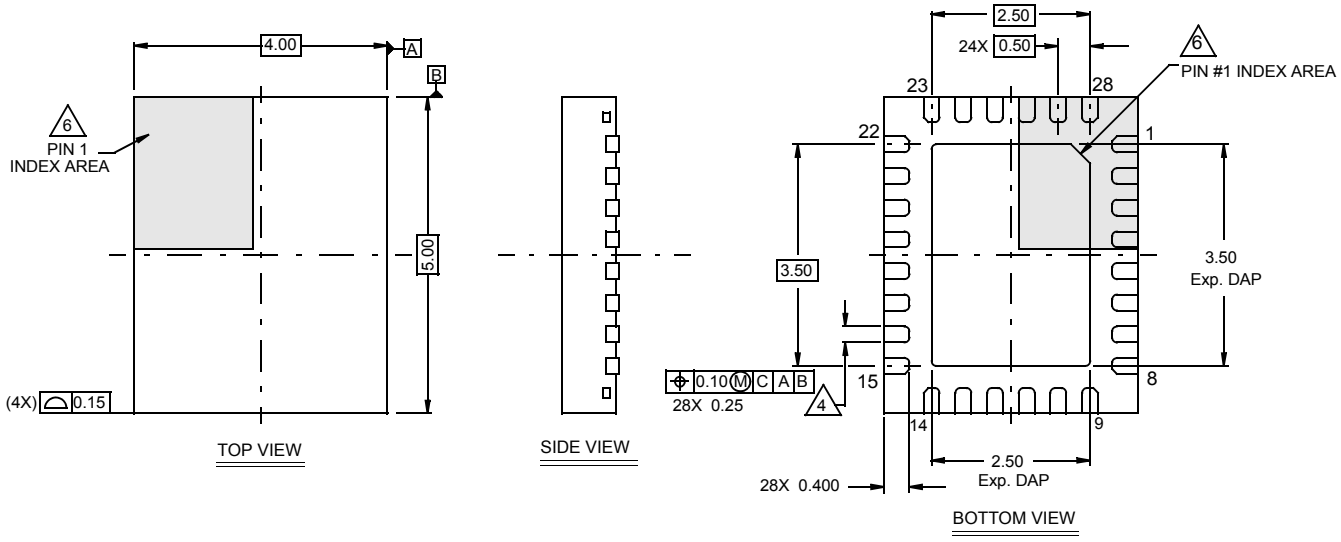
Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

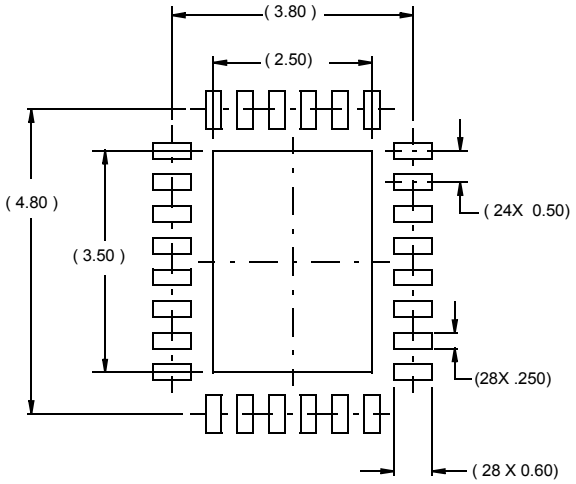
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

Package Outline Drawing

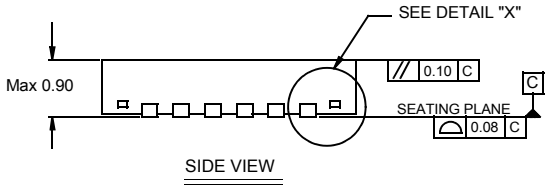
L28.4x5A

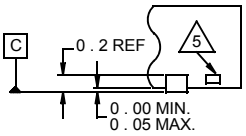
28 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 06/08





TYPICAL RECOMMENDED LAND PATTERN





NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.