

# NP50P06SDG

-60V – -50A – P-channel Power MOS FET

R07DS1511EJ0100

Application : Automotive

Rev.1.00

Jun. 03, 2022

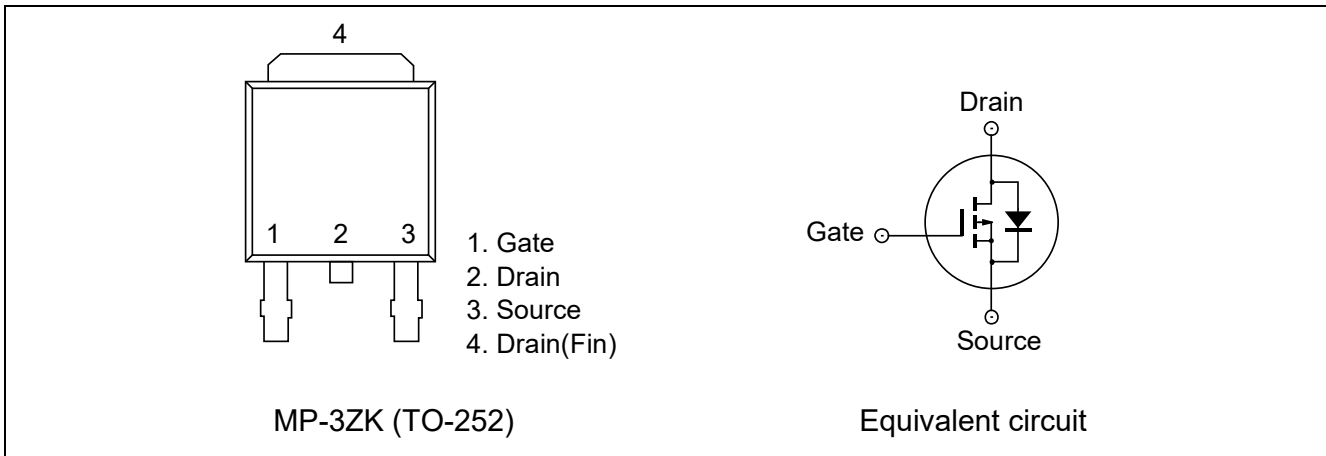
## Description

This product is P-channel MOS Field Effect Transistor designed for high current switching applications.

## Features

- Super low on-state resistance :  $R_{DS(on)} = 16.5 \text{ m}\Omega \text{ Max. ( } V_{GS} = -10 \text{ V, } I_D = -25 \text{ A )}$   
 $R_{DS(on)} = 23.0 \text{ m}\Omega \text{ Max. ( } V_{GS} = -4.5 \text{ V, } I_D = -25 \text{ A )}$
- Low input capacitance :  $C_{iss} = 5000 \text{ pF Typ.}$
- Designed for automotive application and AEC-Q101 qualified.
- Pb-free (This product does not contain Pb in the external electrode)

## Outline



## Absolute Maximum Ratings

( $T_a=25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	-60	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\mp 20$	V
Drain Current (DC) ( $T_c = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\mp 50$	A
Drain Current (pulse)	$I_{D(pulse)}$ <sup>Notes1</sup>	$\mp 150$	A
Total Power Dissipation ( $T_c = 25^\circ\text{C}$ )	$P_{T1}$	84	W
Total Power Dissipation ( $T_a = 25^\circ\text{C}$ )	$P_{T2}$	1.2	W
Channel Temperature	$T_{ch}$	175	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to 175	$^\circ\text{C}$
Single Avalanche Current	$I_{AS}$ <sup>Notes2</sup>	32	A
Single Avalanche Energy	$E_{AS}$ <sup>Notes2</sup>	102	mJ

Notes 1.  $PW \leq 10 \mu\text{s}$  , Duty Cycle  $\leq 1\%$

2. Starting  $T_{ch}=25^\circ\text{C}$  ,  $V_{DD} = -30\text{V}$  ,  $R_G = 25 \Omega$  ,  $V_{GS} = -20 \rightarrow 0\text{V}$  ,  $L = 100\mu\text{H}$

## Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-c)}$ <sup>Notes3</sup>	1.78	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-a)}$ <sup>Notes3</sup>	125	°C/W

## Electrical Characteristics

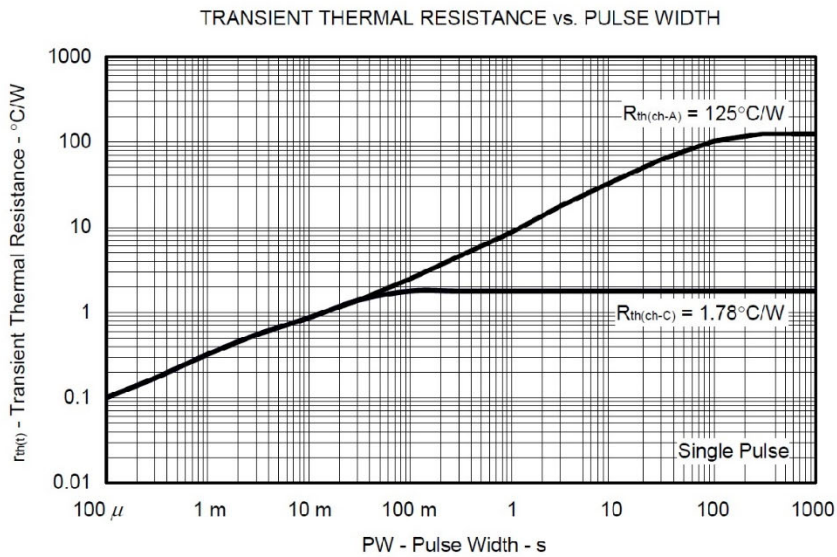
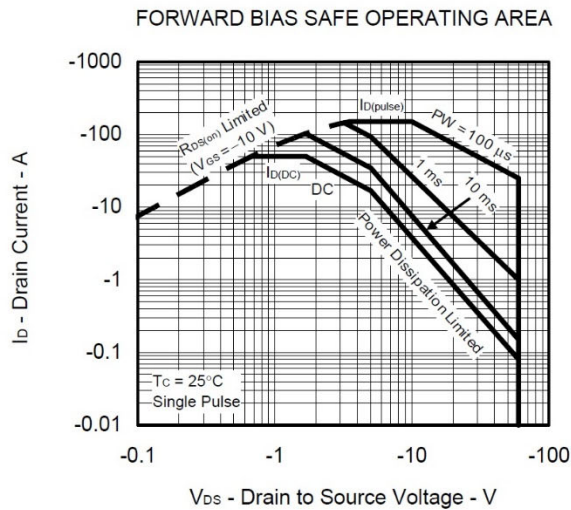
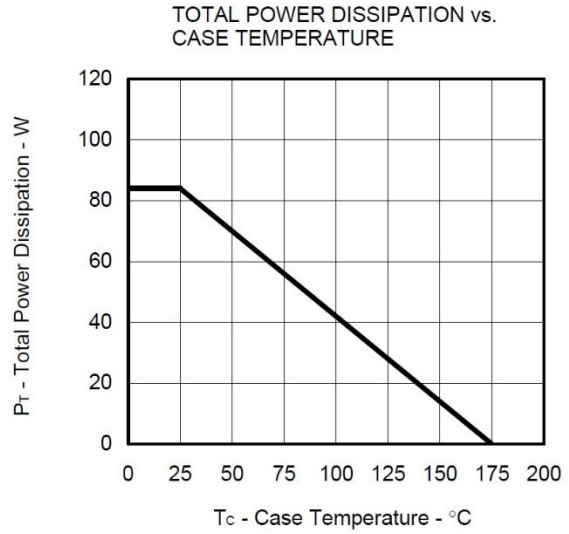
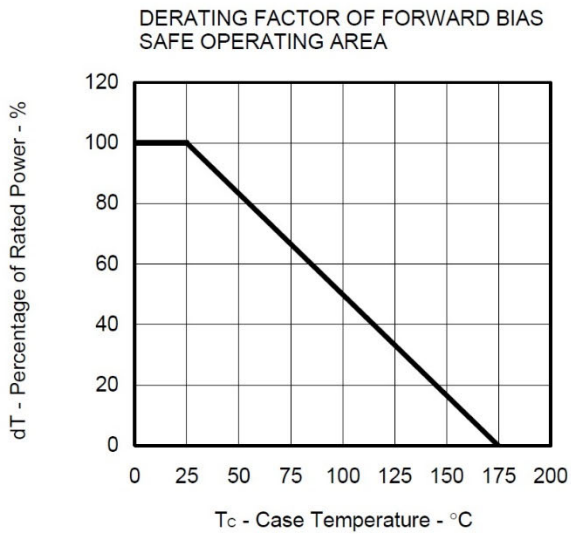
(T<sub>a</sub>=25°C)

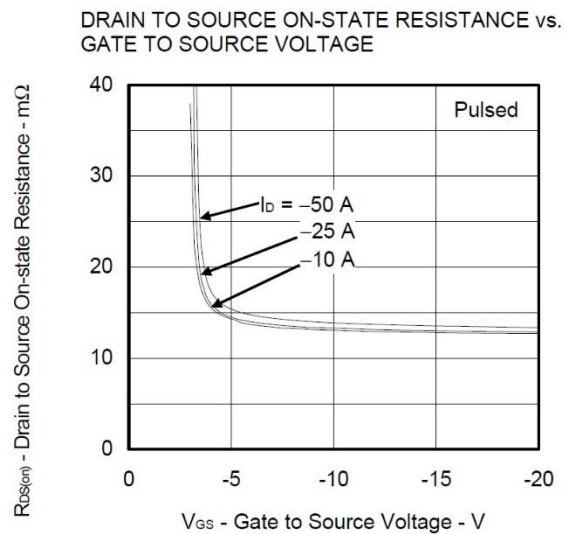
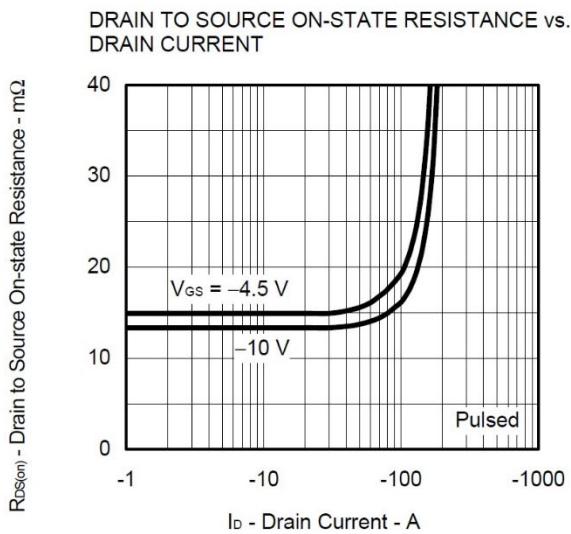
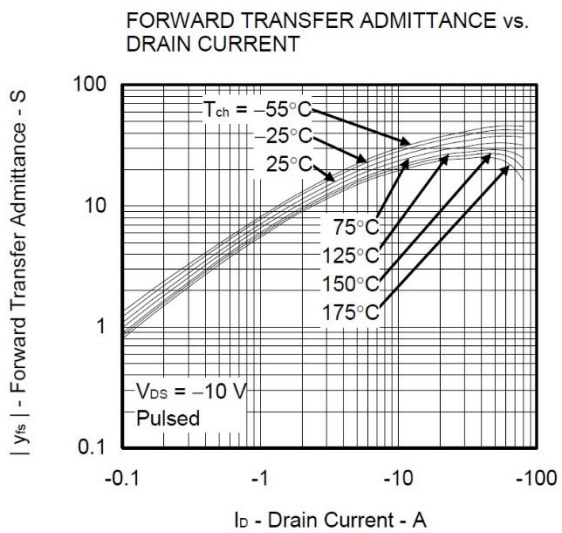
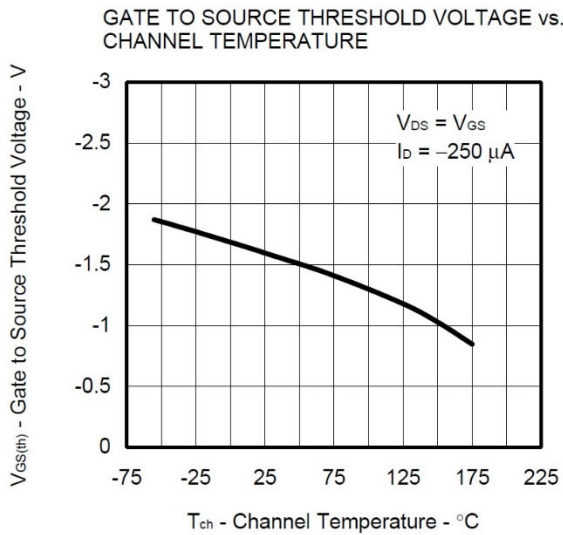
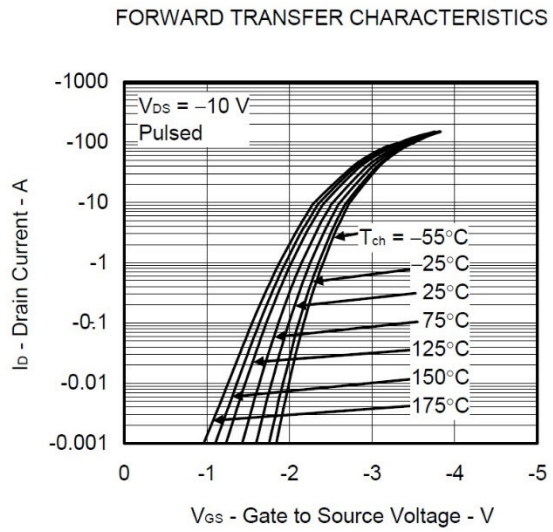
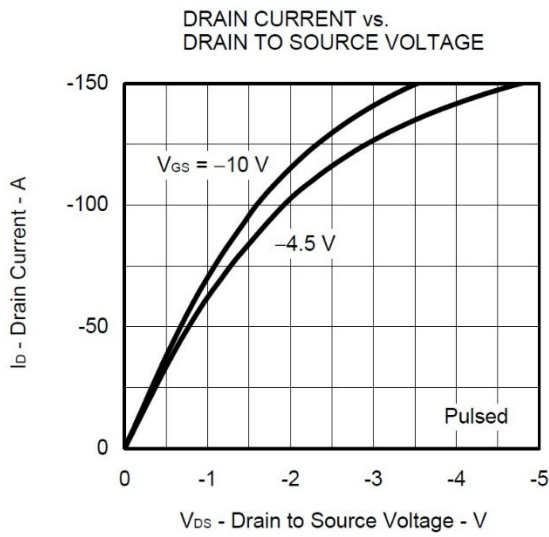
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	-10	μA	V <sub>DS</sub> = -60 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	$I_{GSS}$	—	—	±100	nA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	-1.0	-1.6	-2.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA
Forward Transfer Admittance	y <sub>fs</sub>   <sup>Notes4</sup>	15	33	—	S	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -25 A
Drain to Source On-state Resistance	$R_{DS(on)1}$ <sup>Notes4</sup>	—	13.2	16.5	mΩ	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -25 A
	$R_{DS(on)2}$ <sup>Notes4</sup>	—	14.9	23.0	mΩ	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -25 A
Input Capacitance	C <sub>iss</sub>	—	5000	—	pF	V <sub>DS</sub> = -10 V
Output Capacitance	C <sub>oss</sub>	—	600	—	pF	V <sub>GS</sub> = 0 V
Reverse Transfer Capacitance	C <sub>rss</sub>	—	300	—	pF	f = 1 MHz
Turn-on Delay Time	t <sub>d(on)</sub>	—	13	—	ns	V <sub>DD</sub> = -30 V
Rise Time	t <sub>r</sub>	—	13	—	ns	I <sub>D</sub> = -25 A
Turn-off Delay Time	t <sub>d(off)</sub>	—	405	—	ns	V <sub>GS</sub> = -10 V
Fall Time	t <sub>f</sub>	—	180	—	ns	R <sub>G</sub> = 0 Ω
Total Gate Charge	Q <sub>g</sub>	—	100	—	nC	V <sub>DD</sub> = -48 V
Gate to Source Charge	Q <sub>gs</sub>	—	11	—	nC	V <sub>GS</sub> = -10 V
Gate to Drain Charge	Q <sub>gd</sub>	—	30	—	nC	I <sub>D</sub> = -50 A
Body Diode Forward Voltage	V <sub>F(S-D)</sub> <sup>Notes4</sup>	—	0.97	1.5	V	I <sub>F</sub> = -50 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>	—	50	—	ns	I <sub>F</sub> = -50 A, V <sub>GS</sub> = 0 V
Reverse Recovery Charge	Q <sub>rr</sub>	—	72	—	nC	di/dt = -100 A/μs

Notes 3. Designed target value on Renesas measurement condition. Not subject to production test.

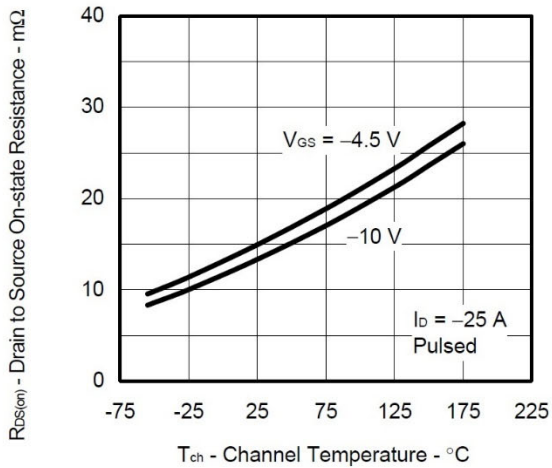
4. Pulse test.

### Typical Characteristics

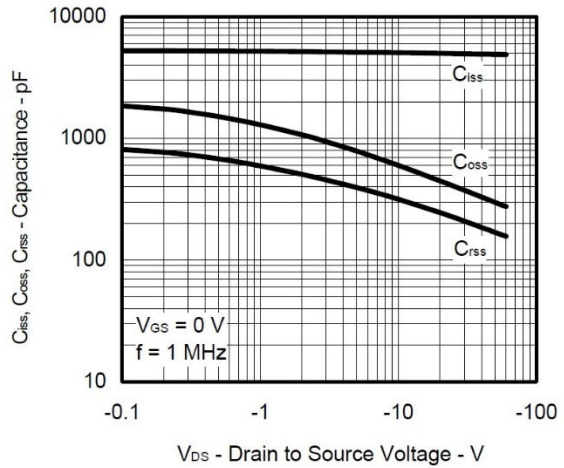




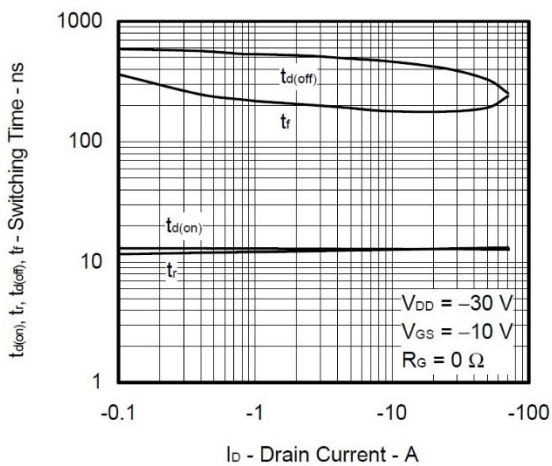
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



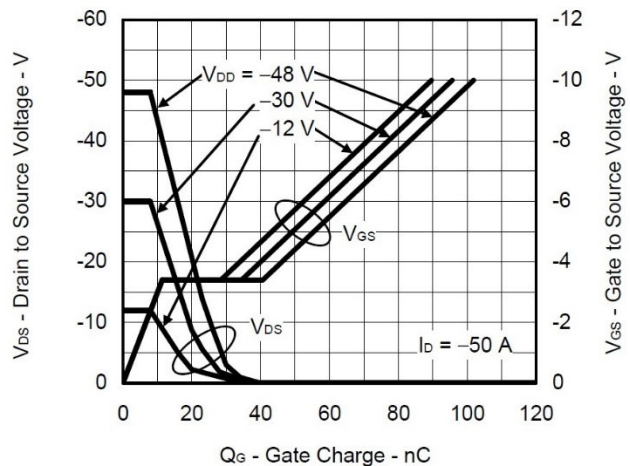
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



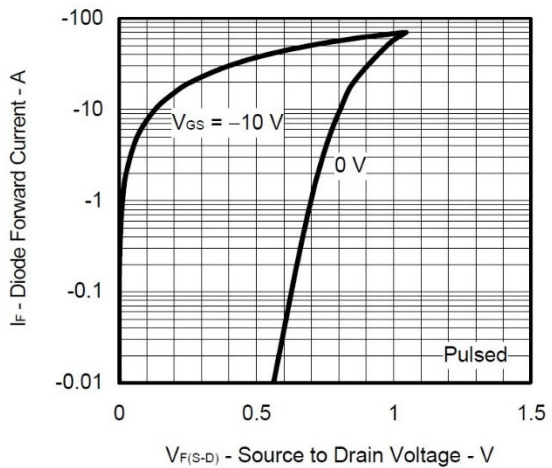
SWITCHING CHARACTERISTICS



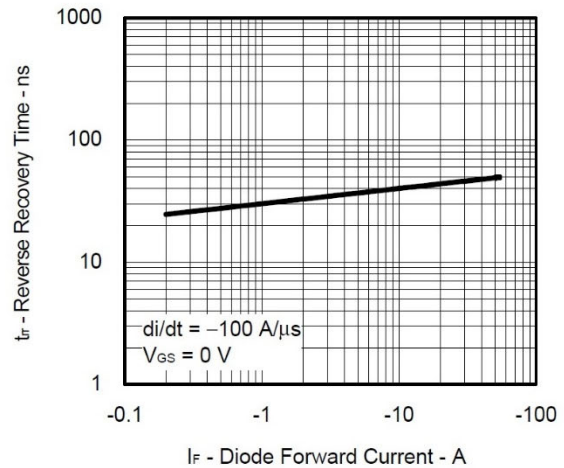
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



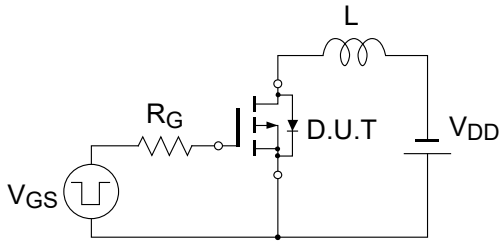
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



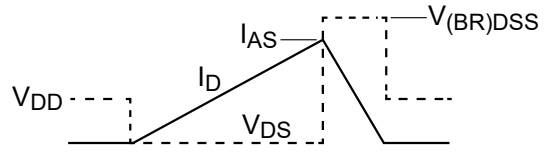
**Test Circuit**

**Avalanche**

Test Circuit



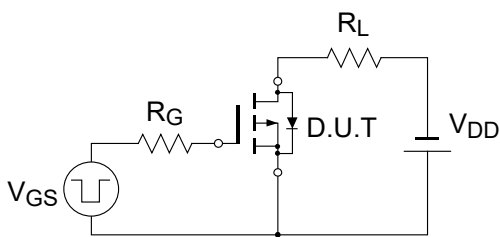
Waveform



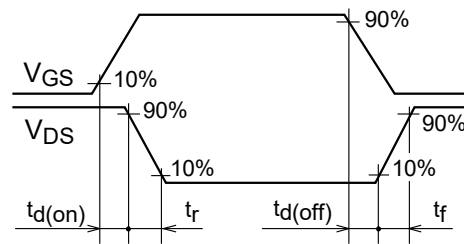
$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2 \cdot \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}$$

**Switching Time**

Test Circuit

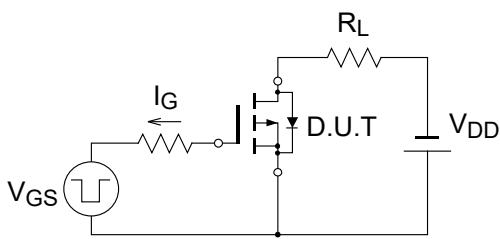


Waveform

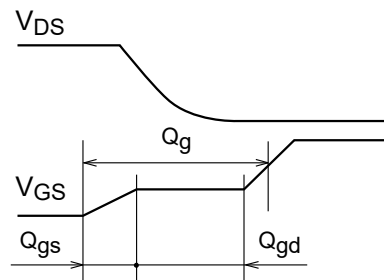


**Gate Charge**

Test Circuit

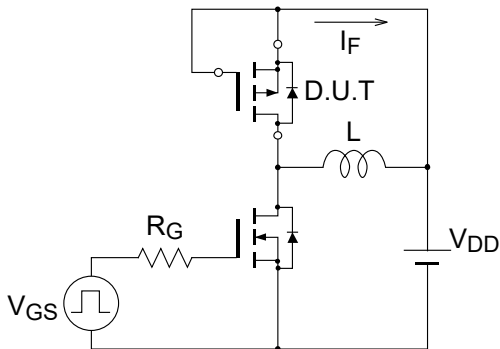


Waveform

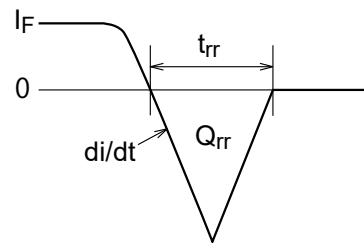


**Reverse Recovery**

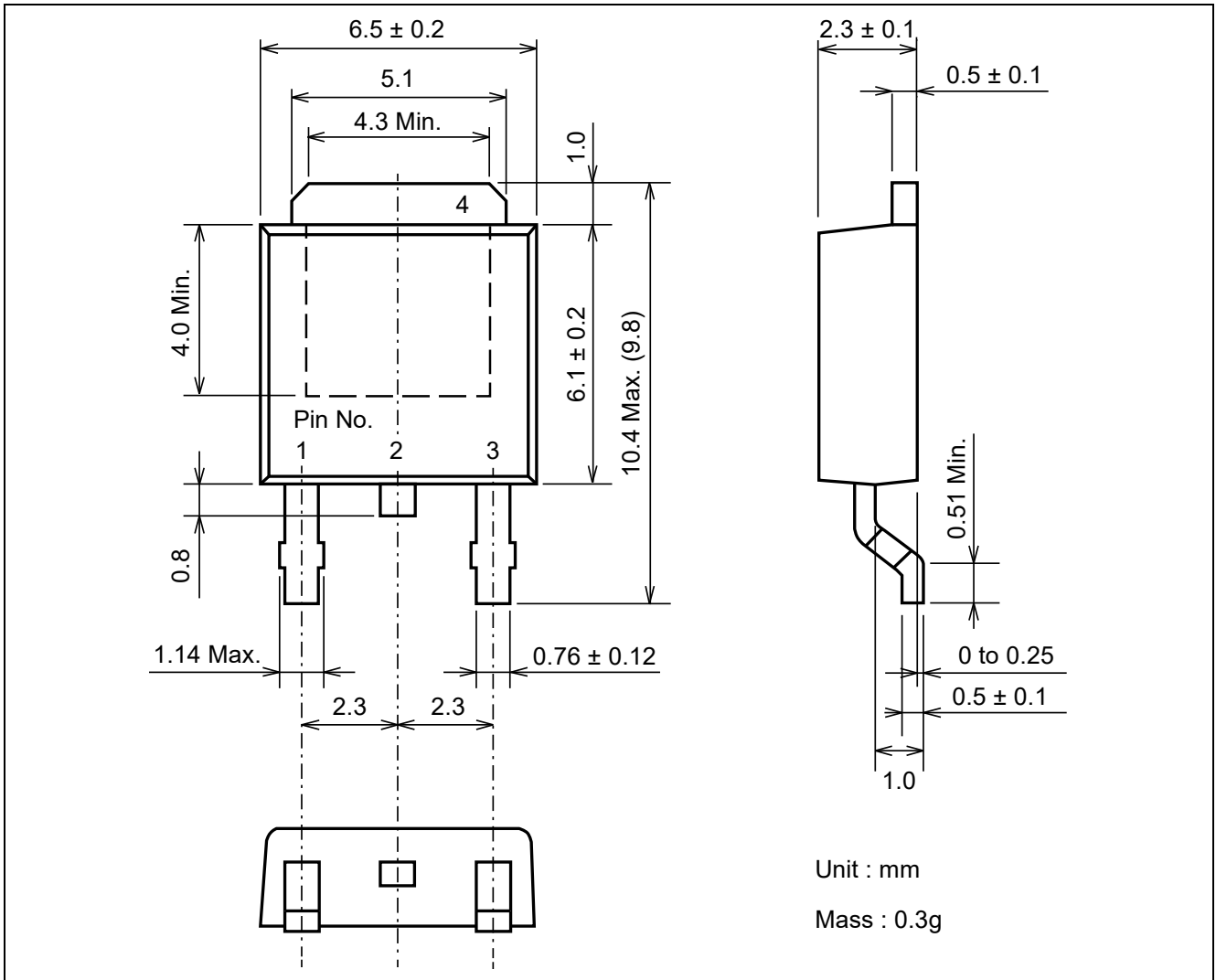
Test Circuit



Waveform



## Package Dimensions



## Ordering Information

Part No.	Quantity	Shipping container
NP50P06SDG-E1-AY	2500pcs/reel	Taping

**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.



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