RAA214403, RAA214404, RAA214405, RAA214409

40V 150mA Low IQ Fixed Output Voltage (3.3V, 3.6V, 5V, 9V) Low Dropout Regulators

The RAA21440x family, RAA214403 (3.3V), RAA214404 (3.6V), RAA214405 (5V), and RAA214409 (9V) are low-quiescent current fixed output voltage low-dropout regulators capable of sourcing up to 150mA to a load. The LDO has a wide input voltage range up to 40V.

The LDOs feature a ±3% output voltage accuracy (over line, load, and temperature), input UVLO with hysteresis, enable control, internal current limit, and over-temperature shutdown protection.

The LDOs are stable with a minimum 2.2µF ceramic output capacitor. The 3.3V and 5V LDOs are available in the 5 Ld SOT-23 and the 3 Ld SOT-89 packages. The 3.6V LDO is available in the 5-Ld SOT-23 package. The 9V LDO is available in the 3 Ld SOT-89 package.

The combination of low-quiescent current, low-shutdown current (shutdown function available with the SOT23 package), and small package size makes this family of LDOs an ideal choice for portable devices and battery powered equipment.

Features

- Typical low-quiescent current: 3.8µA at no load
- Typical shutdown current (SOT23 package): <0.5µA
- Wide input voltage range: up to 40V with 45V line transient tolerance
- Max output current: 150mA
- Output voltage accuracy: ±3% over line, load, and temperature
- Typical dropout voltage: 0.5V at 100mA
- Fixed output voltage options: 3.3V, 3.6V, 5V, and 9V
- Stable with 2.2µF minimum ceramic output capacitor
- Overcurrent and over-temperature protection
- Junction temperature range: -40°C to 125°C

Applications

- Portable and battery-powered equipment
- Notebook computers
- Motor drives

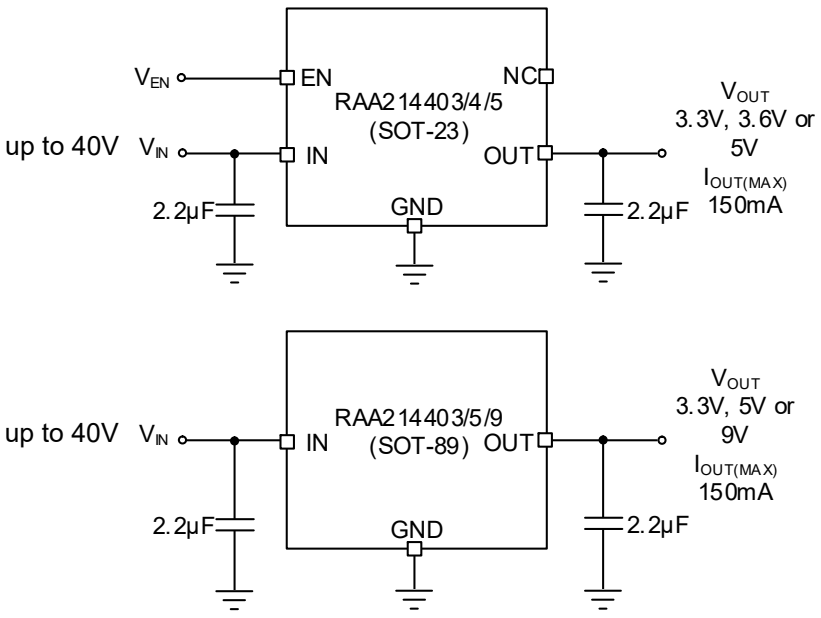


Figure 1. RAA214403/4/5/9 Typical Application Schematics

Contents

1. Overview

1.1 Block Diagram

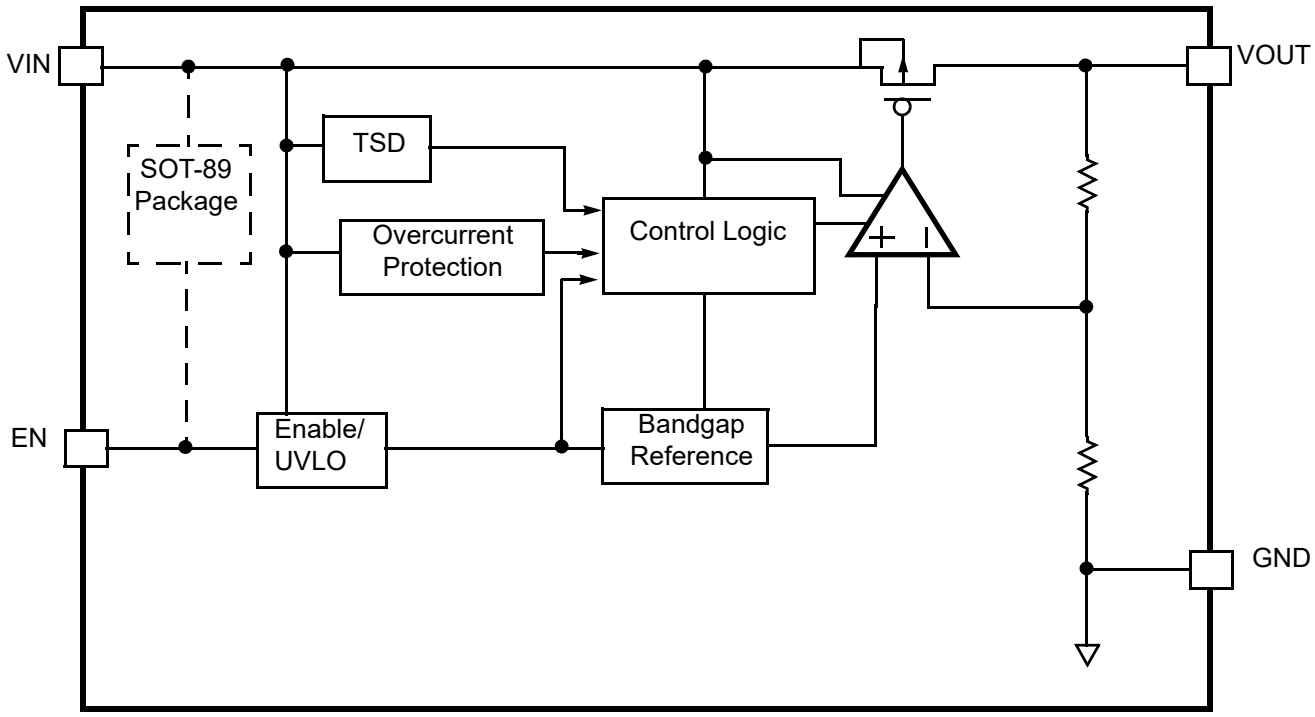
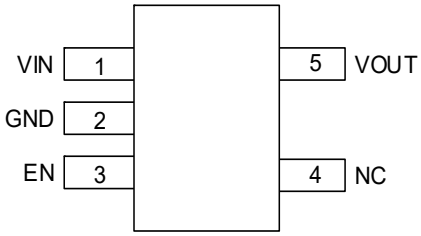


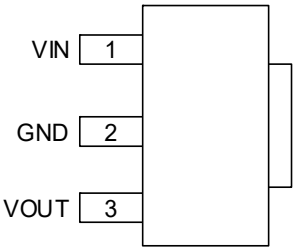
Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments



SOT-23
Top View



SOT-89
Top View

2.2 Pin Descriptions

Pin Number		Pin Name	Description
5-Ld SOT-23	3-Ld SOT-89		
1	1	VIN	VIN is the input voltage pin. This pin supplies power to the regulator. Requires a minimum ceramic bypass capacitor of 2.2µF. Applications with large load transients may require higher input capacitance. Place the input capacitor as close to the device input as possible.
2	2	GND	GND is the ground pin. This pin must be tied to the PCB ground plane.
3	-	EN	EN is the ENABLE pin. When set to LOW, it disables the device; when set to HIGH, it enables the device. This pin must not be left floating. When this pin is not being used, it must be tied to VIN.
4	-	NC	NC (No Connection) This pin can be tied to ground or left floating. No internal connection.
5	3	VOUT	VOUT is the output pin. This pin provides power to the load. For stable operation across the full temperature range, VIN range, output range, and load extremes a minimum 2.2µF capacitor is required from VOUT to GND. For best transient response, use a 4.7µF or larger ceramic capacitor. Place the output capacitor as close to the device output as possible.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter[1]	Minimum	Maximum	Unit
VIN	-0.3	+45	V
VOUT	-0.3	+38	V
VEN	-0.3	+45	V
Maximum Junction Temperature	-	+125	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2017)	-	2	kV
Charged Device Model (Tested per JS-002-2018)	-	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	100	mA

1. All voltages referenced to GND unless otherwise specified.

3.2 Recommended Operating Conditions

Parameter[1]	Minimum	Maximum	Unit
Supply Voltage, VIN	4.5	40	V
Enable Voltage, VEN	2	40	V
Output Current, IOUT	0	150	mA
Output Capacitor, COUT	2.2	47	µF
Junction Temperature	-40	+125	°C

1. All voltages referenced to GND unless otherwise specified.

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance[1]	5-Ld SOT-23	θ_{JA}[2]	Junction to ambient	174	°C/W
		θ_{JC}[3]	Junction to case	58	°C/W
	3-Ld SOT-89	θ_{JA}[2]	Junction to ambient	52	°C/W
		θ_{JC}[3]	Junction to case	14	°C/W

1. Specified at published junction to ambient thermal resistance for a junction temperature of +150°C. See footnote 2 for test conditions to establish junction to ambient thermal resistance.
2. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
3. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.4 Electrical Specifications

Operating conditions unless otherwise noted: T_J = -40°C to +125°C, V_{IN} = V_{OUT} + 300mV, I_{OUT} = 1mA, V_{EN} = 2V, C_{IN} = C_{OUT} = 2.2µF MLCC. Typical values are at T_A = +25°C, unless otherwise specified.

Parameter	Note	Test Conditions	Min.[1]	Typ.	Max.[1]	Unit
Input						
Input Voltage Range V_{IN}	RAA214403	I_{OUT} = 10mA	3.6	-	40	V
	RAA214404		3.9	-	40	
	RAA214405		5.3	-	40	
	RAA214409		9.3	-	40	
Input UVLO Rising Threshold	-	VIN Rising	2.15	2.42	2.68	V
Input UVLO Falling Threshold	-	VIN Falling	1.98	2.2	2.43	V
Quiescent Current I_Q	-	V_{IN} = V_{OUT} + 700mV	-	3.8	7.3	µA
Ground Current I_{GND}	-	I_{OUT} = 10mA, V_{IN} = V_{OUT} + 700mV	-	36	124	µA
		I_{OUT} = 50mA, V_{IN} = V_{OUT} + 700mV	-	79	113	
		I_{OUT} = 150mA, V_{IN} = V_{OUT} + 1.9V	-	159	231	
Shutdown Current I_{SHDN}	-	VEN = 0V	-	248	577	nA
Output						
Output Voltage	RAA214403	I_{OUT} = 10mA, V_{IN} = V_{OUT} + 300mV	3.201	3.3	3.399	V
	RAA214404		3.492	3.6	3.708	
	RAA214405		4.85	5	5.15	
	RAA214409		8.63	9	9.35	
Output Current I_{OUT}	-	-	0	-	150	mA

Operating conditions unless otherwise noted: T_J = -40°C to +125°C, V_{IN} = V_{OUT} + 300mV, I_{OUT} = 1mA, V_{EN} = 2V, C_{IN} = C_{OUT} = 2.2µF MLCC. Typical values are at T_A = +25°C, unless otherwise specified. (Cont.)

Parameter	Note	Test Conditions	Min.[1]	Typ.	Max.[1]	Unit
Dropout Voltage V_{DO}	RAA214403	I_{OUT} = 10mA	-	50	83	mV
		I_{OUT} = 50mA	-	255	581	
		I_{OUT} = 100mA	-	510	1126	
		I_{OUT} = 150mA	-	760	1278	
	RAA214404	I_{OUT} = 10mA	-	50	92	
		I_{OUT} = 50mA	-	245	391	
		I_{OUT} = 100mA	-	495	803	
		I_{OUT} = 150mA	-	760	1337	
	RAA214405	I_{OUT} = 10mA	-	46	83	
		I_{OUT} = 50mA	-	235	509	
		I_{OUT} = 100mA	-	474	1017	
		I_{OUT} = 150mA	-	737	1333	
	RAA214409	I_{OUT} = 10mA	-	49	111	
		I_{OUT} = 50mA	-	236	636	
		I_{OUT} = 100mA	-	487	1309	
		I_{OUT} = 150mA	-	764	1756	
Load Regulation $\Delta V_{OUT}/\Delta I_{OUT}$	-	I_{OUT} = 100µA to 150mA, V_{IN} = V_{OUT} + 1.9V	-	0.003	0.005	%/mA
Line Regulation $\Delta V_{OUT}/\Delta V_{IN}$	-	V_{IN} = V_{OUT} + 250mV to 40V, I_{OUT} = 10mA	-	0.001	0.005	%/V
Start-Up Time	-	Time from V_{IN} = V_{OUT} + 1.9V to 95% of V_{OUT}, I_{OUT} = 0mA	254	755	1106	µs

Operating conditions unless otherwise noted: T_J = -40°C to +125°C, V_{IN} = V_{OUT} + 300mV, I_{OUT} = 1mA, V_{EN} = 2V, C_{IN} = C_{OUT} = 2.2µF MLCC. Typical values are at T_A = +25°C, unless otherwise specified. (Cont.)

Parameter	Note	Test Conditions	Min.[1]	Typ.	Max.[1]	Unit
Power Supply Ripple Rejection Ratio PSRR	RAA214403, RAA214404	C_{IN} = None, V_{IN} = V_{OUT} + 1.9V FREQ = 10Hz	-	78	-	dB
	RAA214405		-	74	-	dB
	RAA214409		-	75	-	dB
	RAA214403, RAA214404	C_{IN} = None, V_{IN} = V_{OUT} + 1.9V FREQ = 100Hz	-	72	-	dB
	RAA214405		-	73	-	dB
	RAA214409		-	69	-	dB
	RAA214403, RAA214404	C_{IN} = None, V_{IN} = V_{OUT} + 1.9V FREQ = 1kHz	-	65	-	dB
	RAA214405		-	57	-	dB
	RAA214409		-	49	-	dB
	RAA214403, RAA214404	C_{IN} = None, V_{IN} = V_{OUT} + 1.9V FREQ = 10kHz	-	49	-	dB
	RAA214405		-	49	-	dB
	RAA214409		-	47	-	dB
	RAA214403, RAA214404	C_{IN} = None, V_{IN} = V_{OUT} + 1.9V FREQ = 10kHz	-	61	-	dB
	RAA214405		-	63	-	dB
	RAA214409		-	62	-	dB
	RAA214403, RAA214404	C_{IN} = None, V_{IN} = V_{OUT} + 1.9V FREQ = 1MHz	-	60	-	dB
	RAA214405		-	67	-	dB
	RAA214409		-	66	-	dB
Output Voltage Noise Vn	RAA214403	V_{IN} = 6V, I_{OUT} = 10mA, BW = 10Hz to 100kHz	-	221	-	µVRMS
	RAA214404	V_{IN} = 6V, I_{OUT} = 10mA, BW = 10Hz to 100kHz	-	243	-	µVRMS
	RAA214405	V_{IN} = 6.3V, I_{OUT} = 10mA, BW = 10Hz to 100kHz	-	295	-	µVRMS
	RAA214409	V_{IN} = 12V, I_{OUT} = 10mA, BW = 10Hz to 100kHz	-	483	-	µVRMS
EN						
V_{EN} Rising Threshold	-	I_{OUT} = 10mA	1.3	1.5	1.68	V
V_{EN} Falling Threshold	-		1.07	1.21	1.34	mV
EN Leakage Current I_{EN}	-	V_{EN} = 40V	-	79	212	nA
Protection						
Output Current Limit I_{LIM}	-	V_{OUT} = V_{NOM}-1V	184	250	320	mA
Thermal Shutdown	-	Temperature Rising	-	150	-	°C
Hysteresis	-	-	-	20	-	°C

1. Compliance to datasheet limits is established by one or more methods: production test, characterization, and/or design.

4. Typical Performance Graphs

Operating conditions unless otherwise noted: T_J = 25°C, V_{IN} = V_{OUT} + 1.9V, I_{OUT} = 10mA, V_{EN} = 2V, C_{IN} = C_{OUT} = 2.2µF MLCC.

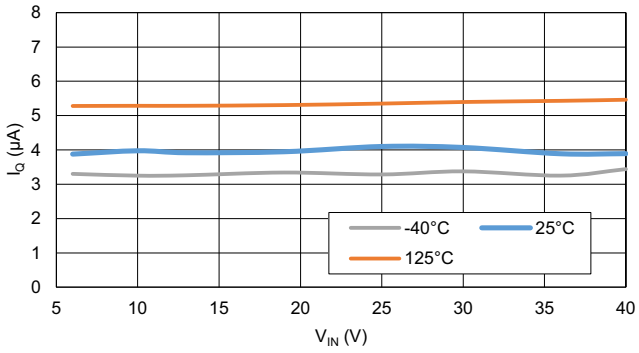


Figure 3. RAA214403 Quiescent Current vs V_{IN}

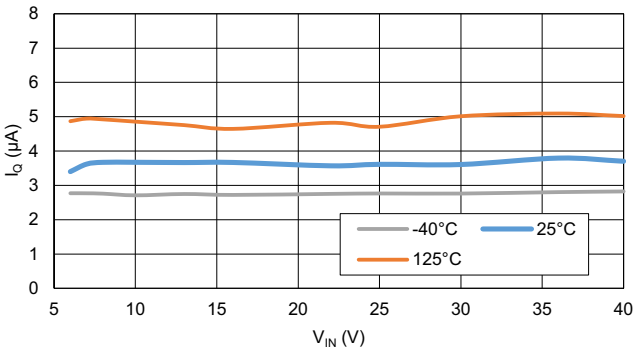


Figure 4. RAA214404 Quiescent Current vs V_{IN}

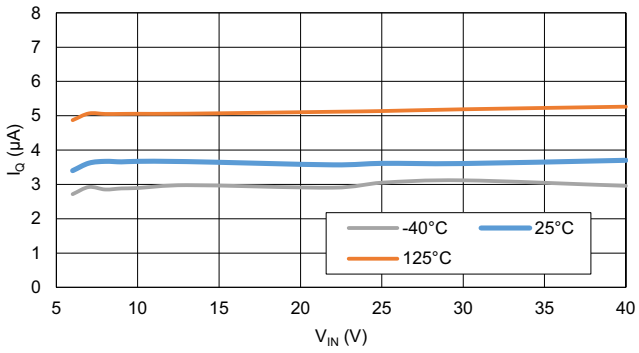


Figure 5. RAA214405 Quiescent Current vs V_{IN}

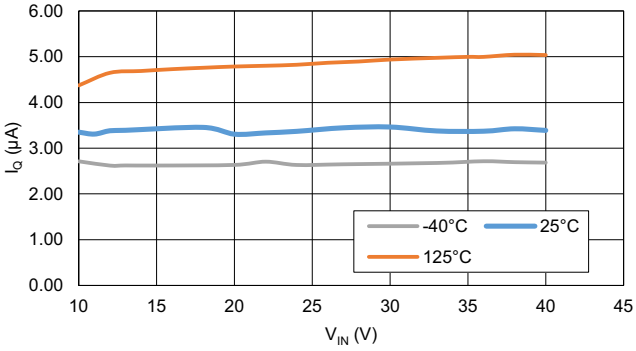


Figure 6. RAA214409 Quiescent Current vs V_{IN}

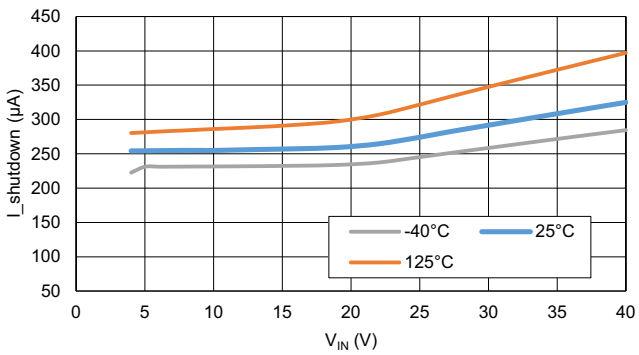


Figure 7. RAA214403 Shutdown Current vs V_{IN}

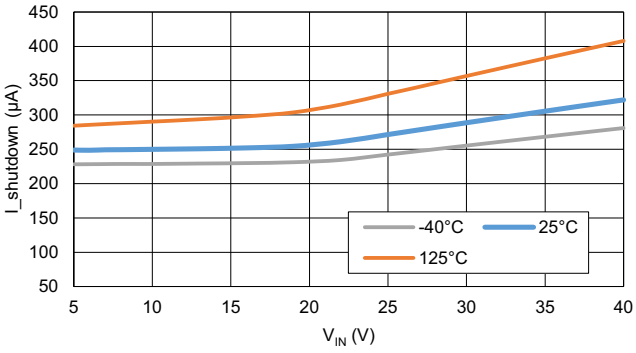


Figure 8. RAA214404 Shutdown Current vs V_{IN}

Operating conditions unless otherwise noted: T_J = 25°C, V_{IN} = V_{OUT} + 1.9V, I_{OUT} = 10mA, V_{EN} = 2V, C_{IN} = C_{OUT} = 2.2µF MLCC. (Cont.)

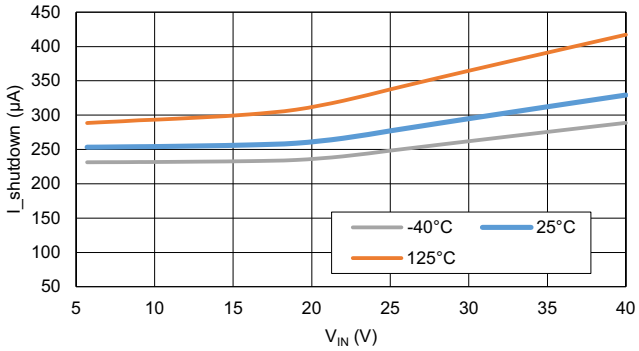


Figure 9. RAA214405 Shutdown Current vs V_{IN}

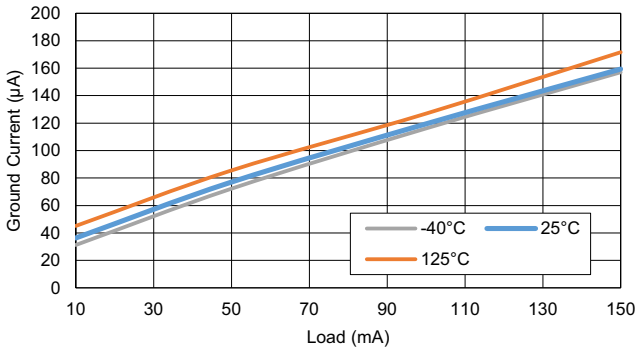


Figure 10. RAA214409 Ground Current vs V_{IN}

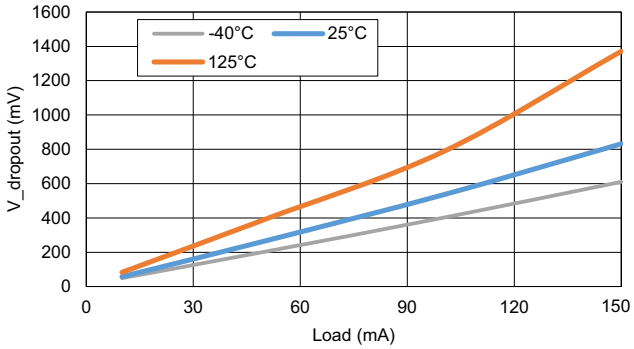


Figure 11. RAA214403 Dropout Voltage vs I_{OUT}

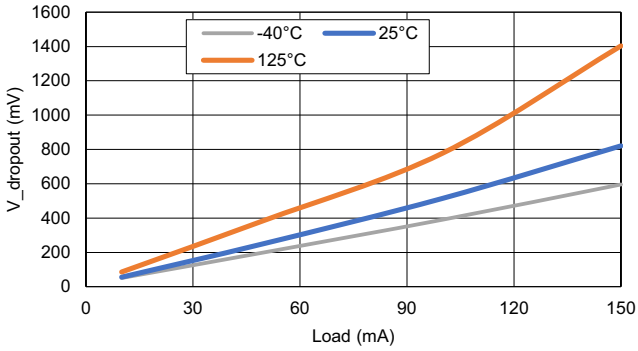


Figure 12. RAA214404 Dropout Voltage vs I_{OUT}

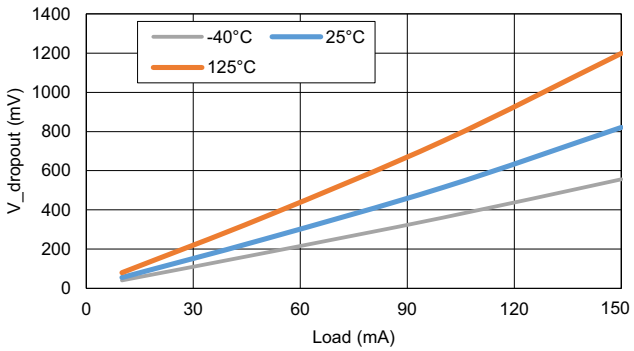


Figure 13. RAA214405 Dropout Voltage vs I_{OUT}

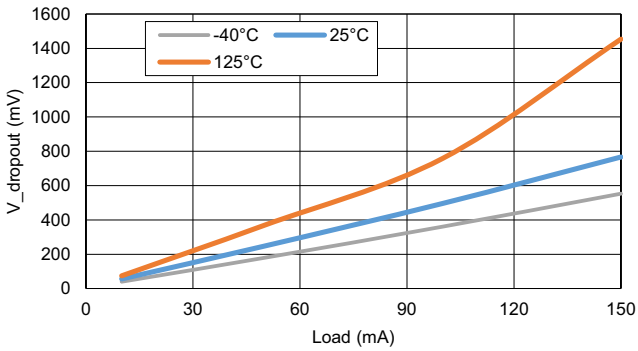


Figure 14. RAA214409 Dropout Voltage vs I_{OUT}

Operating conditions unless otherwise noted: T_J = 25°C, V_{IN} = V_{OUT} + 1.9V, I_{OUT} = 10mA, V_{EN} = 2V, C_{IN} = C_{OUT} = 2.2µF MLCC. (Cont.)

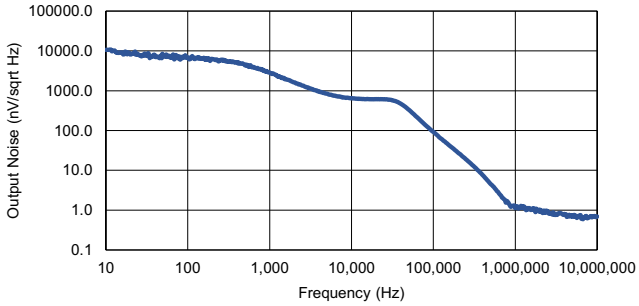


Figure 15. RAA214403 Output Noise

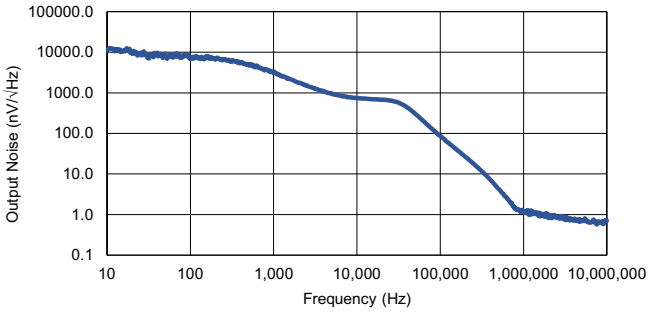


Figure 16. RAA214404 Output Noise

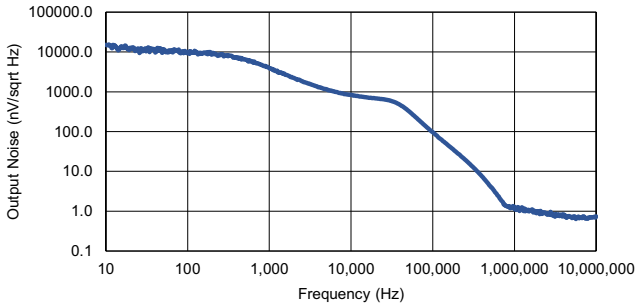


Figure 17. RAA214405 Output Noise

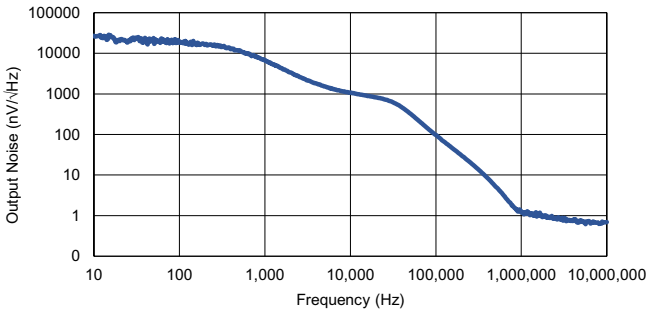


Figure 18. RAA214409 Output Noise

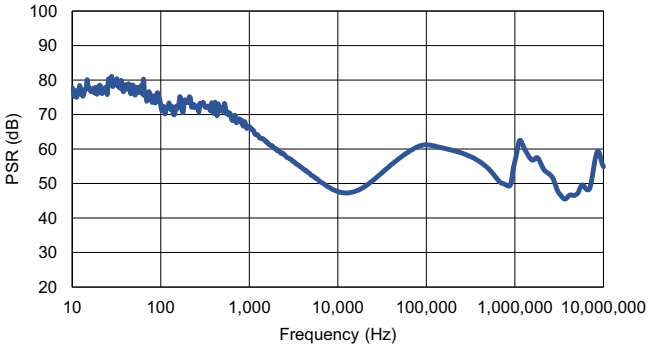


Figure 19. RAA214403 PSRR vs Frequency (I_{OUT} = 1mA)

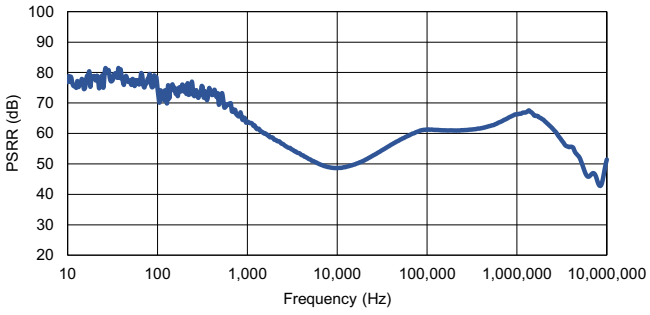


Figure 20. RAA214404 PSRR vs Frequency (I_{OUT} = 1mA)

Operating conditions unless otherwise noted: T_J = 25°C, V_{IN} = V_{OUT} + 1.9V, I_{OUT} = 10mA, V_{EN} = 2V, C_{IN} = C_{OUT} = 2.2µF MLCC. (Cont.)

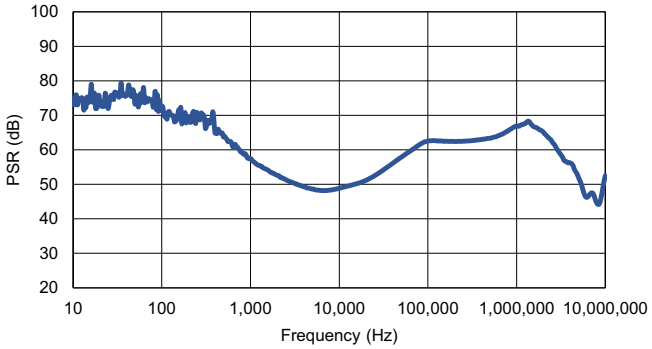


Figure 21. RAA214405 PSRR vs Frequency (I_{OUT} = 1mA)

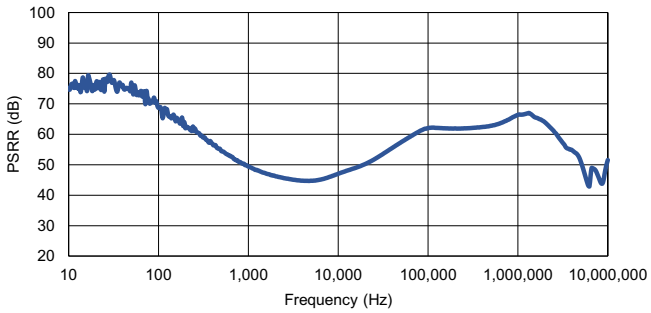


Figure 22. RAA214409 PSRR vs Frequency (I_{OUT} = 1mA)

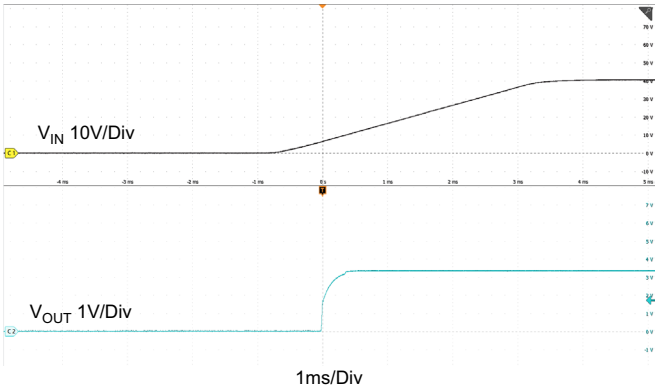


Figure 23. RAA214403 Startup Waveform (V_{IN} =40V, I_{OUT} = 10mA)

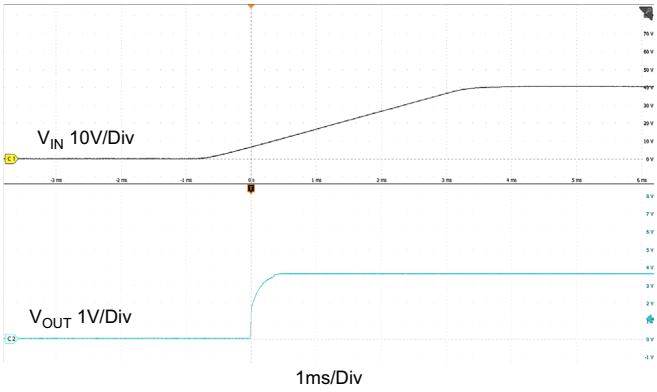


Figure 24. RAA214404 Startup Waveform (V_{IN} =40V, I_{OUT} = 10mA)

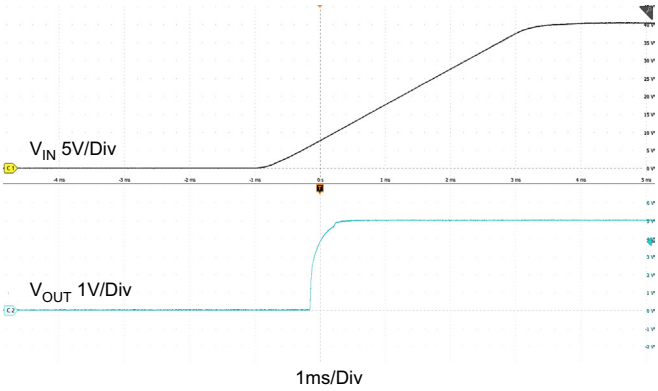


Figure 25. RAA214405 Startup Waveform (V_{IN} =40V, I_{OUT} = 10mA)

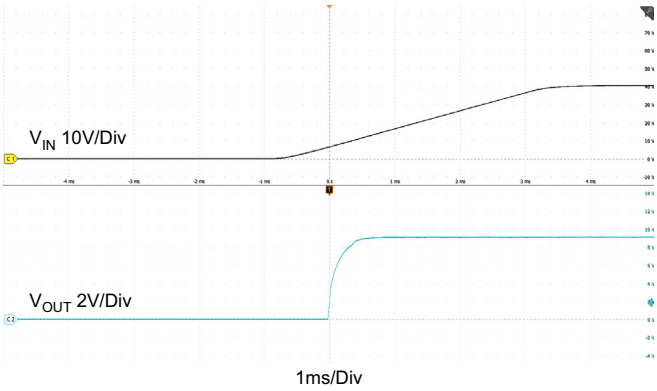


Figure 26. RAA214409 Startup Waveform (V_{IN} =40V, I_{OUT} = 10mA)

Operating conditions unless otherwise noted: T_J = 25°C, V_{IN} = V_{OUT} + 1.9V, I_{OUT} = 10mA, V_{EN} = 2V, C_{IN} = C_{OUT} = 2.2µF MLCC. (Cont.)

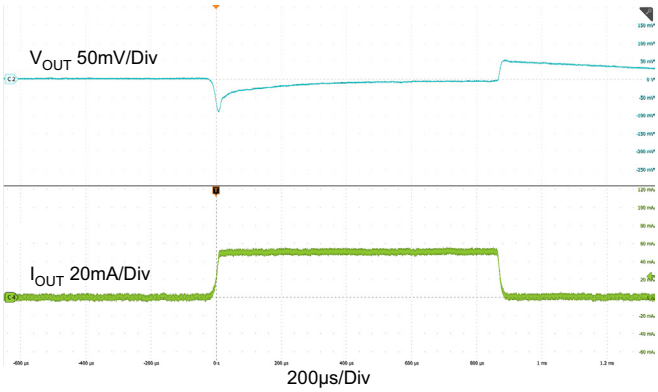


Figure 27. RAA214403 Load Transient Response (0.1mA to 50mA)

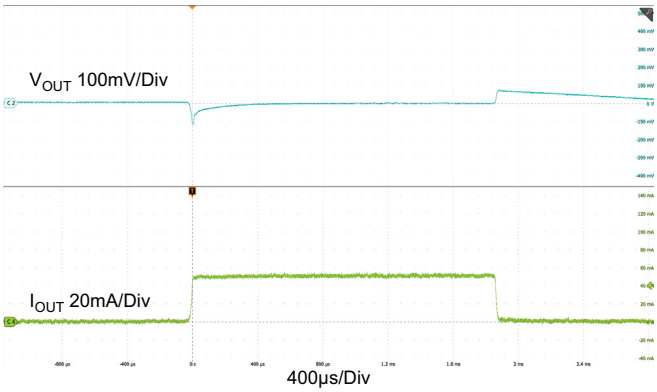


Figure 28. RAA214404 Load Transient Response (0.1mA to 50mA)

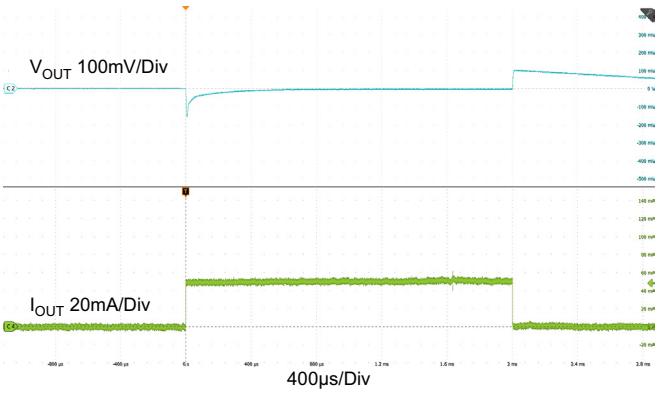


Figure 29. RAA214405 Load Transient Response (0.1mA to 50mA)

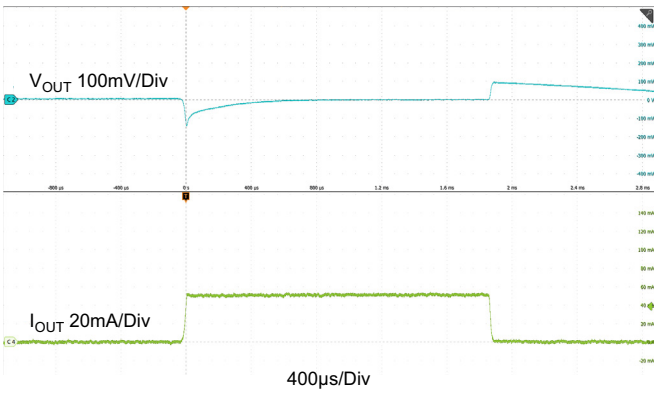


Figure 30. RAA214409 Load Transient Response (0.1mA to 50mA)

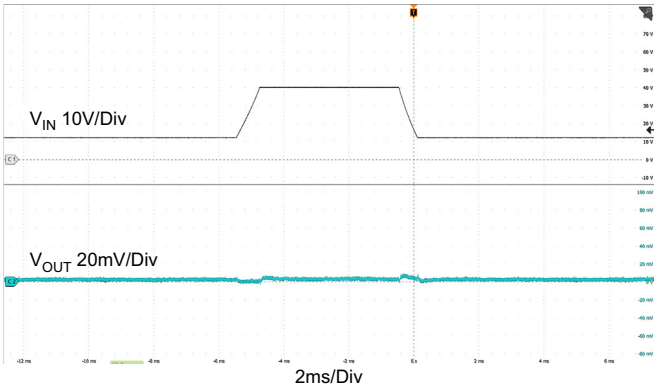


Figure 31. RAA214403 Line Transient Response (12V to 40V, I_{OUT} = 10mA)

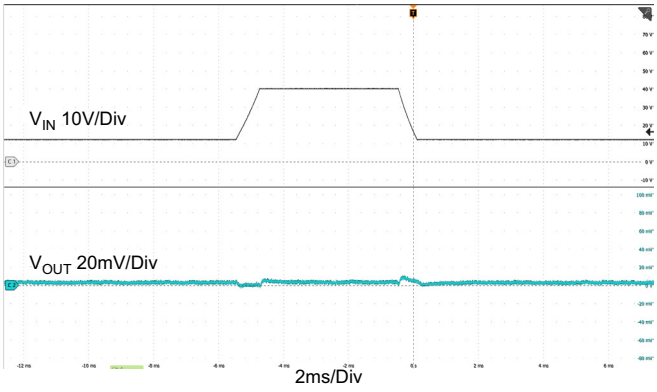


Figure 32. RAA214404 Line Transient Response (12V to 40V, I_{OUT} = 10mA)

Operating conditions unless otherwise noted: T_J = 25°C, V_{IN} = V_{OUT} + 1.9V, I_{OUT} = 10mA, V_{EN} = 2V, C_{IN} = C_{OUT} = 2.2µF MLCC. (Cont.)

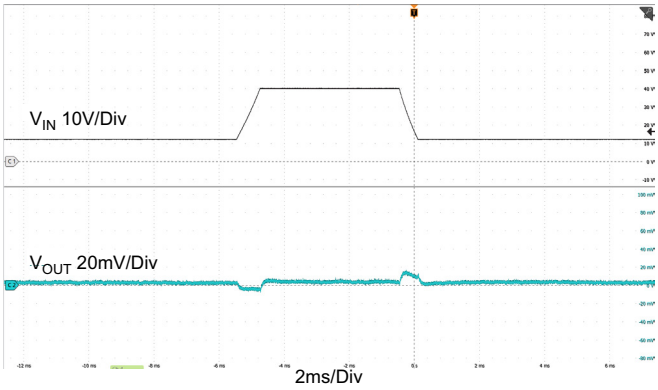


Figure 33. RAA214405 Line Transient Response (12V to 40V, I_{OUT} = 10mA)

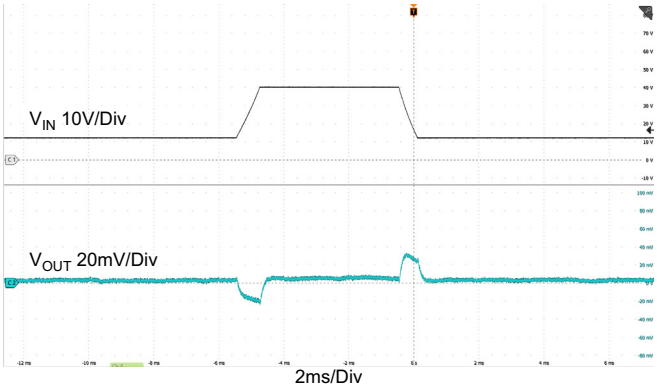


Figure 34. RAA214409 Line Transient Response (12V to 40V, I_{OUT} = 10mA)

5. Application Information

5.1 Overview

The RAA21440x family are fixed output voltage, low-quiescent current, low-dropout regulators capable of sourcing up to 150mA. The LDOs work with a minimum 2.2µF ceramic output capacitor and have a wide input voltage range up to 40V. The LDOs feature a ±3% output voltage accuracy, input UVLO, internal current limit, and over-temperature shutdown protection. The parts in the SOT-23 package include an enable function.

The combination of low-quiescent current, low-shutdown current, and small package size makes this an ideal choice for portable devices and battery-powered equipment.

5.2 Theory of Operation of PMOS LDOs

Like the majority of LDOs with a PMOS pass transistor, the RAA21440x family of DC output voltage (V_{OUT}) regulation can be a modeled with a voltage reference (V_{REF}), PMOS pass-transistor, error amplifier, and feedback (FB) resistors as shown in Figure 35.

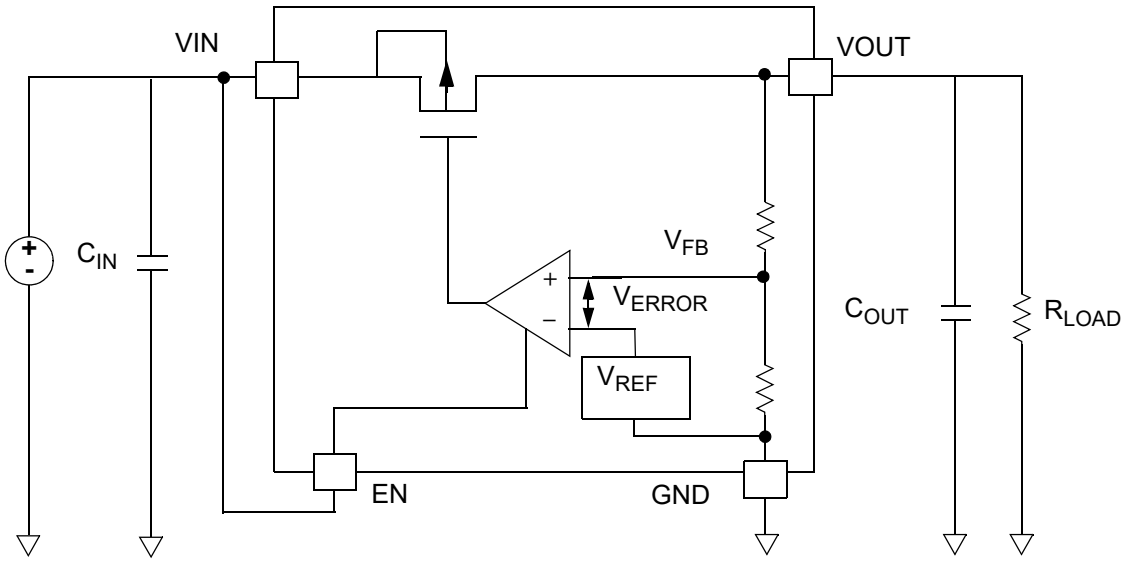


Figure 35. Simple PMOS LDO Regulator Block Diagram

The PMOS pass transistor can be modeled as a variable resistor ($r_{DS(ON)}$) that is controlled by the error amplifier to maintain a constant DC output voltage for changes in load current (I_{OUT}). Assuming the input voltage (V_{IN}) remains constant, the $r_{DS(ON)}$ is adjusted for a given I_{OUT} to set V_{OUT}. This relationship is summarized in Equation 1.

(EQ. 1) $$V_{OUT} = V_{IN} - I_{OUT} \times r_{DS(ON)}$$

V_{OUT} is set by the internal resistors.

The error amplifier compares V_{FB} with the fixed V_{REF} voltage and works to minimize the difference or error voltage between V_{FB} and V_{REF} by changing the gate voltage of the PMOS pass transistor and therefore the $r_{DS(ON)}$.

If the I_{OUT} suddenly increases because of decreased load resistance, V_{OUT} decreases because the regulator has not responded to the change and the $r_{DS(ON)}$ is set too high. V_{FB} correspondingly decreases and is below the V_{REF} voltage therefore, increasing the error voltage. The error amplifier senses and minimizes the error by driving the PMOS gate voltage more negative relative to the FET source to decrease the $r_{DS(ON)}$, which increases the output voltage bringing it back into regulation.

By similar logic, a sudden decrease in I_{OUT} because of increased load resistance causes V_{OUT} to increase because the $r_{DS(ON)}$ is set too low. V_{FB} is then higher than the fixed V_{REF} voltage increasing the error. The error amplifier senses and minimizes the error by driving the PMOS gate voltage more positive relative to the FET source to increase the $r_{DS(ON)}$, which decreases the output voltage bringing it back into regulation.

For a more detailed explanation of the DC regulation operation of a PMOS LDO regulator, see *R16AN0008: Fundamental Theory of PMOS Low-Dropout Voltage Regulators*.

6. Functional Description

6.1 UVLO

The RAA21440x family integrates an internal UVLO circuit to keep the devices safely disabled if the input voltage is below the UVLO threshold. This prevents the parts from turning on in an unpredictable state.

When the input voltage is above the UVLO threshold, the parts are enabled and the output voltage ramps up. The UVLO hysteresis prevents input voltage noise from causing the output to oscillate, and the UVLO hysteresis prevents input voltage droops because of long input traces and wires from the turning off the LDO when it turns on and draws current. Figure 36 illustrates the UVLO operation.

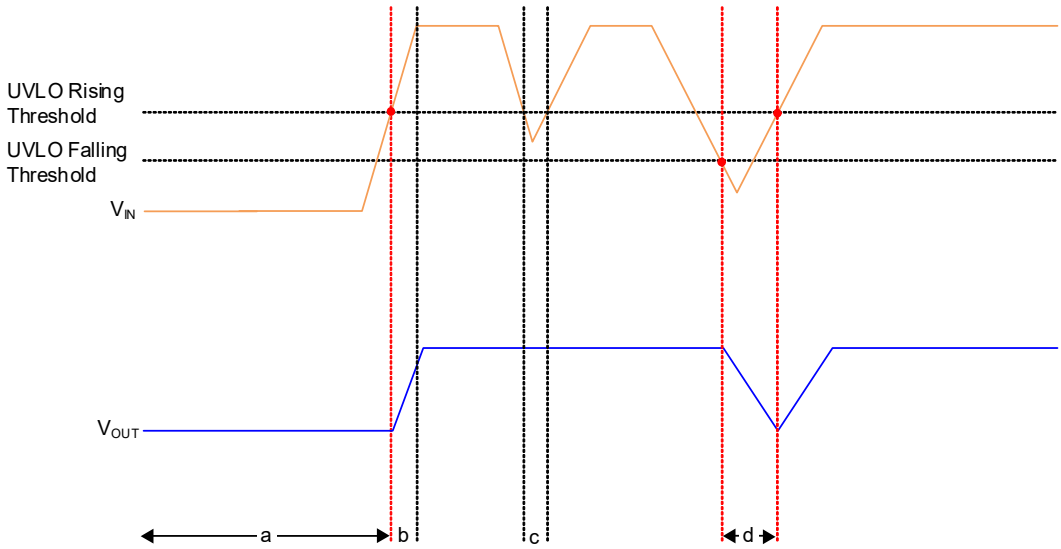


Figure 36. UVLO Operation

a, d The LDO is disabled.

b The LDO is enabled and the output starts to rise.

c The LDO remains enabled because the Input Voltage is still higher than the UVLO falling threshold.

6.2 Enable Control

The RAA21440x family in the SOT-23 package has an EN pin voltage (V_{EN}) to enable or disable the LDOs. If V_{EN} is less than the V_{EN} threshold, the LDO is disabled. If V_{EN} is greater than the V_{EN} threshold, the LDO is enabled. The V_{EN} hysteresis prevents enable voltage noise from causing the output to oscillate. When the LDO is disabled, the shutdown current is typically 0.2µA. When the LDO is enabled the quiescent current is typically 3µA to 4µA no load.

The EN pin can be directly connected to the input voltage for automatic start-up or connected to a logic controller such as an MCU of FPGA. Some logic pins use an open-collector or open-drain transistor to pull LOW and float when HIGH. Make sure to connect a 1kΩ or 10kΩ pull-up resistor to ensure proper logic HIGH. To ensure proper Enable control operation, the V_{EN} signal source should be capable of swinging above and below the threshold values. The devices also have an accurate and stable Enable threshold, which allows programming of the Enable voltage through a resistor divider.

6.3 Short-Circuit Current Limit Protection

The short-circuit protection circuitry (ILIM) limits the maximum output current that the LDO can source during fault conditions such as short-circuits or start-up inrush current. During a short-circuit fault, the LDO becomes a constant current source resulting in a decrease in load resistance that causes a decrease in the output voltage. This relationship is summarized in Equation 2.

(EQ. 2) $$V_{OUT} = ILIM \times R_{FAULT}$$

When the short or overcurrent condition is removed, the LDO returns to normal output voltage regulation. Because of the high power dissipation caused by overcurrent faults, the LDO can begin to cycle ON and OFF because the die junction temperature (T_J) is exceeding thermal fault conditions (typ +150°C) and subsequently cooling down to +130°C when the LDO is disabled.

6.4 Over-Temperature Shutdown (OTSD) Protection

The RAA21440x family is protected against thermal overloads caused by current limit protection or high ambient temperature (T_A). When the die junction temperature (T_J) exceeds typ +150°C, the thermal shutdown circuit disables the LDO reducing the output current (I_{OUT}) to 0A, therefore, reducing the output voltage (V_{OUT}) to 0V and allowing the LDO to cool. A 20°C hysteresis is included to prevent the LDO from uncontrollably heating and cooling.

Prolonged exposure to a T_J exceeding +125°C reduces the long-term stability and life of the LDO. Therefore, it is important that the design considers the T_A the LDO works in, the thermal resistance between T_J and T_A (θ_{JA}), and any fault conditions that can cause the T_J to exceed the recommended operating range. In some applications, a heat sink might be required for implementation.

6.5 Voltage Requirements

6.5.1 Input Voltage

The RAA21440x family operates with an input voltage of 4.5V to 40V on the VIN pin (3.3V output). The input supply must be able to supply enough current to keep the input voltage from drooping during load steps or high load currents.

For proper voltage regulation, the input voltage must be chosen so that it is higher than the sum of the output voltage and the maximum dropout voltage expected for a given application as expressed in Equation 3.

(EQ. 3) $$V_{IN} > V_{OUT} + V_{DROPOUT(MAX)}$$

The difference between V_{IN} and V_{OUT} required for proper regulation is commonly called the headroom voltage ($V_{HEADROOM}$).

6.6 External Capacitor Selection

The RAA21440x family is stable with 2.2µF C_{IN} and C_{OUT} capacitors. For better load transient performance, a 4.7µF or higher output capacitor is recommended.

Multilayer ceramic capacitors (MLCC) are an excellent choice because of their small size, low ESR, low ESL, and wide operating temperature; although, they are not without their problems. Ceramic capacitor values can vary with the DC bias voltage, temperature, and tolerance. Therefore, Renesas recommends using de-rated capacitors.

X5R, X7R, and C0G capacitors are recommended. To ensure the performance of the RAA21440x family, it is important that the effects of DC bias voltage, temperature, and tolerances for a chosen capacitor are evaluated. The X7R type is recommended because it has lower capacitance variation over-temperature.

Place the bypass capacitors as close as is practical to their respective pins to minimize trace inductance.

6.6.1 Input Capacitor

The minimum input capacitor that is recommended is 2.2µF to reduce the negative effects of large input impedances because of long input traces of high source impedances. Renesas recommends connecting this capacitor between VIN and GND. A larger bulk capacitor such as a 10µF might be required to be added to minimize input voltage droops during large changes in load currents, such as during load transients or start-up to not affect stability. Larger input capacitors also improve the line transient response.

6.6.2 Output Capacitor

The RAA21440x family is stable with an 2.2µF minimum output ceramic capacitor.

A large value output capacitor can help minimize the overshoot and undershoot transient response due to large changes in load current. Larger or multiple output capacitors can also be used to improve high-frequency PSRR.

6.7 Power Dissipation and Thermals

To ensure reliable operation, the die junction temperature (T_J) of the RAA21440x family must not exceed +125°C. In applications with high ambient temperature (T_A), large headroom voltages ($V_{HEADROOM}$), and large load currents (I_{OUT}), the heat dissipated in the package can become large enough to cause the T_J to exceed the maximum operating temperature of +125°C.

6.7.1 Power Dissipation

The Power Dissipation (PD) is calculated using Equation 4.

(EQ. 4) $$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_{GND}$$

Because the power dissipation contribution from the quiescent (or ground current) is typically small compared to the current, the LDO must supply to a load; it can be ignored and Equation 4 simplifies to Equation 5.

(EQ. 5) $$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Therefore, to lower the power dissipated inside the die, the $V_{HEADROOM}$ and/or the I_{OUT} can be decreased.

6.7.2 The Junction Temperature and Thermal Resistance

The junction temperature (T_J) is the sum of the environmental ambient temperature (T_A) and the temperature rise in the T_J because of power dissipation, which is calculated using Equation 6.

(EQ. 6) $$T_J = T_A + \theta_{JA} \times PD$$

θ_{JA} is the thermal resistance between the junction temperature and ambient temperature and is largely dependent on the device package and the PCB design.

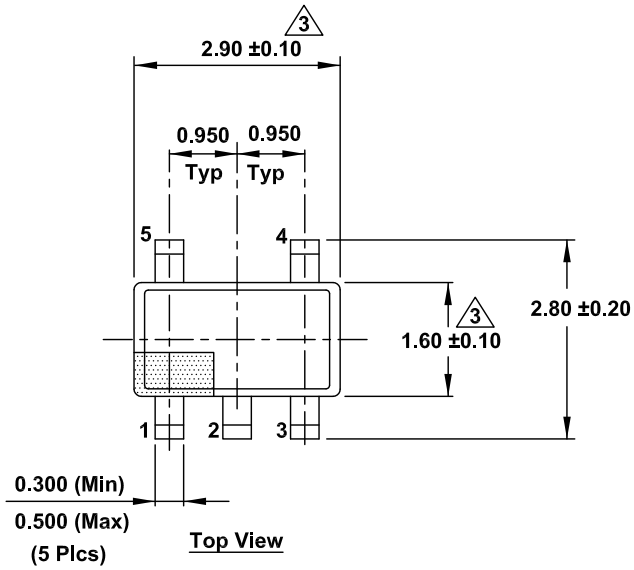
7. Layout Guidelines

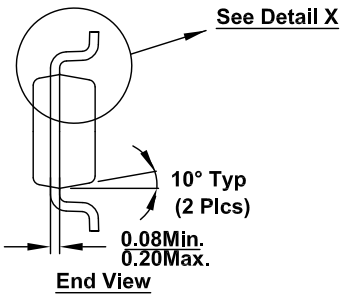
The following are recommendations for the RAA21440x to achieve optimal performance:

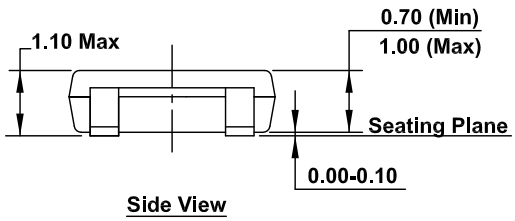
- Place all the required components for the RAA21440x on the same layer as the IC.
- Place a minimum capacitance of 2.2µF ceramic input capacitor to the VIN and GND pins of the LDO as close as practical.
- Place a minimum capacitance of 2.2µF ceramic output capacitor to the VOUT and GND pins of the LDO as close as practical.
- The package thermal EPAD is the largest heat conduction path for the package. It should be soldered to a copper pad on the PCB underneath the part. The PCB thermal pad should have as many plated vias to increase the heat flow from the package thermal EPAD to the inner PCB areas and/or the bottom PCB area. If possible, adding thermal vias around the PCB package helps improve heat spread from the package to other layers of the board.
- Keep the vias small but not so small that their inside diameter prevents solder from wicking through the holes during reflow. For efficient heat transfer, the vias must have low thermal resistance. Do not use thermal relief patterns to connect the vias. It is important to have a complete connection of the plated through-hole to each plane. The top copper GND layer, that the EPAD is connected to is the least thermally resistant path for heat flow. To this end, minimize the components and traces that cut this layer.

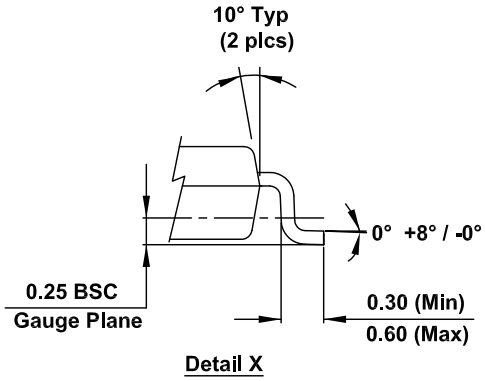
8. Package Outline Drawings

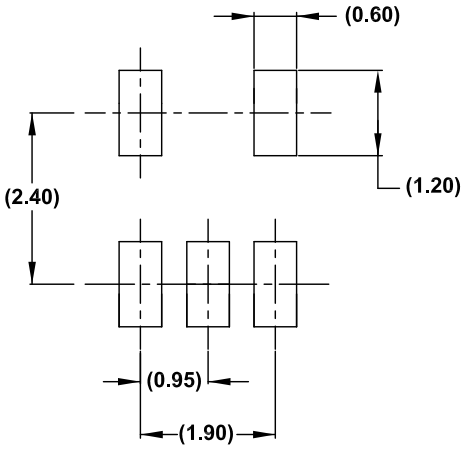
P5.064B
5 Lead Thin Small Outline Transistor (TSOT) Plastic Package
Rev 3, 2/2022







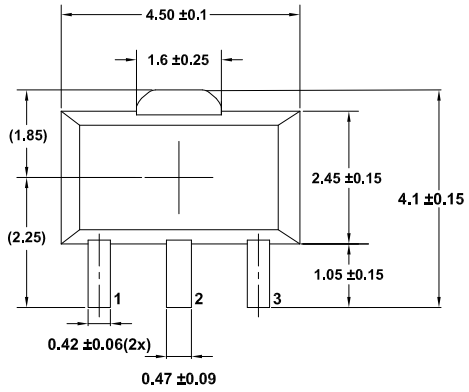




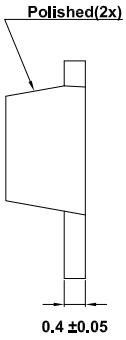
NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
2. Die is facing up for mold. Die is facing down for trim/form, that is reverse trim/form.
3. Dimensions are exclusive of mold flash and gate burr.
4. The footlength measuring is based on the gauge plane method.
5. All specifications comply to JEDEC Spec MO193 Issue C.

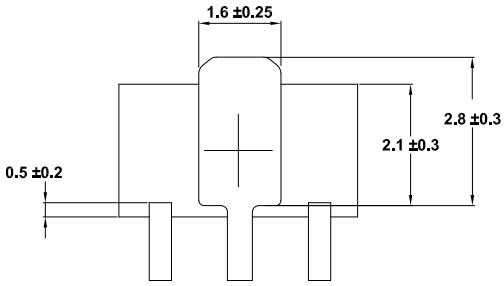
P3.064C
3 Lead Small Outline Transistor Plastic Package (SOT89-3)
Rev 1, 03/2022

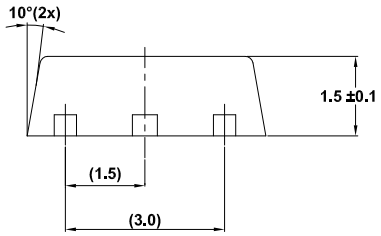


Top View

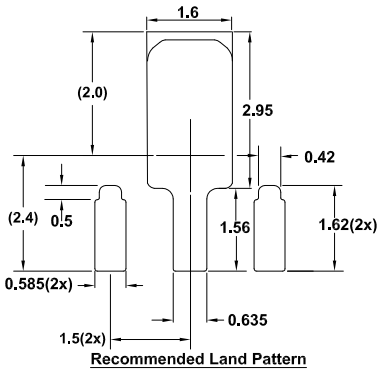


End View





Side View



Recommended Land Pattern

Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Reference: MO-178
4. JEDEC outline: TO-243 AA

9. Ordering Information

Part Number[1][2]	Part Marking[3]	Output Voltage (V)	Package Description[4] (RoHS Compliant)	Pkg. Dwg #	Carrier Type[5]	Temperature Range
RAA2144034GP3#JA0	R403	3.3	5 Ld SOT-23	P5.064B	Reel, 3k	-40°C to +125°C
RAA2144044GP3#JA0	R404	3.6				
RAA2144054GP3#JA0	R405	5				
RAA2144034GQS#GA0	R403	3.3	3 Ld SOT-89	P3.064C	Reel, 4k	
RAA2144054GQS#GA0	R405	5				
RAA2144094GQS#GA0	R409	9				
RTKA214403DE0000BU	3.3V Fixed output voltage evaluation board (SOT-23 package)					
RTKA214403DE0010BU	3.3V Fixed output voltage evaluation board (SOT-89 package)					
RTKA214404DE0000BU	3.6V Fixed output voltage evaluation board (SOT-23 package)					
RTKA214405DE0000BU	5V Fixed output voltage evaluation board (SOT-23 package)					
RTKA214405DE0010BU	5V Fixed output voltage evaluation board (SOT-89 package)					
RTKA214409DE0000BU	9V Fixed output voltage evaluation board (SOT-89 package)					

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For the Moisture Sensitivity Level (MSL) rating, see the corresponding product page, RAA214403 (3.3V), RAA214404 (3.6V), RAA214405 (5V), and RAA214409 (9V). For more information about MSL, see TB363.
3. The part marking is located on the bottom of the part.
4. For the Pb-Free reflow profile, see TB493.
5. See TB347 for details about reel specifications.

10. Revision History

Revision	Date	Description
1.00	Aug 8, 2023	Initial release

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