SLG47525/28

GreenPAK Programmable Mixed-Signal Matrix

The SLG47525/28 provides a small, low power component for commonly used Mixed-Signal functions. The user creates their circuit design by programming the one time programmable (OTP) Non-Volatile Memory (NVM) to configure the interconnect logic, the IO Pins, and the macrocells of the SLG47525/28.

This highly versatile device allows a wide variety of Mixed-Signal functions to be designed within a very small, low power single integrated circuit.

Features

- Four Analog Comparators (ACMP)
- Two Voltage References (V_{REF})
- Nineteen Combination Function Macrocells
  - Three Selectable DFF/LATCH or 2-bit LUTs
  - One Selectable Continuous DFF/LATCH or 3-bit LUT
  - Four Selectable DFF/LATCH or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
  - One Selectable Programmable Function Generator or 2-bit LUT
  - Five 8-bit Delays/Counters or 3-bit LUTs
  - Two 16-bit Delays/Counters or 4-bit LUTs
  - Two Deglitch Filters with Edge Detectors
- State Machine
  - Eight States
  - Flexible Input Logic from State Transitions
- Serial Communications
  - I^2C Protocol Compliant
- Pipe Delay – 16 Stages/3 Outputs (Part of Combination Function Macrocell)
- Programmable Delay
- Additional Logic Function
  - One Inverter
- Two Oscillators (OSC)
  - Configurable 25 kHz/2 MHz
  - 25 MHz RC Oscillator
- Power-On Reset (POR)
- Eight Byte RAM + OTP User Memory
  - RAM Memory Space that is Readable and Writable via I^2C
  - User-defined Initial Values Transferred from OTP
- Read Back Protection (Read Lock)
- Wide Range Power Supply
  - 1.71 V to 5.5 V V_{DD1}
  - 0.95 V to 1.98 V V_{DD2} ($V_{DD2} \leq V_{DD1}$)
- Operating Temperature Range: -40 °C to 85 °C
- RoHS Compliant/Halogen-Free
- Available Package
  - 20-pin STQFN: 2.0 mm x 3.0 mm x 0.55 mm, 0.4 mm pitch (SLG47528)
  - 14-pin STQFN: 2.0 mm x 2.2 mm x 0.55 mm, 0.4 mm pitch (SLG47525)

Applications

- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

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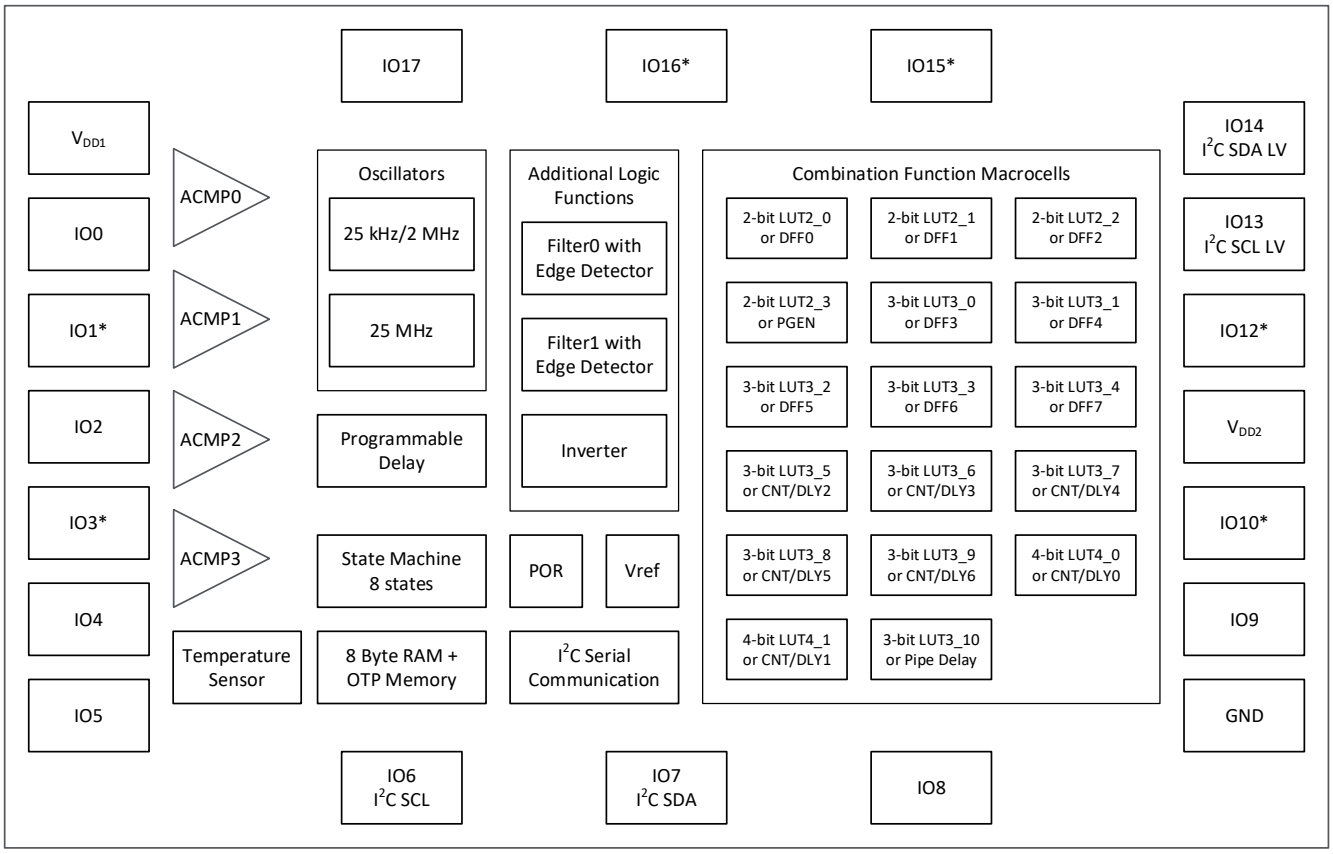
1. Overview

1.1 Block Diagram



Note*: IO1, IO3, IO10, IO12, IO15, IO16 are available in 20-pin package (SLG47528) only

Figure 1. Block Diagram

1.2 User Programmability and Customization

The SLG47525/28 is a user programmable device with one time programmable (OTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

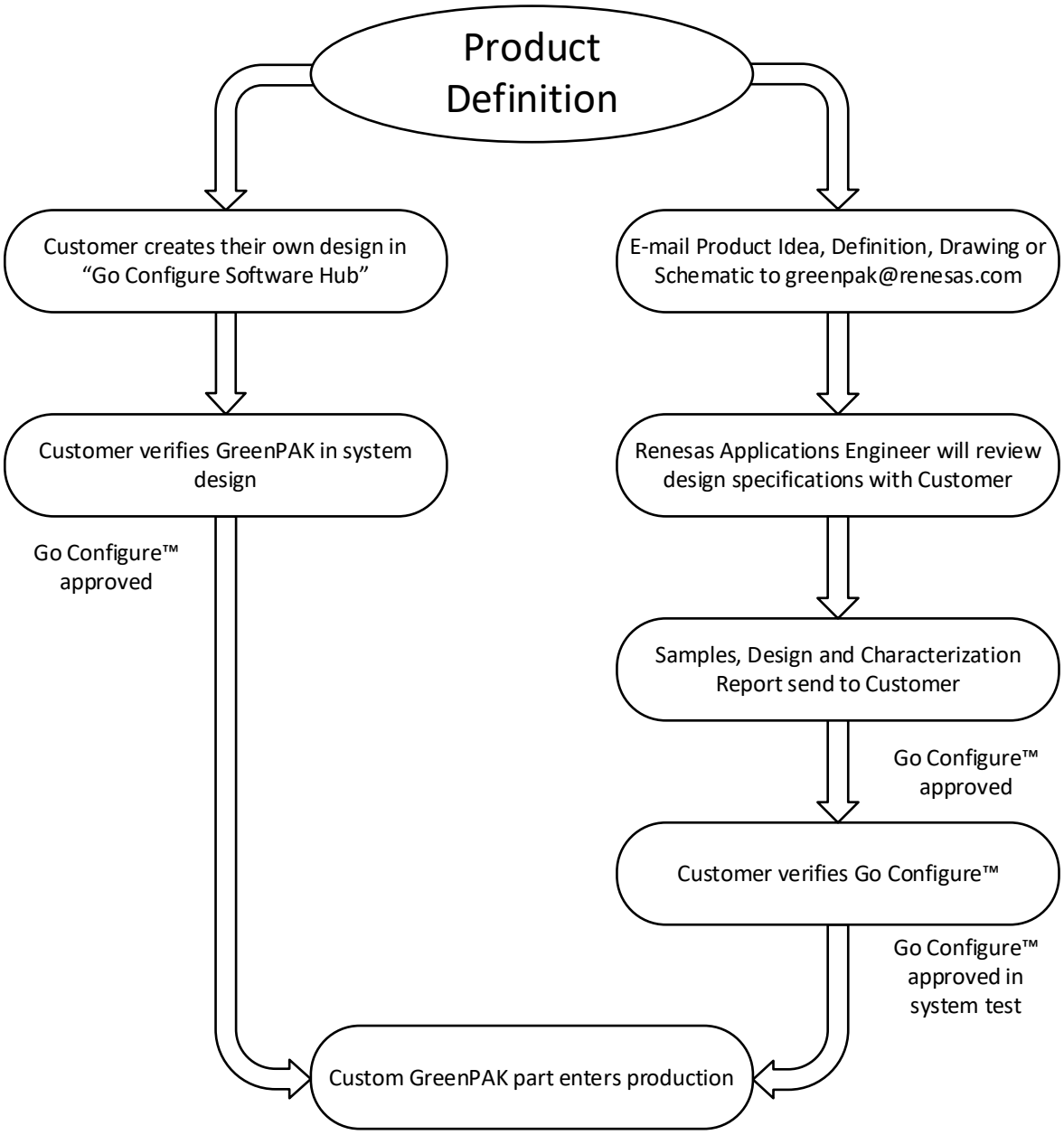


Figure 2. Device Custom Design Procedure

2. Pin Information

2.1 Pin Assignments

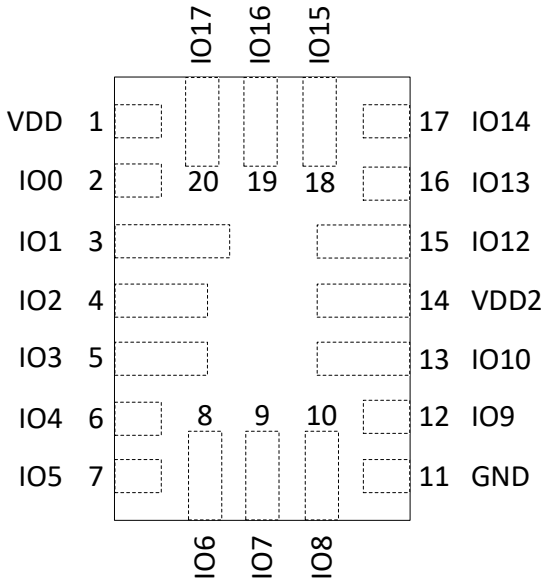


Figure 3. Pin Assignments - STQFN-20 (Top View)

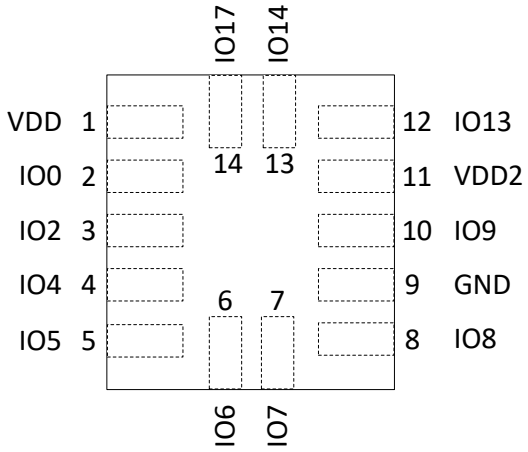


Figure 4. Pin Assignments - STQFN-14 (Top View)

2.2 Pin Descriptions

Table 1. Pin Assignments and Description

Pin Number		Pin Name	Pin Functions
STQFN-20	STQFN-14		
1	1	V_{DD1}	Power Supply 1
2	2	IO0 [1]	GPI
3	--	IO1 [1]	GPIO with OE/ACMP3+
4	3	IO2 [1]	GPIO/ACMP2+
5	--	IO3 [1]	GPIO with OE
6	4	IO4 [1]	GPIO/ACMP0+
7	5	IO5 [1]	GPIO with OE/ACMP3+/ACMP0-
8	6	IO6 [1]	GPIO/SCL
9	7	IO7 [1]	GPIO/SDA
10	8	IO8 [1]	GPIO with OE/ACMP1+
11	9	GND	GND
12	10	IO9 [2]	GPIO/ACMP0-/ACMP1-/ACMP2-/ACMP3-
13	--	IO10 [2]	GPIO with OE

Pin Number		Pin Name	Pin Functions
STQFN-20	STQFN-14		
14	11	V_{DD2}	Power Supply 2
15	--	IO12 [2]	GPIO
16	12	IO13 [2]	GPIO/SCL LV
17	13	IO14 [2]	GPIO/EXT_CLK0 / SDA LV
18	--	IO15 [2]	GPIO with OE/Vref1 out / EXT_CLK1
19	--	IO16 [2]	GPIO with OE/Vref0 out
20	14	IO17 [2]	GPIO with OE/EXT_CLK2

[1] GPIO powered from V_{DD1} domain.
[2] GPIO powered from V_{DD2} domain.

Table 2. Functional Pin Description

Pin Number		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN-20	STQFN-14					
1	1	V_{DD1}	V_{DD1}	Power Supply	-	-
2	2	IO0	IO0	General Purpose Input	Digital Input without Schmitt Trigger	-
					Digital Input with Schmitt Trigger	-
					Low Voltage Digital Input	-
3	--	IO1	IO1	General Purpose IO with OE	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	-
			ACMP3+	Analog Comparator 3 Positive Input	Analog	-
4	3	IO2	IO2	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	Open-Drain PMOS (1x) (2x)
			ACMP2+	Analog Comparator 2 Positive Input	Analog	-

Pin Number		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN-20	STQFN-14					
5	--	IO3	IO3	General Purpose IO with OE	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	-
6	4	IO4	IO4	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	Open-Drain PMOS (1x) (2x)
			ACMP0+	Analog Comparator 0 Positive Input	Analog	-
7	5	IO5	IO5	General Purpose IO with OE	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Low Voltage Digital Input	-
			ACMP3+	Analog Comparator 3 Positive Input	Analog	-
			ACMP0-	Analog Comparator 0 Negative Input	Analog	-
8	6	IO6	IO6	General Purpose IO	Digital Input without Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Digital Input with Schmitt Trigger	-
					Low Voltage Digital Input	-
			SCL	I^2C Serial Clock	Digital Input without Schmitt Trigger	Open-Drain NMOS
					Digital Input with Schmitt Trigger	Open-Drain NMOS
					Low Voltage Digital Input	Open-Drain NMOS

Pin Number		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN-20	STQFN-14					
9	7	IO7	IO7	General Purpose IO	Digital Input without Schmitt Trigger	Open-Drain NMOS (1x) (2x)
					Digital Input with Schmitt Trigger	-
					Low Voltage Digital Input	-
			SDA	I^2C Serial Data	Digital Input without Schmitt Trigger	Open-Drain NMOS
					Digital Input with Schmitt Trigger	Open-Drain NMOS
					Low Voltage Digital Input	Open-Drain NMOS
10	8	IO8	IO8	General Purpose IO with OE	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
					Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x) (4x)
					Low Voltage Digital Input	-
			ACMP1+	Analog Comparator 1 Positive Input	Analog	-
11	9	GND	GND	Ground	-	-
12	10	IO9	IO9	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull
					Digital Input with Schmitt Trigger	Open-Drain NMOS
			ACMP0-	Analog Comparator 0 Negative Input	Analog	-
			ACMP1-	Analog Comparator 1 Negative Input	Analog	-
			ACMP2-	Analog Comparator 2 Negative Input	Analog	-
			ACMP3-	Analog Comparator 3 Negative Input	Analog	-
13	--	IO10	IO10	General Purpose IO with OE	Digital Input without Schmitt Trigger	Push-Pull
					Digital Input with Schmitt Trigger	Open-Drain NMOS
14	11	V_{DD2}	V_{DD2}	Power Supply 2	-	-
15	--	IO12	IO12	General Purpose IO	Digital Input without Schmitt Trigger	Push-Pull
					Digital Input with Schmitt Trigger	Open-Drain NMOS

Pin Number		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN-20	STQFN-14					
16	12	IO13	IO13	General Purpose IO	Digital Input without Schmitt Trigger	Open-Drain NMOS
					Digital Input with Schmitt Trigger	-
			SCL LV	I^2C Serial Clock (Low Voltage)	Digital Input without Schmitt Trigger	Open-Drain NMOS
					Digital Input with Schmitt Trigger	Open-Drain NMOS
17	13	IO14	IO14	General Purpose IO	Digital Input without Schmitt Trigger	Open-Drain NMOS
					Digital Input with Schmitt Trigger	-
			EXT_CLK0	External Clock Connection 0	Digital Input without Schmitt Trigger	-
					Digital Input with Schmitt Trigger	-
			SDA LV	I^2C Serial Data (Low Voltage)	Digital Input without Schmitt Trigger	Open-Drain NMOS
					Digital Input with Schmitt Trigger	Open-Drain NMOS
18	--	IO15	IO15	General Purpose IO with OE	Digital Input without Schmitt Trigger	Push-Pull
					Digital Input with Schmitt Trigger	Open-Drain NMOS
			Vref1 out	Voltage Reference 1 Output	-	Analog
			EXT_CLK1	External Clock Connection 1	Digital Input without Schmitt Trigger	-
					Digital Input with Schmitt Trigger	-
19	--	IO16	IO16	General Purpose IO with OE	Digital Input without Schmitt Trigger	Push-Pull
					Digital Input with Schmitt Trigger	Open-Drain NMOS
			Vref0 out	Voltage Reference 0 Output	-	Analog

Pin Number		Pin Name	Signal Name	Function	Input Options	Output Options
STQFN-20	STQFN-14					
20	14	IO17	IO17	General Purpose IO with OE	Digital Input without Schmitt Trigger	Push-Pull
					Digital Input with Schmitt Trigger	Open-Drain NMOS
			EXT_CLK2	External Clock Connection 2	Digital Input without Schmitt Trigger	-
					Digital Input with Schmitt Trigger	-

3. Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Parameter		Min	Max	Unit
Supply Voltage on V_{DD1} relative to GND		-0.5	7.0	V
Supply Voltage on V_{DD2} relative to GND [1]		-0.5	2.2	V
SCL/IO6 and SDA/IO7 (powered from V_{DD1}) Pin voltage to GND		-0.5	7.0	V
SCL LV/IO13 and SDA LV/IO14 (powered from V_{DD2}) Pin voltage to GND		-0.5	2.2	V
IO0, IO1, IO2, IO3, IO4, IO5, and IO8 (GPIOs powered from V_{DD1}) Pin voltage to GND		- 0.5	V_{DD1} + 0.5, up to 7.0	V
IO9, IO10, IO12, IO15, IO16, and IO17 (GPIOs powered from V_{DD2}) Pin voltage to GND		- 0.5	V_{DD2} + 0.5, up to 2.2	V
Maximum Average or DC Current through V_{DD} Pin (Per chip side [2])	T_J = 85 °C	--	45	mA
	T_J = 110 °C	--	22	
Maximum Average or DC Current through GND Pin (Per chip side [2])	T_J = 85 °C	--	86	mA
	T_J = 110 °C	--	41	
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
	Push-Pull 2x	--	16	
	OD 1x	--	11	
	OD 2x	--	21	
	OD 4x	--	43	
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
Moisture Sensitive Level		1		

[1] $V_{DD2} \leq V_{DD1}$

[2] The GreenPAK's power rails are divided into two sides. IOs 0, 1, 2, 3, 4, 5, 6, 7, and 8 are connected to one side, IOs 9, 10, 12, 13, 14, 15, 16, and 17 to another.

3.2 Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	500	--	V

3.3 Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
Supply Voltage (V_{DD1})		1.71	5.5	V
Supply Voltage 2 (V_{DD2})		0.95	1.98	V
IO0, IO1, IO2, IO3, IO4, IO5 and IO8 (GPIOs powered from V_{DD1}) Pin voltage to GND		- 0.3	V_{DD1} + 0.3, up to 5.5	V
IO9, IO10, IO12, IO15, IO16, and IO17 (GPIOs powered from V_{DD2}) Pin voltage to GND		- 0.3	V_{DD2} + 0.3, up to 1.98	V
SCL/IO6 and SDA/IO7 (powered from V_{DD1}) I^2C Pin voltage to GND		- 0.3	5.5	V
SCL LV/IO13 and SDA LV/IO14 (powered from V_{DD2}) I^2C Pin voltage to GND		- 0.3	1.98	V
Operating Temperature (T_A)		-40	85	°C
Typical Capacitor Value at V_{DD}		0.1	--	µF

3.4 Electrical Characteristics

3.4.1. Logic IO Characteristics (Powered from V_{DD1})

V_{DD1} = 1.71 V to 5.5 V, V_{DD2} = 0.95 V to 1.98 V, T_A = -40 °C to +85 °C, Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
HIGH-Level Input Voltage IOs 1, 2, 3, 4, 5, 6, 7, 8	V_{IH1}	Logic Input [1]	0.65 x V_{DD1}	--	--	V
		Logic Input with Schmitt Trigger	0.7 x V_{DD1}	--	--	V
		Low-voltage Logic Input, V_{DD1} = 1.8 V ±5 %	0.94	--	--	V
		Low-voltage Logic Input, V_{DD1} = 3.3 V ±5 %	1.06	--	--	V
		Low-voltage Logic Input, V_{DD1} = 5.0 V ±5 %	1.15	--	--	V
LOW-Level Input Voltage IOs 1, 2, 3, 4, 5, 6, 7, 8	V_{IL1}	Logic Input [1]	--	--	0.35 x V_{DD1}	V
		Logic Input with Schmitt Trigger	--	--	0.3 x V_{DD1}	V
		Low-voltage Logic Input, V_{DD1} = 1.8 V ±5 %	--	--	0.52	V
		Low-voltage Logic Input, V_{DD1} = 3.3 V ±5 %	--	--	0.67	V
		Low-voltage Logic Input, V_{DD1} = 5.0 V ±5 %	--	--	0.72	V
Schmitt Trigger Hysteresis Voltage IOs 1, 2, 3, 4, 5, 6, 7, 8	V_{HYS1}	Logic Input with Schmitt Trigger	0.1 x V_{DD1}	--	0.4 x V_{DD1}	V

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
HIGH-Level Output Voltage IOs 1, 2, 3, 4, 5, 6, 7, 8	V_{OH1}	Push-Pull, 1x Drive, V_{DD1} = 1.8 V ±5 %, I_{OH} = 100 µA	0.988 x V_{DD1}	0.994 x V_{DD1}	--	V
		Push-Pull, 1x Drive, V_{DD1} = 3.3 V ±5 %, I_{OH} = 3 mA	0.913 x V_{DD1}	0.945 x V_{DD1}	--	V
		Push-Pull, 1x Drive, V_{DD1} = 5.0 V ±5 %, I_{OH} = 5 mA	0.922 x V_{DD1}	0.952 x V_{DD1}	--	V
		Push-Pull, 2x Drive, V_{DD1} = 1.8 V ±5 %, I_{OH} = 100 µA	0.994 x V_{DD1}	0.994 x V_{DD1}	--	V
		Push-Pull, 2x Drive, V_{DD1} = 3.3 V ±5 %, I_{OH} = 3 mA	0.957 x V_{DD1}	0.973 x V_{DD1}	--	V
		Push-Pull, 2x Drive, V_{DD1} = 5.0 V ±5 %, I_{OH} = 5 mA	0.960 x V_{DD1}	0.978 x V_{DD1}	--	V
		PMOS OD, 1x Drive, IO2, IO4, V_{DD1} = 1.8 V ±5 %, I_{OH} = 100 µA	0.988 x V_{DD1}	0.994 x V_{DD1}	--	V
		PMOS OD, 1x Drive, IO2, IO4, V_{DD1} = 3.3 V ±5 %, I_{OH} = 3 mA	0.913 x V_{DD1}	0.945 x V_{DD1}	--	V
		PMOS OD, 1x Drive, IO2, IO4, V_{DD1} = 5.0 V ±5 %, I_{OH} = 5 mA	0.924 x V_{DD1}	0.952 x V_{DD1}	--	V
		PMOS OD, 2x Drive, IO2, IO4, V_{DD1} = 1.8 V ±5 %, I_{OH} = 100 µA	0.994 x V_{DD1}	0.994 x V_{DD1}	--	V
		PMOS OD, 2x Drive, IO2, IO4, V_{DD1} = 3.3 V ±5 %, I_{OH} = 3 mA	0.957 x V_{DD1}	0.972 x V_{DD1}	--	V
		PMOS OD, 2x Drive, IO2, IO4, V_{DD1} = 5.0 V ±5 %, I_{OH} = 5 mA	0.962 x V_{DD1}	0.978 x V_{DD1}	--	V
LOW-Level Output Voltage IOs 1, 2, 3, 4, 5, 6, 7, 8	V_{OL1}	Push-Pull, 1x Drive, V_{DD1} = 1.8 V ±5 %, I_{OL}= 100 µA	--	0.006 x V_{DD1}	0.018 x V_{DD1}	V
		Push-Pull, 1x Drive, V_{DD1} = 3.3 V ±5 %, I_{OL}= 3 mA	--	0.043 x V_{DD1}	0.077 x V_{DD1}	V
		Push-Pull, 1x Drive, V_{DD1} = 5.0 V ±5 %, I_{OL}= 5 mA	--	0.042 x V_{DD1}	0.053 x V_{DD1}	V
		Push-Pull, 2x Drive, V_{DD1} = 1.8 V ±5 %, I_{OL} = 100 µA	--	0.006 x V_{DD1}	0.006 x V_{DD1}	V
		Push-Pull, 2x Drive, V_{DD1} = 3.3 V ±5 %, I_{OL} = 3 mA	--	0.020 x V_{DD1}	0.037 x V_{DD1}	V
		Push-Pull, 2x Drive, V_{DD1} = 5.0 V ±5 %, I_{OL} =5 mA	--	0.020 x V_{DD1}	0.027 x V_{DD1}	V
		NMOS OD, 1x Drive, V_{DD1} = 1.8 V ±5 %, I_{OL} = 100 µA	--	0.006 x V_{DD1}	0.012 x V_{DD1}	V
		NMOS OD, 1x Drive, V_{DD1} = 3.3 V ±5 %, I_{OL} = 3 mA	--	0.027 x V_{DD1}	0.05 x V_{DD1}	V

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
LOW-Level Output Voltage IOs 1, 2, 3, 4, 5, 6, 7, 8	V_{OL1}	NMOS OD, 1x Drive, V_{DD1} = 5.0 V ±5 %, I_{OL} = 5 mA	--	0.027 x V_{DD1}	0.036 x V_{DD1}	V
		NMOS OD, 2x Drive, V_{DD1} = 1.8 V ±5 %, I_{OL} = 100 µA	--	0.006 x V_{DD1}	0.012 x V_{DD1}	V
		NMOS OD, 2x Drive, V_{DD1} = 3.3 V ±5 %, I_{OL} = 3 mA	--	0.013 x V_{DD1}	0.027 x V_{DD1}	V
		NMOS OD, 2x Drive, V_{DD1} = 5.0 V ±5 %, I_{OL} = 5 mA	--	0.016 x V_{DD1}	0.018 x V_{DD1}	V
		NMOS OD, 4x Drive, IO8, V_{DD1} = 1.8 V ±5 %, I_{OL} = 100 µA	--	0.001 x V_{DD1}	0.001 x V_{DD1}	V
		NMOS OD, 4x Drive, IO8, V_{DD1} = 3.3 V ±5 %, I_{OL} = 3 mA	--	0.007 x V_{DD1}	0.013 x V_{DD1}	V
		NMOS OD, 4x Drive, IO8, V_{DD1} = 5.0 V ±5 %, I_{OL} = 5 mA	--	0.007 x V_{DD1}	0.011 x V_{DD1}	V
HIGH-Level Output Current [2] IOs 1, 2, 3, 4, 5, 6, 7, 8	I_{OH1}	Push-Pull, 1x Drive, V_{DD1} = 1.8 V ±5 %, V_{OH} = V_{DD1} - 0.2	1.03	1.52	--	mA
		Push-Pull, 1x Drive, V_{DD1} = 3.3 V ±5 %, V_{OH} = 2.4 V	6.05	12.08	--	mA
		Push-Pull, 1x Drive, V_{DD1} = 5.0 V ±5 %, V_{OH} = 2.4 V	22.08	34.04	--	mA
		Push-Pull, 2x Drive, V_{DD1} = 1.8 V ±5 %, V_{OH} = V_{DD1} - 0.2	2.03	2.99	--	mA
		Push-Pull, 2x Drive, V_{DD1} = 3.3 V ±5 %, V_{OH} = 2.4 V	11.54	24.16	--	mA
		Push-Pull, 2x Drive, V_{DD1} = 5.0 V ±5 %, V_{OH} = 2.4 V	41.76	68.08	--	mA
		PMOS OD, 1x Drive, IO2, IO4, V_{DD1} = 1.8 V ±5 %, V_{OH} = V_{DD1} - 0.2	1.04	1.52	--	mA
		PMOS OD, 1x Drive, IO2, IO4, V_{DD1} = 3.3 V ±5 %, V_{OH} = 2.4 V	6.05	11.18	--	mA
		PMOS OD, 1x Drive, IO2, IO4, V_{DD1} = 5.0 V ±5 %, V_{OH} = 2.4 V	22.08	31.00	--	mA
		PMOS OD, 2x Drive, IO2, IO4, V_{DD1} = 1.8 V ±5 %, V_{OH} = V_{DD1} - 0.2	2.04	3.00	--	mA
		PMOS OD, 2x Drive, IO2, IO4, V_{DD1} = 3.3 V ±5 %, V_{OH} = 2.4 V	11.52	21.84	--	mA
		PMOS OD, 2x Drive, IO2, IO4, V_{DD1} = 5.0 V ±5 %, V_{OH} = 2.4 V	41.69	60.24	--	mA

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
LOW-Level Output Current [2] IOs 1, 2, 3, 4, 5, 6, 7, 8	I_{OL1}	Push-Pull, 1x Drive, V_{DD1} = 1.8 V ±5 %, V_{OL} = 0.15 V	0.92	1.69	--	mA
		Push-Pull, 1x Drive, V_{DD1} = 3.3 V ±5 %, V_{OL} = 0.4 V	4.88	8.24	--	mA
		Push-Pull, 1x Drive, V_{DD1} = 5.0 V ±5 %, V_{OL} = 0.4 V	7.22	11.58	--	mA
		Push-Pull, 2x Drive, V_{DD1} = 1.8 V ±5 %, V_{OL} = 0.15 V	1.83	3.38	--	mA
		Push-Pull, 2x Drive, V_{DD1} = 3.3 V ±5 %, V_{OL} = 0.4 V	9.75	16.49	--	mA
		Push-Pull, 2x Drive, V_{DD1} = 5.0 V ±5 %, V_{OL} = 0.4 V	13.38	23.16	--	mA
		NMOS OD, 1x Drive, V_{DD1} = 1.8 V ±5 %, V_{OL} = 0.15 V	1.38	2.53	--	mA
		NMOS OD, 1x Drive, V_{DD1} = 3.3 V ±5 %, V_{OL} = 0.4 V	7.31	12.37	--	mA
		NMOS OD, 1x Drive, V_{DD1} = 5.0 V ±5 %, V_{OL} = 0.4 V	10.82	17.38	--	mA
		NMOS OD, 2x Drive, V_{DD1} = 1.8 V ±5 %, V_{OL} = 0.15 V	2.75	5.07	--	mA
		NMOS OD, 2x Drive, V_{DD1} = 3.3 V ±5 %, V_{OL} = 0.4 V	14.54	24.74	--	mA
		NMOS OD, 2x Drive, VDD1 = 5.0 V ±5 %, VOL = 0.4 V	17.34	34.76	--	mA
		NMOS OD, 4x Drive, IO8, V_{DD1} = 1.8 V ±5 %, V_{OL} = 0.15 V	7.13	9.00	--	mA
		NMOS OD, 4x Drive, IO8, V_{DD1} = 3.3 V ±5 %, V_{OL} = 0.4 V	31.32	41.06	--	mA
		NMOS OD, 4x Drive, IO8, V_{DD1} = 5.0 V ±5 %, V_{OL} = 0.4 V	41.06	55.18	--	mA
Pull-up or Pull-down Resistance	R_{PULL}	1 M Pull-up to V_{DD1}: V_{IN} = GND; Pull-down to GND: V_{IN} = V_{DD1}	--	1000	--	kΩ
		100 k Pull-up to V_{DD1}: V_{IN} = GND; Pull-down to GND: V_{IN} = V_{DD1}	--	100	--	kΩ
		10 k Pull-up to V_{DD1}: V_{IN} = GND; Pull-down to GND: V_{IN} = V_{DD1}	--	10	--	kΩ
Input Leakage Current for Each IO Pin IOs 1, 2, 3, 4, 5, 6, 7, 8	I_{LKG1}	Absolute Value	--	1	1000	nA
Startup Time	t_{SU}	From V_{DD} rising past PON_{THR}	0.21	1.23	1.83	ms
Power-On Threshold	PON_{THR}	V_{DD} Level required to start up the device	1.39	1.54	1.70	V

Parameter	Symbol	Condition/Note	Min	Typ	Max	Unit
Power-Off Threshold	$POFF_{THR}$	V_{DD} Level required to switch off the device	0.88	1.17	1.40	V

[1] No hysteresis.
[2] DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

3.4.2. Low-voltage Logic IO Characteristics (Powered from V_{DD2})

V_{DD1} = 1.71 V to 5.5 V, V_{DD2} = 0.95 V to 1.98 V, T_A = -40 °C to +85 °C, Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
HIGH-Level Input Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	V_{IH2}	Logic Input [1]	0.65 x V_{DD2}	--	--	V
		Logic Input with Schmitt Trigger	0.7 x V_{DD2}	--	--	V
LOW-Level Input Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	V_{IL2}	Logic Input [1]	--	--	0.35 x V_{DD2}	V
		Logic Input with Schmitt Trigger	--	--	0.3 x V_{DD2}	V
Positive Going Threshold Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	V_{TP2}	Logic Input with Schmitt Trigger	0.4 x V_{DD2}	--	0.7 x V_{DD2}	V
Negative Going Threshold Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	V_{TN2}	Logic Input with Schmitt Trigger	0.3 x V_{DD2}	--	0.6 x V_{DD2}	V
Schmitt Trigger Hysteresis Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	V_{HYS2}	Logic Input with Schmitt Trigger	0.1 x V_{DD2}	--	0.4 x V_{DD2}	V
HIGH-Level Output Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	V_{OH2}	Push-Pull, V_{DD2} = 1.2 V ± 0.1 V, I_{OH} = 2 mA	0.8 x V_{DD2}	0.969 x V_{DD2}	--	V
		Push-Pull, V_{DD2} = 1.8 V ± 0.15V, I_{OH} = 2 mA	0.8 x V_{DD2}	0.984 x V_{DD2}	--	V
LOW-Level Output Voltage IOs 9, 10, 12, 13, 14, 15, 16, 17	V_{OL2}	Push-Pull, V_{DD2} = 1.2 V ± 0.1 V, I_{OL} = 2 mA	--	0.015 x V_{DD2}	0.2 x V_{DD2}	V
		Push-Pull, V_{DD2} = 1.8 V ± 0.15V, I_{OL} = 2 mA	--	0.011 x V_{DD2}	0.2 x V_{DD2}	V
		NMOS OD, V_{DD2} = 1.2 V ± 0.1 V, I_{OL} = 2 mA	--	0.015 x V_{DD2}	0.2 x V_{DD2}	V
		NMOS OD, V_{DD2} = 1.8 V ± 0.15V, I_{OL} = 2 mA	--	0.011 x V_{DD2}	0.2 x V_{DD2}	V
HIGH-Level Output Current [2] IOs 9, 10, 12, 13, 14, 15, 16, 17	I_{OH2}	Push-Pull, V_{DD2} = 1.2 V ± 0.1 V, V_{OH2} = 0.7 x V_{DD2}	9.00	14.02	--	mA
		Push-Pull, V_{DD2} = 1.8 V ± 0.15 V, V_{OH2} = 0.7 x V_{DD2}	19.90	32.64	--	mA

Parameter	Symbol	Condition	Min	Typ	Max	Unit
LOW-Level Output Current [2] IOs 9, 10, 12, 13, 14, 15, 16, 17	I_{OL2}	Push-Pull, NMOS OD, V_{DD2} = 1.2 V ± 0.1 V, V_{OL} = 0.3 x V_{DD2}	14.20	23.07	--	mA
		Push-Pull, NMOS OD, V_{DD2} = 1.8 V ± 0.15 V, V_{OL} = 0.3 x V_{DD2}	26.25	49.27	--	mA
Pull-up or Pull-down Resistance	R_{PULL}	500k Pull-up to V_{DD2}, V_{IN} = GND; Pull-down to GND, V_{IN} = V_{DD2}	--	500	--	kΩ
		100k Pull-up to V_{DD2}, V_{IN} = GND; Pull-down to GND, V_{IN} = V_{DD2}	--	100	--	kΩ
		10k Pull-up to V_{DD2}, V_{IN} = GND; Pull-down to GND, V_{IN} = V_{DD2}	--	10	--	kΩ
Input Capacitance for each IO Pin	C_{IN}		--	4	--	pF
Input Leakage Current for Each IO Pin IOs 9, 10, 12, 13, 14, 15, 16, 17	I_{LKG2}	Absolute Value	--	1.4	500	nA
Power-On Threshold of V_{DD2} Detector	PON_{TVDET}	V_{DD2} Level Required to Start Up the Pins Powered from V_{DD2}	0.32	0.48	0.66	V
Power-Off Threshold of V_{DD2} Detector	$POFF_{TVDET}$	V_{DD2} Level Required to Switch Off the Pins Powered from V_{DD2}	0.29	0.46	0.63	V

[1] No hysteresis.
[2] DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

3.4.3. I²C Pins Characteristics (Powered from V_{DD1})

V_{DD1} = 1.71 V to 5.5 V, V_{DD2} = 0.95 V to 1.98 V, T_A = -40 °C to +85 °C, Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Condition	Fast-Mode		Unit
			Min	Max	
LOW-Level Input Voltage	V_{IL}	Logic Input [1]	--	0.35 x V_{DD1}	V
		Logic Input with Schmitt Trigger	--	0.3 x V_{DD1}	V
HIGH-Level Input Voltage	V_{IH}	Logic Input [1]	0.65 x V_{DD1}	--	V
		Logic Input with Schmitt Trigger	0.7 x V_{DD1}	--	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	Logic Input with Schmitt Trigger	0.05 x V_{DD1}	--	V
LOW-Level Output Voltage 1	V_{OL1}	Open-Drain at 3 mA sink current V_{DD1} > 2 V	0	0.4	V
LOW-Level Output Voltage 2	V_{OL2}	Open-Drain at 2 mA sink current V_{DD1} ≤ 2 V	0	0.2 x V_{DD1}	V

Parameter	Symbol	Condition	Fast-Mode		Unit
			Min	Max	
LOW-Level Output Current	I_{OL}	V_{OL} = 0.4 V	3	--	mA
		V_{OL} = 0.6 V	6	--	mA
Output Fall Time from V_{IHmin} to V_{ILmax}	t_{of}		--	250	ns
Pulse Width of Spikes That Must be Suppressed by the Input Filter	t_{SP}	SDA line	0	50	ns
		SCL line	0	30 [2]	
Input Current Each IO Pin	I_i	0.1 x V_{DD1} < V_I < 0.9 x V_{DD1max}	-10	+10	µA
Capacitance for Each IO Pin	C_i		--	10	pF

[1] No hysteresis. Does not meet standard I^2C specifications: the inputs of Fast-mode devices incorporate spike suppression and a Schmitt trigger at the SDA and SCL inputs.
[2] Does not meet standard I2C specifications: pulse width of spikes that must be suppressed by the input filter – 50 ns.

3.4.4. Low-Voltage I^2C Pins Characteristics (Powered from V_{DD2})

V_{DD1} = 1.71 V to 5.5 V, V_{DD2} = 0.95 V to 1.98 V, T_A = -40 °C to +85 °C, Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Condition	Fast-Mode		Unit
			Min	Max	
LOW-Level Input Voltage	V_{IL}	Logic Input [1]	--	0.35 x V_{DD2}	V
		Logic Input with Schmitt Trigger	--	0.3 x V_{DD2}	V
HIGH-Level Input Voltage	V_{IH}	Logic Input [1]	0.65 x V_{DD2}	1.98	V
		Logic Input with Schmitt Trigger	0.7 x V_{DD2}	1.98	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	Logic Input with Schmitt Trigger	0.05 x V_{DD2}	--	V
LOW-Level Output Voltage 2	V_{OL2}	Open-Drain at 2 mA sink current V_{DD2} ≤ 2 V	0	0.2 x V_{DD2}	V
LOW-Level Output Current	I_{OL}	V_{OL} = 0.4 V	3	--	mA
		V_{OL} = 0.6 V	6	--	mA
Output Fall Time from V_{IHmin} to V_{ILmax}	t_{of}		--	250	ns
Pulse Width of Spikes That Must be Suppressed by the Input Filter	t_{SP}	SDA line	0	50	ns
		SCL line	0	30 [2]	
Input Current Each IO Pin	I_i	0.1 x V_{DD2} < V_I < 0.9 x V_{DD2max}	-10	+10	µA
Capacitance for Each IO Pin	C_i		--	10	pF

[1] No hysteresis. Does not meet standard I^2C specifications: the inputs of Fast-mode devices incorporate spike suppression and a Schmitt trigger at the SDA and SCL inputs.
[2] Does not meet standard I2C specifications: pulse width of spikes that must be suppressed by the input filter – 50 ns.

3.4.5. I²C Pins Timing Characteristics

V_{DD1} = 1.71 V to 5.5 V, V_{DD2} = 0.95 V to 1.98 V, T_A = -40 °C to +85 °C, Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Condition	Fast-Mode		Unit
			Min	Max	
Clock Frequency, SCL	f_{SCL}		--	400	kHz
Clock Pulse Width Low	t_{LOW}		1300	--	ns
Clock Pulse Width High	t_{HIGH}		600	--	ns
Start Hold Time	t_{HD_STA}		600	--	ns
Set-up Time for a Repeated START Condition	t_{SU_STA}		600	--	ns
Data Hold Time	t_{HD_DAT}		0	--	ns
Data Set-up Time	t_{SU_DAT}		100	--	ns
Rise Time of Both SDA and SCL Signals	t_R		--	300	ns
Fall Time of Both SDA and SCL Signals	t_F		--	300	ns
Set-up Time for STOP Condition	t_{SU_STO}		600	--	ns
Bus Free Time between STOP and START Condition	t_{BUF}		1300	--	ns
Capacitive Load for Each Bus Line	C_b		--	400	pF
Data Valid Time	t_{VD_DAT}		--	900	ns
Data Valid Acknowledge Time	t_{VD_ACK}		--	900	ns

3.4.6. Estimated Typical Current of Macrocell Configurations

V_{DD2} = 0.95 V to 1.98 V, Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Note	V_{DD1} = 1.8 V	V_{DD1} = 3.3 V	V_{DD1} = 5.0 V	Unit
Current	I_{DD}	Device Quiescent Current, I_{DD1}	0.33	0.64	1.00	µA
		Device Quiescent Current, I_{DD2}	0.02	0.02	0.02	µA
		OSC 2 MHz, Pre-divider = 1	41.48	64.00	94.89	µA
		OSC 2 MHz, Pre-divider = 8	25.68	32.41	43.22	µA
		OSC 25 kHz, Pre-divider = 1	7.16	7.94	9.25	µA
		OSC 25 kHz, Pre-divider = 8	6.97	7.60	8.68	µA
		OSC 25 MHz, Pre-divider = 1	87.25	238.27	428.66	µA
		OSC 25 MHz, Pre-divider = 1, Force On	87.25	238.27	428.67	µA
		OSC 25 MHz, Pre-divider = 8	78.01	212.45	390.17	µA
		ACMP (each)	54.96	52.64	60.81	µA
		ACMP with buffer (each)	75.06	72.74	81.25	µA
		V_{REF} (each)	49.70	47.32	55.60	µA
		V_{REF} with buffer (each)	71.93	71.27	79.62	µA

3.4.7. Estimated Typical Delay of Each Macrocell (Powered from V_{DD1})

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Note	V_{DD1} = 1.8 V		V_{DD1} = 3.3 V		V_{DD1} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
GPIO Macrocell (powered from V_{DD1})									
Delay	t_{PD}	Digital Input to PP 1x	42	45	17	19	12	13	ns
Delay	t_{PD}	Digital Input with Schmitt Trigger to PP 1x	42	43	16	17	18	12	ns
Delay	t_{PD}	Low Voltage Digital input to PP 1x	45	428	17	177	12	120	ns
Delay	t_{PD}	Digital input to PMOS output	42	--	17	--	12	--	ns
Delay	t_{PD}	Digital input to NMOS output	--	80	--	27	--	18	ns
Delay	t_{PD}	Output enable from pin, OE Hi-Z to 1	53	--	21	--	15	--	ns
Delay	t_{PD}	Output enable from pin, OE Hi-Z to 0	50	--	20	--	14	--	ns
Combination Function Macrocell									
Delay	t_{PD}	LUT 2-bit (LATCH)	34	33	14	13	10	9	ns
Delay	t_{PD}	LATCH (LUT 2-bit)	30	34	14	13	10	9	ns
Delay	t_{PD}	LUT 3-bit (LATCH)	38	37	18	15	13	10	ns
Delay	t_{PD}	LATCH + nRESET (LUT 3-bit)	45	42	21	17	15	12	ns
Delay	t_{PD}	LUT 4-bit	28	33	14	13	10	9	ns
Delay	t_{PD}	LUT 2-bit	19	26	10	10	7	7	ns
Delay	t_{PD}	LUT 3-bit	28	34	14	13	10	9	ns
Delay	t_{PD}	CNT/DLY Logic	40	38	18	15	13	11	ns
Programmable Delay Macrocell									
Delay	t_{PD}	P_DLY1C	367	356	165	160	123	119	ns
Delay	t_{PD}	P_DLY2C	720	718	314	312	233	231	ns
Delay	t_{PD}	P_DLY3C	1061	1060	462	460	343	341	ns
Delay	t_{PD}	P_DLY4C	1396	1400	609	609	451	451	ns
Deglitch Filter Macrocell									
Delay	t_{PD}	Filter0	202	213	97	101	71	73	ns
Delay	t_{PD}	Filter1	152	160	71	74	51	53	ns
Other Macrocells									
Delay	t_{PD}	ACMP (5 mV overdrive, IN- = 600 mV)	3000	3000	2000	2000	2000	2000	ns
Pulse Width	t_W	IO with 1x push-pull (min transmitted)	20	20	20	20	20	20	ns
Pulse Width	t_W	Filter0 (min transmitted)	156	171	79	84	58	62	ns
Pulse Width	t_W	Filter1 (min transmitted)	106	118	52	57	38	42	ns

3.4.8. Estimated Typical Delay of Each Macrocell (Powered from V_{DD2})

V_{DD1} = 1.71 V to 5.5 V, Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Note	V_{DD2} = 0.95 V		V_{DD2} = 1.2 V		V_{DD2} = 1.5 V		V_{DD2} = 1.8 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	Rising	Falling	
GPIO Macrocell (powered from V_{DD2})											
Delay	t_{PD}	Digital Input to PP	22	24	20	22	19	21	17	19	ns
Delay	t_{PD}	Digital Input with Schmitt Trigger to PP	22	25	20	22	19	21	17	19	ns
Delay	t_{PD}	Digital Input to NMOS	--	24	--	22	--	21	--	19	ns
Delay	t_{PD}	Output enable from Pin, OE Hi-Z to 1	25	--	23	--	22	--	20	--	ns
Delay	t_{PD}	Output enable from Pin, OE Hi-Z to 0	25	--	23	--	22	--	20	--	ns
Delay	t_{PD}	PP 3 State Hi-Z to 1	25	--	23	--	22	--	20	--	ns
Delay	t_{PD}	PP 3 State Hi-Z to 0	25	--	23	--	22	--	20	--	ns

3.4.9. Maximum Operating Frequency on GPIO

V_{DD1} = 1.71 V to 5.5 V, V_{DD2} = 0.95 V to 1.98 V, T_A = -40 °C to +85 °C, Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
External OSC Frequency Input to PAD	F_{OSC_EXT}		--	80	--	MHz
Internal OSC Frequency Output to PAD	F_{OSC_INT}	C_{PAD} = 12 pF, V_{DD1}≥2.5V [1]	25	--	--	MHz

[1] 25 MHz RC OSC1 performance is not guaranteed at V_{DD} < 2.5 V.

3.4.10. Typical Counter/Delay Offset

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	OSC Frequency	OSC Power Control	V_{DD1} = 1.8 V	V_{DD1} = 3.3 V	V_{DD1} = 5.0 V	Unit
Offset (Power-On Delay)	25 kHz	auto	1.6	1.6	1.6	µs
Offset (Power-On Delay), Fast Start	25 kHz	auto	2.1	2.1	2.1	µs
Offset (Power-On Delay)	2 MHz	auto	0.4	0.2	0.2	µs
Offset (Power-On Delay), Fast Start	2 MHz	auto	0.7	0.5	0.4	µs
Offset (Power-On Delay)	25 MHz	auto	0.01	0.05	0.04	µs
Frequency Settling Time	25 kHz	auto	19	14	12	µs
	2 MHz	auto	14	14	14	

Parameter	OSC Frequency	OSC Power Control	V_{DD1} = 1.8 V	V_{DD1} = 3.3 V	V_{DD1} = 5.0 V	Unit
Variable (CLK Period)	25 kHz	forced	0 - 40	0 - 40	0 - 40	µs
	2 MHz	forced	0 - 0.5	0 - 0.5	0 - 0.5	
	25 MHz		0 - 0.04	0 - 0.04	0 - 0.04	
T_{PD} (Non-Delayed Edge)	25 kHz/2 MHz	either	35	14	10	ns

3.4.11. Programmable Delay Expected Typical Delays and Pulse Width

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Note	V_{DD1} = 1.8 V	V_{DD1} = 3.3 V	V_{DD1} = 5.0 V	Unit
Pulse Width, 1 cell	t_W	mode: (any) edge detect, edge detect output	296	135	101	ns
Pulse Width, 2 cell	t_W	mode: (any) edge detect, edge detect output	597	272	203	ns
Pulse Width, 3 cell	t_W	mode: (any) edge detect, edge detect output	898	410	305	ns
Pulse Width, 4 cell	t_W	mode: (any) edge detect, edge detect output	1195	546	407	ns
Delay, 1 cell	time1	mode: (any) edge detect, edge detect output	55	24	18	ns
Delay, 2 cell	time1	mode: (any) edge detect, edge detect output	55	24	18	ns
Delay, 3 cell	time1	mode: (any) edge detect, edge detect output	55	24	18	ns
Delay, 4 cell	time1	mode: (any) edge detect, edge detect output	55	24	18	ns
Delay, 1 cell	time2	mode: both edge delay, edge detect output	367	165	106	ns
Delay, 2 cell	time2	mode: both edge delay, edge detect output	667	300	193	ns
Delay, 3 cell	time2	mode: both edge delay, edge detect output	968	440	279	ns
Delay, 4 cell	time2	mode: both edge delay, edge detect output	1265	575	365	ns

3.4.12. Typical Filter Rejection Pulse Width

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	V_{DD1} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered Pulse Width for Filter 0	< 157	< 77	< 55	ns
Filtered Pulse Width for Filter 1	< 106	< 51	< 36	ns

3.4.13. Asynchronous State Machine (ASM) Specifications

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Asynchronous State Machine Output Delay Time	$t_{st\_out\_delay}$	V_{DD1} = 1.8 V ± 5 %	104	--	213	ns
		V_{DD1} = 3.3 V ± 10 %	44	--	89	
		V_{DD1} = 5.0 V ± 10 %	32	--	58	

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Asynchronous State Machine Output Transition Time	t_{st_out}	V_{DD1} = 1.8 V ± 5 %	--	--	165	ns
		V_{DD1} = 3.3 V ± 10 %	--	--	70	
		V_{DD1} = 5.0 V ± 10 %	--	--	45	
Asynchronous State Machine Input Pulse Acceptance Time	t_{st_pulse}	V_{DD1} = 1.8 V ± 5 %	14	--	--	ns
		V_{DD1} = 3.3 V ± 10 %	6	--	--	
		V_{DD1} = 5.0 V ± 10 %	5	--	--	
Asynchronous State Machine Input Compete Time	t_{st_comp}	V_{DD1} = 1.8 V ± 5 %	--	--	20	ns
		V_{DD1} = 3.3 V ± 10 %	--	--	8	
		V_{DD1} = 5.0 V ± 10 %	--	--	5	

3.5 Oscillator Characteristics

3.5.1. 25 kHz RC OSC0 Frequency

Power Supply Range (V_{DD1}) V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5 %	23.792	26.288	23.275	27.089	21.728	29.173
3.3 V ±10 %	24.473	25.526	23.357	26.028	23.357	27.002
5 V ±10 %	24.316	25.939	23.309	26.177	23.309	27.181
2.5 V to 4.5 V	24.438	25.559	23.336	26.051	23.336	27.038
1.71 V to 5.5 V	23.354	26.670	22.828	27.483	21.301	29.545

3.5.2. 25 kHz RC OSC0 Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD1}) V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5 %	-4.83	5.15	-6.90	8.36	-13.09	16.69
3.3 V ±10 %	-2.11	2.10	-6.57	4.11	-6.57	8.01
5 V ±10 %	-2.73	3.76	-6.76	4.71	-6.76	8.72
2.5 V to 4.5 V	-2.25	2.24	-6.66	4.21	-6.66	8.15
1.71 V to 5.5 V	-6.58	6.68	-8.69	9.93	-14.80	18.18

3.5.3. 2 MHz RC OSC0 Frequency

Power Supply Range (V_{DD1}) V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5 %	1.915	2.062	1.832	2.103	1.810	2.144
3.3 V ±10 %	1.937	2.070	1.858	2.132	1.813	2.145
5 V ±10 %	1.894	2.233	1.853	2.270	1.767	2.270
2.5 V to 4.5 V	1.907	2.124	1.836	2.171	1.784	2.171
1.71 V to 5.5 V	1.760	2.274	1.706	2.305	1.629	2.305

3.5.4. 2 MHz RC OSC0 Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD1}) V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5 %	-4.26	3.12	-8.38	5.17	-9.50	7.20
3.3 V ±10 %	-3.14	3.49	-7.10	6.58	-9.33	7.24
5 V ±10 %	-5.31	11.66	-7.37	13.50	-11.67	13.50
2.5 V to 4.5 V	-4.65	6.18	-8.22	8.57	-10.81	8.57
1.71 V to 5.5 V	-12.01	13.72	-14.69	15.23	-18.57	15.23

3.5.5. 25 MHz RC OSC1 Frequency

Power Supply Range (V_{DD1}) V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
2.5 V ±10 %	22.316	27.220	21.771	27.572	21.771	27.912
3.3 V ±10 %	23.430	26.220	22.389	26.679	22.389	27.014
5 V ±10 %	23.289	26.651	22.500	27.305	22.500	27.486
2.5 V to 4.5 V	23.383	26.220	20.725	26.679	20.725	27.014
1.71 V to 5.5 V	12.643	26.220	12.203	26.679	11.317	27.014

3.5.6. 25 MHz RC OSC1 Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD1}) V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±10 %	-10.73	8.88	-12.92	10.29	-12.92	11.65
3.3 V ±10 %	-6.28	4.88	-10.44	6.72	-10.44	8.06
5 V ±10 %	-6.84	6.61	-10.00	9.22	-10.00	9.95
2.5 V to 4.5 V	-14.47	4.88	-17.10	6.72	-17.10	8.06
1.71 V to 5.5 V	-49.43	4.88	-51.19	6.72	-54.73	8.06
[1] 25 MHz RC OSC1 performance is not guaranteed at V_{DD} < 2.5 V.						

3.5.7. Oscillators Power-On Delay

T_A = +25 °C, unless otherwise specified. DLY/CNT Counter data = 100, RC OSC power setting: "Auto Power-On", RC OSC clock to matrix input: "Enable".

Power Supply Range (V_{DD1}) V	RC OSC0 2 MHz		RC OSC0 25 kHz		RC OSC1 25 MHz	
	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs	Typical Value, ns	Maximum Value, ns
1.71	602	644	0.63	0.67	127	164
1.80	581	615	0.61	0.64	115	132
1.89	564	593	0.59	0.62	105	119
2.25	521	546	1.54	18.35	80	99
2.50	503	522	2.95	22.09	70	82
2.75	490	507	5.30	17.35	64	70
3.00	480	496	5.16	13.87	60	65
3.30	469	485	4.13	14.10	57	61
3.60	460	475	1.58	11.02	54	57
4.00	450	465	1.10	2.05	51	54
5.00	430	445	1.77	2.14	45	47
5.50	422	436	1.78	2.16	43	45

3.5.8. Oscillators Power-On Delay (Fast Start-up Time Mode)

T_A = +25 °C, unless otherwise specified. DLY/CNT Counter data = 100, RC OSC power setting: "Auto Power-On", RC OSC clock to matrix input: "Enable", Fast Start-up Time Mode.

Power Supply Range (V_{DD1}) V	RC OSC0 2 MHz		RC OSC0 25 kHz	
	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs
1.71	559	594	10.72	20.86
1.80	544	573	10.69	20.86
1.89	532	557	10.66	20.85
2.25	568	832	10.59	20.79
2.50	642	830	10.57	20.84
2.75	644	880	12.56	31.66
3.00	642	898	15.18	65.66
3.30	643	925	20.27	21.91
3.60	646	961	20.37	21.07
4.00	651	1011	20.38	21.17
5.00	679	1114	20.72	21.44
5.50	661	1047	20.65	21.50

3.6 Analog Comparator Characteristics

3.6.1. ACMP Characteristics

V_{DD1} = 1.71 V to 5.5 V, T_A = -40 °C to +85 °C, Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Description/Note	Conditions	Min	Typ	Max	Unit
ACMP Input Voltage Range	V_{ACMP}	Positive Input		0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
ACMP Input Offset Voltage	V_{Offset}	Low Bandwidth - Enable, V_{HYS} = 0 mV, Gain = 1, V_{REF} = 50 mV to 1200 mV	T = 25 °C	-9.1	--	8.4	mV
			T = -40 °C to 85 °C	-10.9	--	10.9	mV
		Low Bandwidth - Disable, V_{HYS} = 0 mV, Gain =1, V_{REF} = 50 mV to 1200 mV	T = 25 °C	-7.5	--	7.2	mV
			T = -40 °C to 85 °C	-10.7	--	10.5	mV

Parameter	Symbol	Description/Note	Conditions	Min	Typ	Max	Unit
ACMP Start Time	t_{Start}	ACMP Power-On Delay, Minimal Required Wake Time for the "Wake and Sleep function", Regulator and Charge Pump Set to Automatic ON/OFF	BG = 550 µs, T = 25 °C	--	609.7	862.2	µs
			BG = 550 µs, T = -40 °C to 85 °C	--	675.0	1028.8	µs
			BG = 100 µs, T = 25 °C V_{DD} = 2.7 V to 5.5 V	--	132.4	176.2	µs
			BG = 100 µs, T = -40 °C to 85 °C V_{DD} = 2.7 V to 5.5 V	--	149.4	213.5	µs
		ACMP Power-On Delay, Minimal Required Wake Time for the "Wake and Sleep function", Regulator and Charge Pump Always OFF	BG = 550 µs, T = 25 °C V_{DD} = 3.0 V to 5.5 V	--	609.5	862.0	µs
			BG = 550 µs, T = -40 °C to 85 °C V_{DD} = 3.0 V to 5.5 V	--	674.6	1027.5	µs
			BG = 100 µs, T = 25 °C V_{DD} = 3.0 V to 5.5 V	--	131.6	176.0	µs
			BG = 100 µs, T = -40 °C to 85 °C V_{DD} = 3.0 V to 5.5 V	--	149.2	213.3	µs
Built-in Hysteresis	V_{HYS}	V_{HYS} = 25 mV V_{IL} = Vin - V_{HYS}/2 V_{IH} = Vin + V_{HYS}/2	LB - Enabled, T = 25 °C	7.32	--	35.5	mV
			LB - Disabled, T = 25 °C	10.0	--	38.5	mV
		V_{HYS} = 50 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = 25 °C	42.9	--	57.8	mV
			LB - Disabled, T = 25 °C	44.2	--	54.3	mV
		V_{HYS} = 200 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = 25 °C	192.7	--	208.7	mV
			LB - Disabled, T = 25 °C	193.3	--	204.8	mV
		V_{HYS} = 25 mV V_{IL} = Vin - V_{HYS}/2 V_{IH} = Vin + V_{HYS}/2	LB - Enabled, T = -40 °C to +85 °C	0.0	--	58.0	mV
			LB - Disabled, T = -40 °C to +85 °C	0.0	--	52.9	mV
		V_{HYS} = 50 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = -40 °C to +85 °C	22.5	--	86.9	mV
			LB - Disabled, T = -40 °C to +85 °C	29.2	--	76.5	mV

Parameter	Symbol	Description/Note	Conditions	Min	Typ	Max	Unit
Built-in Hysteresis	V_{HYS}	V_{HYS} = 200 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = -40 °C to +85 °C	157.1	--	251.6	mV
			LB - Disabled, T = -40 °C to +85 °C	160.2	--	245.3	mV
Series Input Resistance	R_{Sin}	Gain = 1x		--	100.0	--	MΩ
		Gain = 0.5x		--	1.0	--	MΩ
		Gain = 0.33x		--	0.8	--	MΩ
		Gain = 0.25x		--	1.0	--	MΩ
Propagation Delay, Response Time	PROP	Low Bandwidth - Enable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 5 mV, V_{REF} = 50 mV	LOW to HIGH, T = -40 °C to +85 °C	--	35.99	216.56	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	39.36	208.81	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 5 mV, V_{REF} = 50 mV	LOW to HIGH, T = -40 °C to +85 °C	--	1.85	3.04	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	2.17	4.10	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 5 mV, V_{REF} = 50 mV	LOW to HIGH, T = -40 °C to +85 °C	--	25.22	129.31	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	28.31	145.47	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 5 mV, V_{REF} = 50 mV	LOW to HIGH, T = -40 °C to +85 °C	--	1.55	2.63	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	1.93	3.83	µs
Propagation Delay, Response Time	PROP	Low Bandwidth - Enable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 5 mV, V_{REF} = 250 mV	LOW to HIGH, T = -40 °C to +85 °C	--	36.46	216.78	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	39.79	216.05	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 5 mV, V_{REF} = 250 mV	LOW to HIGH, T = -40 °C to +85 °C	--	2.04	3.37	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	2.21	4.12	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 5 mV, V_{REF} = 250 mV	LOW to HIGH, T = -40 °C to +85 °C	--	25.81	132.94	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	28.65	142.43	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 5 mV, V_{REF} = 250 mV	LOW to HIGH, T = -40 °C to +85 °C	--	1.74	2.93	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	1.97	3.96	µs

Parameter	Symbol	Description/Note	Conditions	Min	Typ	Max	Unit
Propagation Delay, Response Time	PROP	Low Bandwidth - Enable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 5 mV, V_{REF} = 600 mV	LOW to HIGH, T = -40 °C to +85 °C	--	37.36	222.82	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	40.67	219.61	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 5 mV, V_{REF} = 600 mV	LOW to HIGH, T = -40 °C to +85 °C	--	2.23	4.02	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	2.23	4.33	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 5 mV, V_{REF} = 600 mV	LOW to HIGH, T = -40 °C to +85 °C	--	26.41	135.47	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	29.32	149.01	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 5 mV, V_{REF} = 600 mV	LOW to HIGH, T = -40 °C to +85 °C	--	1.92	3.53	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	2.00	4.25	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 5 mV, V_{REF} = 850 mV	LOW to HIGH, T = -40 °C to +85 °C	--	38.36	232.64	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	41.67	232.78	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 5 mV, V_{REF} = 850 mV	LOW to HIGH, T = -40 °C to +85 °C	--	2.26	4.20	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	2.25	4.60	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 5 mV, V_{REF} = 850 mV	LOW to HIGH, T = -40 °C to +85 °C	--	27.08	137.02	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	29.89	146.92	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 5 mV, V_{REF} = 850 mV	LOW to HIGH, T = -40 °C to +85 °C	--	1.91	3.57	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	1.98	4.34	µs
		Low Bandwidth - Enable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 5 mV, V_{REF} = 1200 mV	LOW to HIGH, T = -40 to +85 °C	--	103.93	1853.68	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	101.06	1656.70	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 1.71 V to 3.3 V, Overdrive = 5 mV, V_{REF} = 1200 mV	LOW to HIGH, T = -40 °C to +85 °C	--	68.29	1753.33	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	63.06	1568.55	µs

Parameter	Symbol	Description/Note	Conditions	Min	Typ	Max	Unit
Propagation Delay, Response Time	PROP	Low Bandwidth - Enable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 5 mV, V_{REF} = 1200 mV	LOW to HIGH, T = -40 °C to +85 °C	--	30.62	167.56	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	33.54	181.40	µs
		Low Bandwidth - Disable, Gain = 1, V_{DD} = 3.3 V to 5.5 V, Overdrive = 5 mV, V_{REF} = 1200 mV	LOW to HIGH, T = -40 °C to +85 °C	--	5.00	32.61	µs
			HIGH to LOW, T = -40 °C to +85 °C	--	5.24	33.88	µs
Gain Error (Including Threshold and Internal V_{REF} Error), T = -40 °C to +85 °C	G	G = 1, V_{DD} = 1.71 V	V_{REF} = 50 mV to 1200 mV	--	1	--	
		G = 1, V_{DD} = 3.3 V		--	1	--	
		G = 1, V_{DD} = 5.5 V		--	1	--	
		G = 0.5, V_{DD} = 1.71 V		-1.00	--	0.93	%
		G = 0.5, V_{DD} = 3.3 V		-0.96	--	0.82	%
		G = 0.5, V_{DD} = 5.5 V		-1.04	--	0.90	%
		G = 0.33, V_{DD} = 1.71V		-1.75	--	2.10	%
		G = 0.33, V_{DD} = 3.3 V		-1.95	--	1.69	%
		G = 0.33, V_{DD} = 5.5 V		-2.03	--	1.77	%
		G = 0.25, V_{DD} = 1.71V		-1.91	--	2.13	%
		G = 0.25, V_{DD} = 3.3 V		-1.98	--	1.80	%
		G = 0.25, V_{DD} = 5.5 V		-2.12	--	1.90	%
Internal V_{REF} Error, Vref = 1200 mV	V_{REF}	V_{DD} = 1.8 V ± 5 %	T = 25 °C	-0.58	--	0.56	%
			T = -40 °C to +85 °C	-1.01	--	0.70	%
		V_{DD} = 3.3 V ± 10 %	T = 25 °C	-0.59	--	0.58	%
			T = -40 °C to +85 °C	-1.06	--	0.72	%
		V_{DD} = 5.0 V ± 10 %	T = 25 °C	-0.64	--	0.60	%
			T = -40 °C to +85 °C	-1.16	--	0.74	%
Internal V_{REF} Error, Vref = 1000 mV		V_{DD} = 1.8 V ± 5 %	T = 25 °C	-0.57	--	0.58	%
			T = -40 °C to +85 °C	-1.14	--	0.76	%
		V_{DD} = 3.3 V ± 10 %	T = 25 °C	-0.59	--	0.58	%
			T = -40 °C to +85 °C	-1.04	--	0.73	%
		V_{DD} = 5.0 V ± 10 %	T = 25 °C	-0.67	--	0.64	%
			T = -40 °C to +85 °C	-1.15	--	0.73	%

Parameter	Symbol	Description/Note	Conditions	Min	Typ	Max	Unit
Internal V_{REF} Error, V_{REF} = 500 mV	V_{REF}	V_{DD} = 1.8 V ± 5 %	T = 25 °C	-0.64	--	0.64	%
			T = -40 °C to +85 °C	-1.11	--	0.75	%
		V_{DD} = 3.3 V ± 10 %	T = 25 °C	-0.63	--	0.63	%
			T = -40 °C to +85 °C	-1.10	--	0.78	%
		V_{DD} = 5.0 V ± 10 %	T = 25 °C	-0.72	--	0.70	%
			T = -40 °C to +85 °C	-1.15	--	0.80	%

3.7 Analog Temperature Sensor Characteristics

3.7.1. TS Output vs. Temperature (Output Range 1)

T, °C	V_{DD} = 1.8 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V	
	Typical, V	Accuracy, %	Typical, V	Accuracy, %	Typical, V	Accuracy, %
-40	1.20	±3.33	1.20	±3.29	1.20	±3.29
-30	1.16	±3.35	1.16	±3.32	1.16	±3.29
-20	1.13	±3.49	1.13	±3.42	1.13	±3.42
-10	1.10	±3.42	1.10	±3.33	1.10	±3.38
0	1.06	±3.51	1.06	±3.46	1.06	±3.45
10	1.03	±3.63	1.03	±3.60	1.03	±3.60
20	0.99	±3.72	0.99	±3.61	0.99	±3.58
30	0.96	±4.00	0.96	±3.92	0.96	±3.87
40	0.92	±3.73	0.92	±3.64	0.92	±3.64
50	0.88	±4.01	0.88	±3.90	0.88	±3.92
60	0.85	±4.11	0.85	±4.03	0.85	±3.97
70	0.81	±4.18	0.81	±4.12	0.81	±4.06
80	0.78	±4.43	0.78	±4.36	0.78	±4.26
90	0.75	±4.98	0.75	±4.89	0.75	±4.81

3.7.2. TS Output vs. Temperature (Output Range 2)

T, °C	V_{DD} = 1.8 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V	
	Typical, V	Accuracy, %	Typical, V	Accuracy, %	Typical, V	Accuracy, %
-40	0.99	±3.29	0.99	±3.28	0.99	±3.28
-30	0.96	±3.33	0.96	±3.24	0.96	±3.31
-20	0.93	±3.37	0.93	±3.30	0.93	±3.34
-10	0.90	±3.46	0.90	±3.39	0.90	±3.40
0	0.87	±3.45	0.87	±3.39	0.87	±3.40
10	0.85	±3.62	0.85	±3.51	0.85	±3.53

T, °C	V_{DD} = 1.8 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V	
	Typical, V	Accuracy, %	Typical, V	Accuracy, %	Typical, V	Accuracy, %
20	0.82	±3.66	0.82	±3.58	0.82	±3.53
30	0.79	±3.93	0.79	±3.81	0.79	±3.80
40	0.76	±3.71	0.76	±3.65	0.76	±3.62
50	0.73	±3.97	0.73	±3.90	0.73	±3.91
60	0.70	±4.02	0.70	±3.97	0.70	±4.00
70	0.67	±4.22	0.67	±4.13	0.67	±4.08
80	0.64	±4.38	0.64	±4.29	0.64	±4.26
90	0.61	±4.89	0.61	±4.88	0.61	±4.77

3.7.3. TS Output Error (Output Range 1)

V_{DD}, V	Error at T						
	-40 °C, %	-20 °C, %	0 °C, %	20 °C, %	40 °C, %	60 °C, %	80 °C, %
1.71	±3.34	±3.50	±3.56	±3.69	±3.73	±4.09	±4.43
1.80	±3.33	±3.49	±3.51	±3.72	±3.73	±4.11	±4.43
1.89	±3.33	±3.47	±3.55	±3.70	±3.72	±4.11	±4.40
2.30	±3.31	±3.46	±3.50	±3.69	±3.66	±4.05	±4.38
2.50	±3.31	±3.44	±3.51	±3.62	±3.66	±4.03	±4.36
2.70	±3.30	±3.46	±3.46	±3.64	±3.65	±3.97	±4.31
3.00	±3.31	±3.46	±3.46	±3.62	±3.64	±4.07	±4.34
3.30	±3.29	±3.42	±3.46	±3.61	±3.64	±4.03	±4.36
3.60	±3.25	±3.42	±3.46	±3.59	±3.62	±3.98	±4.34
4.20	±3.28	±3.42	±3.45	±3.62	±3.62	±4.01	±4.30
4.50	±3.32	±3.41	±3.46	±3.63	±3.62	±4.01	±4.29
5.00	±3.29	±3.42	±3.45	±3.58	±3.64	±3.97	±4.26
5.50	±3.30	±3.47	±3.50	±3.61	±3.64	±4.02	±4.31

3.7.4. TS Output Error (Output Range 2)

V_{DD}, V	Error at T						
	-40 °C, %	-20 °C, %	0 °C, %	20 °C, %	40 °C, %	60 °C, %	80 °C, %
1.71	±3.28	±3.38	±3.43	±3.67	±3.72	±4.13	±4.42
1.80	±3.29	±3.37	±3.45	±3.66	±3.71	±4.02	±4.38
1.89	±3.21	±3.38	±3.44	±3.63	±3.72	±4.06	±4.39
2.30	±3.23	±3.34	±3.46	±3.56	±3.66	±4.03	±4.32
2.50	±3.27	±3.37	±3.44	±3.59	±3.68	±4.03	±4.26
2.70	±3.24	±3.31	±3.39	±3.59	±3.65	±4.04	±4.29
3.00	±3.27	±3.33	±3.39	±3.57	±3.65	±4.02	±4.26

V_{DD}, V	Error at T						
	-40 °C, %	-20 °C, %	0 °C, %	20 °C, %	40 °C, %	60 °C, %	80 °C, %
3.30	±3.28	±3.30	±3.39	±3.58	±3.65	±3.97	±4.29
3.60	±3.28	±3.28	±3.34	±3.58	±3.64	±3.96	±4.30
4.20	±3.23	±3.36	±3.34	±3.58	±3.62	±4.04	±4.28
4.50	±3.27	±3.31	±3.38	±3.56	±3.61	±4.03	±4.26
5.00	±3.28	±3.34	±3.40	±3.53	±3.62	±4.00	±4.26
5.50	±3.26	±3.37	±3.44	±3.57	±3.61	±4.01	±4.22

4. IO Pins

The SLG47525/28 has a total of 16 GPIO pins, which can function as either a user-defined inputs or outputs, and 1 GPI pin.

4.1 GPI Pin

IO0 serves as a general purpose input pin.

4.2 GPIO Pins

Pins from IO1 to IO17 serve as general purpose IO pins.

IOs 0, 1, 2, 3, 4, 5, 6, 7, and 8 are powered from V_{DD1} and IOs 9, 10, 12, 13, 14, 15, 16, and 17 are powered from V_{DD2} (refer to section 5 Power Architecture).

4.3 Pull-Up/Down Resistors

All IO pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ for IOs 0, 1, 2, 3, 4, 5, 6, 7, 8 and 10 kΩ, 100 kΩ, and 500 kΩ for IOs 9, 10, 12, 13, 14, 15, 16, 17. In the case of IOs 0, 6, 7, 13, 14, the resistors are fixed to a pull-down configuration. In the case of all other IO pins, the internal resistors can be configured as either pull-ups or pull-downs.

4.4 Input Modes

Each IO pin can be configured as a digital input pin with/without buffered Schmitt Trigger. IOs 0, 1, 2, 3, 4, 5, 6, 7, and 8 can also be configured as low voltage digital inputs. IOs 1, 2, 4, 5, 8, and 9 can also be configured to serve as analog inputs to the on-chip comparators.

4.5 Output Modes

IOs 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 12, 13, 14, 15, 16, and 17 can all be configured as digital output pins.

4.6 GPI Structure

4.6.1. GPI Structure (for IO0)

Input Mode [1:0]
00b : Digital Input w/o Schmitt Trigger, WOSMT_EN=1, OE=0
01b : Digital Input with Schmitt Trigger, SMT_EN=1, OE=0
10b : Low Voltage Digital Input, LV_EN=1, OE=0
11b: Reserved

RES_SEL [1:0]
00b: Floating
01b: 10kΩ
10b: 100kΩ
11b: 1MΩ

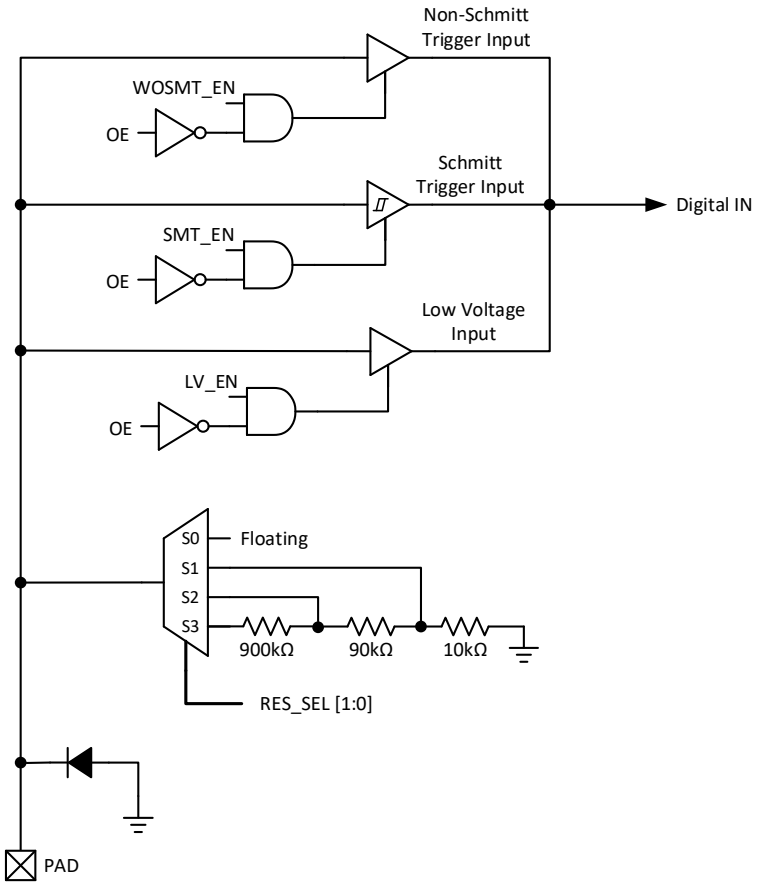


Figure 5. IO0 GPI Structure Diagram

4.7 GPIO with I²C Mode IO Structure

4.7.1. GPIO with I²C Mode IO Structure (for IOs 6 and 7)

MODE [2:0]
000b : Digital Input w/o Schmitt Trigger, WOSMT_EN=1, OE=0
001b : Digital Input with Schmitt Trigger, SMT_EN=1, OE=0
010b : Low Voltage Digital Input, LV_EN=1, OE=0
011b: Reserved
100b: Reserved
101b : Open Drain NMOS, OE=OD_EN=1
110b: Reserved
111b: Reserved

RES_SEL [1:0]
00b: Floating
01b: 10kΩ
10b: 100kΩ
11b: 1MΩ

Note1:
- "Digital OUT" is Matrix Output
- "Digital IN" is a Matrix Input
- "OE" cannot be selected by user and is controlled by register

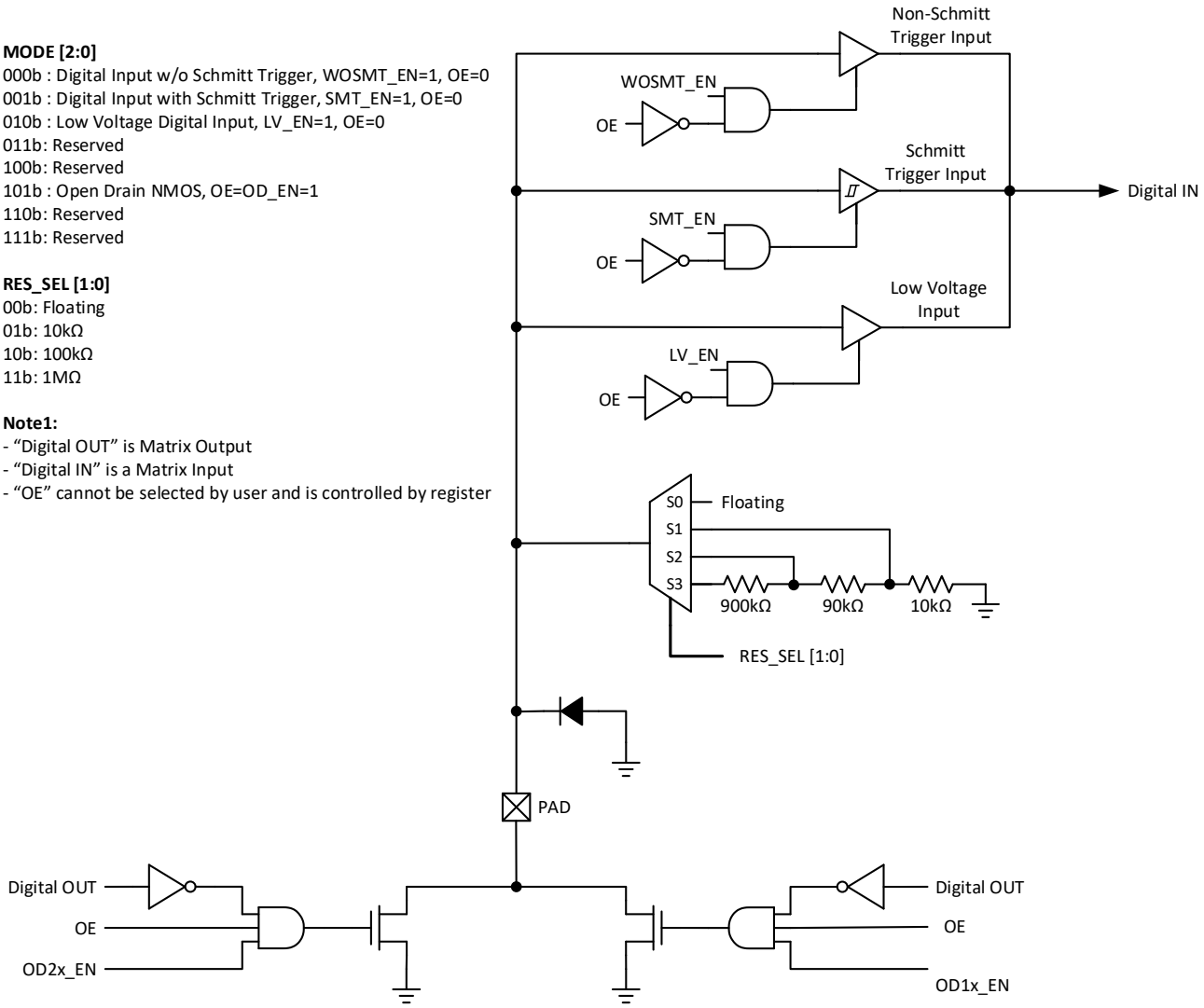


Figure 6. GPIO with I²C Mode IO Structure Diagram (for GPIO Powered from V_{DD1})

4.7.2. GPIO with I²C Mode IO Structure (for IOs 13 and 14)

MODE [2:0]
000b : Digital Input w/o Schmitt Trigger, WOSMT_EN=1, OE=0
001b : Digital Input with Schmitt Trigger, SMT_EN=1, OE=0
01xb : Reserved
1xxb : Open Drain NMOS, OE=OD_EN=1

RES_SEL [1:0]
00b: Floating
01b: 10kΩ
10b: 100kΩ
11b: 500kΩ

Note1:
- "Digital OUT" is Matrix Output
- "Digital IN" is a Matrix Input
- "OE" cannot be selected by user and is controlled by register

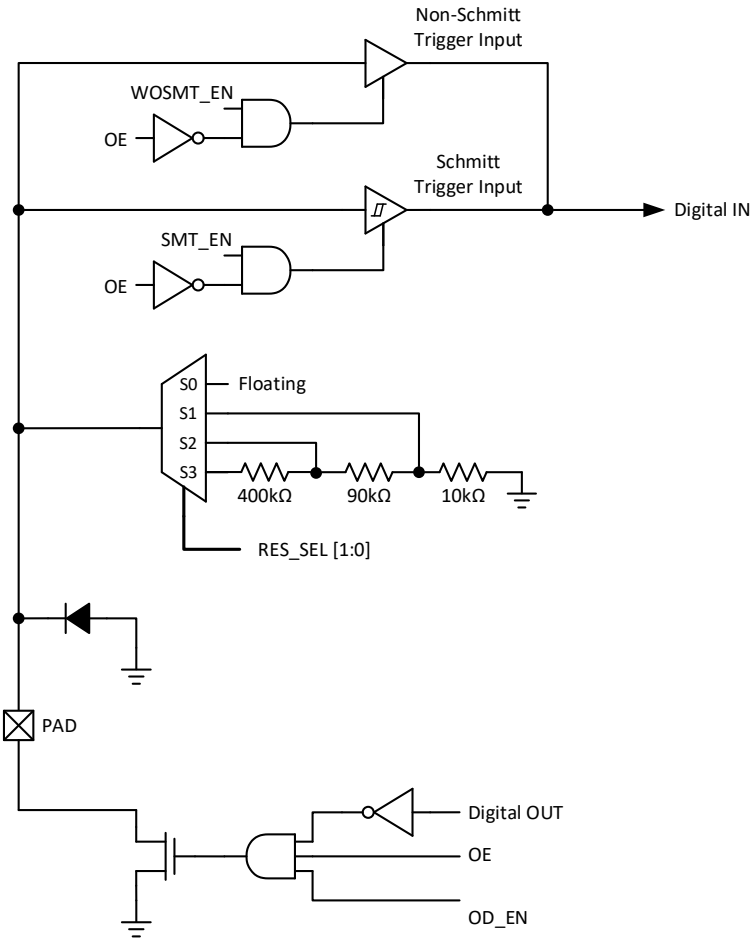


Figure 7. GPIO with I²C Mode IO Structure Diagram (for GPIO Powered from V_{DD2})

4.8 Matrix OE IO Structure

4.8.1. Matrix OE IO Structure (for IOs 1, 3, 5)

Input Mode[1:0]
00b : Digital Input w/o Schmitt Trigger, WOSMT_EN=1, OE=0
01b : Digital Input with Schmitt Trigger, SMT_EN=1, OE=0
10b : Low Voltage Digital Input, LV_EN=1, OE=0
11b : Analog Input mode

Output Mode[0]
00b: Push-pull 1x mode, PP1x_EN=1
01b: Push-pull 2x mode, PP2_EN=1, PP1x_EN=1
10b : Open Drain NMOS 1x, OD1x_EN=1
11b : Open Drain NMOS 2x, OD2x_EN=1, OD1x_EN=1

RES_SEL [1:0]
00b: Floating
01b: 10kΩ
10b: 100kΩ
11b: 1MΩ

Note1:
- "Digital OUT" is Matrix Output
- "Digital IN" is a Matrix Input
- "OE" is Matrix Output

Note2:
Can be varied over PVT (for reference only)

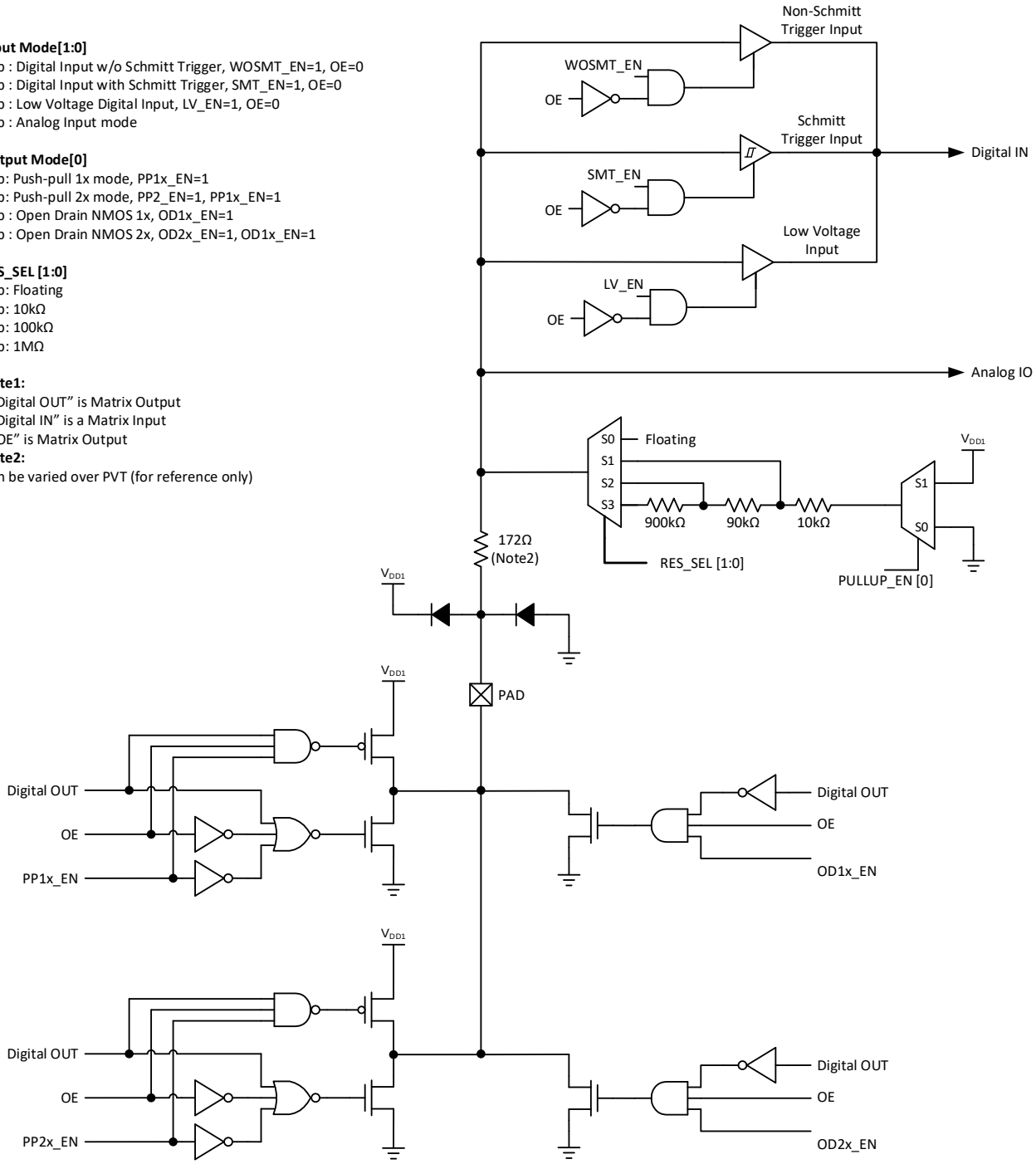


Figure 8. Matrix OE IO Structure Diagram (for GPIO Powered from V_{DD1})

4.8.2. Matrix OE IO Structure (for IOs 10, 15, 16, 17)

Input Mode[1:0]
00b : Digital Input w/o Schmitt Trigger, WOSMT_EN=1, OE=0
01b : Digital Input with Schmitt Trigger, SMT_EN=1, OE=0
1xb : Analog Input mode for IO 15, 16
Reserved for IO 10, 17

Output Mode[0]
0b : Push-pull mode, OD_EN=0
1b : Open Drain NMOS, OD_EN=1

RES_SEL [1:0]
00b: Floating
01b: 10kΩ
10b: 100kΩ
11b: 500kΩ

Note1:
- "Digital OUT" is Matrix Output
- "Digital IN" is a Matrix Input
- "OE" is Matrix Output

Note2:
Can be varied over PVT (for reference only)

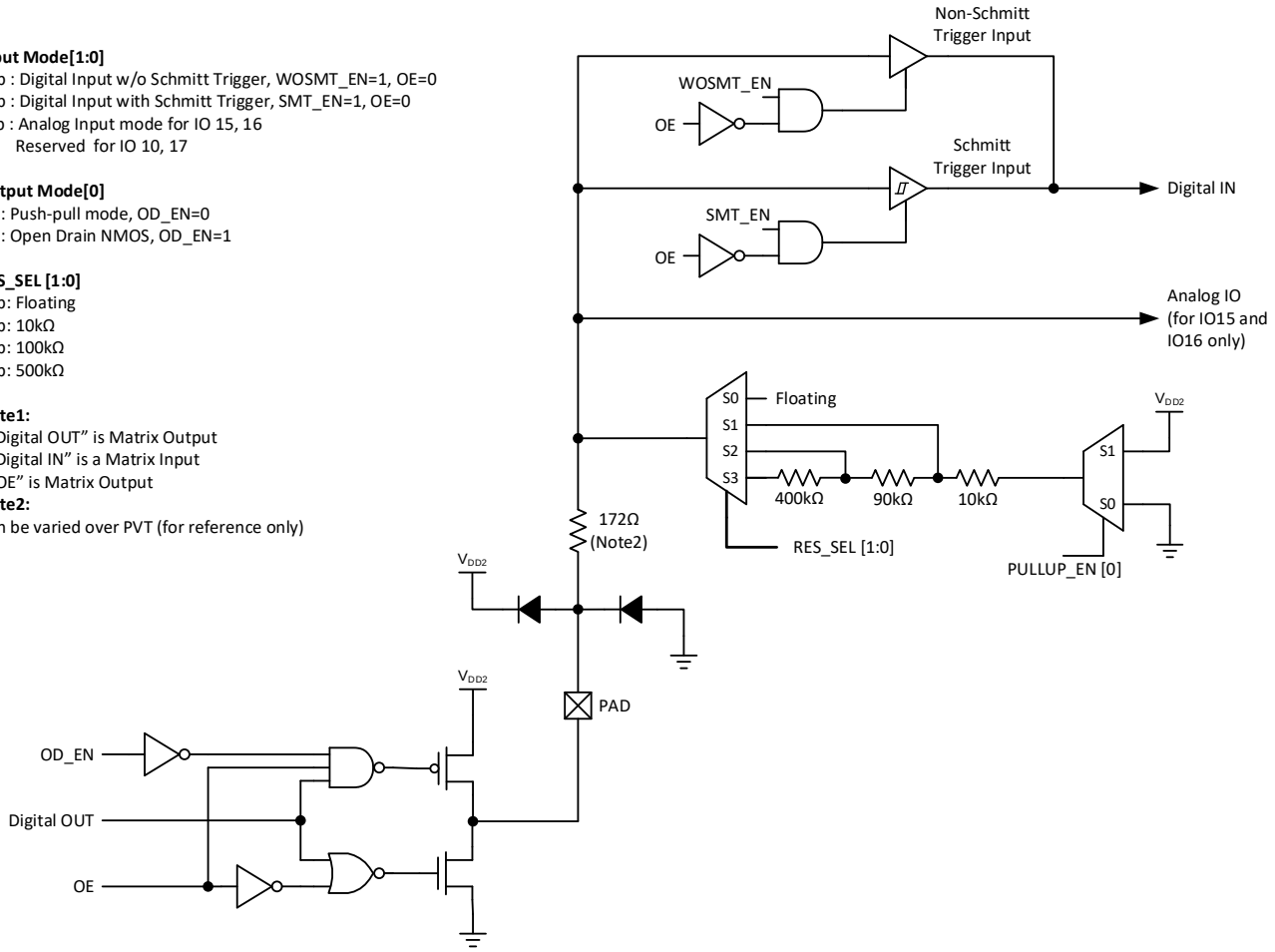


Figure 9. Matrix OE IO Structure Diagram (for GPIO Powered from V_{DD2})

4.8.3. Matrix OE 4x Drive Structure (for IO8)

Input Mode[1:0]
00b : Digital Input w/o Schmitt Trigger, WOSMT_EN=1, OE=0
01b : Digital Input with Schmitt Trigger, SMT_EN=1, OE=0
10b : Low Voltage Digital Input, LV_EN=1, OE=0
11b : Analog Input mode

Output Mode[0]
00b: Push-pull 1x mode, PP1x_EN=1
01b: Push-pull 2x mode, PP2_EN=1, PP1x_EN=1
10b : Open Drain NMOS 1x, OD1x_EN=1, ODn_EN=1
11b : Open Drain NMOS 2x, OD2x_EN=1, OD1x_EN=1, ODn_EN=1

RES_SEL [1:0]
00b: Floating
01b: 10kΩ
10b: 100kΩ
11b: 1MΩ

Note1:
- "Digital OUT" is Matrix Output
- "Digital IN" is a Matrix Input
- "OE" is Matrix Output

Note2:
Can be varied over PVT (for reference only)

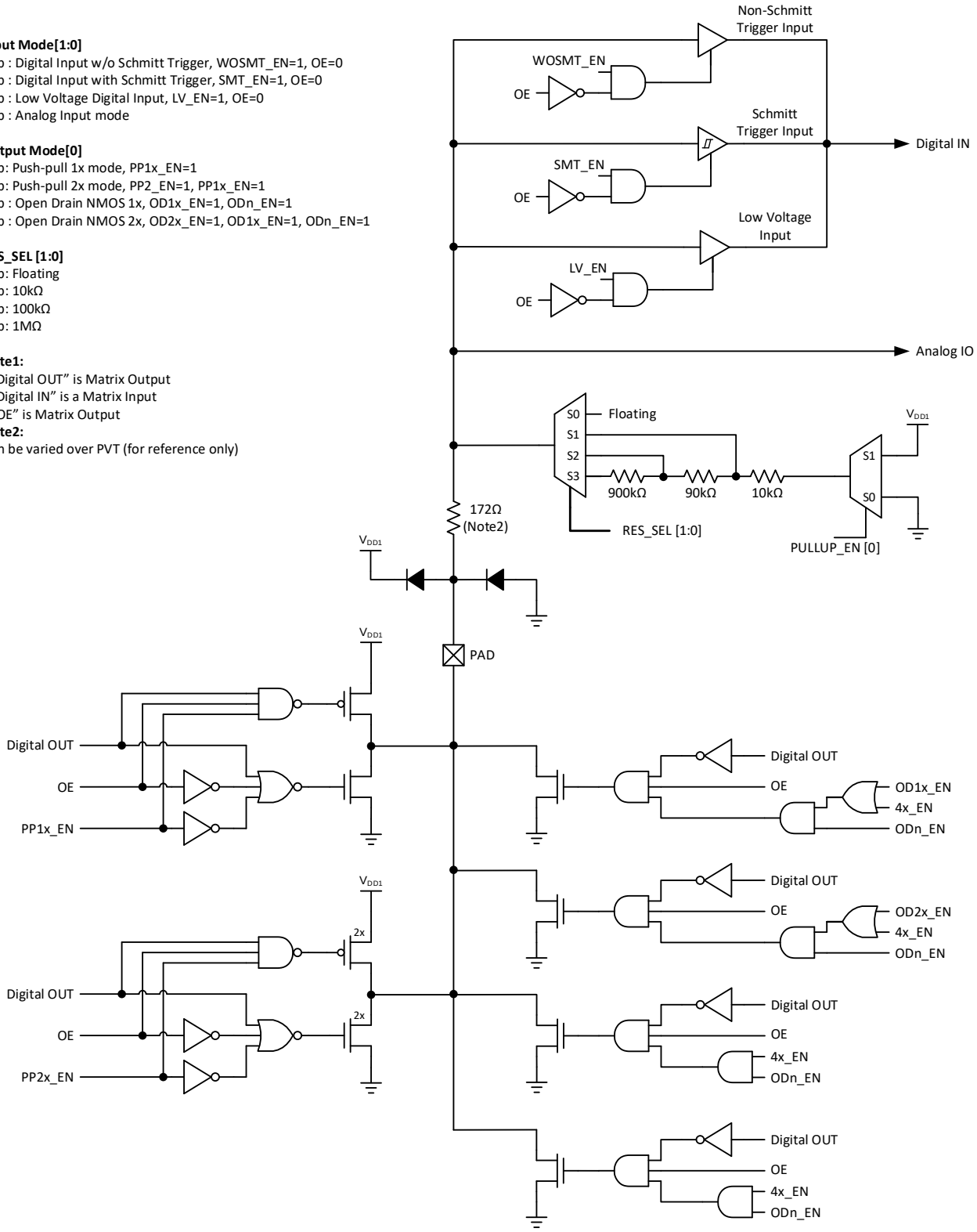


Figure 10. Matrix OE IO 4x Drive Structure Diagram

4.9 Register OE IO Structure

4.9.1. Register OE IO Structure (for IOs 2 and 4)

Mode[2:0]
000b: Digital Input w/o Schmitt Trigger, WOSMT_EN=1, OE=0
001b: Digital Input with Schmitt Trigger, SMT_EN=1, OE=0
010b: Low Voltage Digital Input, LV_EN=1, OE=0
011b: Analog Input mode
100b: Push-pull mode, PP_EN=1, OE=1
101b: Open Drain NMOS, ODN_EN=1, OE=1
110b: Open Drain PMOS, OD2x_EN=1, OD1x_EN=1
111b: Analog Input and NMOS open-drain mode, ODn_EN=1, AIO_EN=1

RES_SEL [1:0]
00b: Floating
01b: 10kΩ
10b: 100kΩ
11b: 1MΩ

Note1:
- "Digital OUT" is Matrix Output
- "Digital IN" is a Matrix Input
- "OE" cannot be selected by user and is controlled by register

Note2:
Can be varied over PVT (for reference only)

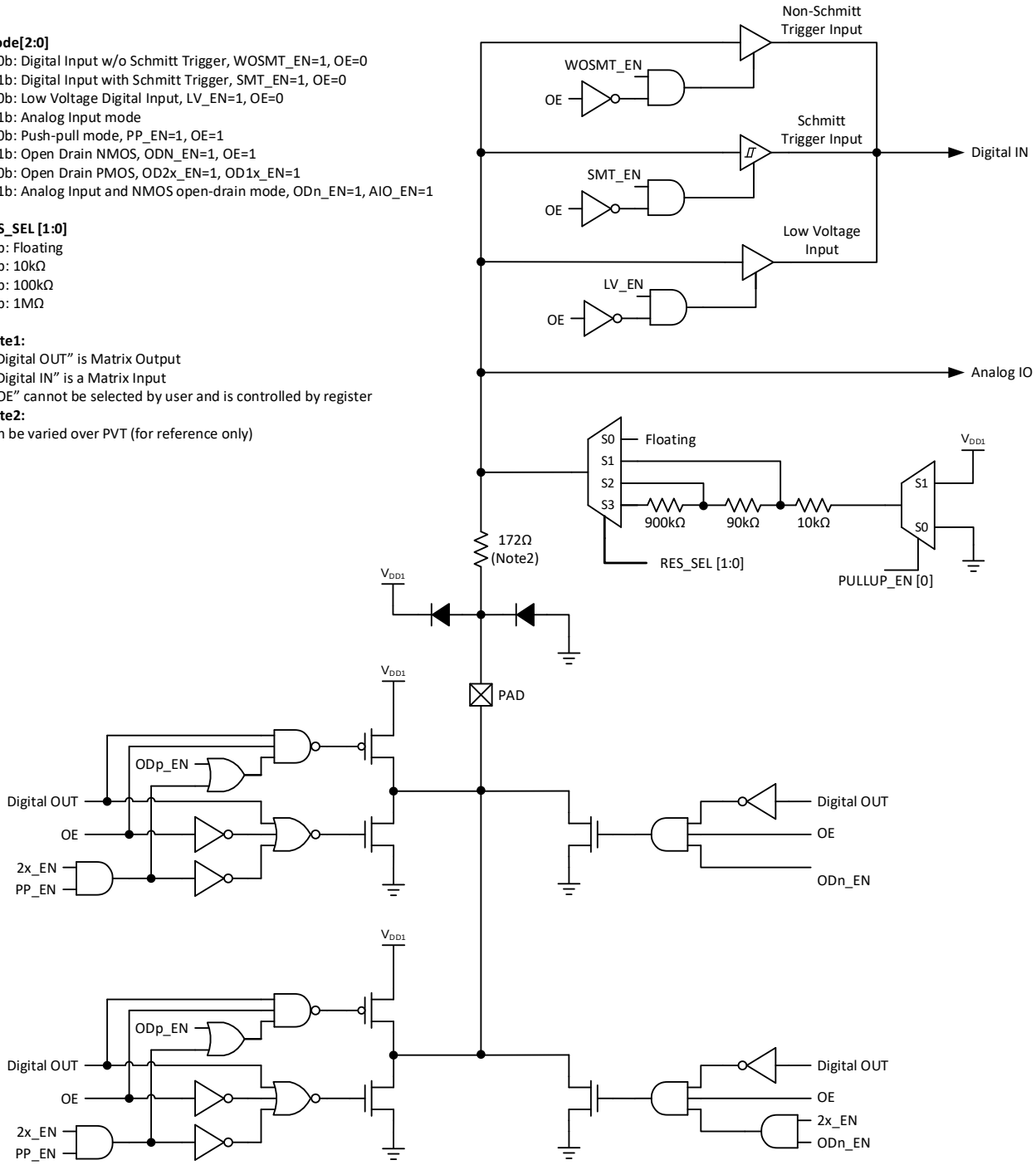


Figure 11. Register OE IO Structure Diagram (for GPIO Powered from V_{DD1})

4.9.2. Register OE IO Structure (for IOs 9, 12)

MODE [3:0]
000xb : Digital Input w/o Schmitt Trigger, WOSMT_EN=1, OE=0
001xb : Digital Input with Schmitt Trigger, SMT_EN=1, OE=0
01xxb : Analog Input mode for IO 9
Reserved for IO 12
1xx0b : Push-pull Output, OD_EN=0
1xx1b : Open Drain NMOS, OD_EN=1

RES_SEL [1:0]
00b: Floating
01b: 10kΩ
10b: 100kΩ
11b: 500kΩ

Note1:
- "Digital OUT" is Matrix Output
- "Digital IN" is a Matrix Input
- "OE" cannot be selected by user and is controlled by register

Note2:
Can be varied over PVT (for reference only)

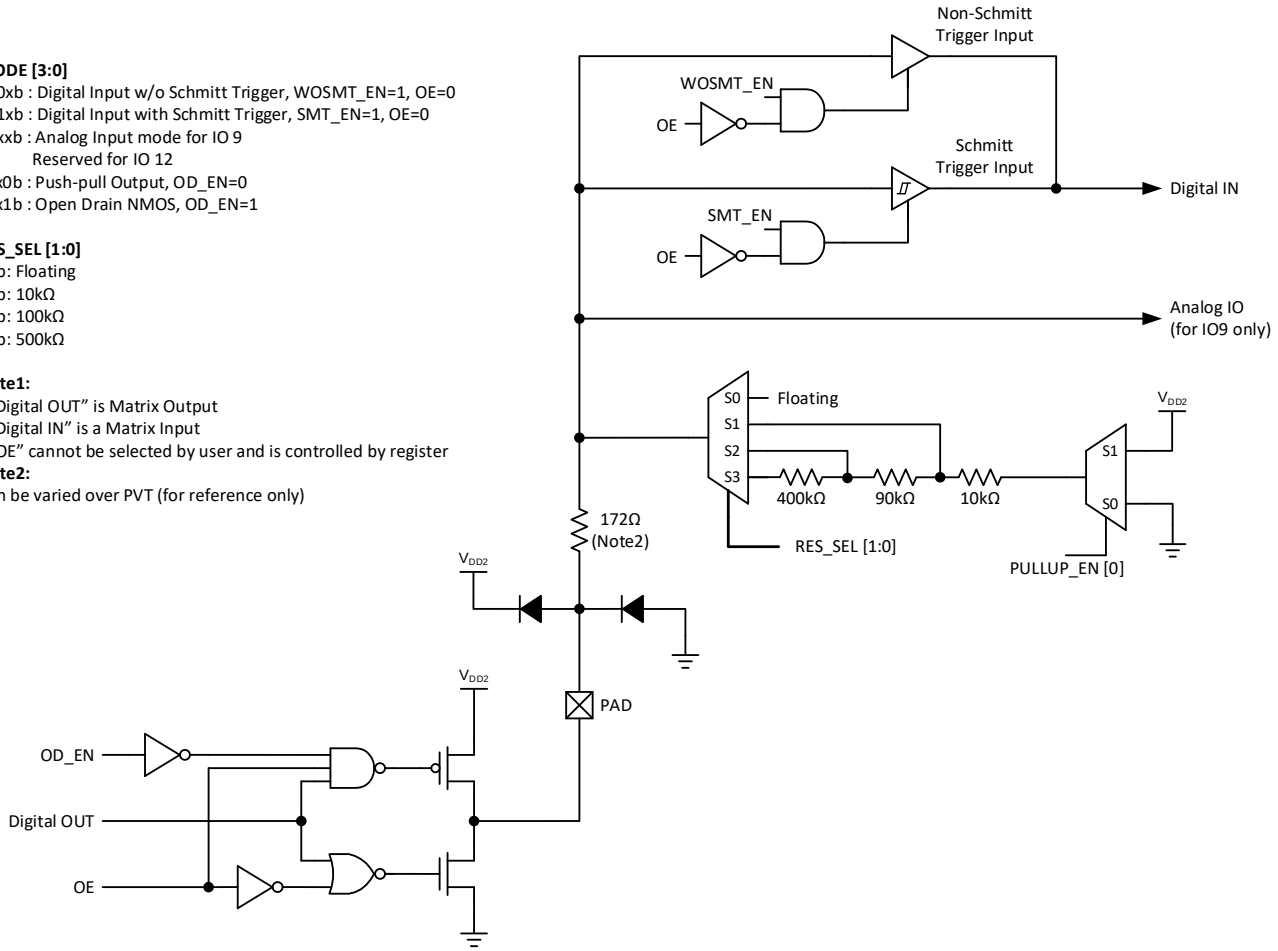


Figure 12. Register OE IO Structure Diagram (for GPIO Powered from V_{DD2})

5. Power Architecture

All internal macrocells and IOs 0, 1, 2, 3, 4, 5, 6, 7, and 8 are powered from V_{DD1}. IOs 9, 10, 12, 13, 14, 15, 16, and 17 are powered from V_{DD2}.

During the start-up event, V_{DD2} can be higher than V_{DD1} without damage for the chip, but not exceeding Absolute Maximum limits.

In case V_{DD1} pin is floating and any pin powered from V_{DD1} is configured as input, ESD pin protection diodes must be considered when applying an input signal to the pin. This will cause a current flow through ESD diodes from input to V_{DD1}.

In case V_{DD2} pin is floating and any pin powered from V_{DD2} is configured as input, ESD pin protection diodes must be considered when applying an input signal to the pin. This will cause a current flow through ESD diodes from input to V_{DD2}.

It is allowed to apply supply voltage to V_{DD2} pin while V_{DD1} pin is floating. Otherwise, it is allowed to apply supply voltage to V_{DD1} pin while V_{DD2} pin is floating. The states of GPIOs and macrocells depending on V_{DD1} and V_{DD2}.

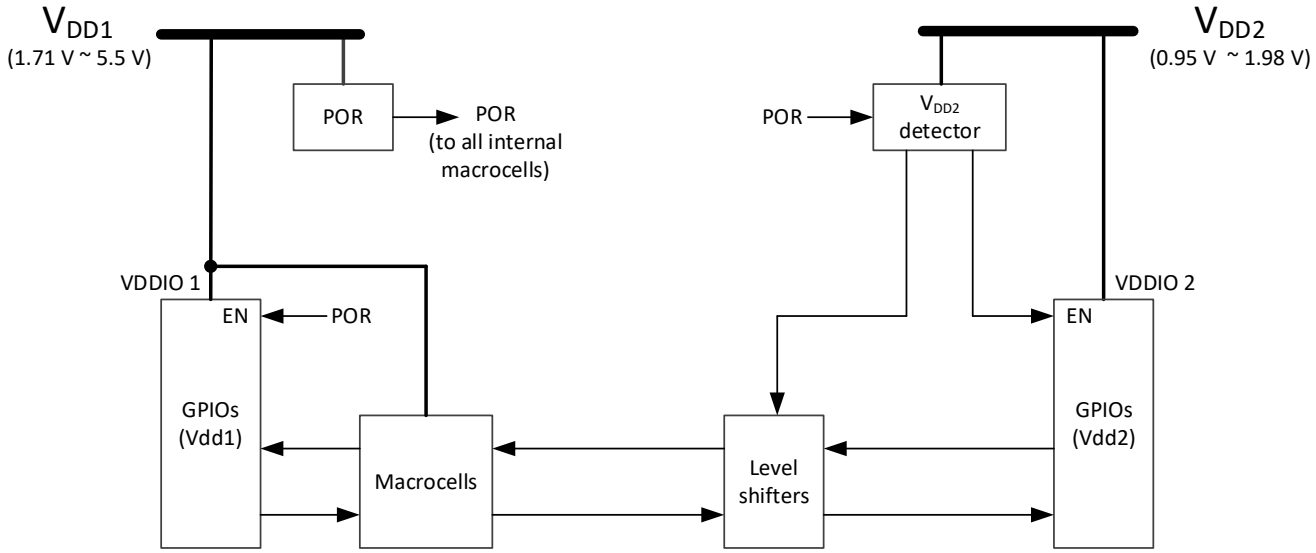


Figure 13. Power Architecture

Table 3. Power States of GPIOs and Macrocells

V_{DD1} and V_{DD2} State	GPIOs Powered from V_{DD1}	GPIOs Powered from V_{DD2}	Internal Macrocells	Other
V_{DD1} > Power-On threshold V_{DD2} > Detector threshold	Function according to configuration	Function according to configuration	Function according to configuration	--
V_{DD1} < Power-On threshold V_{DD2} > Detector threshold	Hi-Z	Hi-Z	OFF	--
V_{DD1} > Power-On threshold V_{DD2} < Detector threshold	Function according to configuration	Hi-Z	Function according to configuration	No internal pull-up/down on GPIO from V_{DD2} domain. All input signals from GPIO powered from V_{DD2} are in strong LOW.
V_{DD1} < Power-On threshold V_{DD2} < Detector threshold (Chip powered off)	Hi-Z	Hi-Z	OFF	--

6. Connection Matrix

The Connection Matrix in the SLG47525/28 is used to create the internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG47525/28 has a specific digital bit code assigned to it, that is either set to active HIGH or inactive LOW, based on the design that is created. Once the 2048 register bits within the SLG47525/28 are programmed, a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 110 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IO pins, LUTs, analog comparators, other digital resources, such as V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

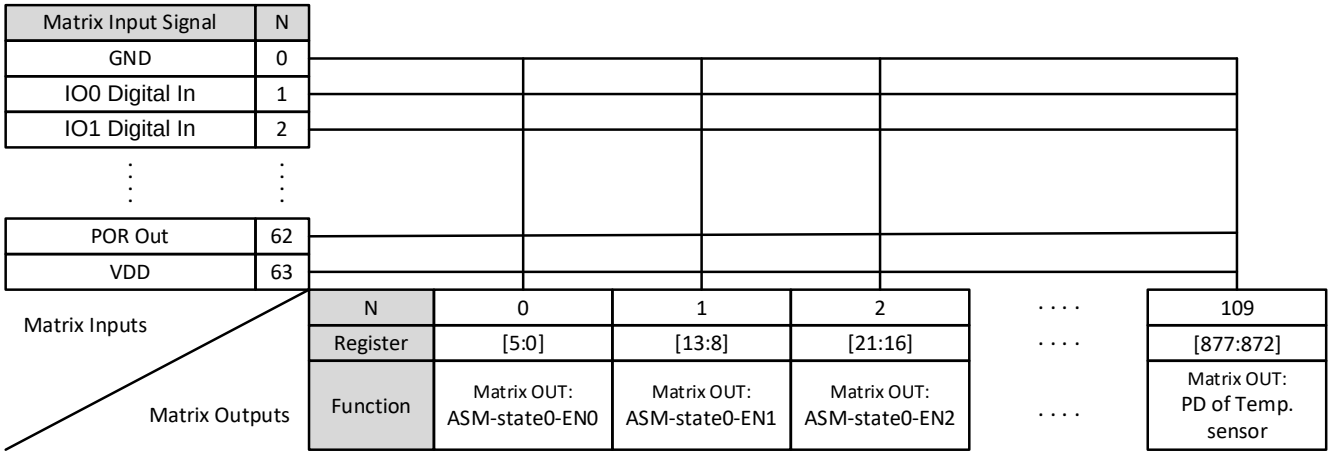


Figure 14. Connection Matrix

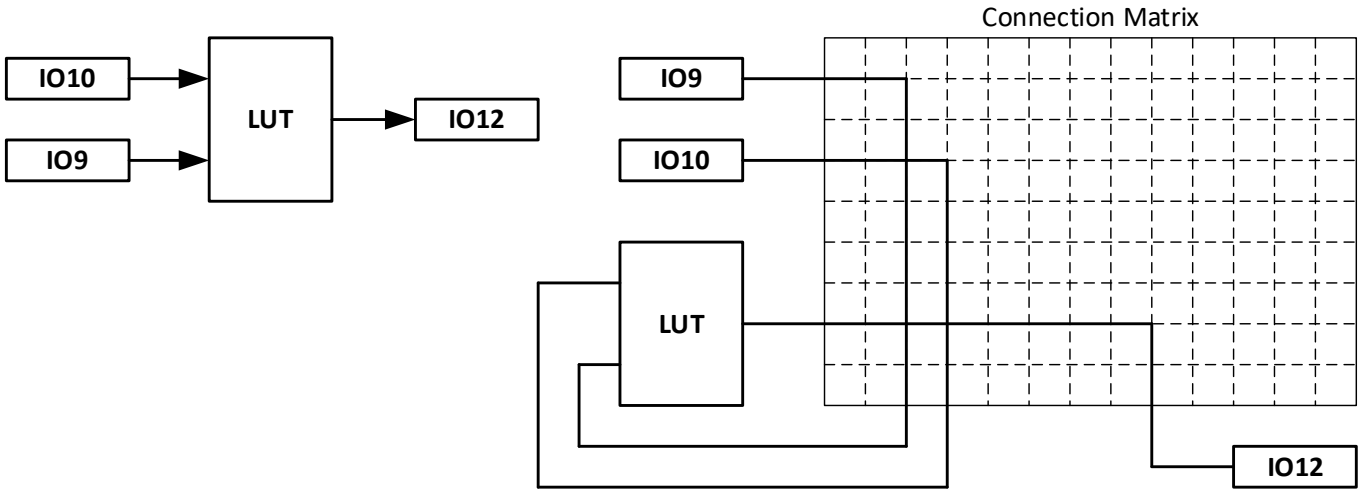


Figure 15. Connection Matrix Usage Example

6.1 Matrix Input Table

Table 4. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	IO0 Digital Input	0	0	0	0	0	1
2	IO1 Digital Input	0	0	0	0	1	0
3	IO2 Digital Input	0	0	0	0	1	1
4	IO3 Digital Input	0	0	0	1	0	0
5	IO4 Digital Input	0	0	0	1	0	1
6	IO5 Digital Input	0	0	0	1	1	0
7	IO8 Digital Input	0	0	0	1	1	1
8	LUT2_0/DFF0 Output	0	0	1	0	0	0
9	LUT2_1/DFF1 Output	0	0	1	0	0	1
10	LUT2_2/DFF2 Output	0	0	1	0	1	0
11	LUT2_3/PGEN Output	0	0	1	0	1	1
12	LUT3_0/DFF3 Output	0	0	1	1	0	0
13	LUT3_1/DFF4 Output	0	0	1	1	0	1
14	LUT3_2/DFF5 Output	0	0	1	1	1	0
15	LUT3_3/DFF6 Output	0	0	1	1	1	1
16	LUT3_4/DFF7 Output	0	1	0	0	0	0
17	LUT3_5/CNT_DLY2 (8-bit) Output	0	1	0	0	0	1
18	LUT3_6/CNT_DLY3 (8-bit) Output	0	1	0	0	1	0
19	LUT3_7/CNT_DLY4 (8-bit) Output	0	1	0	0	1	1
20	LUT3_8/CNT_DLY5 (8-bit) Output	0	1	0	1	0	0
21	LUT3_9/CNT_DLY6 (8-bit) Output	0	1	0	1	0	1
22	LUT4_0/CNT_DLY0 (16-bit) Output	0	1	0	1	1	0
23	LUT4_1/CNT_DLY1 (16-bit) Output	0	1	0	1	1	1
24	LUT3_10/Pipe Delay (1st stage) Output	0	1	1	0	0	0
25	Pipe Delay Output0	0	1	1	0	0	1
26	Pipe Delay Output1	0	1	1	0	1	0
27	Internal OSC Pre-Divided by 1/2/4/8 Output and Post-Divided by 1/2/3/4/8/12/24/64 Output0 (25 kHz/2 MHz)	0	1	1	0	1	1
28	Internal OSC Pre-Divided by 1/2/4/8 Output and Post-Divided by 1/2/3/4/8/12/24/64 Output1 (25 kHz/2 MHz)	0	1	1	1	0	0
29	Internal OSC Pre-Divided by 1/2/4/8 Output (25 MHz)	0	1	1	1	0	1
30	Filter0/Edge Detect0 Output	0	1	1	1	1	0

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
31	Filter1/Edge Detect1 Output	0	1	1	1	1	1
32	IO6 Digital or I2C_virtual_0 Input	1	0	0	0	0	0
33	IO7 Digital or I2C_virtual_1 Input	1	0	0	0	0	1
34	I2C_virtual_2 Input	1	0	0	0	1	0
35	I2C_virtual_3 Input	1	0	0	0	1	1
36	I2C_virtual_4 Input	1	0	0	1	0	0
37	I2C_virtual_5 Input	1	0	0	1	0	1
38	I2C_virtual_6 Input	1	0	0	1	1	0
39	I2C_virtual_7 Input	1	0	0	1	1	1
40	ASM-stateX-dout0	1	0	1	0	0	0
41	ASM-stateX-dout1	1	0	1	0	0	1
42	ASM-stateX-dout2	1	0	1	0	1	0
43	ASM-stateX-dout3	1	0	1	0	1	1
44	ASM-stateX-dout4	1	0	1	1	0	0
45	ASM-stateX-dout5	1	0	1	1	0	1
46	ASM-stateX-dout6	1	0	1	1	1	0
47	ASM-stateX-dout7	1	0	1	1	1	1
48	IO9 Digital Input	1	1	0	0	0	0
49	IO10 Digital Input	1	1	0	0	0	1
50	Inverter Output	1	1	0	0	1	0
51	IO12 Digital Input	1	1	0	0	1	1
52	IO13 Digital Input	1	1	0	1	0	0
53	IO14 Digital Input	1	1	0	1	0	1
54	IO15 Digital Input	1	1	0	1	1	0
55	IO16 Digital Input	1	1	0	1	1	1
56	IO17 Digital Input	1	1	1	0	0	0
57	ACMP_0 Output	1	1	1	0	0	1
58	ACMP_1 Output	1	1	1	0	1	0
59	ACMP_2 Output	1	1	1	0	1	1
60	ACMP_3 Output	1	1	1	1	0	0
61	Programmable Delay with Edge Detector Output	1	1	1	1	0	1
62	nRST_core (POR) as matrix input	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

6.2 Matrix Output Table

Table 5. Matrix Output Table

Register Bit Address	Matrix Output Signal Function Note: For each address, the two most significant bits are not used.	Matrix Output Number
[7:0]	Matrix OUT: ASM-state0-EN0	0
[15:8]	Matrix OUT: ASM-state0-EN1	1
[23:16]	Matrix OUT: ASM-state0-EN2	2
[31:24]	Matrix OUT: ASM-state1-EN0	3
[39:32]	Matrix OUT: ASM-state1-EN1	4
[47:40]	Matrix OUT: ASM-state1-EN2	5
[55:48]	Matrix OUT: ASM-state2-EN0	6
[63:56]	Matrix OUT: ASM-state2-EN1	7
[71:64]	Matrix OUT: ASM-state2-EN2	8
[79:72]	Matrix OUT: ASM-state3-EN0	9
[87:80]	Matrix OUT: ASM-state3-EN1	10
[95:88]	Matrix OUT: ASM-state3-EN2	11
[103:96]	Matrix OUT: ASM-state4-EN0	12
[111:104]	Matrix OUT: ASM-state4-EN1	13
[119:112]	Matrix OUT: ASM-state4-EN2	14
[127:120]	Matrix OUT: ASM-state5-EN0	15
[135:128]	Matrix OUT: ASM-state5-EN1	16
[143:136]	Matrix OUT: ASM-state5-EN2	17
[151:144]	Matrix OUT: ASM-state6-EN0	18
[159:152]	Matrix OUT: ASM-state6-EN1	19
[167:160]	Matrix OUT: ASM-state6-EN2	20
[175:168]	Matrix OUT: ASM-state7-EN0	21
[183:176]	Matrix OUT: ASM-state7-EN1	22
[191:184]	Matrix OUT: ASM-state7-EN2	23
[199:192]	Matrix OUT: ASM-state-nRST	24
[207:200]	Matrix OUT: IO1 Digital Output Source	25
[215:208]	Matrix OUT: IO1 Output Enable	26
[223:216]	Matrix OUT: IO2 Digital Output Source	27
[231:224]	Matrix OUT: IO3 Digital Output Source	28
[239:232]	Matrix OUT: IO3 Output Enable	29
[247:240]	Matrix OUT: IO4 Digital Output Source	30
[255:248]	Matrix OUT: IO5 Digital Output Source	31

Register Bit Address	Matrix Output Signal Function Note: For each address, the two most significant bits are not used.	Matrix Output Number
[263:256]	Matrix OUT: IO5 Output Enable	32
[271:264]	Matrix OUT: IO6 Digital Output Source (SCL with VI/Input and NMOS open-drain)	33
[279:272]	Matrix OUT: IO7 Digital Output Source (SDA with VI/Input and NMOS open-drain)	34
[287:280]	Matrix OUT: IO8 Digital Output Source	35
[295:288]	Matrix OUT: IO8 Output Enable	36
[303:296]	Matrix OUT: IO9 Digital Output Source	37
[311:304]	Matrix OUT: IO10 Digital Output Source	38
[319:312]	Matrix OUT: IO10 Output Enable	39
[327:320]	Matrix OUT: Inverter Input	40
[335:328]	Reserved	41
[343:336]	Matrix OUT: IO12 Digital Output Source	42
[351:344]	Matrix OUT: IO13 Digital Output Source	43
[359:352]	Matrix OUT: IO14 Digital Output Source	44
[367:360]	Matrix OUT: IO15 Digital Output Source	45
[375:368]	Matrix OUT: IO15 Output Enable	46
[383:376]	Matrix OUT: IO16 Digital Output Source	47
[391:384]	Matrix OUT: IO16 Output Enable	48
[399:392]	Matrix OUT: IO17 Digital Output Source	49
[407:400]	Matrix OUT: IO17 Output Enable	50
[415:408]	Matrix OUT: ACMP0 PDB (Power-Down)	51
[423:416]	Matrix OUT: ACMP1 PDB (Power-Down)	52
[431:424]	Matrix OUT: ACMP2 PDB (Power-Down)	53
[439:432]	Matrix OUT: ACMP3 PDB (Power-Down)	54
[447:440]	Matrix OUT: Input of Filter_0 with fixed time edge detector	55
[455:448]	Matrix OUT: Input of Filter_1 with fixed time edge detector	56
[463:456]	Matrix OUT: Input of Programmable Delay and Edge Detector	57
[471:464]	Matrix OUT: OSC 25 kHz/2 MHz PD (Power-Down)	58
[479:472]	Matrix OUT: OSC 25 MHz PD (Power-Down)	59
[487:480]	Matrix OUT: IN0 of LUT2_0 or Clock Input of DFF0	60
[495:488]	Matrix OUT: IN1 of LUT2_0 or Data Input of DFF0	61
[503:496]	Matrix OUT: IN0 of LUT2_1 or Clock Input of DFF1	62
[511:504]	Matrix OUT: IN1 of LUT2_1 or Data Input of DFF1	63
[519:512]	Matrix OUT: IN0 of LUT2_2 or Clock Input of DFF2	64
[527:520]	Matrix OUT: IN1 of LUT2_2 or Data Input of DFF2	65

Register Bit Address	Matrix Output Signal Function Note: For each address, the two most significant bits are not used.	Matrix Output Number
[535:528]	Matrix OUT: IN0 of LUT2_3 or Clock Input of PGen	66
[543:536]	Matrix OUT: IN1 of LUT2_3 or nRST of PGen	67
[551:544]	Matrix OUT: IN0 of LUT3_0 or Clock Input of DFF3	68
[559:552]	Matrix OUT: IN1 of LUT3_0 or Data Input of DFF3	69
[567:560]	Matrix OUT: IN2 of LUT3_0 or nRST (nSET) of DFF3	70
[575:568]	Matrix OUT: IN0 of LUT3_1 or Clock Input of DFF4	71
[583:576]	Matrix OUT: IN1 of LUT3_1 or Data Input of DFF4	72
[591:584]	Matrix OUT: IN2 of LUT3_1 or nRST (nSET) of DFF4	73
[599:592]	Matrix OUT: IN0 of LUT3_2 or Clock Input of DFF5	74
[607:600]	Matrix OUT: IN1 of LUT3_2 or Data Input of DFF5	75
[615:608]	Matrix OUT: IN2 of LUT3_2 or nRST (nSET) of DFF5	76
[623:616]	Matrix OUT: IN0 of LUT3_3 or Clock Input of DFF6	77
[631:624]	Matrix OUT: IN1 of LUT3_3 or Data Input of DFF6	78
[639:632]	Matrix OUT: IN2 of LUT3_3 or nRST (nSET) of DFF6	79
[647:640]	Matrix OUT: IN0 of LUT3_4 or Clock Input of DFF7	80
[655:648]	Matrix OUT: IN1 of LUT3_4 or Data Input of DFF7	81
[663:656]	Matrix OUT: IN2 of LUT3_4 or nRST (nSET) of DFF7	82
[671:664]	Matrix OUT: IN0 of LUT3_5 or Delay2 Input (or Counter2 RST Input)	83
[679:672]	Matrix OUT: IN1 of LUT3_5 or External Clock Input of Delay2 (or Counter2)	84
[687:680]	Matrix OUT: IN2 of LUT3_5	85
[695:688]	Matrix OUT: IN0 of LUT3_6 or Delay3 Input (or Counter3 RST Input)	86
[703:696]	Matrix OUT: IN1 of LUT3_6 or External Clock Input of Delay3 (or Counter3)	87
[711:704]	Matrix OUT: IN2 of LUT3_6	88
[719:712]	Matrix OUT: IN0 of LUT3_7 or Delay4 Input (or Counter4 RST Input)	89
[727:720]	Matrix OUT: IN1 of LUT3_7 or External Clock Input of Delay4 (or Counter4)	90
[735:728]	Matrix OUT: IN2 of LUT3_7	91
[743:736]	Matrix OUT: IN0 of LUT3_8 or Delay5 Input (or Counter5 RST Input)	92
[751:744]	Matrix OUT: IN1 of LUT3_8 or External Clock Input of Delay5 (or Counter5)	93
[759:752]	Matrix OUT: IN2 of LUT3_8	94
[767:760]	Matrix OUT: IN0 of LUT3_9 or Delay6 Input (or Counter6 RST Input)	95
[775:768]	Matrix OUT: IN1 of LUT3_9 or External Clock Input of Delay6 (or Counter6)	96
[783:776]	Matrix OUT: IN2 of LUT3_9	97
[791:784]	Matrix OUT: IN0 of LUT3_10 or Input of Pipe Delay	98
[799:792]	Matrix OUT: IN1 of LUT3_10 or nRST of Pipe Delay	99

Register Bit Address	Matrix Output Signal Function Note: For each address, the two most significant bits are not used.	Matrix Output Number
[807:800]	Matrix OUT: IN2 of LUT3_10 or Clock of Pipe Delay	100
[815:808]	Matrix OUT: IN0 of LUT4_0 or Delay0 Input (or Counter0 RST/SET Input)	101
[823:816]	Matrix OUT: IN1 of LUT4_0 or External Clock Input of Delay0 (or Counter0)	102
[831:824]	Matrix OUT: IN2 of LUT4_0 or UP Input of FSM0	103
[839:832]	Matrix OUT: IN3 of LUT4_0 or KEEP Input of FSM0	104
[847:840]	Matrix OUT: IN0 of LUT4_1 or Delay1 Input (or Counter1 RST/SET Input)	105
[855:848]	Matrix OUT: IN1 of LUT4_1 or External Clock Input of Delay1 (or Counter1)	106
[863:856]	Matrix OUT: IN2 of LUT4_1 or UP Input of FSM1	107
[871:864]	Matrix OUT: IN3 of LUT4_1 or KEEP Input of FSM1	108
[879:872]	Matrix OUT: PD of Temperature sensor by register [1269]	109

6.3 Connection Matrix Virtual Inputs

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I^2C address for reading and writing these register values is at byte 0244.

Six of the eight Connection Matrix Virtual Inputs are dedicated to this virtual input function. An I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

Two of the eight Connection Matrix Virtual Inputs are shared with Pin digital inputs, (IO6 Digital or I2C_virtual_0 Input) and (IO7 Digital or I2C_virtual_1 Input). If the virtual input mode is selected, an I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. Two register bits select whether the Connection Matrix input comes from the pin input or from the virtual register:

- register [1074] selects SCL and Virtual Input 0 or IO6
- register [1082] selects SDA and Virtual Input 1 or IO7.

See Table 6 for Connection Matrix Virtual Inputs.

Table 6. Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
32	I2C_virtual_0 Input	[1952]
33	I2C_virtual_1 Input	[1953]
34	I2C_virtual_2 Input	[1954]
35	I2C_virtual_3 Input	[1955]
36	I2C_virtual_4 Input	[1956]
37	I2C_virtual_5 Input	[1957]

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
38	I2C_virtual_6 Input	[1958]
39	I2C_virtual_7 Input	[1959]

6.4 Connection Matrix Virtual Outputs

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via I^2C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I^2C addresses for reading these register values are at bytes 0240 to 0247. Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at byte 0244).

7. Combination Function Macrocells

The SLG47525/28 has 17 combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells.

- Three macrocells that can serve as either 2-bit LUTs or as D Flip Flops
- Five macrocells that can serve as either 3-bit LUTs or as D Flip Flops with Set/Reset Input
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGen)
- Five macrocells that can serve as either 3-bit LUTs or as 8-Bit Counter/Delays
- Two macrocells that can serve as either 4-bit LUTs or as 16-Bit Counter/Delays.

Inputs/Outputs for the 17 combination function macrocells are configured from the Connection Matrix with specific logic functions being defined by the state of NVM bits.

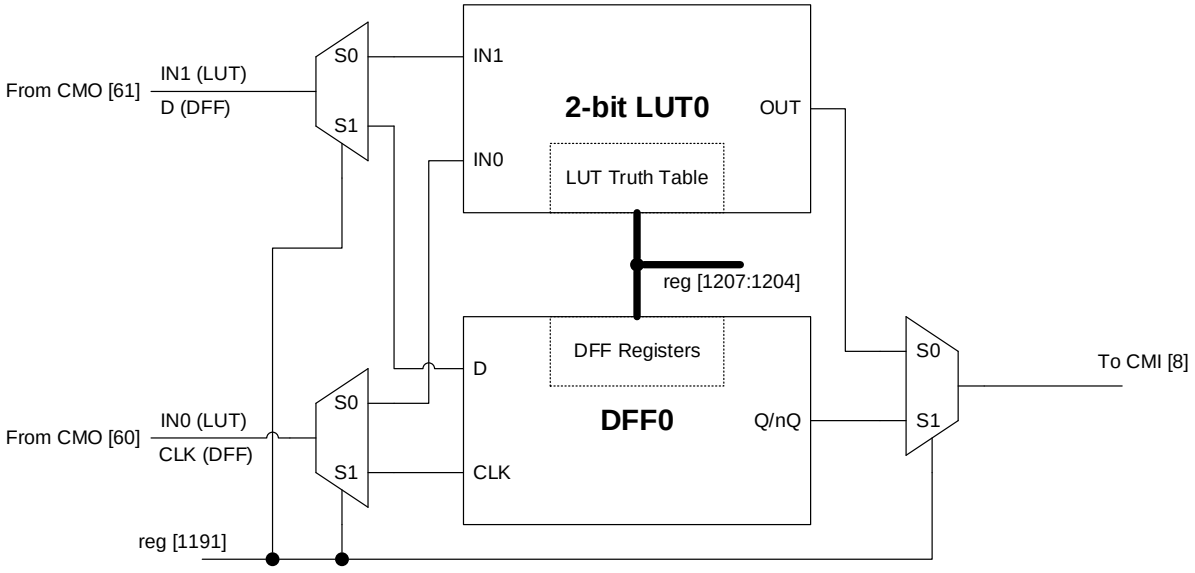
When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user-defined function, including the following standard digital logic devices - AND, NAND, OR, NOR, XOR, XNOR.

7.1 2-Bit LUT or D Flip Flop Macrocells

The 2-bit LUTs each takes in two input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used to implement D Flip-Flop function, the two input signals from the Connection Matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the Connection Matrix.

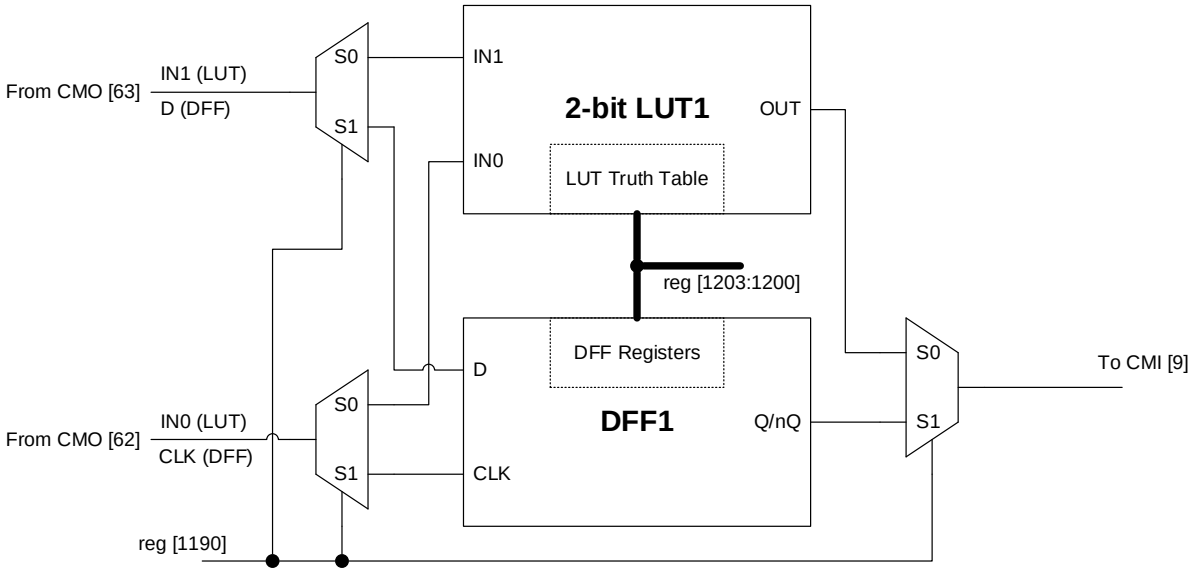
The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

- DFF: CLK is rising edge triggered, then Q = D; otherwise, Q will not change.
- LATCH: when CLK is LOW, then Q = D; otherwise, Q remains its previous value (input D has no effect on the output, when CLK is HIGH).



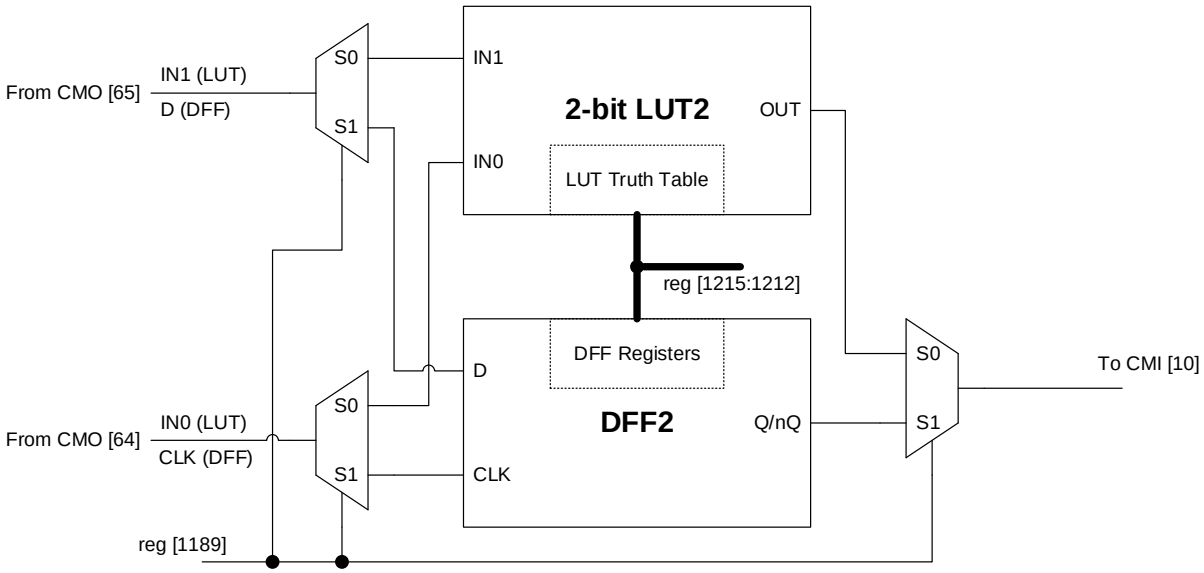
Registers definitions:
reg [1191] → LUT or DFF/Latch select
reg [1207] → DFF or Latch Select
reg [1206] → Output Select (Q or nQ)
reg [1205] → DFF Initial Polarity Select

Figure 16. 2-bit LUT0 or DFF0



Registers definitions:
reg [1190] → LUT or DFF/Latch select
reg [1203] → DFF or Latch Select
reg [1202] → Output Select (Q or nQ)
reg [1201] → DFF Initial Polarity Select

Figure 17. 2-bit LUT1 or DFF1



Registers definitions:
reg [1189] → LUT or DFF/Latch select
reg [1215] → DFF or Latch Select
reg [1214] → Output Select (Q or nQ)
reg [1213] → DFF Initial Polarity Select

Figure 18. 2-bit LUT2 or DFF2

7.1.1. 2-Bit LUT or D Flip Flop Macrocells Used as 2-Bit LUTs

Each Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

- 2-Bit LUT0 is defined by registers [1207:1204]
- 2-Bit LUT1 is defined by registers [1203:1200]
- 2-Bit LUT2 is defined by registers [1215:1212].

Table 7. 2-bit LUT0, LUT1, and LUT2 Truth Table

IN1	IN0	OUT 2-bit LUT0	OUT 2-bit LUT1	OUT 2-bit LUT2	
0	0	register [1204]	register [1200]	register [1212]	LSB
0	1	register [1205]	register [1201]	register [1213]	
1	0	register [1206]	register [1202]	register [1214]	
1	1	register [1207]	register [1203]	register [1215]	MSB

Table 8 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the three 2-bit LUT logic cells.

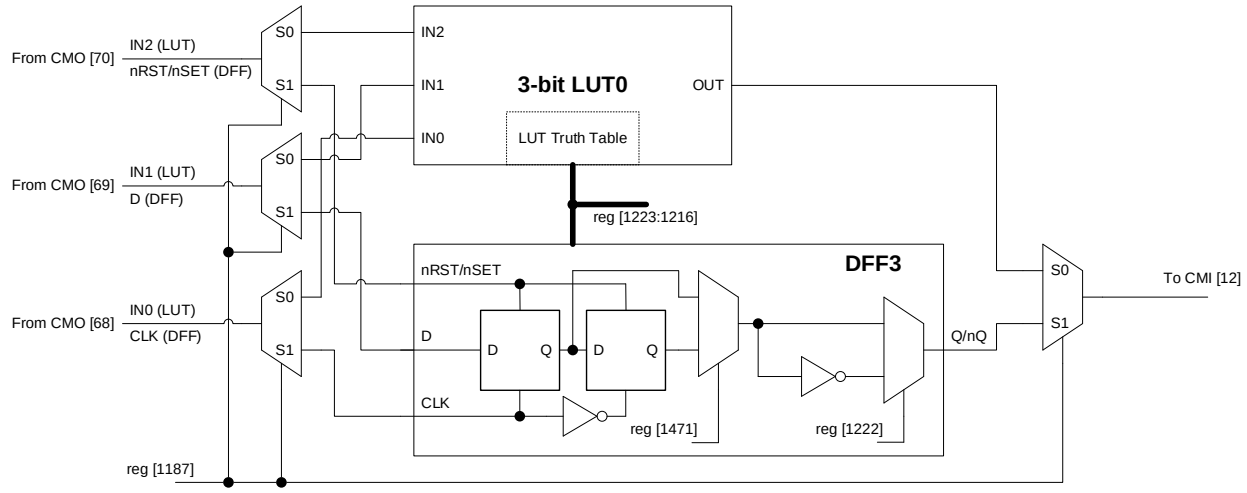
Table 8. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.2 3-Bit LUT or D Flip-Flop with Set/Reset Macrocells

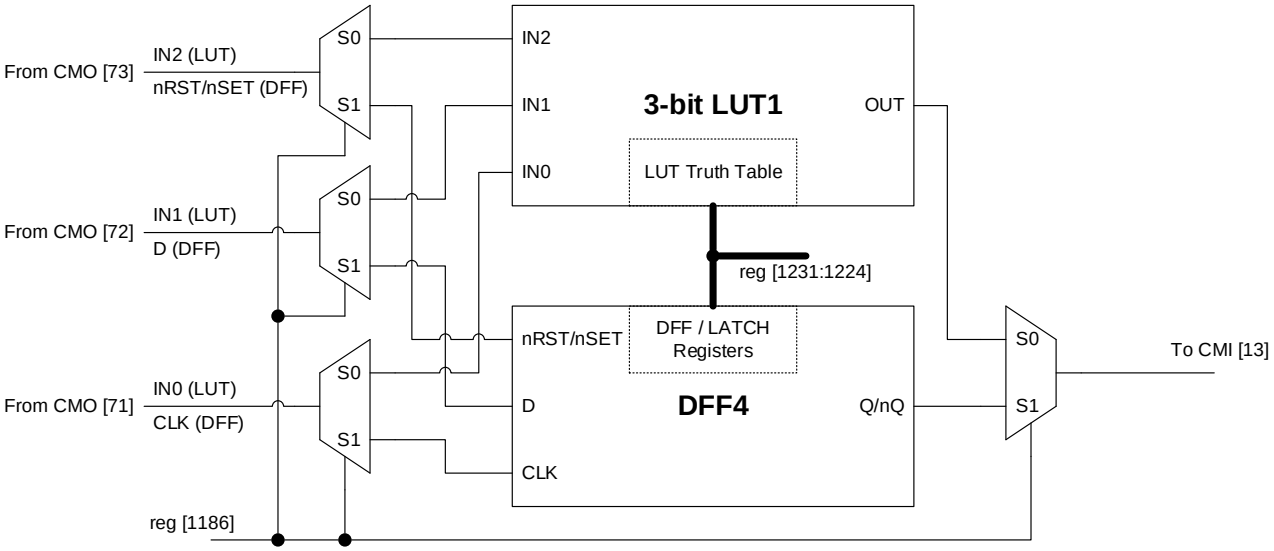
There are five macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each takes in three input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used to implement D Flip-Flop function, the three input signals from the Connection Matrix go to the data (D) and clock (CLK) and Set/Reset (nRST/nSET) inputs for the Flip-Flop, with the output going back to the Connection Matrix.

DFF3 has a user selectable option to allow the macrocell output to either come from the Q/nQ output of one D Flip-Flop, or two D Flip-Flops in series, with the first D Flip-Flop triggering on the rising clock edge, and the second D Flip-Flop triggering on the falling clock edge.



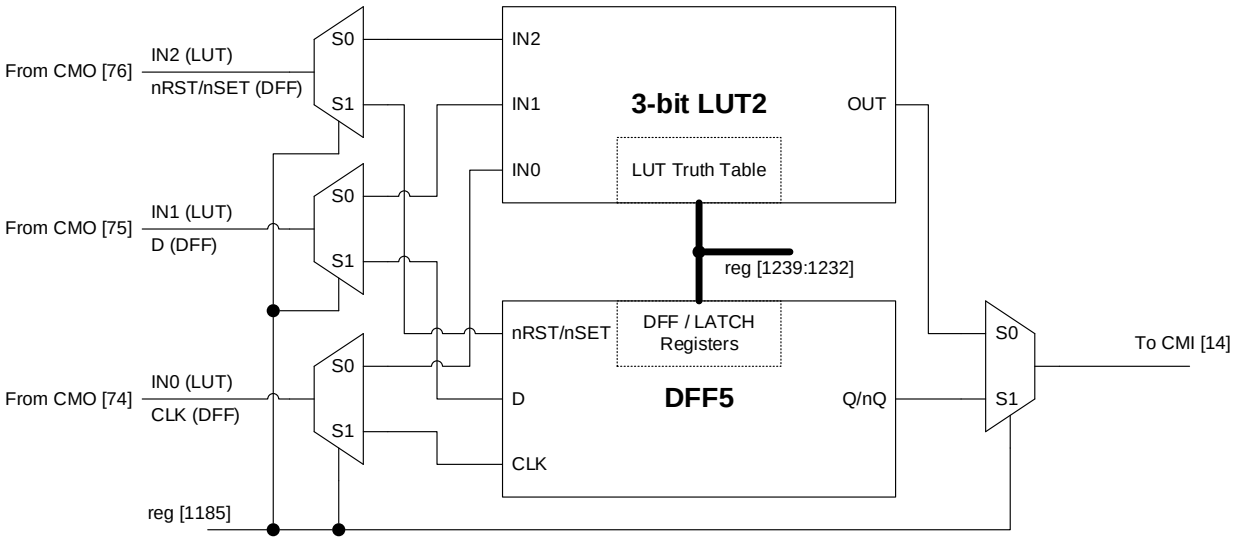
Registers definitions:
reg [1187] → LUT or DFF/Latch select
reg [1223] → DFF or Latch Select
reg [1222] → Output Select (Q or nQ)
reg [1221] → DFF nRST or nSET Select
reg [1220] → DFF Initial Polarity Select
reg [1471] → Selects output from one or two DFF

Figure 19. 3-bit LUT0 or DFF3 with RST/SET



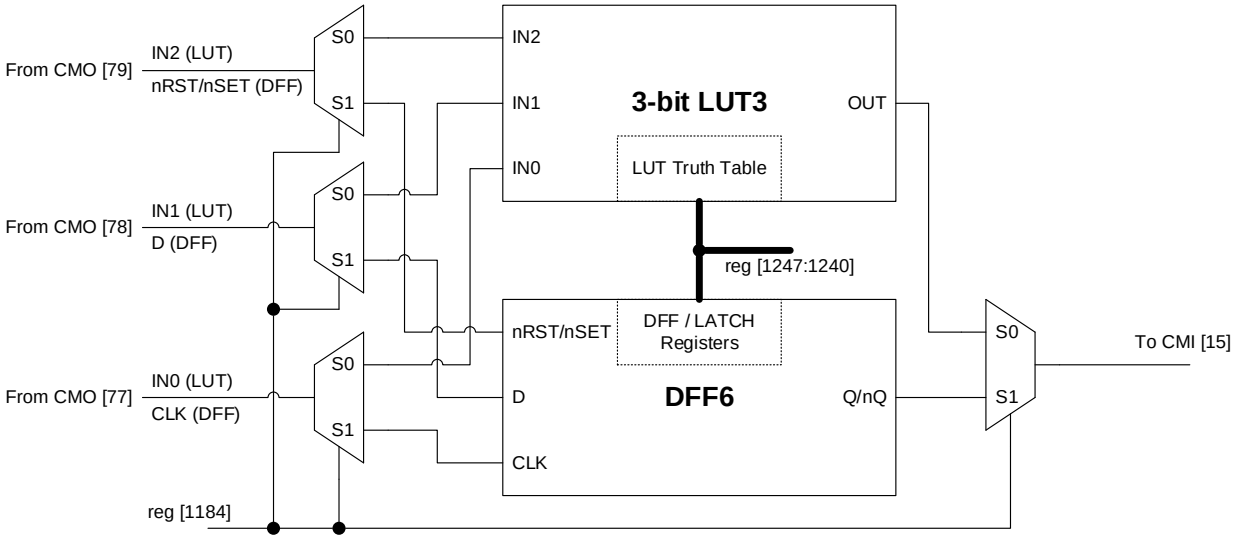
Registers definitions:
reg [1186] → LUT or DFF/Latch select
reg [1231] → DFF or Latch Select
reg [1230] → Output Select (Q or nQ)
reg [1229] → DFF nRST or nSET Select
reg [1228] → DFF Initial Polarity Select

Figure 20. 3-bit LUT1 or DFF4 with RST/SET



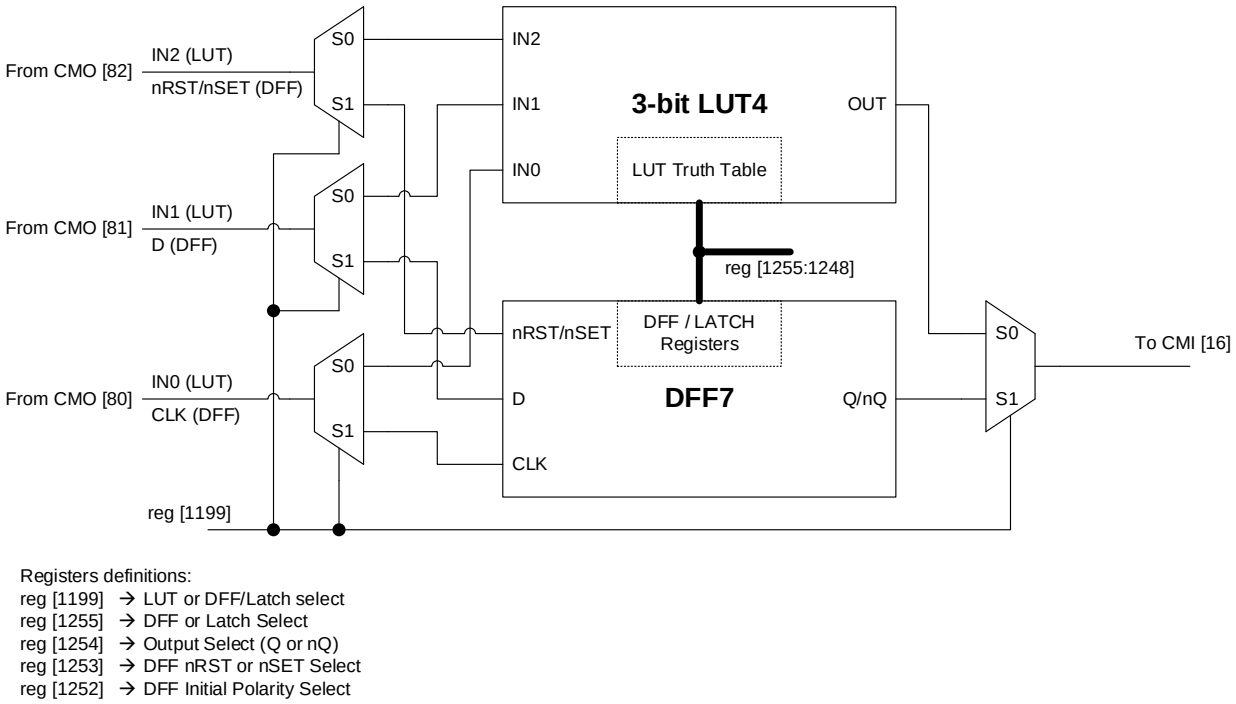
Registers definitions:
reg [1185] → LUT or DFF/Latch select
reg [1239] → DFF or Latch Select
reg [1238] → Output Select (Q or nQ)
reg [1237] → DFF nRST or nSET Select
reg [1236] → DFF Initial Polarity Select

Figure 21. 3-bit LUT2 or DFF5 with RST/SET



Registers definitions:
reg [1184] → LUT or DFF/Latch select
reg [1247] → DFF or Latch Select
reg [1246] → Output Select (Q or nQ)
reg [1245] → DFF nRST or nSET Select
reg [1244] → DFF Initial Polarity Select

Figure 22. 3-bit LUT3 or DFF6 with RST/SET



Registers definitions:
reg [1199] → LUT or DFF/Latch select
reg [1255] → DFF or Latch Select
reg [1254] → Output Select (Q or nQ)
reg [1253] → DFF nRST or nSET Select
reg [1252] → DFF Initial Polarity Select

Figure 23. 3-bit LUT4 or DFF7 with RST/SET

7.2.1. 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Each Macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

- 3-Bit LUT0 is defined by registers [1223:1216]
- 3-Bit LUT1 is defined by registers [1231:1224]
- 3-Bit LUT2 is defined by registers [1239:1232]
- 3-Bit LUT3 is defined by registers [1247:1240]
- 3-Bit LUT4 is defined by registers [1255:1248].

Table 9. 3-bit LUT0 to 3-bit LUT4, 3-bit LUT11 to 3-bit LUT17 Truth Table

IN2	IN1	IN0	OUT 3-bit LUT0	OUT 3-bit LUT1	OUT 3-bit LUT2	OUT 3-bit LUT3	OUT 3-bit LUT4	
0	0	0	register [1216]	register [1224]	register [1232]	register [1240]	register [1248]	LSB
0	0	1	register [1217]	register [1225]	register [1233]	register [1241]	register [1249]	
0	1	0	register [1218]	register [1226]	register [1234]	register [1242]	register [1250]	
0	1	1	register [1219]	register [1227]	register [1235]	register [1243]	register [1251]	
1	0	0	register [1220]	register [1228]	register [1236]	register [1244]	register [1252]	
1	0	1	register [1221]	register [1229]	register [1237]	register [1245]	register [1253]	
1	1	0	register [1222]	register [1230]	register [1238]	register [1246]	register [1254]	
1	1	1	register [1223]	register [1231]	register [1239]	register [1247]	register [1255]	MSB

Table 10 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the twelve 3-bit LUT logic cells.

Table 10. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.3 Initial Polarity Operations

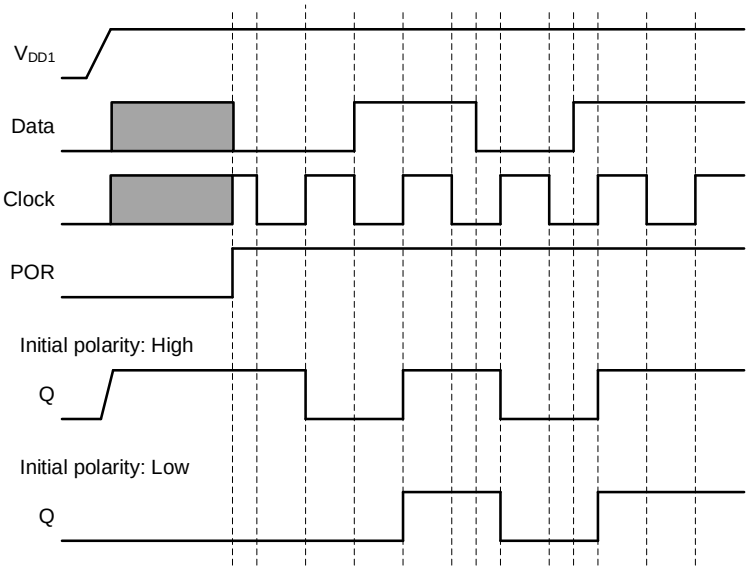


Figure 24. DFF Polarity Operations

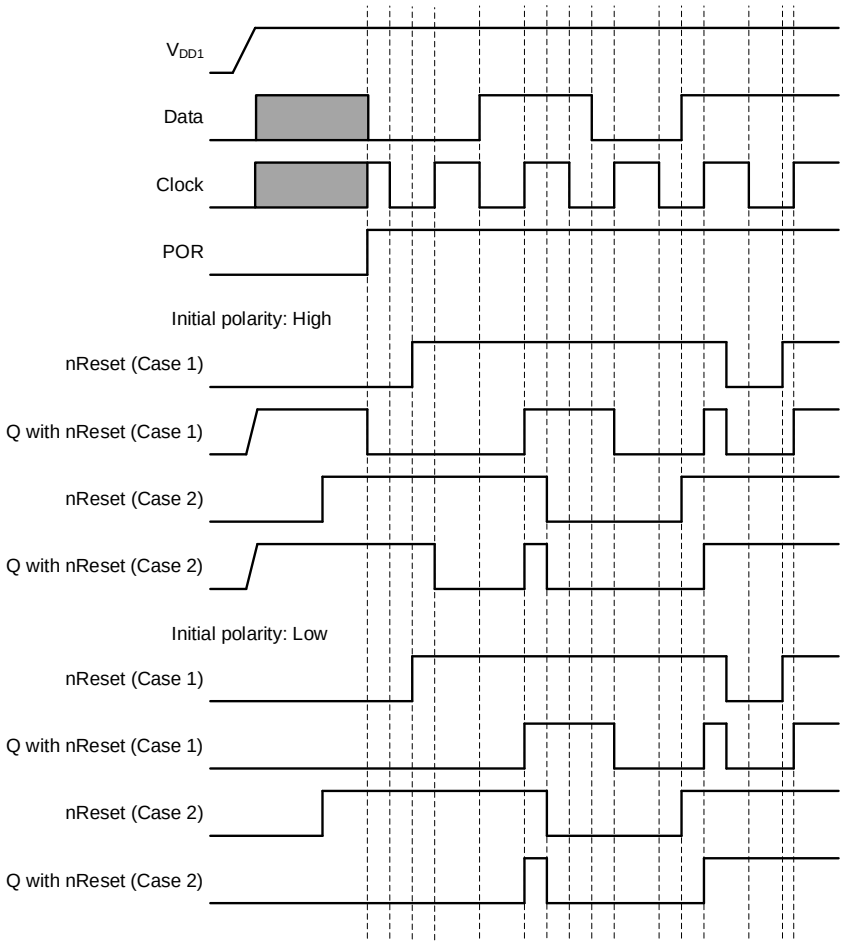


Figure 25. DFF Polarity Operations with nReset

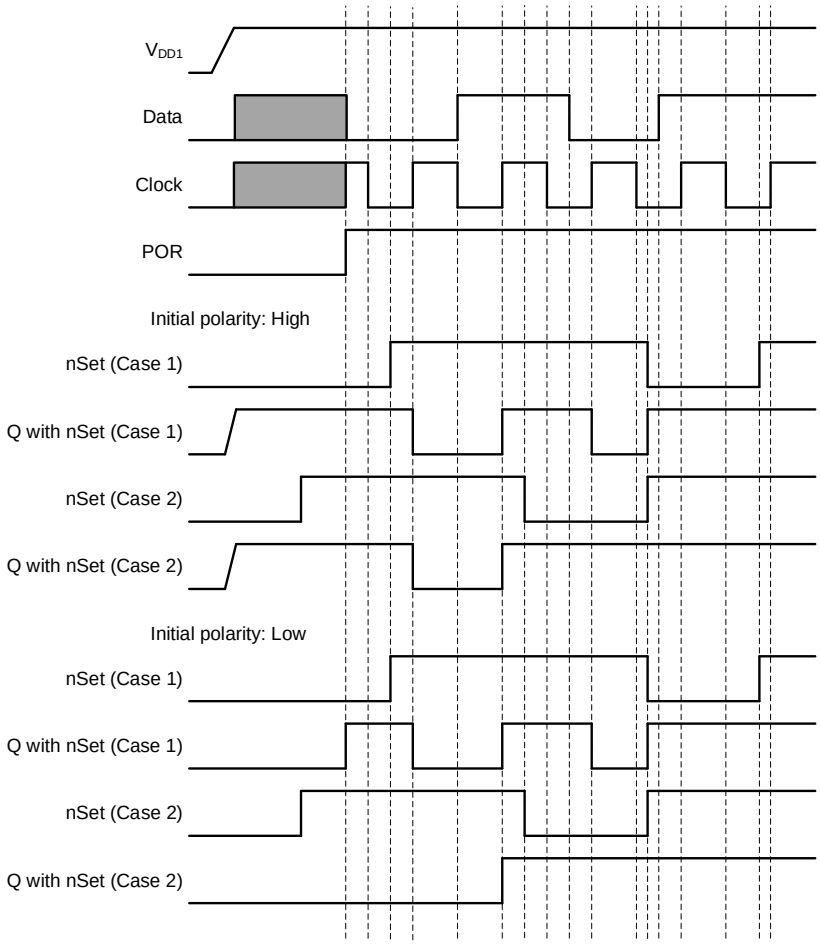


Figure 26. DFF Polarity Operations with nSet

7.4 3-Bit LUT or Pipe Delay Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix.

When used as a Pipe Delay, there are three input signals from the matrix: Input (IN), Clock (CLK), and Reset (nRST). The Pipe Delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series, where the output (Q) of each delay cell goes to the next DFF cell. The first delay option (OUT2) is fixed at the output of the first flip-flop stage. The other two outputs (OUT0 and OUT1) provide user selectable options for 1 to 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 16-input MUX that is controlled by registers [1259:1256] for OUT0 and registers [1263:1260] for OUT1. The 16-input MUX is used to select the amount of delay.

The overall time of the delay is based on the clock used in the SLG47525/28 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the RC Oscillator within the SLG47525/28). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

Note: CLK is rising edge triggered.

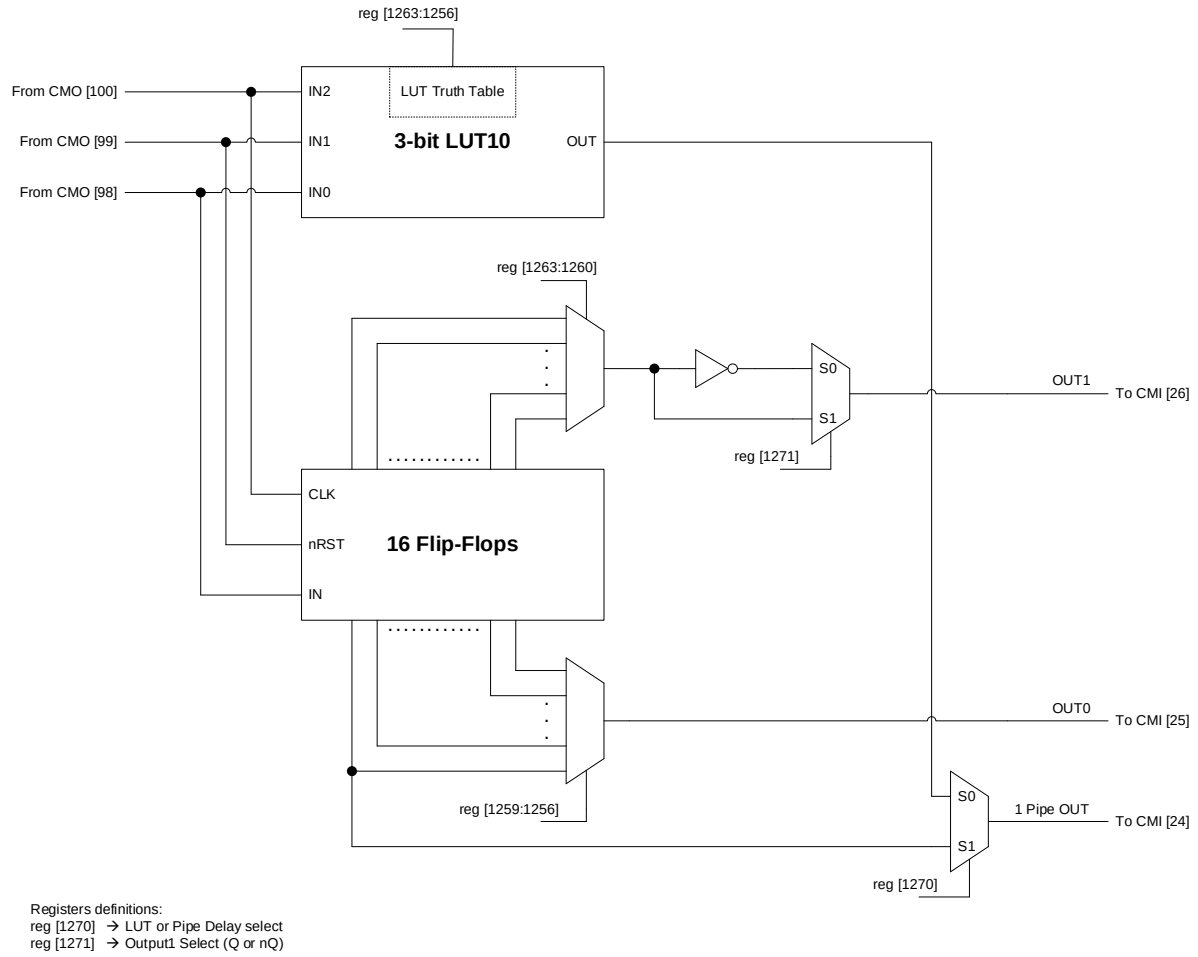


Figure 27. 3-bit LUT10 or Pipe Delay

7.4.1. 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUTs

Each Macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

- 3-Bit LUT10 is defined by registers [1263:1256].

Table 11. 3-bit LUT0 to 3-bit LUT4, 3-bit LUT11 to 3-bit LUT17 Truth Table

IN2	IN1	IN0	OUT 3-bit LUT10	
0	0	0	register [1256]	LSB
0	0	1	register [1257]	
0	1	0	register [1258]	
0	1	1	register [1259]	
1	0	0	register [1260]	
1	0	1	register [1261]	
1	1	0	register [1262]	
1	1	1	register [1263]	MSB

7.5 3-Bit LUT or 8-Bit Counter/Delay Macrocells

There are five macrocells that can serve as either 3-bit LUTs or as Counter/Delays. When used to implement LUT function, the 3-bit LUT takes in three input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used to implement 8-bit Counter/Delay function, two of the three input signals from the Connection Matrix go to the external clock (EXT_CLK) and reset (DLY_IN/CNT_Reset) for the Counter/Delay, with the output going back to the Connection Matrix.

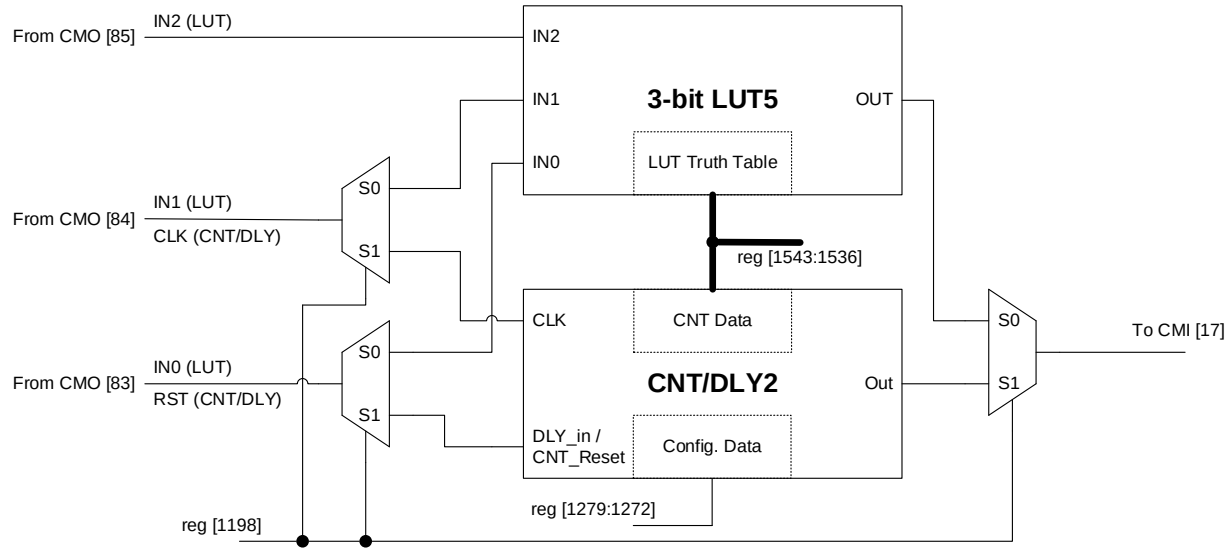
These macrocells can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

These macrocells can also operate in a frequency detection or edge detection mode.

For timing diagrams refer to section 7.7 CNT/DLY/FSM Timing Diagrams.

Note: Counters initialize with counter data after POR.

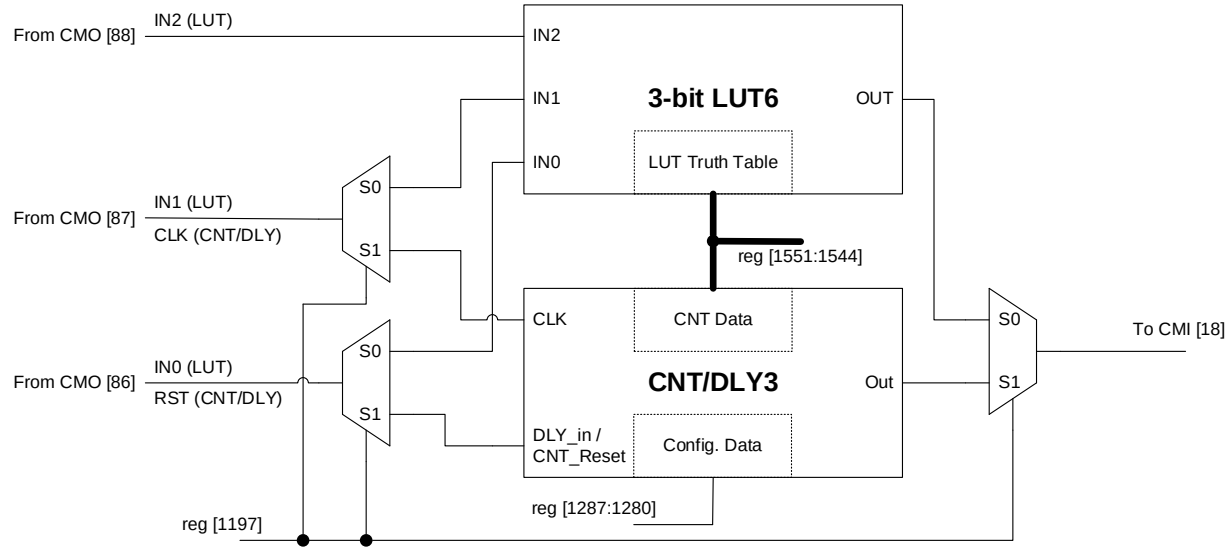
Two of the five macrocells can have their active count value read via I²C (CNT4 and CNT6). See section 16.4.7 Reading Counter Data via I2C for further details.



Registers definitions:

reg [1198]	→ LUT or CNT/DLY select
reg [1279:1278]	→ DLY/CNT Mode Selection
reg [1277]	→ DLY/CNT Output Selection
reg [1276:1274]	→ DLY/CNT Clock Source Select
reg [1273:1272]	→ DLY Mode Select or Asynchronous CNT Reset

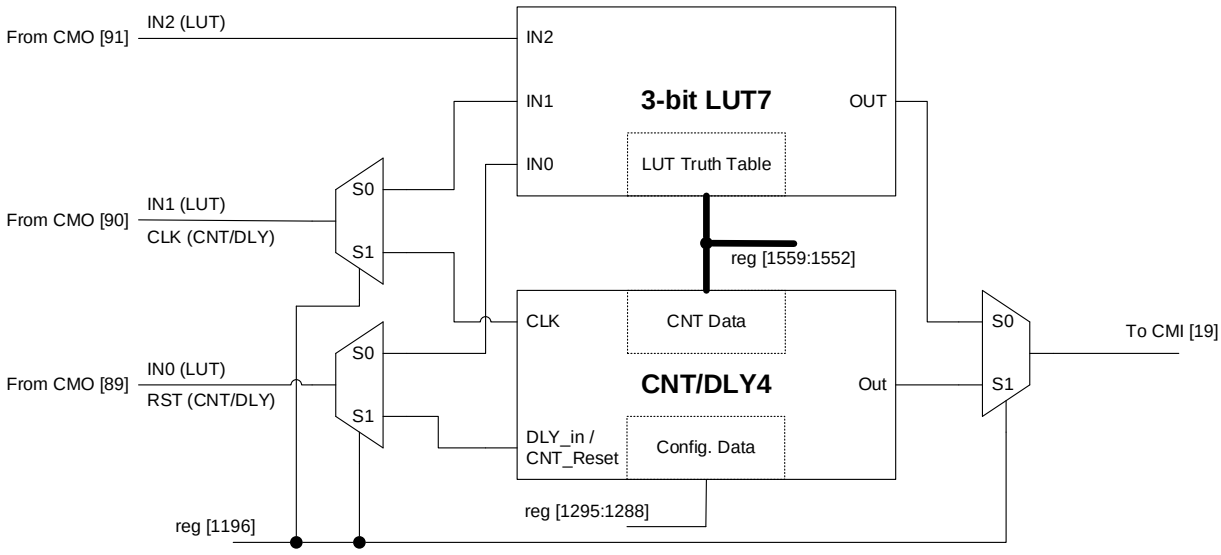
Figure 28. 3-bit LUT5 or CNT/DLY2



Registers definitions:

reg [1197]	→ LUT or CNT/DLY select
reg [1287:1286]	→ DLY/CNT Mode Selection
reg [1285]	→ DLY/CNT Output Selection
reg [1284:1282]	→ DLY/CNT Clock Source Select
reg [1281:1280]	→ DLY Mode Select or Asynchronous CNT Reset

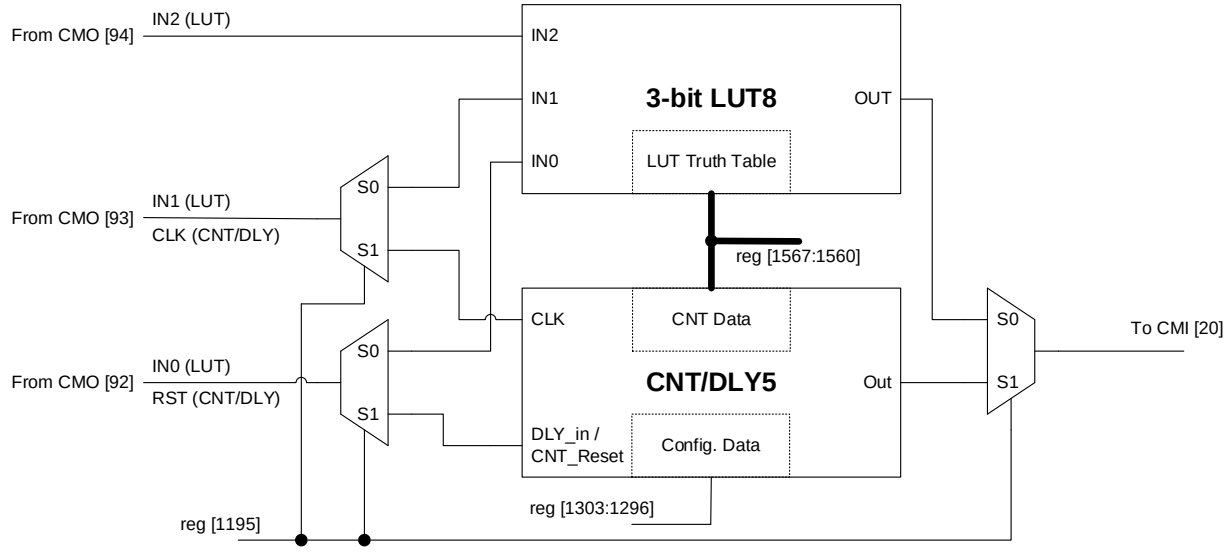
Figure 29. 3-bit LUT6 or CNT/DLY3



Registers definitions:

reg [1196]	→ LUT or CNT/DLY select
reg [1295:1294]	→ DLY/CNT Mode Selection
reg [1293]	→ DLY/CNT Output Selection
reg [1292:1290]	→ DLY/CNT Clock Source Select
reg [1289:1288]	→ DLY Mode Select or Asynchronous CNT Reset

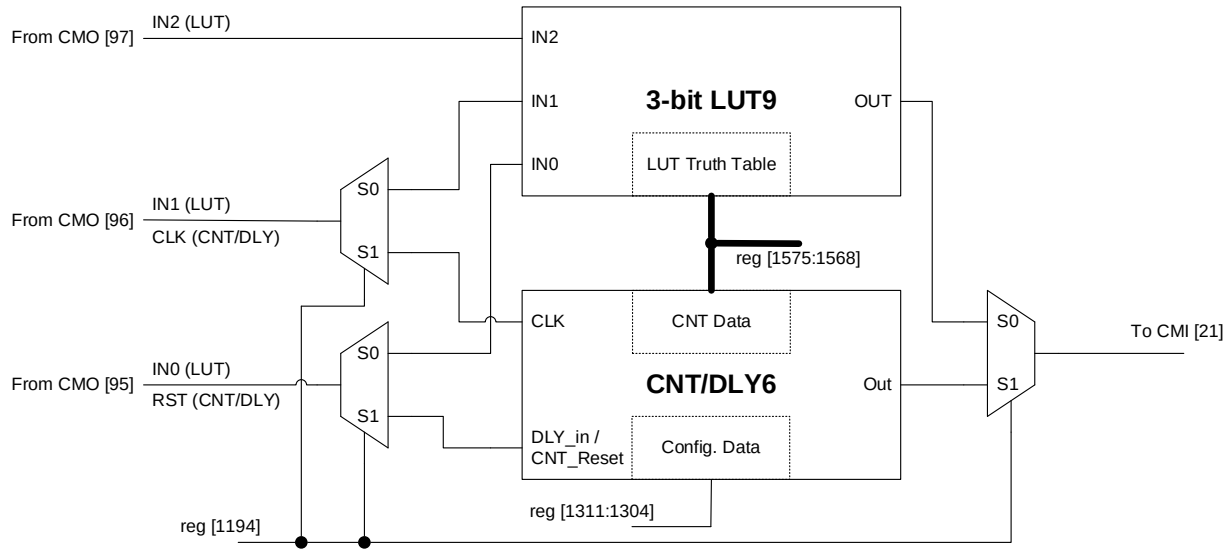
Figure 30. 3-bit LUT7 or CNT/DLY4



Registers definitions:

reg [1195]	→ LUT or CNT/DLY select
reg [1303:1302]	→ DLY/CNT Mode Selection
reg [1301]	→ DLY/CNT Output Selection
reg [1300:1298]	→ DLY/CNT Clock Source Select
reg [1297:1296]	→ DLY Mode Select or Asynchronous CNT Reset

Figure 31. 3-bit LUT8 or CNT/DLY5



Registers definitions:

reg [1194]	→ LUT or CNT/DLY select
reg [1311:1310]	→ DLY/CNT Mode Selection
reg [1309]	→ DLY/CNT Output Selection
reg [1308:1306]	→ DLY/CNT Clock Source Select
reg [1305:1304]	→ DLY Mode Select or Asynchronous CNT Reset

Figure 32. 3-bit LUT9 or CNT/DLY6

7.5.1. 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Each Macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

- 3-Bit LUT5 is defined by registers [1543:1536]
- 3-Bit LUT6 is defined by registers [1551:1544]
- 3-Bit LUT7 is defined by registers [1559:1552]
- 3-Bit LUT8 is defined by registers [1567:1560]
- 3-Bit LUT9 is defined by registers [1575:1568].

Table 12. 3-bit LUT5 to 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT 3-bit LUT5	OUT 3-bit LUT6	OUT 3-bit LUT7	OUT 3-bit LUT8	OUT 3-bit LUT9	
0	0	0	register [1536]	register [1544]	register [1552]	register [1560]	register [1568]	LSB
0	0	1	register [1537]	register [1545]	register [1553]	register [1561]	register [1569]	
0	1	0	register [1538]	register [1546]	register [1554]	register [1562]	register [1570]	
0	1	1	register [1539]	register [1547]	register [1555]	register [1563]	register [1571]	
1	0	0	register [1540]	register [1548]	register [1556]	register [1564]	register [1572]	
1	0	1	register [1541]	register [1549]	register [1557]	register [1565]	register [1573]	
1	1	0	register [1542]	register [1550]	register [1558]	register [1566]	register [1574]	
1	1	1	register [1543]	register [1551]	register [1559]	register [1567]	register [1575]	MSB

Table 13 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the five 3-bit LUT logic cells.

Table 13. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.6 4-Bit LUT or 16-Bit Counter/Delay Macrocells

There are two macrocells that can serve as either 4-bit LUTs or as 16-bit Counter/Delays. When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used to implement 16-Bit Counter/Delay function, four input signals from the Connection Matrix go to the external clock (EXT_CLK) and reset (DLY_IN/CNT_Reset), Keep and Up for the Counter/Delay, with the output going back to the Connection Matrix.

These two macrocells have an optional Finite State Machine (FSM) function. There are two matrix inputs for Up and Keep to support FSM functionality. Any counter within GreenPAK is counting down by default. In FSM mode (CNT/DLY0 and CNT/DLY1), it is possible to reverse counting by applying High level to Up input. Also, there is a possibility to pause counting by applying High level to Keep input, after the level goes LOW, the counter will

proceed counting. These macrocells can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

These macrocells can also operate in a frequency detection mode.

Delay time and Output Period can be calculated using the following formulas:

- Delay time: [(Counter data + 2) / CLK input frequency – Offset (Note 1)]
- Output Period: [(Counter data + 1) / CLK input frequency – Offset (Note 1)].

One Shot pulse width can be calculated using formula:

- Pulse width = [(Counter Data + 2) / CLK input frequency – Offset (Note 1)].

Note 1: Offset is the asynchronous time offset between the input signal and the first clock pulse.

For timing diagrams refer to section 7.7 CNT/DLY/FSM Timing Diagrams.

Note 2: Counters initialize with counter data after POR.

Both macrocells can have their active count value read via I²C. See section 16.4.7 Reading Counter Data via I2C for further details.

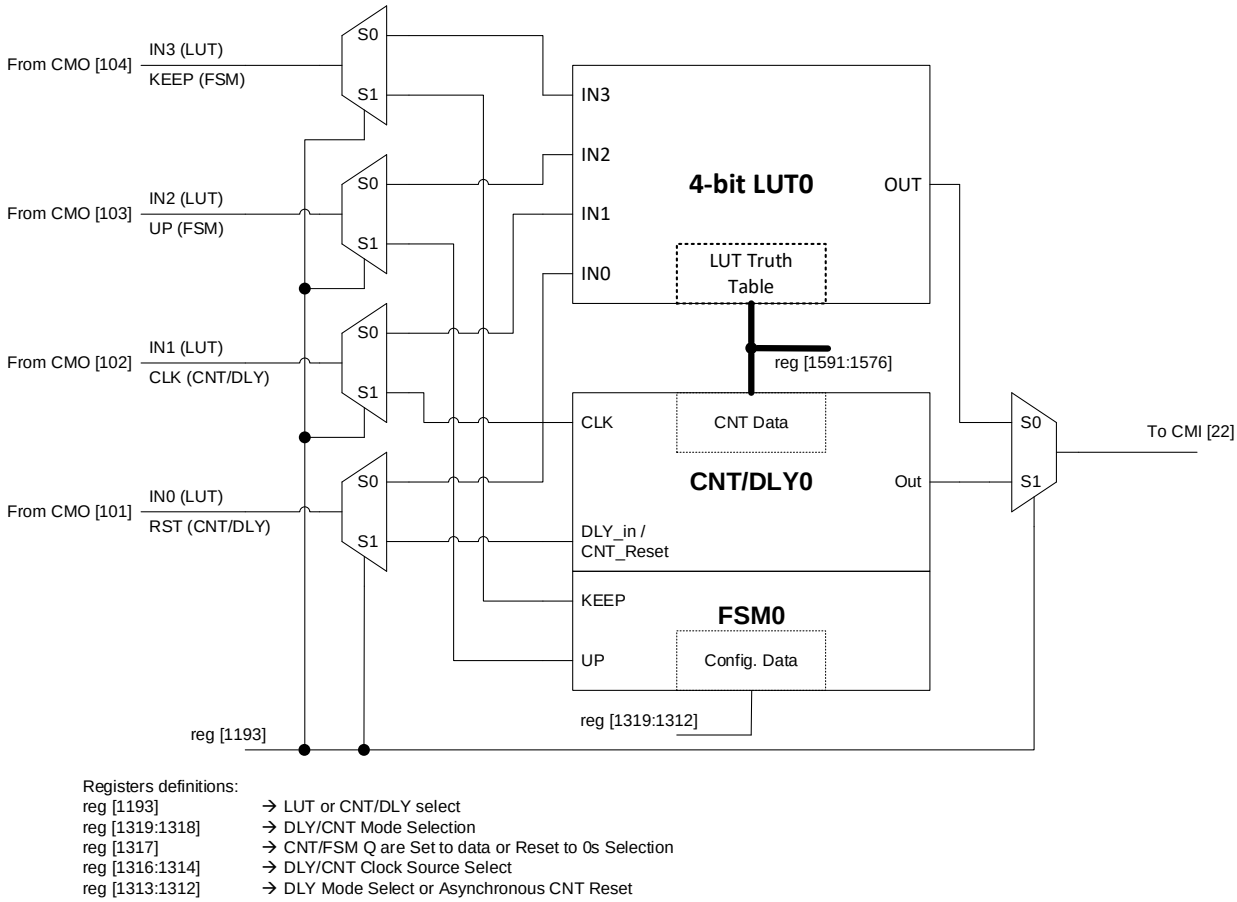


Figure 33. 4-bit LUT0 or CNT/DLY0

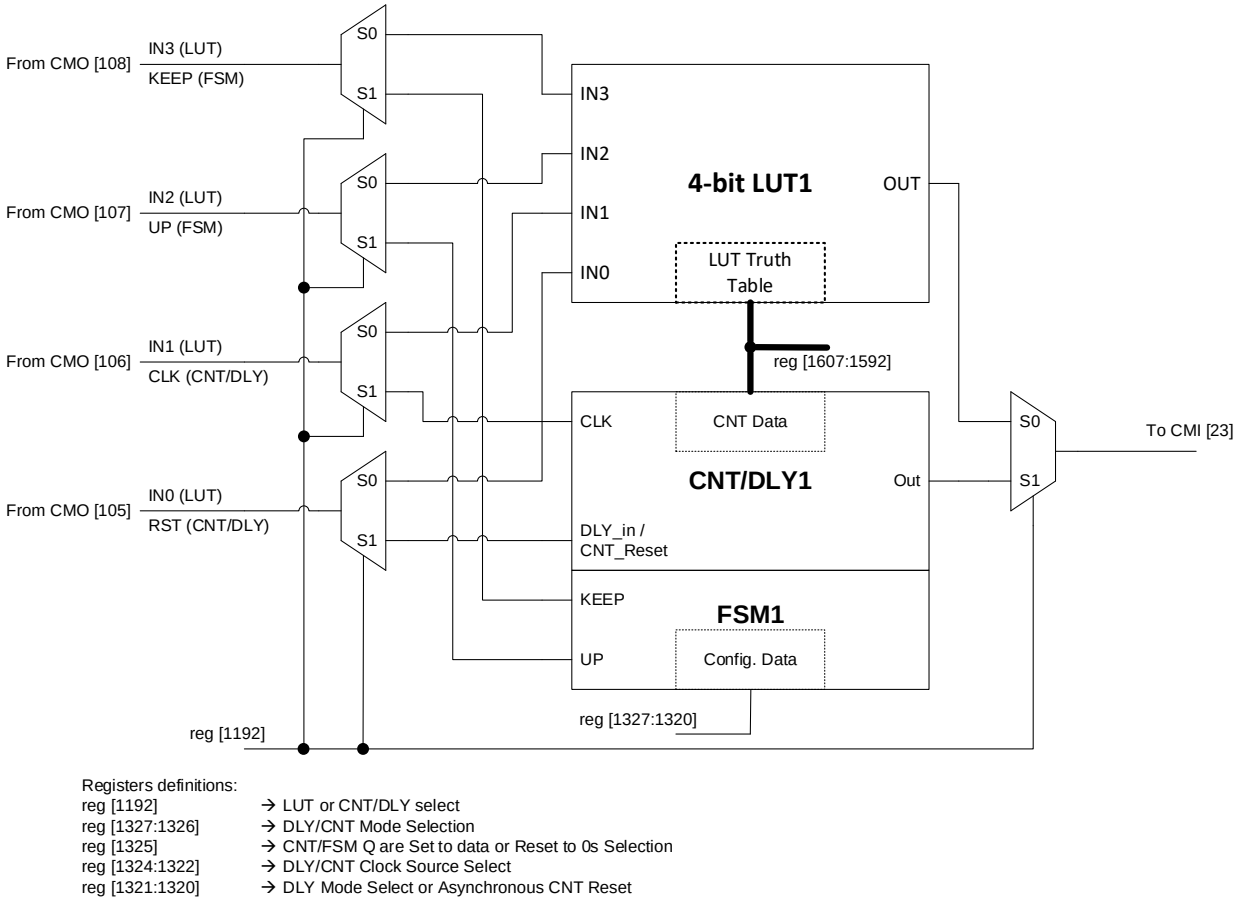


Figure 34. 4-bit LUT1 or CNT/DLY1

7.6.1. 4-Bit LUT or 16-Bit Counter/Delay Macrocells Used as 4-Bit LUTs

Each Macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

- 4-Bit LUT0 is defined by registers [1591:1576]
- 4-Bit LUT1 is defined by registers [1607:1592].

Table 14. 4-bit LUT0 and LUT1 Truth Table

IN3	IN2	IN1	IN0	4-bit LUT0 OUT	4-bit LUT1 OUT	
0	0	0	0	register [1576]	register [1592]	LSB
0	0	0	1	register [1577]	register [1593]	
0	0	1	0	register [1578]	register [1594]	
0	0	1	1	register [1579]	register [1595]	
0	1	0	0	register [1580]	register [1596]	
0	1	0	1	register [1581]	register [1597]	
0	1	1	0	register [1582]	register [1598]	
0	1	1	1	register [1583]	register [1599]	

IN3	IN2	IN1	IN0	4-bit LUT0 OUT	4-bit LUT1 OUT	
1	0	0	0	register [1584]	register [1600]	
1	0	0	1	register [1585]	register [1601]	
1	0	1	0	register [1586]	register [1602]	
1	0	1	1	register [1587]	register [1603]	
1	1	0	0	register [1588]	register [1604]	
1	1	0	1	register [1589]	register [1605]	
1	1	1	0	register [1590]	register [1606]	
1	1	1	1	register [1591]	register [1607]	MSB

Table 15 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 4-bit LUT logic cells.

Table 15. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

7.7 CNT/DLY/FSM Timing Diagrams

7.7.1. Delay Mode (Edge Select: Both, Counter Data: 3) CNT/DLY2 to CNT/DLY6

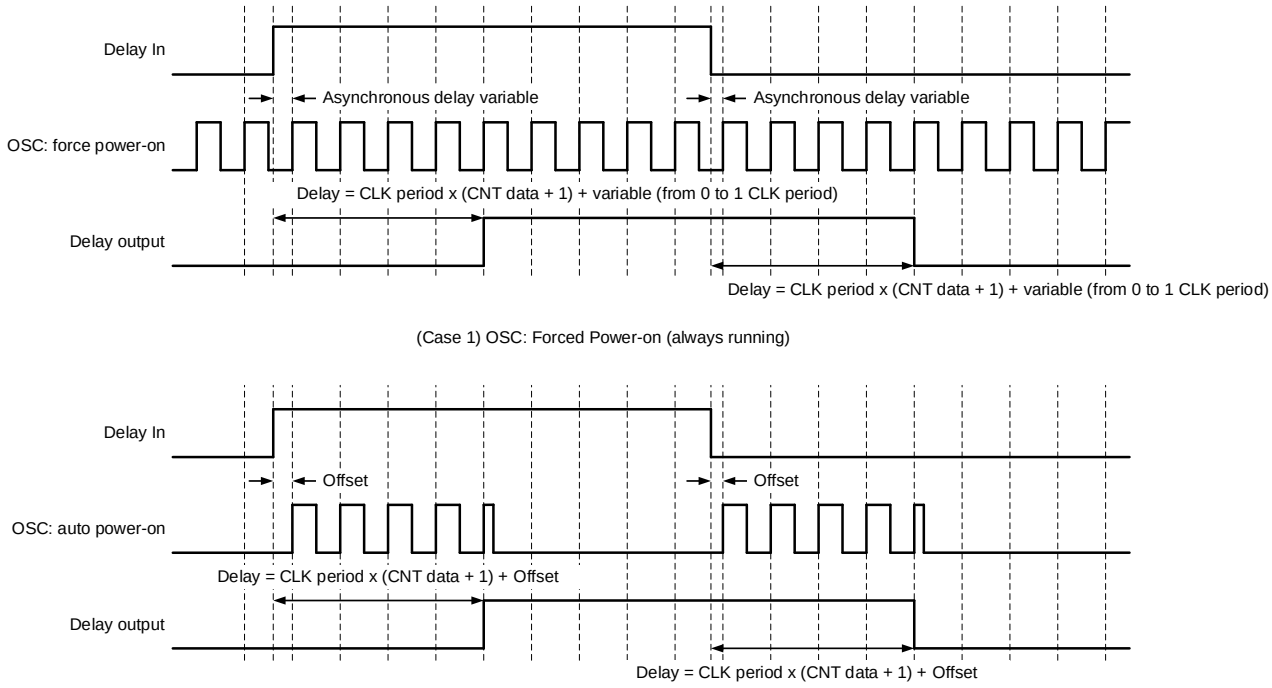


Figure 35. Delay Mode Timing Diagram

7.7.2. Counter Mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY2 to CNT/DLY6

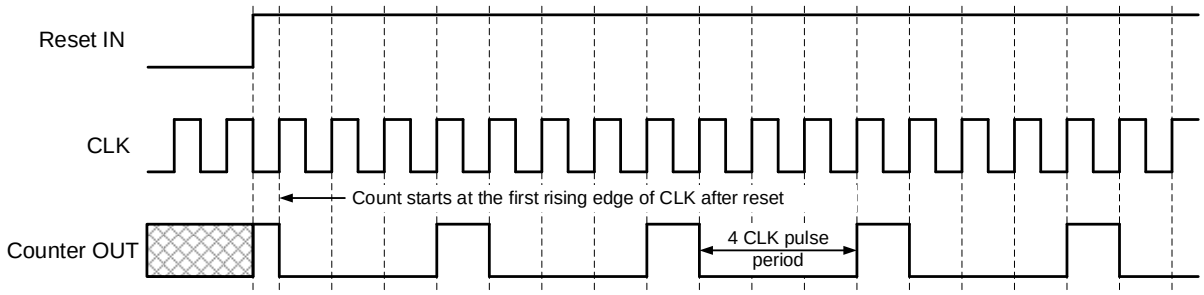


Figure 36. Counter Mode Timing Diagram

7.7.3. One-Shot Mode CNT/DLY0 to CNT/DLY6

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width is determined by counter data and clock selection properties. The output pulse polarity (non-inverted or inverted) is selected by register bit. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

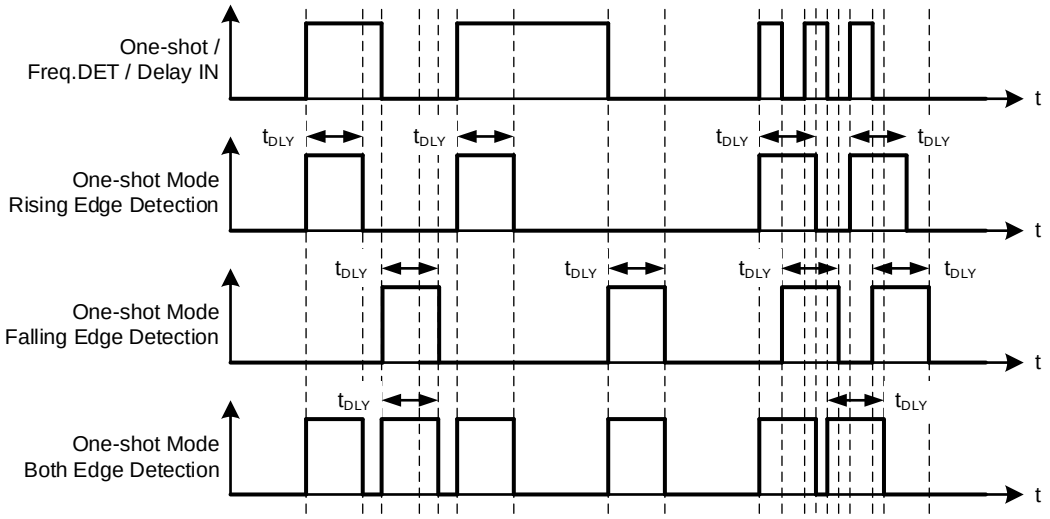


Figure 37. One-Shot Function Timing Diagram

This macrocell generates a High level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is HIGH.

7.7.4. Frequency Detection Mode CNT/DLY0 to CNT/DLY6

Rising Edge: The output goes HIGH if the time between two successive edges is less than the delay. The output goes LOW if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes HIGH if the time between two falling edges is less than the set time. The output goes LOW if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes HIGH if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes LOW if after the last rising/falling edge and specified time the second edge has not come.

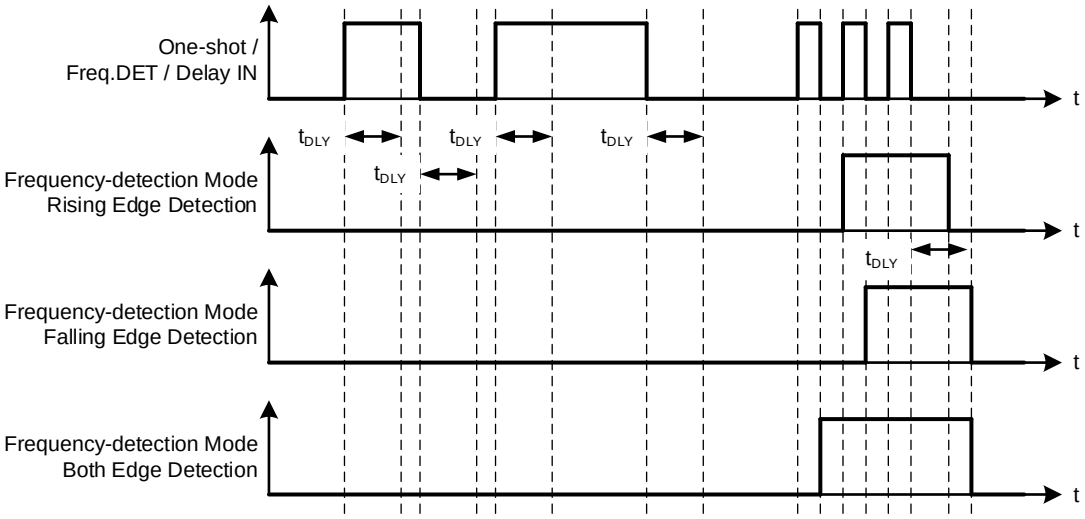


Figure 38. Frequency Detection Mode Timing Diagram

7.7.5. Edge Detection Mode CNT/DLY2 to CNT/DLY6

The macrocell generates High level short pulse when detecting the respective edge. See section 3.4.11 Programmable Delay Expected Typical Delays and Pulse Width.

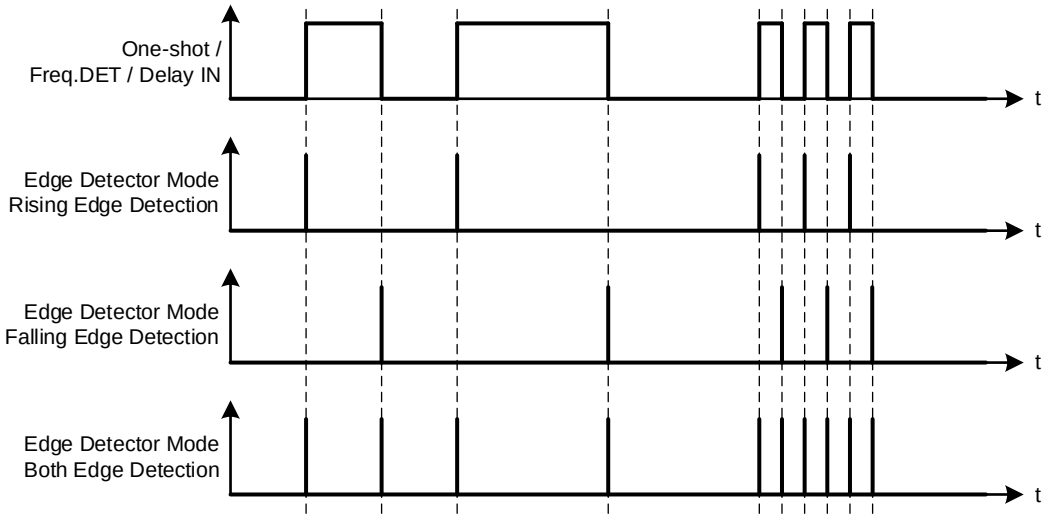


Figure 39. Edge Detection Mode Timing Diagram

7.7.6. Delay Mode CNT/DLY0 to CNT/DLY6

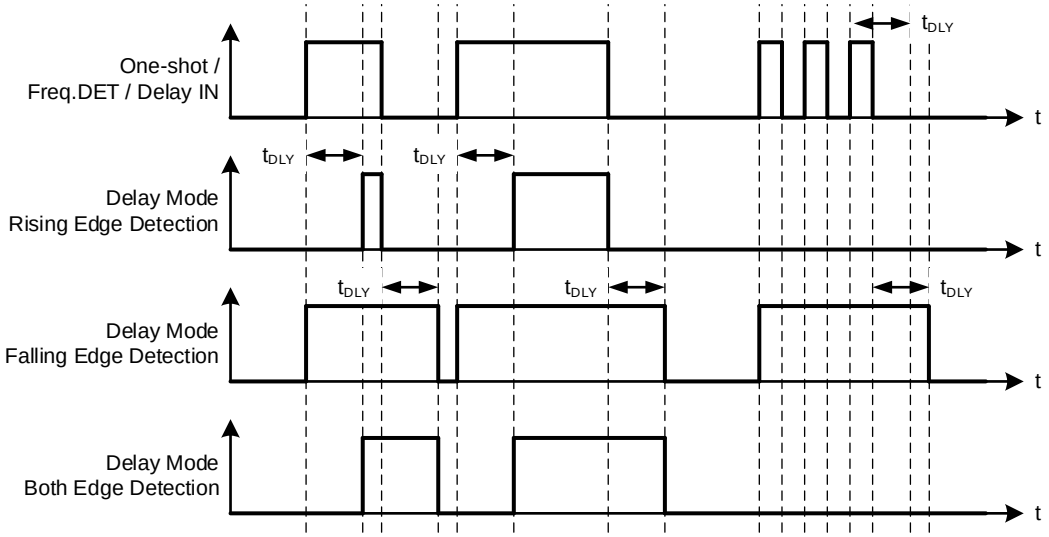
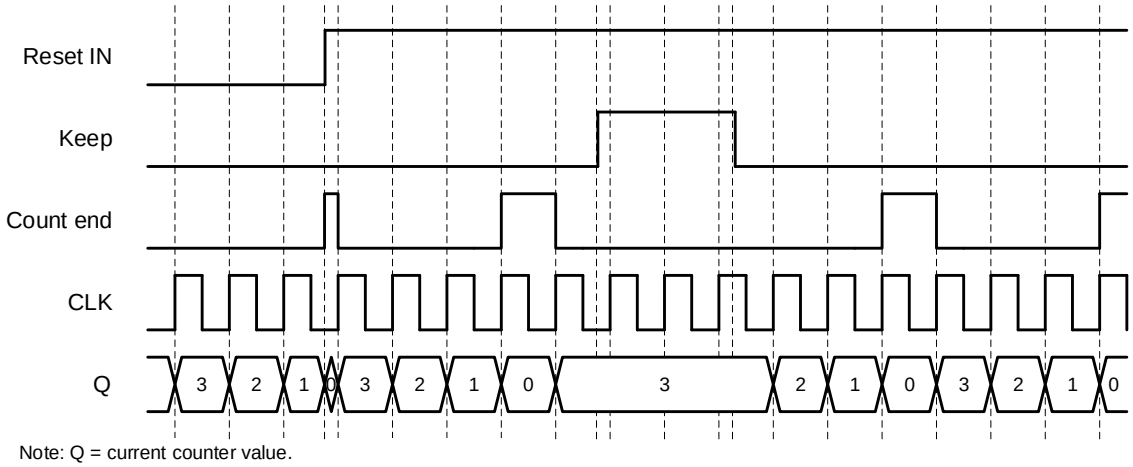


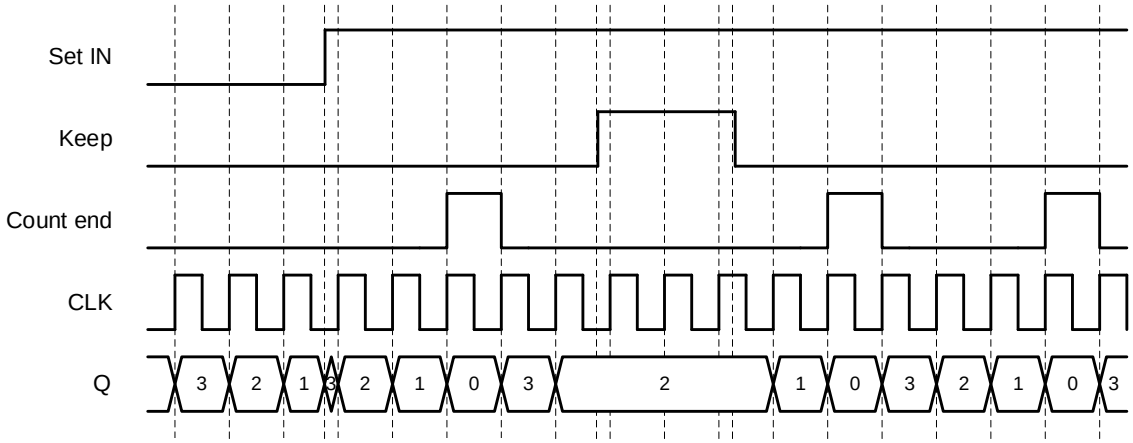
Figure 40. Delay Mode Timing Diagram

7.7.7. CNT/FSM Mode CNT/DLY0, CNT/DLY1



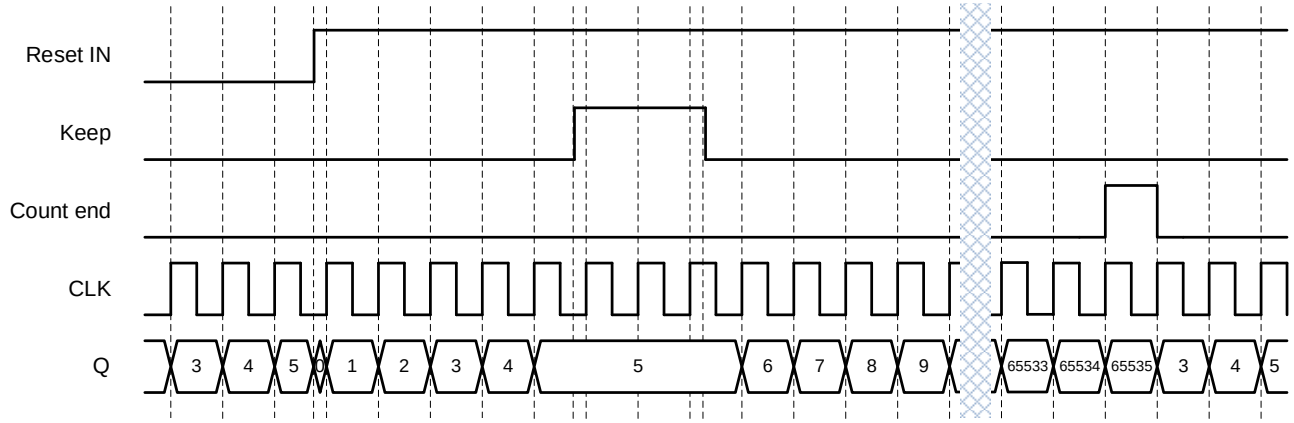
Note: Q = current counter value.

Figure 41. CNT/FSM Timing Diagram (Reset Rising Edge Mode, OSC is Forced On, UP = 0) for CNT Data = 3



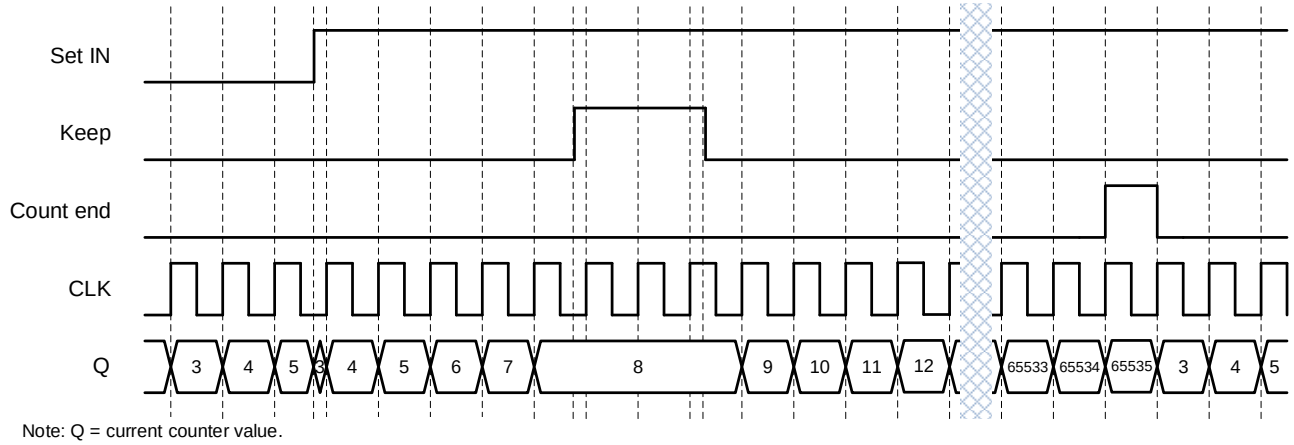
Note: Q = current counter value.

Figure 42. CNT/FSM Timing Diagram (Set Rising Edge Mode, OSC is Forced On, UP = 0) for CNT Data = 3



Note: Q = current counter value.

Figure 43. CNT/FSM Timing Diagram (Reset Rising Edge Mode, OSC is Forced On, UP = 1) for CNT Data = 3



Note: Q = current counter value.

Figure 44. CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 1) for CNT Data = 3

7.7.8. Difference in Counter Value for Counter, Delay, One-Shot, and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. The counter value is shifted for two rising edges of the clock signal in Delay/One-Shot/Frequency Detect modes compared to Counter mode. See Figure 45.

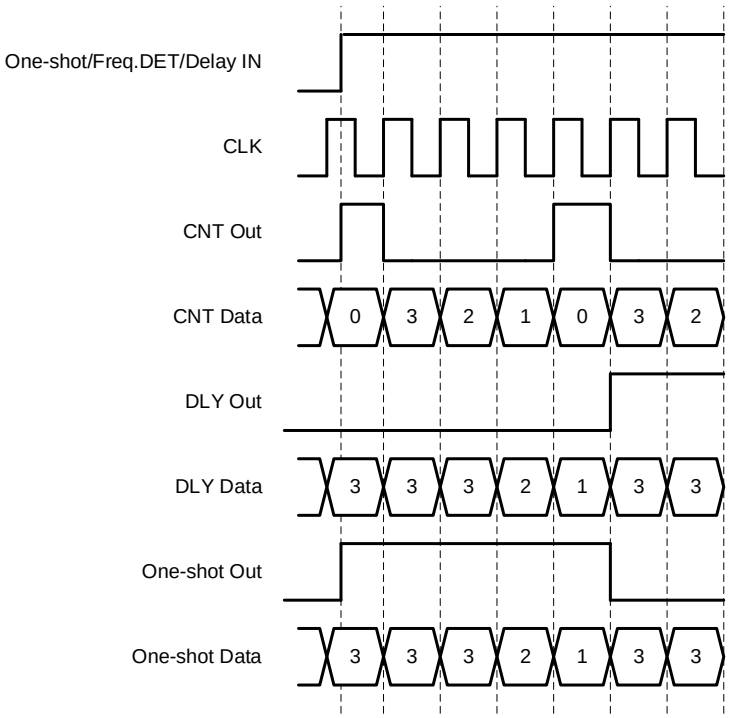


Figure 45. Counter Value, Counter Data = 3

7.8 2-bit LUT or Programmable Pattern Generator

The SLG47525/28 has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or Programmable Pattern Generator (PGen).

When used to implement LUT functions, the 2-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user-defined function, including the following standard digital logic devices - AND, NAND, OR, NOR, XOR, XNOR. The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

When operating as a Programmable Pattern Generator, the output of the macrocell with clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats. See Figure 47.

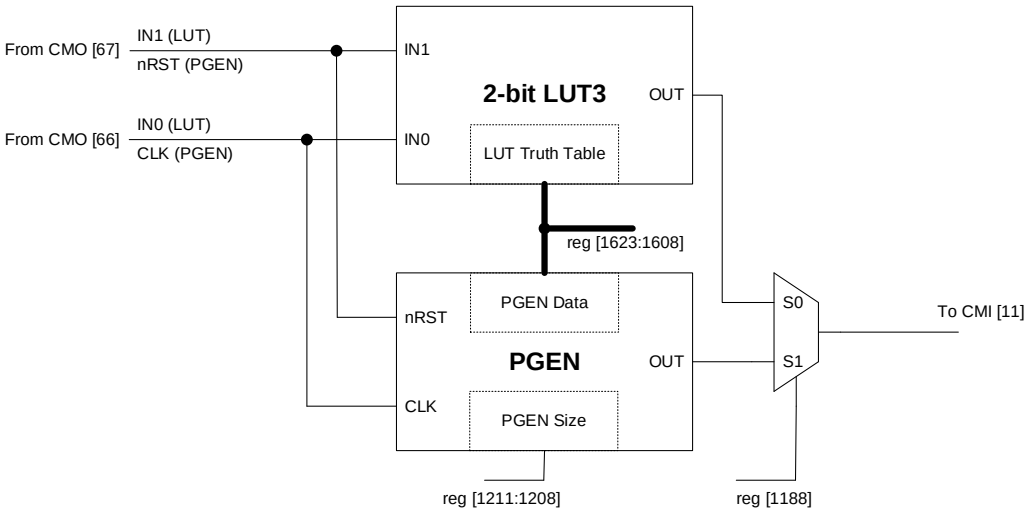


Figure 46. 2-bit LUT3 or PGen

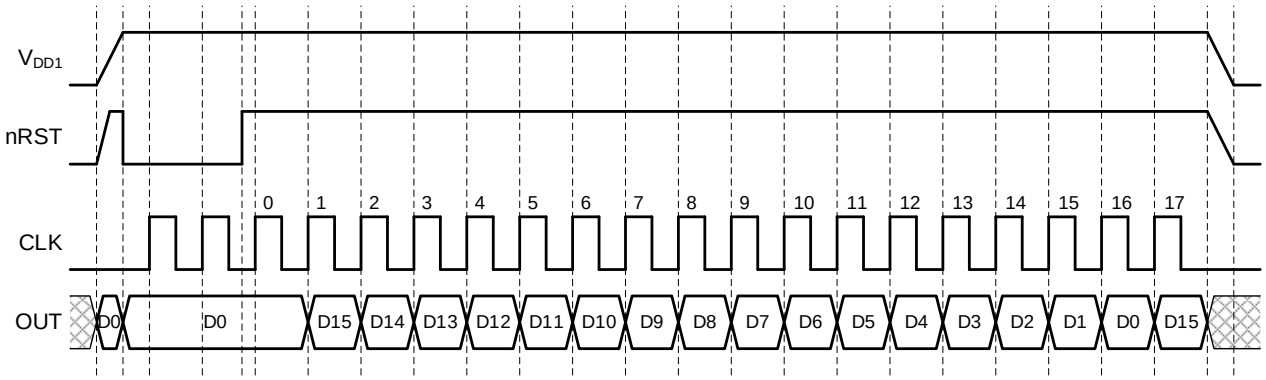


Figure 47. PGen Timing Diagram

7.9 Wake and Sleep Controller

The SLG47525/28 has a Wake and Sleep (WS) function for all ACMPs. The macrocell CNT/DLY0 can be reconfigured for this purpose by setting registers [1319:1318] = 11 and register [1495] = 1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 16-bit counter.

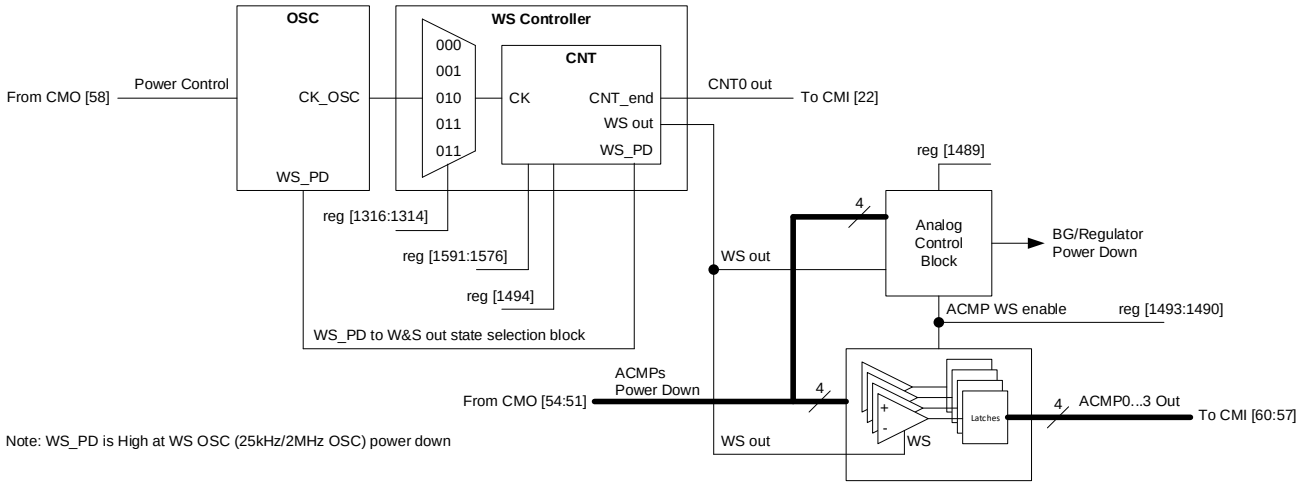


Figure 48. Wake and Sleep Controller

To use any ACMP under WS controller the following settings must be done:

- ACMP Power-Up Input from matrix = 1 (for each ACMP separately)
- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMPs)
- Register WS enable (for each ACMP separately)
- CNT/DLY0 set/reset input = 0 (for all ACMPs)
- In case of using OSC1 (25 MHz), OSC0 must be set to Force Power-On.

Any oscillator with any pre-divider can be used as the OSC. The user can select a period of time while the ACMPs are sleeping in a range of 0 - 65535 clock cycles. Before they are sent to sleep their outputs are latched, so the ACMPs remain their state (HIGH or LOW) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (HIGH/LOW).
  If OSC is powered off (Power-down option is selected; power-down input = 1) and Wake and Sleep Output State = HIGH, the ACMP is continuously ON.
  If OSC is powered off (Power-down option is selected; power-down input = 1) and Wake and Sleep Output State = LOW, the ACMP is continuously OFF.
  Both cases WS function is turned off.

- Counter Data (Range: 0 - 65535).
  The user can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.
- Q mode - defines the state of WS counter data when Set/Reset signal appears.
  Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn the ACMPs on. When Reset signal goes out, the WS counter will go LOW and turn the ACMPs off until the counter counts up to the end.
  Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn the ACMPs off. When Set signal goes out, the WS counter will continue counting and High level signal will turn the ACMPs on while counter is counting up to the end.
- Edge Select defines the edge for Q mode.
  High level Set/Reset - switches mode Set/Reset when level is HIGH.
  Note: Q mode operates only in case of High Level Set/Reset.
- Wake time selection - time required for wake signal to turn the ACMPs on.
  Normal Wake Time - when WS signal is HIGH, it takes a BG time (100/550 µs) to turn the ACMPs on. They will stay ON until WS signal is LOW again. Wake time is one clock period. It should be longer than BG turn on time and minimal required comparing time of the ACMP.
  Short Wake Time - when WS signal is HIGH, it takes a BG time (100/550 µs) to turn the ACMPs on. They will stay ON for 1 µs and turn off regardless of WS signal. The WS signal width does not matter.
- Keep - pauses counting while Keep = 1.
- Up - reverses counting.
  If Up = 1, CNT is counting up from the user selected value to 65535.
  If Up = 0, CNT is counting down from the user selected value to 0.

8. Analog Comparators

There are four Analog Comparator (ACMP) macrocells in the SLG47525/28. For the ACMP cells to be used in a GreenPAK design, the power-up signals (ACMPx_pd) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be always ON, always OFF, or power cycled based on a digital signal coming from the Connection Matrix. Also, all ACMPs have Wake and Sleep function (WS), see section 7.9 Wake and Sleep Controller. When ACMP is powered down, output is LOW.

- PWR UP = 1 - ACMP is powered up.
- PWR UP = 0 - ACMP is powered down.

During ACMP power-up, its output will remain LOW, and then becomes valid 1.03 ms (max) after ACMP power-up signal goes HIGH, see Figure 54. If V_{DD} is greater or equal to 2.7 V, it is possible to decrease turn-on time by setting the BG_OK delay to 100 µs, see Figure 55. The ACMP cells have an input "Low bandwidth" signal selection, which can be used to save power and reduce noise impact when lower bandwidth signals are being compared. To ensure proper chip startup operation, it is recommended to enable the ACMPs with the POR signal, and not the V_{DD} signal.

Note: Regulator and Charge Pump set to automatic ON/OFF.

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources. There is also a selectable gain stage (1x, 0.5x, 0.33x, 0.25x) before connection to the analog comparator. The Gain divider is unbuffered and consists of 250 kΩ (typical) resistors, see Table 16. For gain divider accuracy refer to Table 17. IN- voltage range: 0 V to 1.2 V. To maintain this input range, V_{REF} selection V_{DD}/4 and V_{DD}/3 can be used.

Input bias current < 1 nA (typical).

Table 16. Gain Divider Input Resistance

Gain	x1	x0.5	x0.33	x0.25
Input Resistance	100 MΩ	1 MΩ	0.75 MΩ	1 MΩ

Table 17. Gain Divider accuracy

Gain	x0.5	x0.33	x0.25
Accuracy	±0.51 %	±0.34 %	±0.25 %

Each cell also has a hysteresis selection, to offer hysteresis of 0 mV, 25 mV, 50 mV, or 200 mV. The 50 mV and 200 mV hysteresis options can be used with internal voltage reference only, while 25 mV hysteresis option can be used with both internal and external voltage reference. The 50 mV and 200 mV hysteresis options are one way hysteresis. It means that the actual thresholds will be V_{REF} (high threshold) and V_{REF} - hysteresis (low threshold). The ACMP output will retain its previous value if the input voltage is within threshold window (between V_{REF} and V_{REF} - hysteresis). Note that for the 25 mV hysteresis option threshold levels will be V_{REF} + hysteresis/2 (high threshold) and Vref – hysteresis/2 (low threshold).

Note: Any ACMP powered on enables the Bandgap internal circuit as well. An analog voltage will appear on V_{REF} even when the Force Bandgap option is set as Disabled.

For high input impedance, when using the gain divider (x0.25, x0.33, x0.5), it is possible to use the input buffer. However, this will add some offset, see Figure 56 to Figure 57. It is not recommended to use ACMP buffer when V_{DD} < 2.5 V.

Table 18. Built-In Hysteresis Tolerance at T = 25 °C

V_{HYS}, (mV)	V_{DD} = 1.7 V to 1.8 V						V_{DD} = 1.89 V to 5.5 V					
	V_{REF} = 50 mV to 500 mV		V_{REF} = 550 mV to 1000 mV		V_{REF} = 1050 mV to 1200 mV		V_{REF} = 50 mV to 500 mV		V_{REF} = 550 mV to 1000 mV		V_{REF} = 1050 mV to 1200 mV	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
25	8.6	32.2	8.6	32.3	7.0	32.5	8.5	32.3	8.5	32.3	7.8	34.0
50	44.8	56.5	43.9	56.7	42.7	56.4	44.2	56.8	43.6	57.3	43.1	56.0
200	192.8	207.9	194.0	208.0	192.7	205.4	192.0	208.6	193.0	209.5	190.8	207.7

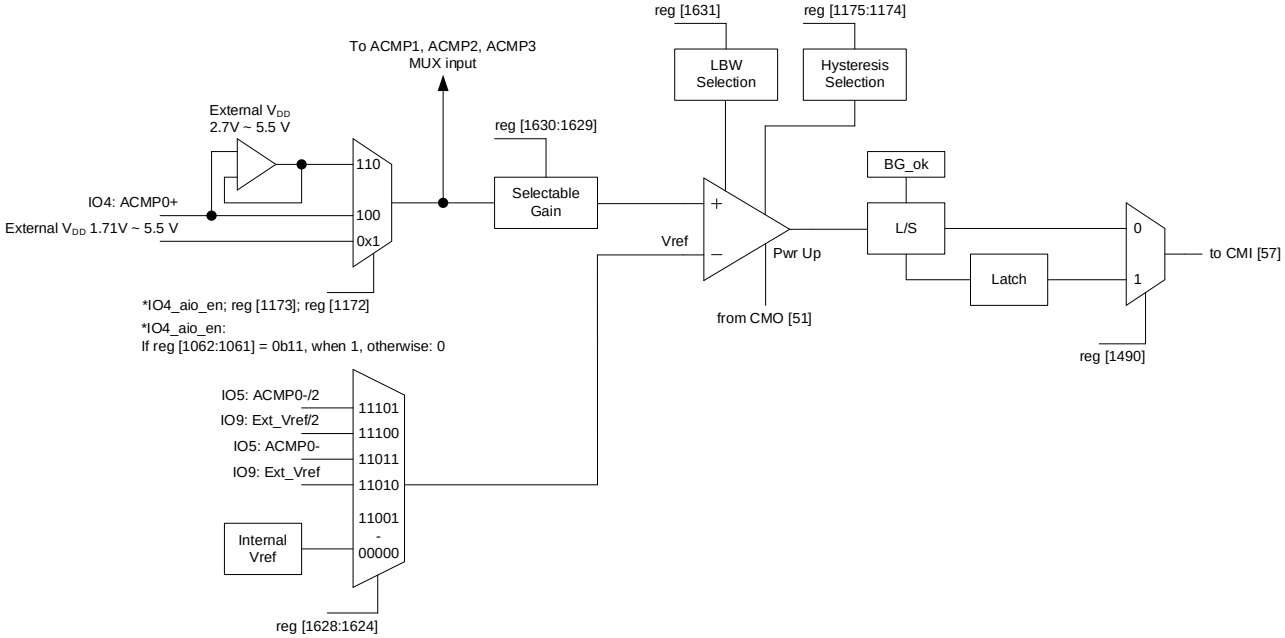
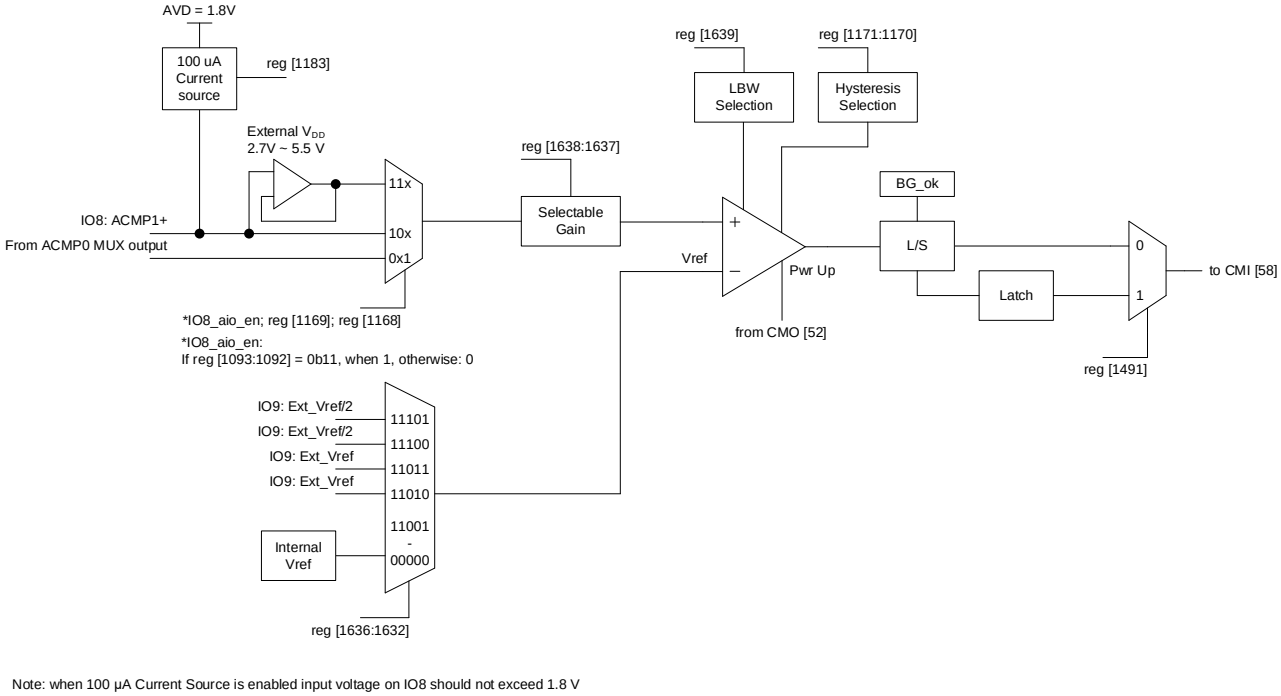


Figure 49. ACMP0 Block Diagram



Note: when 100 µA Current Source is enabled input voltage on IO8 should not exceed 1.8 V

Figure 50. ACMP1 Block Diagram

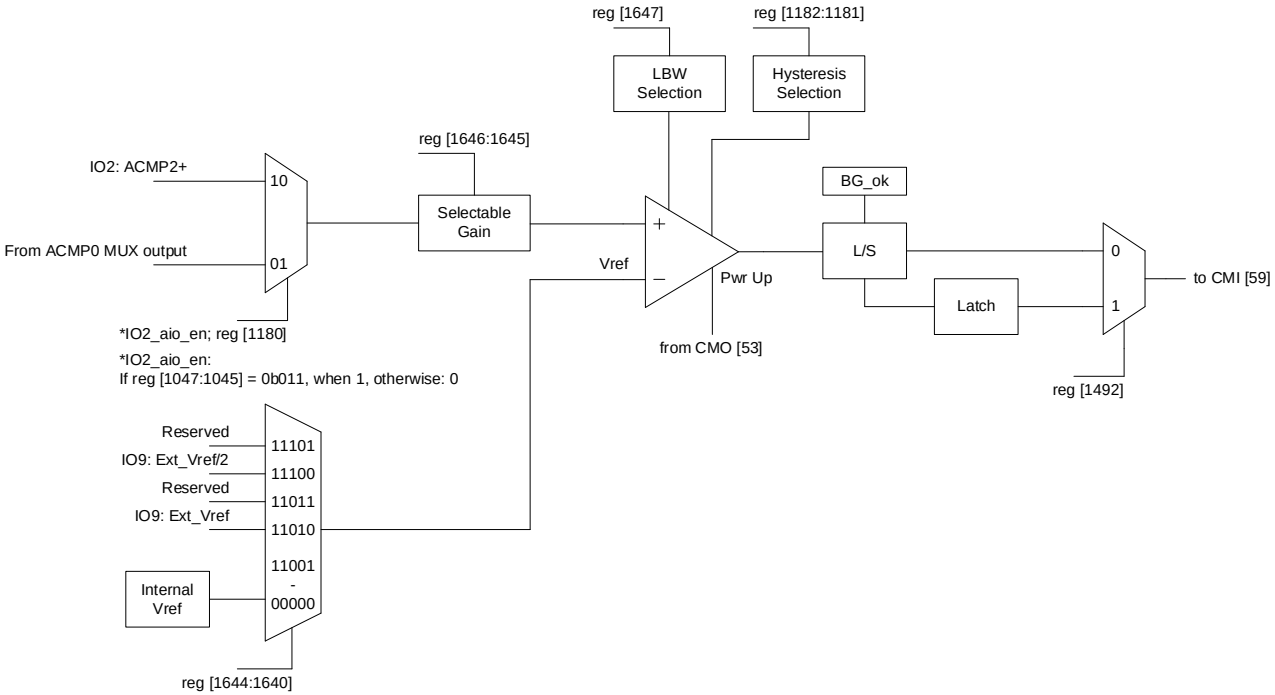


Figure 51. ACMP2 Block Diagram

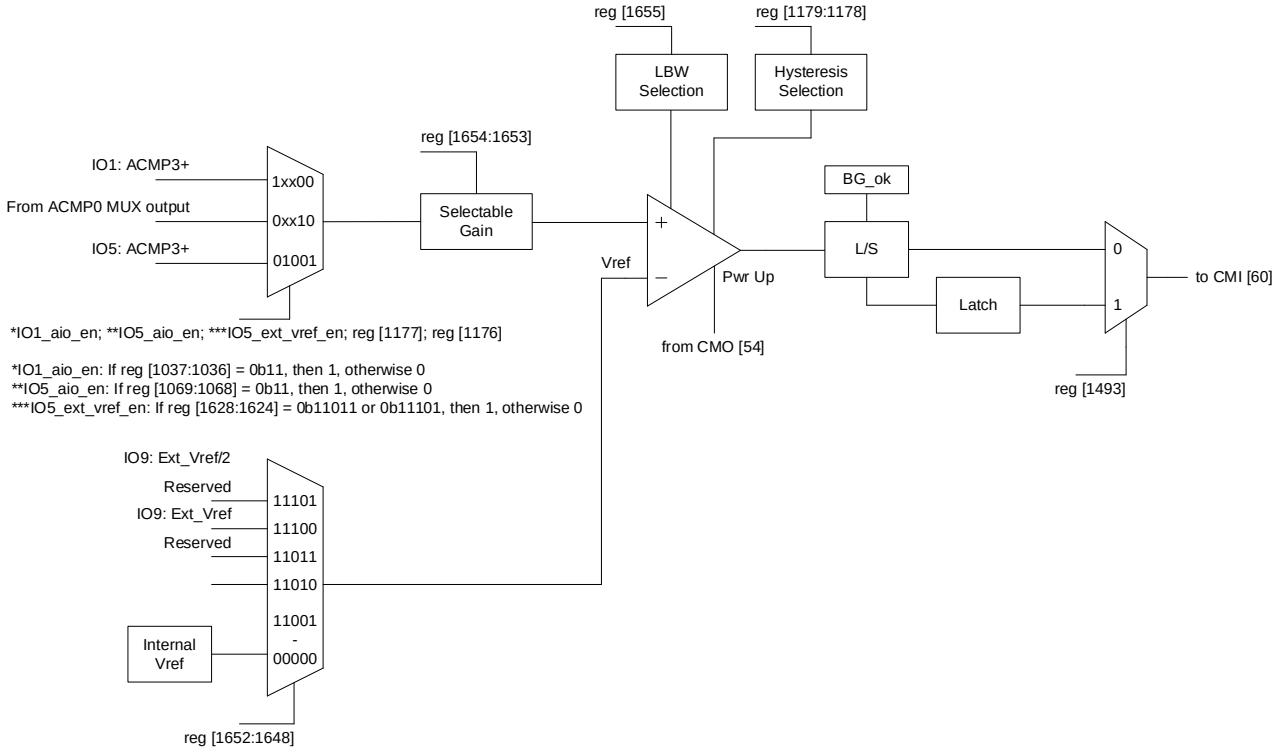


Figure 52. ACMP3 Block Diagram

8.1 ACMP Typical Performance

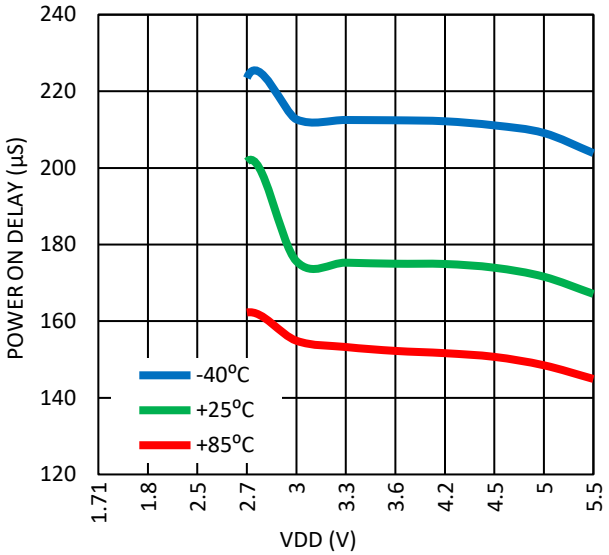


Figure 53. Maximum Power-On Delay vs. V_{DD}, BG = Auto-Delay

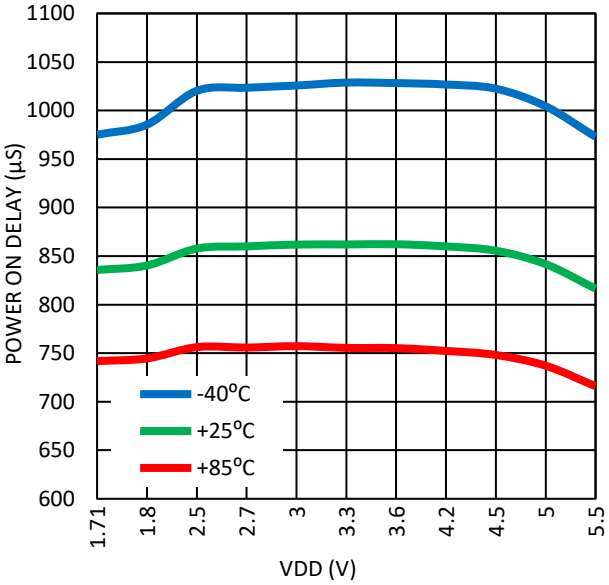


Figure 54. Maximum Power-On Delay vs. V_{DD}, BG = 550 µs

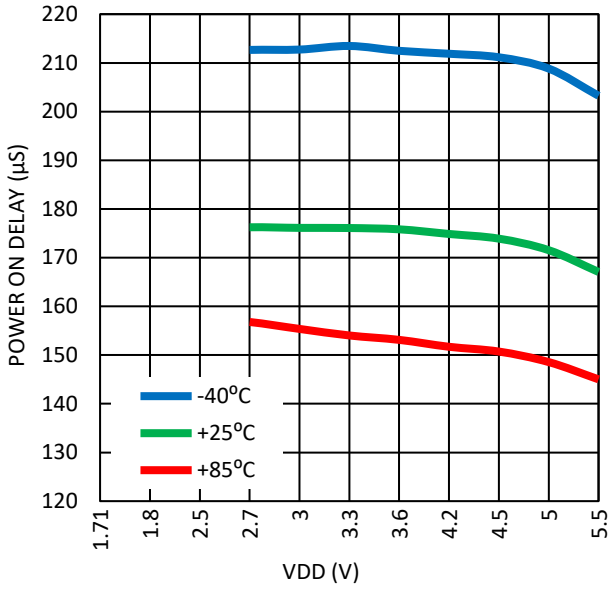


Figure 55. Maximum Power-On Delay vs. V_{DD}, BG = 100 µs

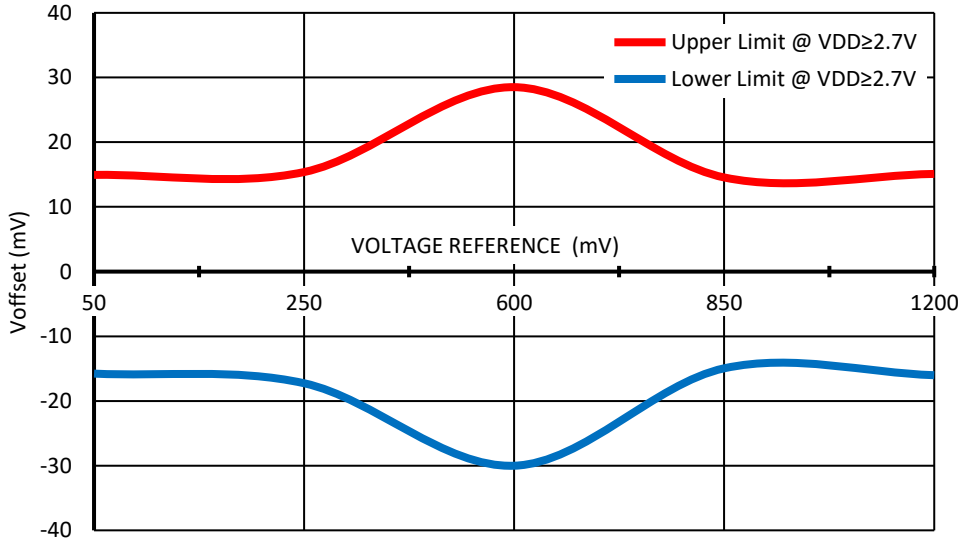


Figure 56. Typical Buffer Input Voltage Offset vs. Voltage Reference at T = -40 °C to +85 °C, Buffer Bandwidth = 1 kHz, V_{HYS} = 0 mV, Gain = 1

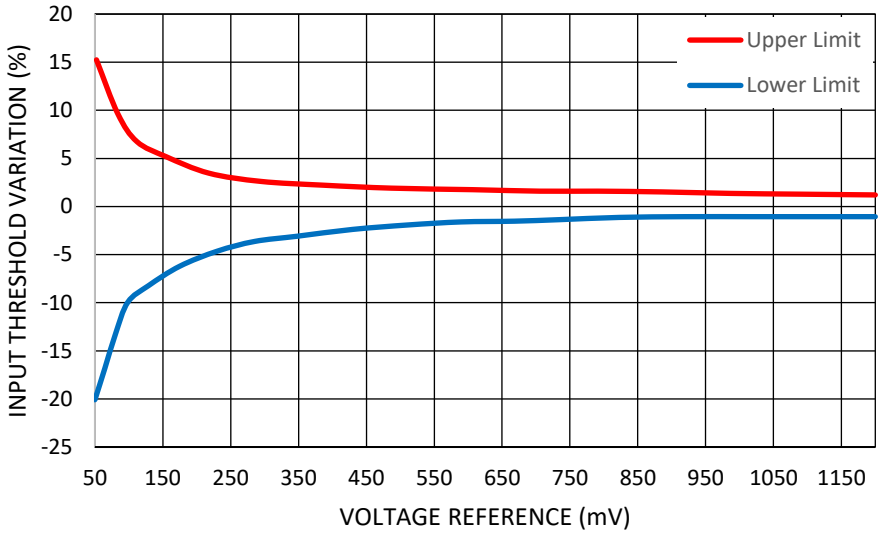


Figure 57. Typical Input Threshold Variation (Including V_{REF} Variation, ACMP Offset) vs. Voltage Reference at T = -40 °C to +85 °C, LMB Mode - Disable, V_{HYS} = 0 mV

9. Pipe Delay

The SLG47525/28 has a Pipe Delay logic cell that is shared with the 3-bit LUT10 in one of the Combination Function macrocells. The user can select one of these functions to use in a design, but not both. See section 7.4 3-Bit LUT or Pipe Delay Macrocell for the description of this Combination Function macrocell.

10. Programmable Delay/Edge Detector

The SLG47525/28 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. See Figure 59 for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

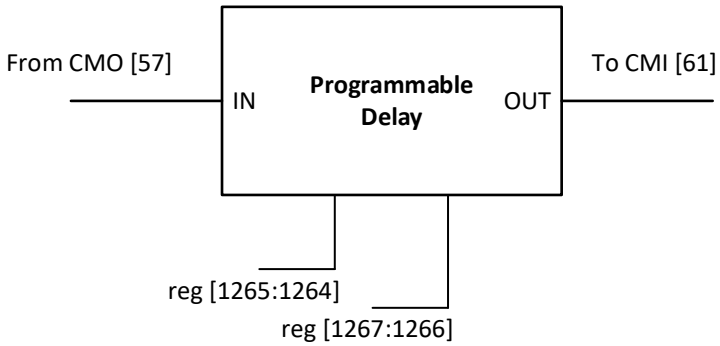
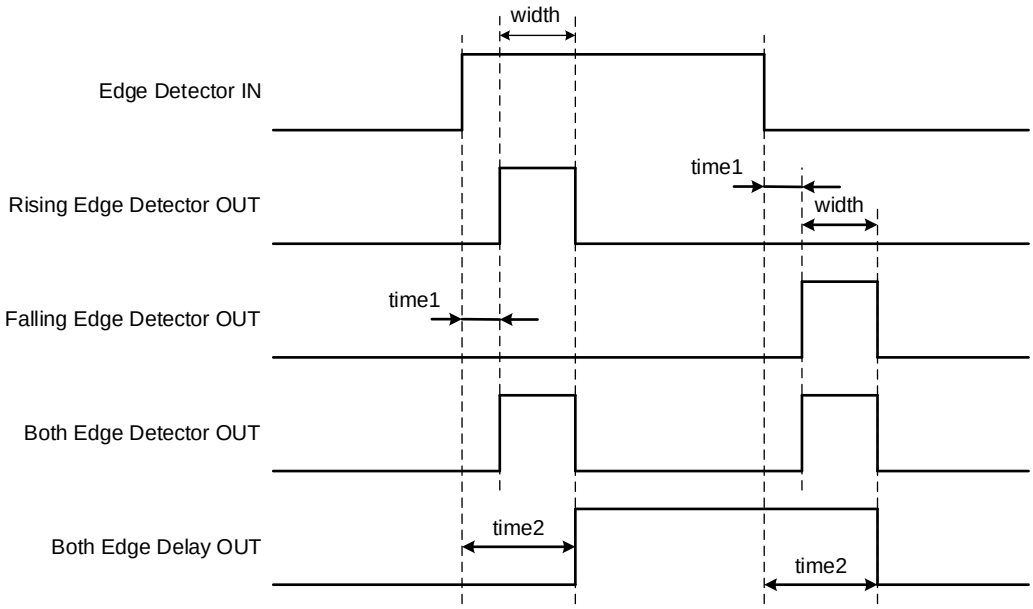


Figure 58. Programmable Delay



Note: time1 is a fixed value, time2 delay value is selected via register

Figure 59. Edge Detector Output

Please refer to section 3.4.11 Programmable Delay Expected Typical Delays and Pulse Width.

11. Additional Logic Functions

The SLG47525/28 has three additional logic functions that are connected directly to the Connection Matrix inputs and outputs. There are two deglitch filters, each with edge detector functions, and an Inverter (INV) gate. See section 3.4.12 Typical Filter Rejection Pulse Width.

11.1 Deglitch Filter/Edge Detector

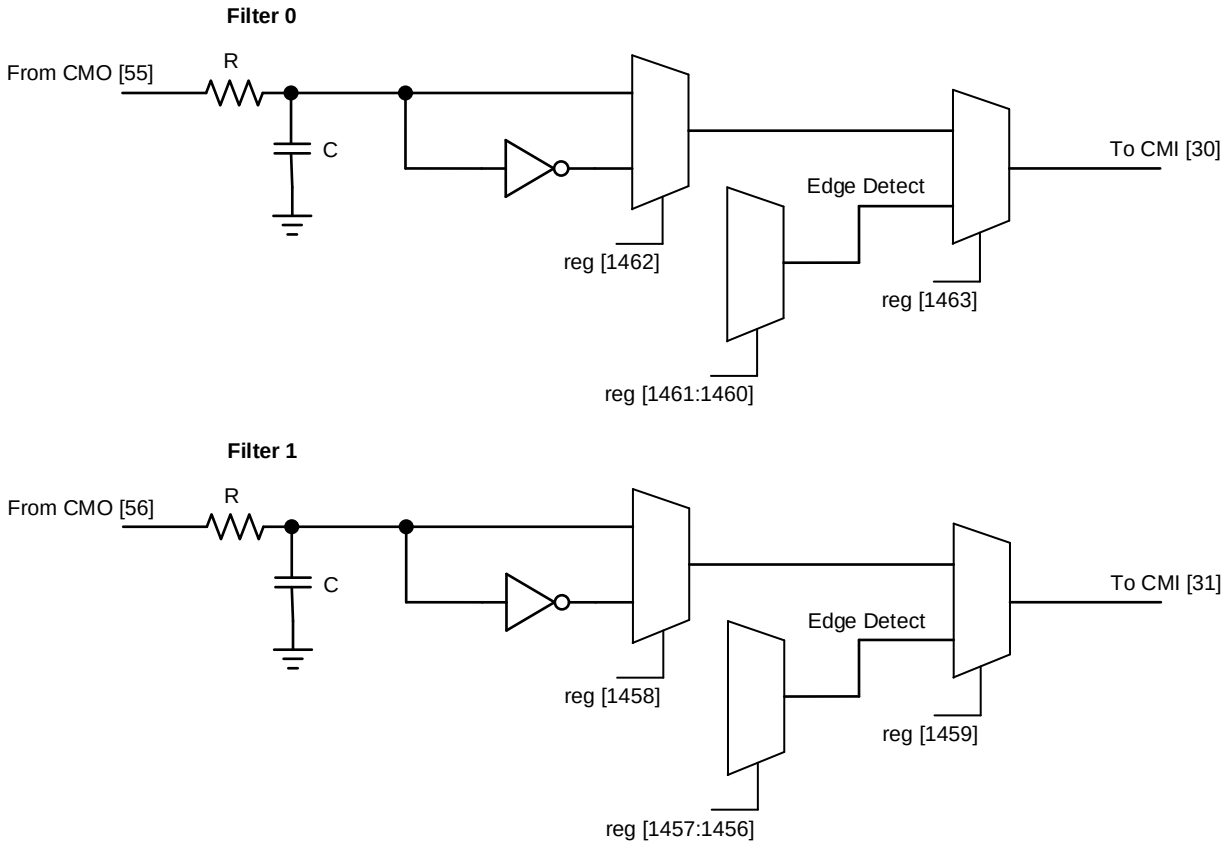


Figure 60. Deglitch Filter/Edge Detector

11.2 Inverter Gate

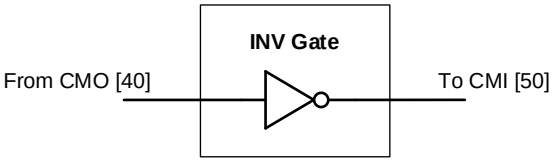


Figure 61. Inverter Gate

12. Voltage Reference

The SLG47525/28 has a Voltage Reference (V_{REF}) macrocell to provide references to the four analog comparators. This macrocell can supply a user selection of fixed voltage references, /3 and /4 reference of the V_{DD} power supply to the device, and externally supplied voltage references from IOs 5 and 9. The macrocell also has the option to output reference voltages on IOs 15 and 16. See Table 19 for the available selections for each analog comparator. Also, see Figure 62, which shows the reference output structure.

Table 19. V_{REF} Selection Table

SEL [4:0]	ACMP0_VREF	ACMP1_VREF	ACMP2_VREF	ACMP3_VREF
11101	vref_ext_acmp0/2	vref_ext_acmp1/2	Reserved	Reserved
11100	vref_ext_acmp1/2	vref_ext_acmp1/2	vref_ext_acmp1/2	vref_ext_acmp1/2
11011	vref_ext_acmp0	vref_ext_acmp1	Reserved	Reserved
11010	vref_ext_acmp1	vref_ext_acmp1	vref_ext_acmp1	vref_ext_acmp1
11001	V_{DD} / 4	V_{DD} / 4	V_{DD} / 4	V_{DD} / 4
11000	V_{DD} / 3	V_{DD} / 3	V_{DD} / 3	V_{DD} / 3
10111	1.20	1.20	1.20	1.20
10110	1.15	1.15	1.15	1.15
10101	1.10	1.10	1.10	1.10
10100	1.05	1.05	1.05	1.05
10011	1.00	1.00	1.00	1.00
10010	0.95	0.95	0.95	0.95
10001	0.90	0.90	0.90	0.90
10000	0.85	0.85	0.85	0.85
01111	0.80	0.80	0.80	0.80
01110	0.75	0.75	0.75	0.75
01101	0.70	0.70	0.70	0.70
01100	0.65	0.65	0.65	0.65
01011	0.60	0.60	0.60	0.60
01010	0.55	0.55	0.55	0.55
01001	0.50	0.50	0.50	0.50
01000	0.45	0.45	0.45	0.45
00111	0.40	0.40	0.40	0.40
00110	0.35	0.35	0.35	0.35
00101	0.30	0.30	0.30	0.30
00100	0.25	0.25	0.25	0.25
00011	0.20	0.20	0.20	0.20

SEL [4:0]	ACMP0_VREF	ACMP1_VREF	ACMP2_VREF	ACMP3_VREF
00010	0.15	0.15	0.15	0.15
00001	0.10	0.10	0.10	0.10
00000	0.05	0.05	0.05	0.05

Table 20. Practical Vref Range of Voltage Reference Macrocell

V_{DD}	Practical V_{REF} Range	Note
2.0 V - 5.5 V	50 mV ~ 1.2 V	
1.7 V - 2.0 V	50 mV ~ 1.0 V	Do not operate above 1.0 V

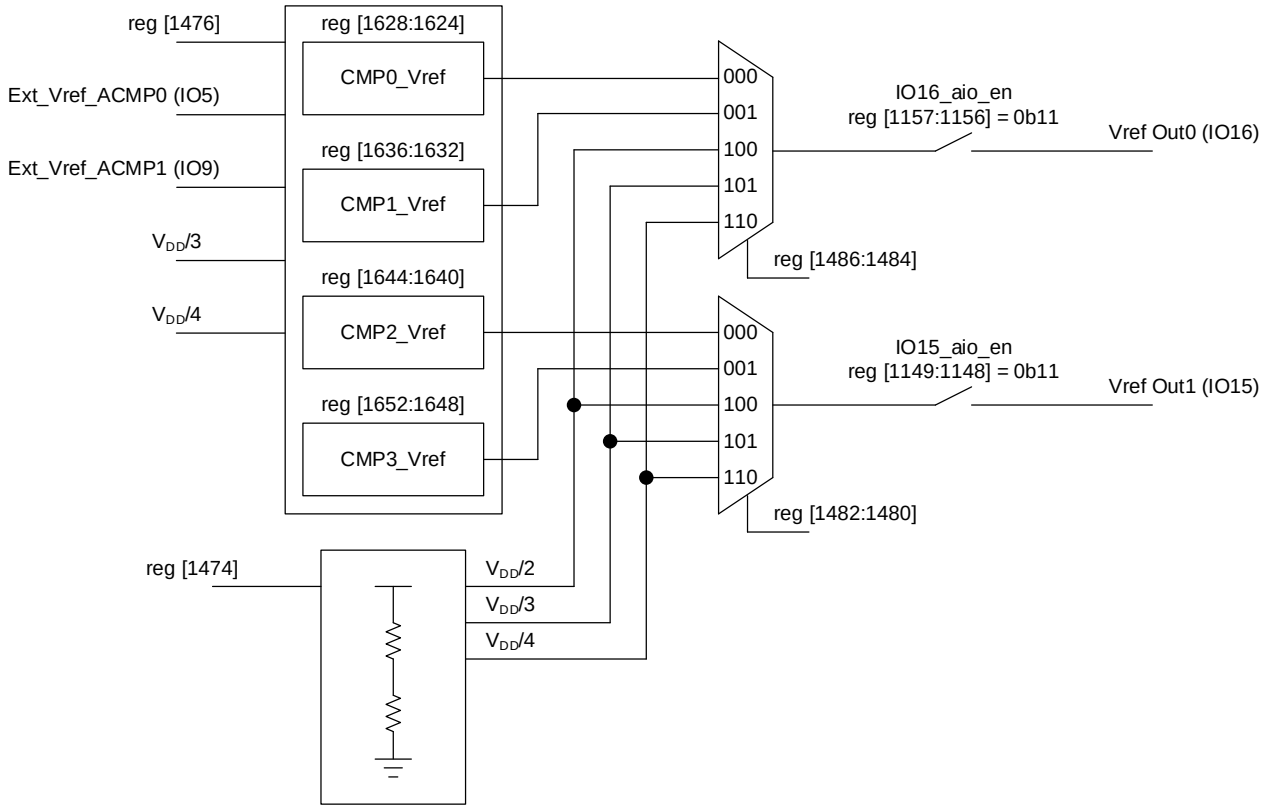


Figure 62. Voltage Reference Block Diagram

12.1 V_{REF} Typical Performance

Note: V_{REF} buffer performance is not guaranteed at V_{DD} < 2.7 V.

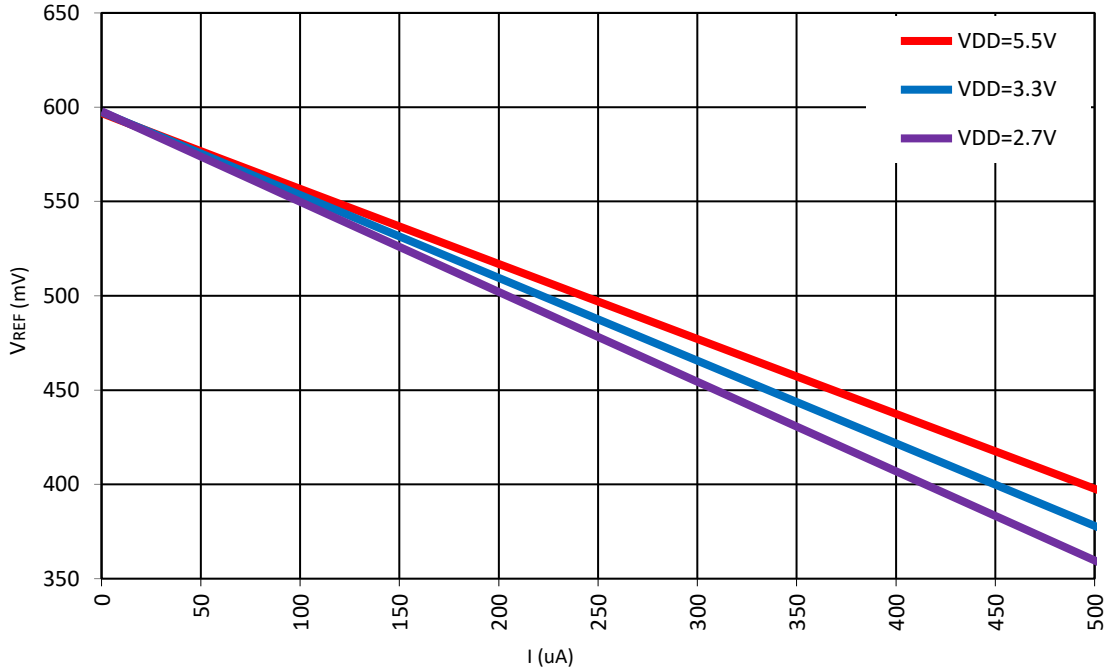


Figure 63. Typical Load Regulation, V_{REF} = 600 mV, T = -40 °C to +85 °C, Buffer - Enable

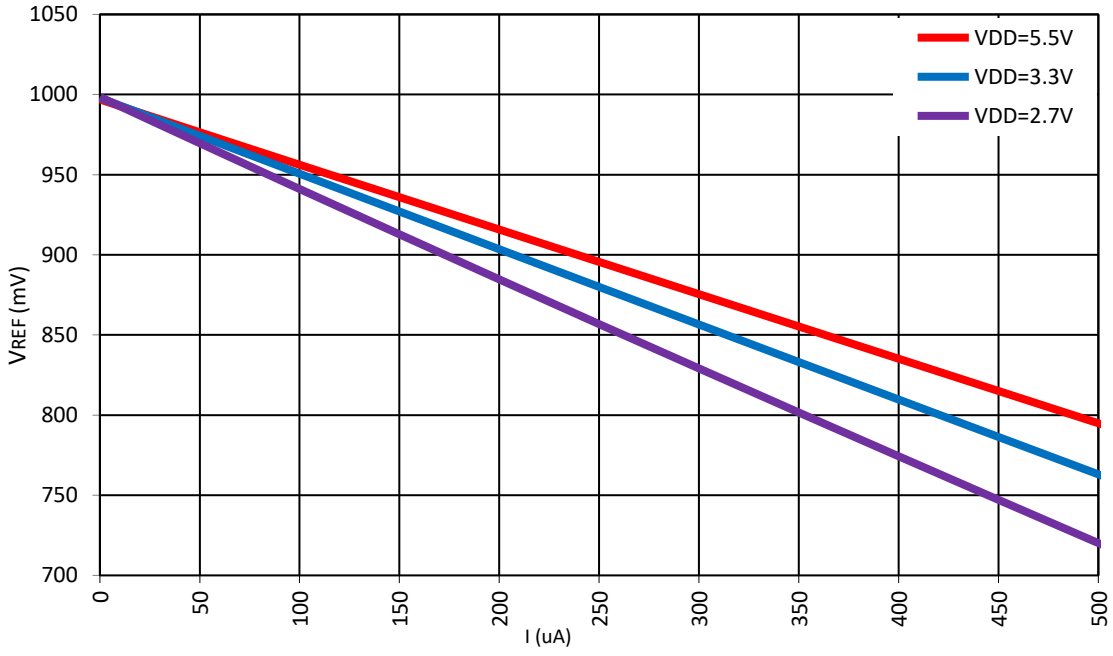


Figure 64. Typical Load Regulation, V_{REF} = 1000 mV, T = -40 °C to +85 °C, Buffer - Enable

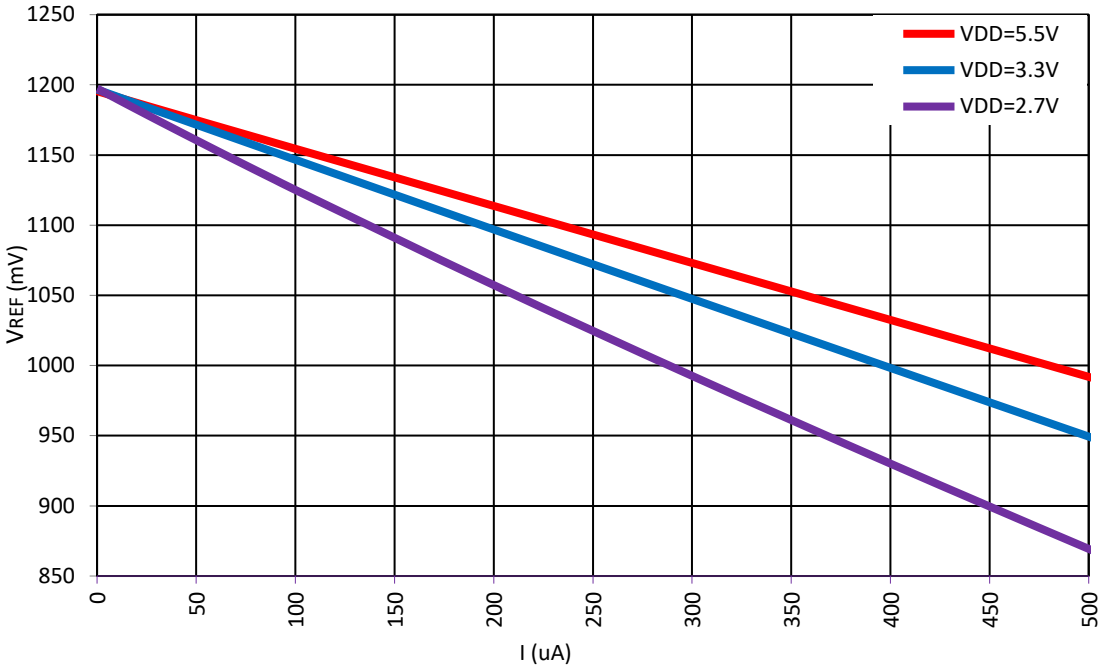


Figure 65. Typical Load Regulation, V_{REF} = 1200 mV, T = -40 °C to +85 °C, Buffer - Enable

13. Clocking

13.1 RC Oscillator

The SLG47525/28 has two internal oscillators. RC Oscillator (RC OSC) that runs at 25 kHz/2 MHz (OSC0), and oscillator that runs at 25 MHz (OSC1). It is possible to use all two oscillators simultaneously. The fundamental frequency can also come from clock input (IO15 or IO17 for 25 kHz/2 MHz and IO14 for 25 MHz), see section 13.2 External Clocking.

13.1.1. 25 kHz/2 MHz and 25 MHz RC Oscillators

There are two divider stages that gives the user flexibility for introducing clock signals on various Connection Matrix Input lines. The pre-divider allows the selection of /1, /2, /4, or /8 to divide down frequency from the fundamental. The second stage divider (only for 25 kHz/2 MHz oscillator) has an input of frequency from the pre-divider, and outputs one of seven different frequencies on Connection Matrix Input lines [27] (OUT0) and [28] (OUT1). See Figure 66 and Figure 67 below for details.

There are two modes of the POWER CONTROL pin, (register [1658] for 25 kHz/2 MHz OSC and register [1657] for 25 MHz OSC):

- POWER DOWN [0]. If PWR CONTROL input of oscillator is LOW, the oscillator will be turned on. If PWR CONTROL input of oscillator is HIGH, the oscillator will be turned off and OSC divider will reset.
- FORCE ON [1]. If PWR CONTROL input of oscillator is HIGH, the oscillator will be turned on. If PWR CONTROL input of oscillator is LOW, the oscillator will be turned off.

The PWR CONTROL signal has the highest priority.

The SLG47525/28 has a 25 kHz/2 MHz OSC FAST START-UP function register [1338] (1 – ON, 0 – OFF). It allows the OSC to run immediately after power-up, which decreases the settling time. Note that when OSC FAST START-UP is ON, the current consumption will rise.

The user can select two OSC power modes (register [1343] for 25 kHz/2 MHz OSC and register [1341] for 25 MHz OSC):

- If AUTO POWER ON [0] is selected, the OSC will run when any macrocell that uses OSC is powered on.
- If FORCE POWER ON [1] is selected, the OSC will run when the SLG47525/28 is powered on.

OSC can be turned on by:

- Register control (force power-on)
- Delay mode when delay requires OSC
- CNT/FSM.

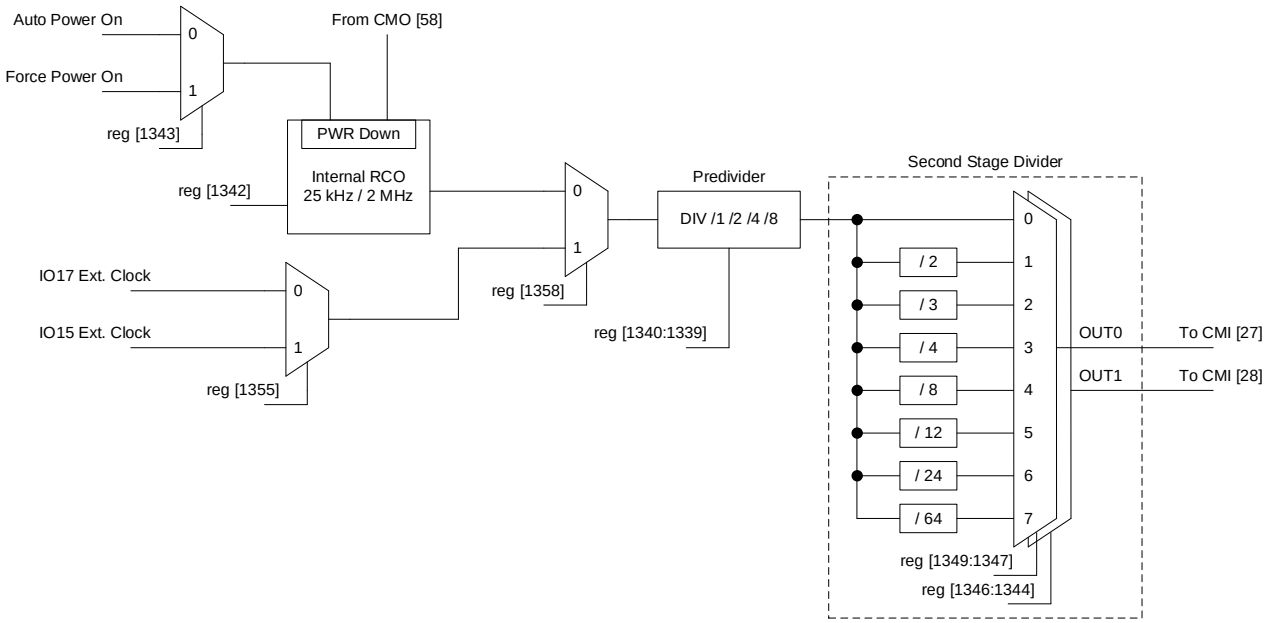


Figure 66. 25 kHz/2 MHz RC OSC Block Diagram

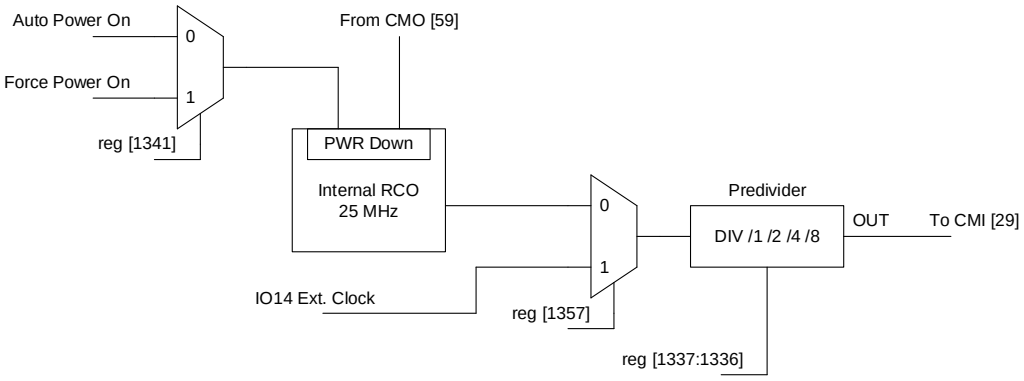


Figure 67. 25 MHz RC OSC Block Diagram

13.1.2. Oscillator Power-On Delay

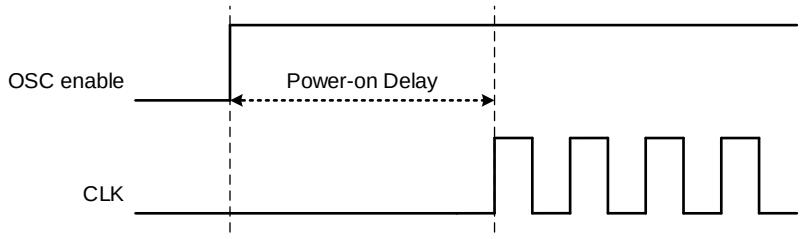


Figure 68. Oscillator Startup Diagram

Note 1: OSC power mode: "Auto Power-On".

Note 2: 'OSC enable' signal appears when any macrocell that uses OSC is powered on.

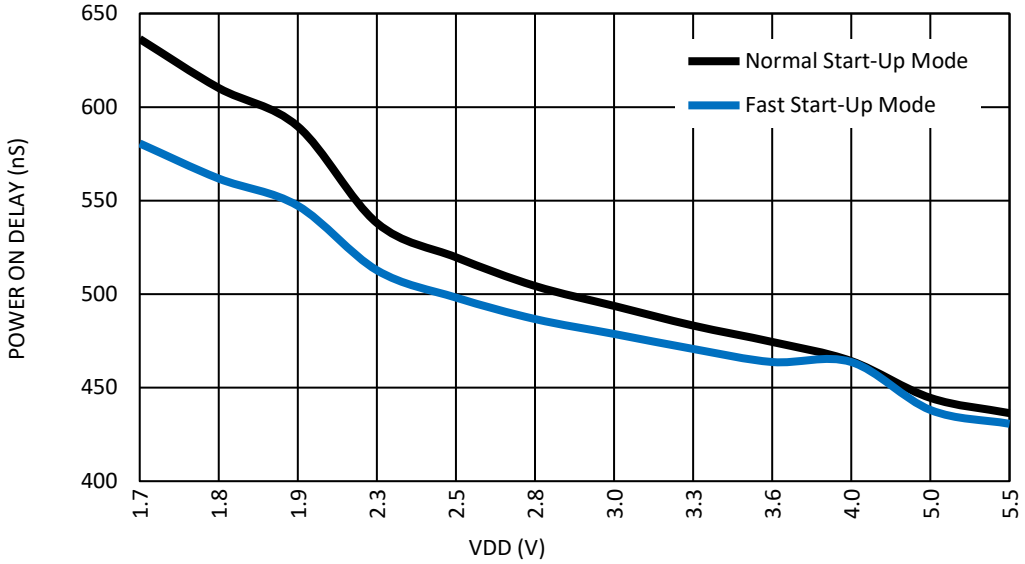


Figure 69. RC Oscillator Maximum Power-On Delay vs. V_{DD} at Room Temperature, OSC0 = 2 MHz

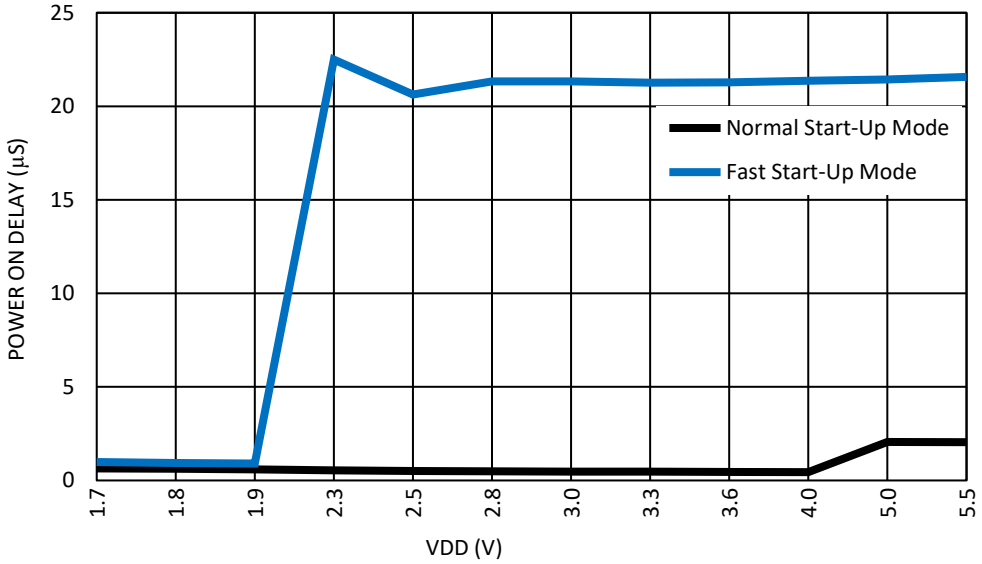


Figure 70. RC Oscillator Maximum Power-On Delay vs. V_{DD} at 85 °C, OSC0 = 25 kHz

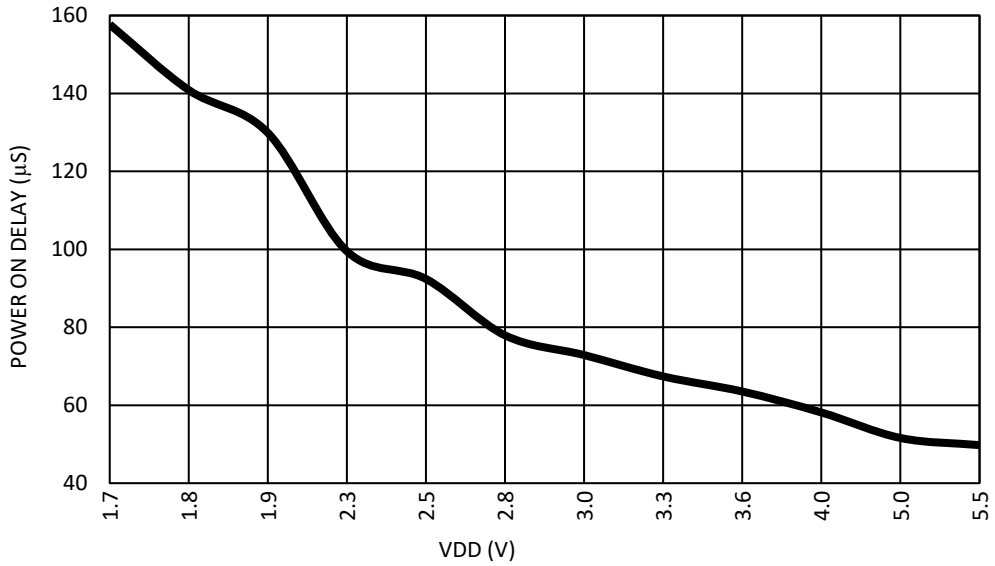


Figure 71. OSC1 (25 MHz) Maximum Power-On Delay vs. V_{DD} at 85°C

13.1.3. Oscillator Accuracy

Note 1: OSC power setting: Force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

Note 2: For more information see section 3.5 Oscillator Characteristics.

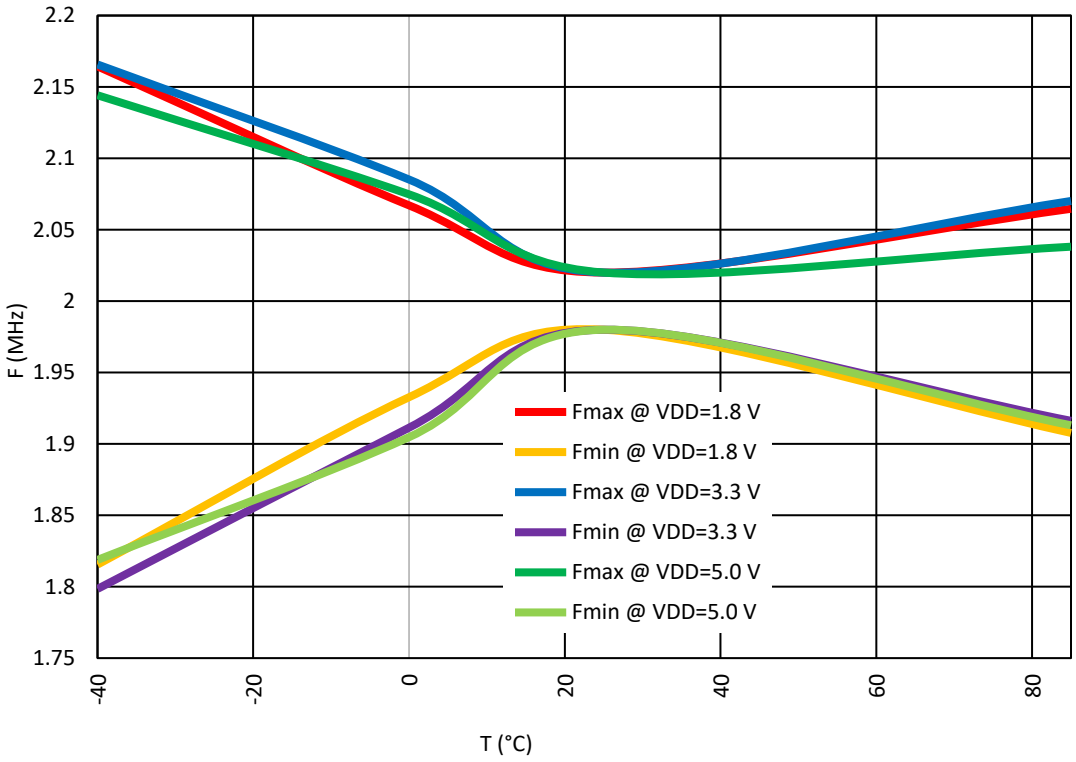


Figure 72. RC Oscillator Frequency vs. Temperature, RC OSC0 = 2 MHz

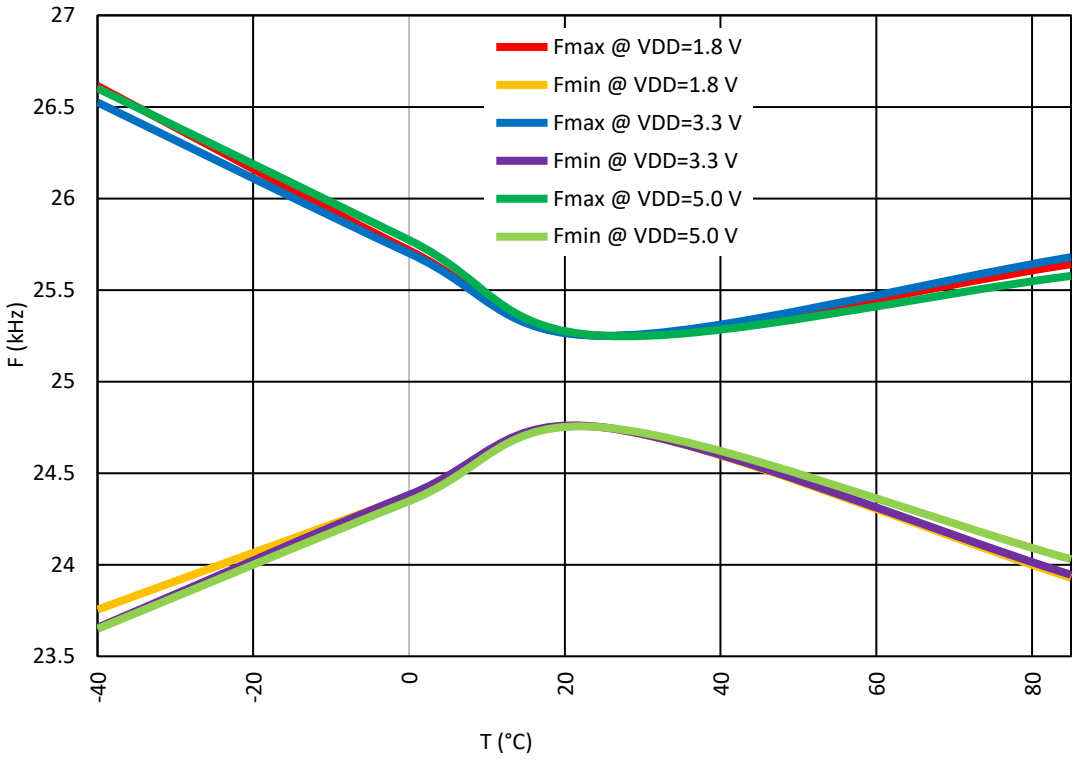


Figure 73. RC Oscillator Frequency vs. Temperature, RC OSC0 = 25 kHz

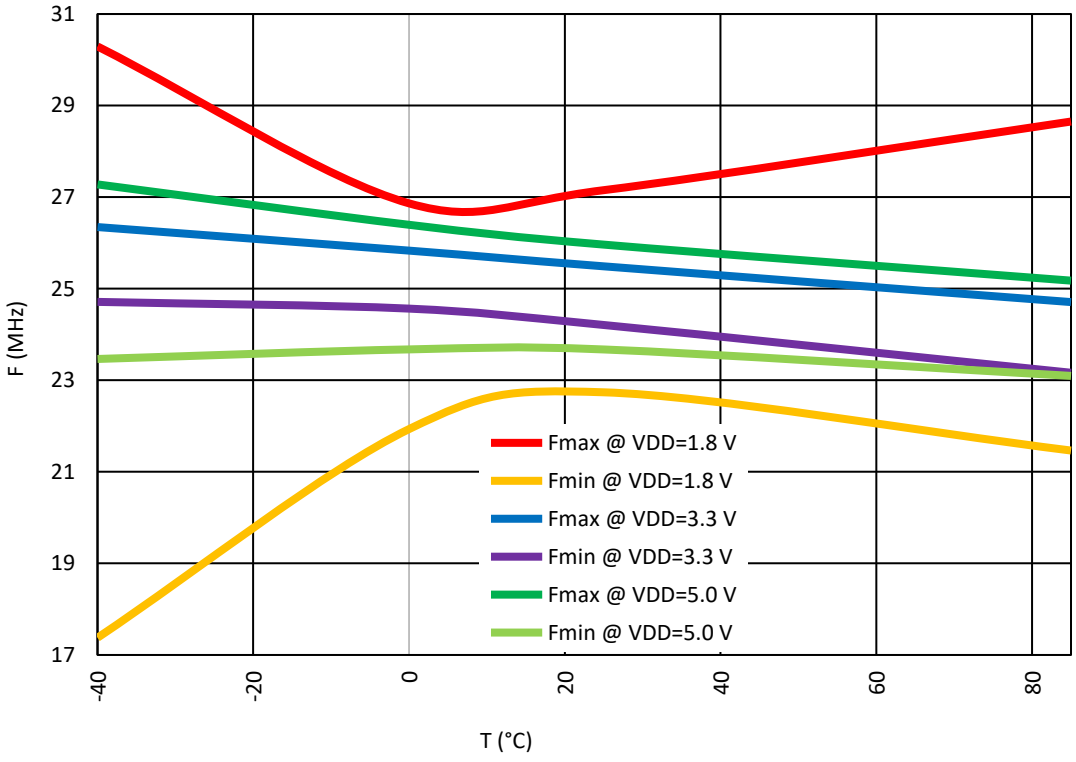


Figure 74. OSC1 (25 MHz) Frequency vs. Temperature

Note: 25 MHz RC OSC1 performance is not guaranteed at V_{DD} < 2.5 V.

13.2 External Clocking

The SLG47525/28 supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

13.2.1. IO17 or IO15 Source for 25 kHz/2 MHz Clock

When register [1358] is set to 1, an external clocking signal on IOs 15 or 17 will be routed in place of the internal RC Oscillator derived 25 kHz/2 MHz clock source. When register [1355] is set to 0 – IO17 is in use, when set to 1 – IO15 is in use. See Figure 66. The high and low limits for external frequency that can be selected are 0 MHz and 77 MHz.

13.2.2. IO14 Source for 25 MHz Clock

When register [1357] is set to 1, an external clocking signal on IO14 will be routed in place of the internal RC Oscillator derived 25 MHz clock source. See Figure 67. The high and low limits for external frequency that can be selected are 0 MHz and 80 MHz.

14. Power-On Reset

The SLG47525/28 has a Power-On Reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IO pins.

14.1 General Operation

To start the POR sequence in the SLG47525/28, the voltage applied on the V_{DD} should be higher than the Power-On threshold (see Note 1). The full operational V_{DD} range for the SLG47525/28 is 1.71 V to 5.5 V (1.8 V ±5 % to 5.0 V±10 %). This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power-On threshold. After the POR sequence has started, the SLG47525/28 will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device) and will be ready and completely operational after the POR sequence is complete.

The SLG47525/28 is guaranteed to be powered down and non-operational when the V_{DD} voltage (voltage on V_{DD}) is less than Power-Off Threshold (see section 3.4 Electrical Characteristics), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (see Note 2) than the V_{DD} voltage is applied to any other pin. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other pin is incorrect, and can lead to incorrect or unexpected device behavior.

Note 1: The Power-On threshold is defined in section 3.4 Electrical Characteristics.

Note 2: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To power down the chip the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down it should be less than Power-Off Threshold.

All pins are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before, the voltage on pins cannot be bigger than the V_{DD}. This rule also applies to the case when the chip is powered on.

Note that V_{DD2} has no influence on POR sequence, all internal macrocells are powered from V_{DD}. It means, V_{DD2} can be switched on/off while V_{DD} is ON. If voltage on V_{DD2} appears after the POR sequence, IOs 9, 10, 12, 13, 14, 15, 16, 17 become available when V_{DD2} reaches PON_{TVDET} (see section 3.4.2 Low-voltage Logic IO Characteristics (Powered from VDD2)).

14.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 75.

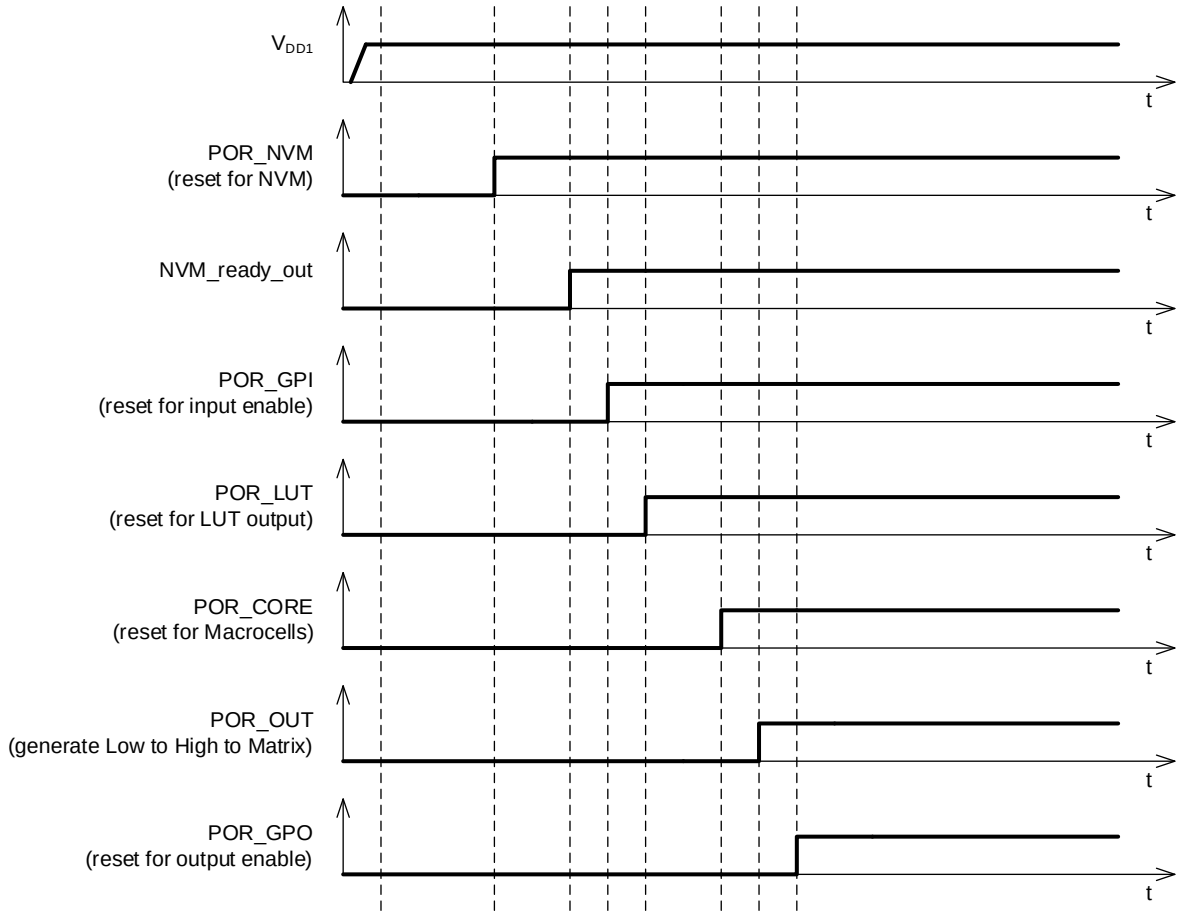


Figure 75. POR Sequence

As can be seen from Figure 75, after the V_{DD} has start ramping up and crosses the Power-On threshold, first, the on-chip NVM memory is reset. Next the chip reads the data from NVM and transfers this information to SRAM registers that serve to configure each macrocell and the Connection Matrix, which routes signals between macrocells. The third stage causes the reset of the input pins, and then enables them. After that, the LUTs are reset and become active. After LUTs, the Delay cells, RC OSC, DFFs, LATCHES, and Pipe Delay are initialized. Only after all macrocells are initialized, internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output pins, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature, and even will vary from chip to chip (process influence).

14.3 Macrocells Output States During POR Sequence

To have a full picture of the SLG47525/28 operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (Figure 76 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output pins which are in high impedance state). Before the NVM is ready, all macrocell outputs are unpredictable (except the output pins). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P_DLY macrocell configured as edge detector becomes active at this time. After

that input pins are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output pins that become active and determined by the input signals.

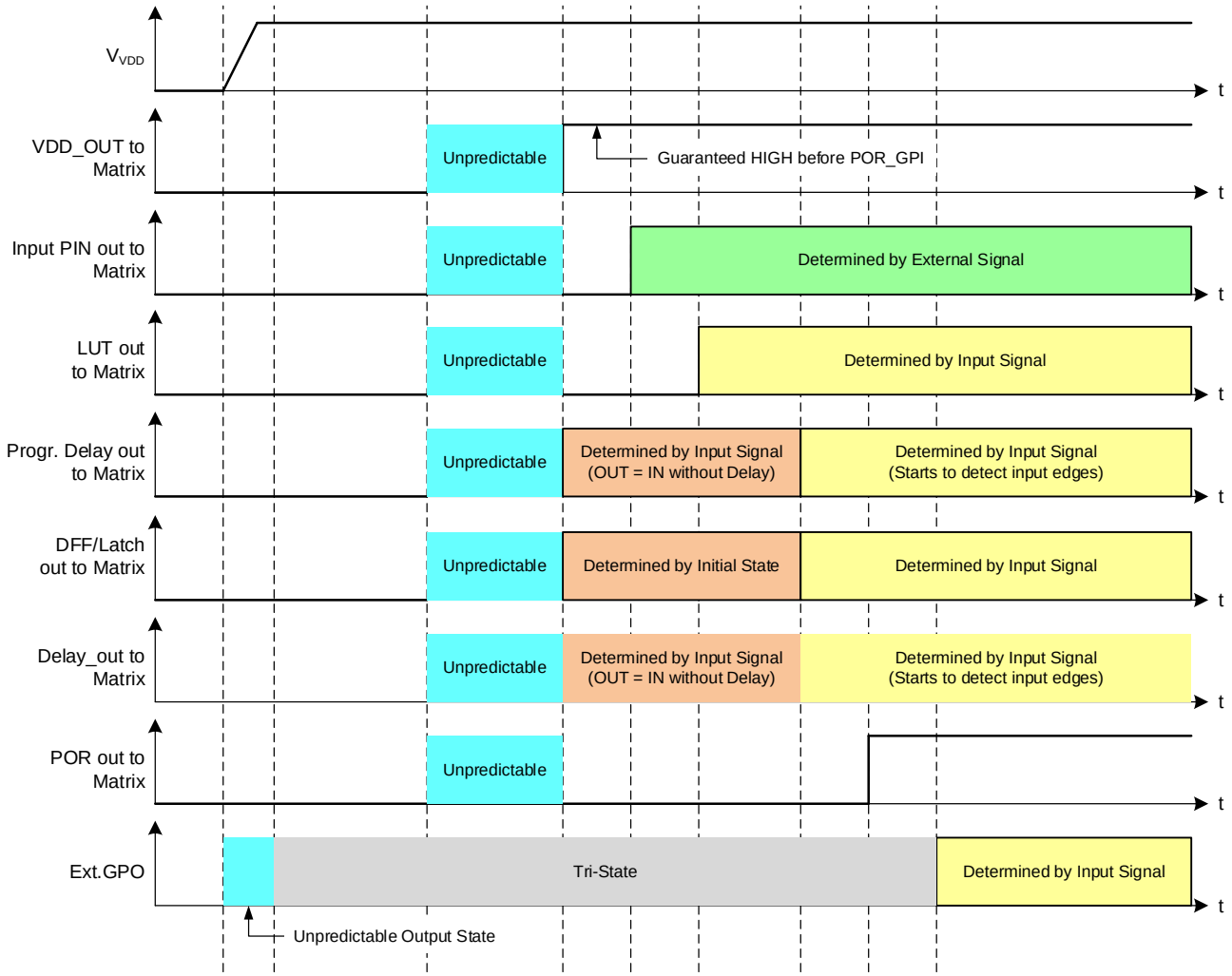


Figure 76. Internal Macrocell States during POR Sequence

14.3.1. Initialization

All internal macrocells by default have an initial low level. Starting from indicated power-up time of 1.15 V - 1.6 V, macrocells in GPAK are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. I^2C.
2. Input pins, ACMP, pull-up/down.
3. LUTs.
4. DFFs, Delays/Counters, Pipe Delay.
5. POR output to matrix.
6. Output pin corresponds to the internal logic.

The V_{REF} output pin driving signal can precede POR output signal going HIGH by 3 µs - 5 µs. The POR signal going HIGH indicates the mentioned power-up sequence is complete.

Note: The maximum voltage applied to any pin should not be higher than the V_{DD} level. There are ESD Diodes between pin –> V_{DD} and pin –> GND on each PIN. So, if the input signal applied to pin is higher than V_{DD}, then current will sink through the diode to V_{DD}. Exceeding V_{DD} results in leakage current on the input pin, and V_{DD} will be pulled up, following the voltage on the input pin. There is no effect from input pin when input voltage is applied at the same time as V_{DD}.

14.3.2. Power-Down

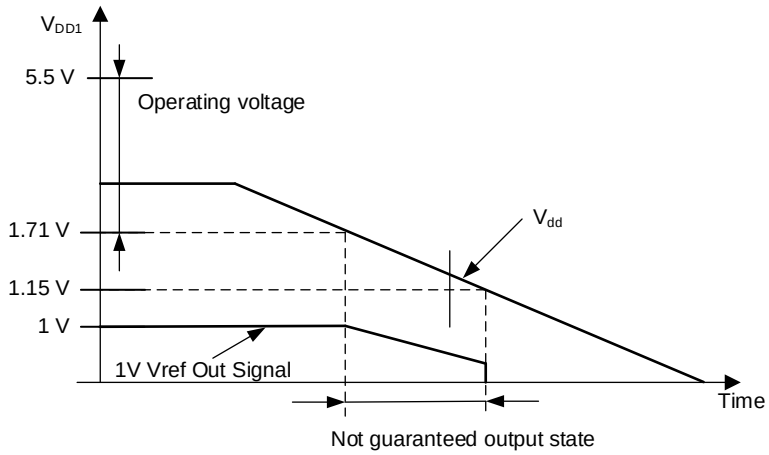


Figure 77. Power-Down

During power-down, macrocells in the SLG47525/28 are powered off after V_{DD} falling down below Power-Off Threshold. Please note that during a slow rampdown, outputs can possibly switch state during this time.

15. Asynchronous State Machine Macrocell

15.1 Asynchronous State Machine Macrocell Overview

The Asynchronous State Machine (ASM) macrocell is designed to allow the user to create state machines with between 2 to 8 states. The user has a flexibility to define the available states, the available state transitions, and the input signals (a, b, c …) that will cause transitions from one state to another state, as shown in Figure 78.

This macrocell has a total of 25 inputs, as shown in Figure 79, which come from the Connection Matrix outputs. Of these 25 inputs, 24 are user selectable for driving general state transitions, and 1 is for driving a state transition to an Initial/Reset state. Each of the 24 inputs is level sensitive and active HIGH, meaning that a high level input will drive the user selected transition from one state to another. The fact that there are 24 inputs puts the upper bound of 24 possible state transitions total in the user-defined state machine design. There is one nReset input, which will drive an immediate state transition to the user-defined Initial/Reset state when active, shown in red, in the Figure 78. For more details refer to section 15.2 ASM Inputs.

There are a total of 8 outputs, which go to the Connections Matrix inputs, and from there can be routed to other internal macrocells or pins. The 8 outputs are user-defined for each of the possible 8 states. This information is held in the Connection Matrix Output RAM. For more details refer to section 15.3 ASM Outputs.

In using this macrocell, the user must take into consideration the critical timing required on all input and output signals. The timing waveforms and timing specifications for this macrocell are all measured relative to the input signals (which come into the macrocell on the Connection Matrix outputs) and on the outputs from the macrocell (which are direct connections to the Connection Matrix inputs). The user must consider any delays from other logic and internal chip connections, including IO delays, to ensure that signals are properly processed, and state transitions are deterministic.

The GPAK Designer development tools support user designs for the ASM macrocell at both physical level and logic level. Figure 78 is a representation of the user design at the logical level. Figure 79 shows the physical resources inside the macrocell. To best utilize this macrocell, the user must develop a logical representation of their desired state machine, as well as a physical mapping of the input and outputs required for the desired functionality.

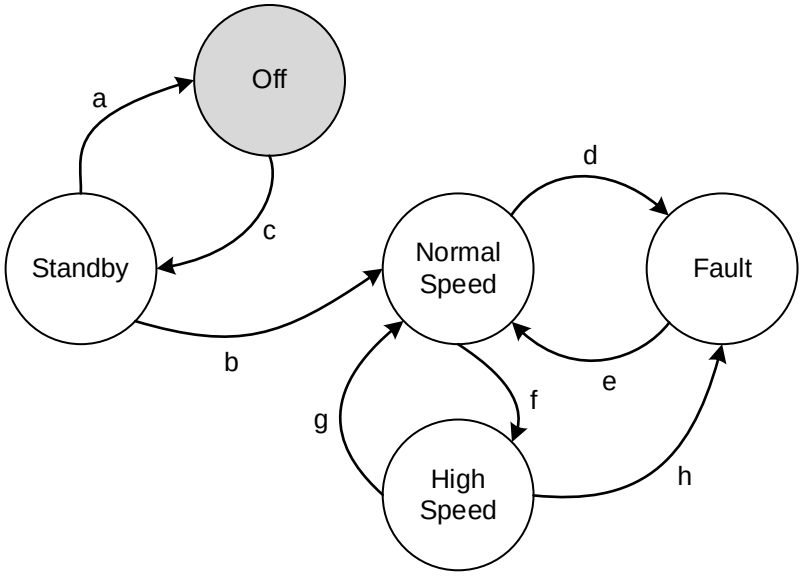


Figure 78. Asynchronous State Machine State Transitions

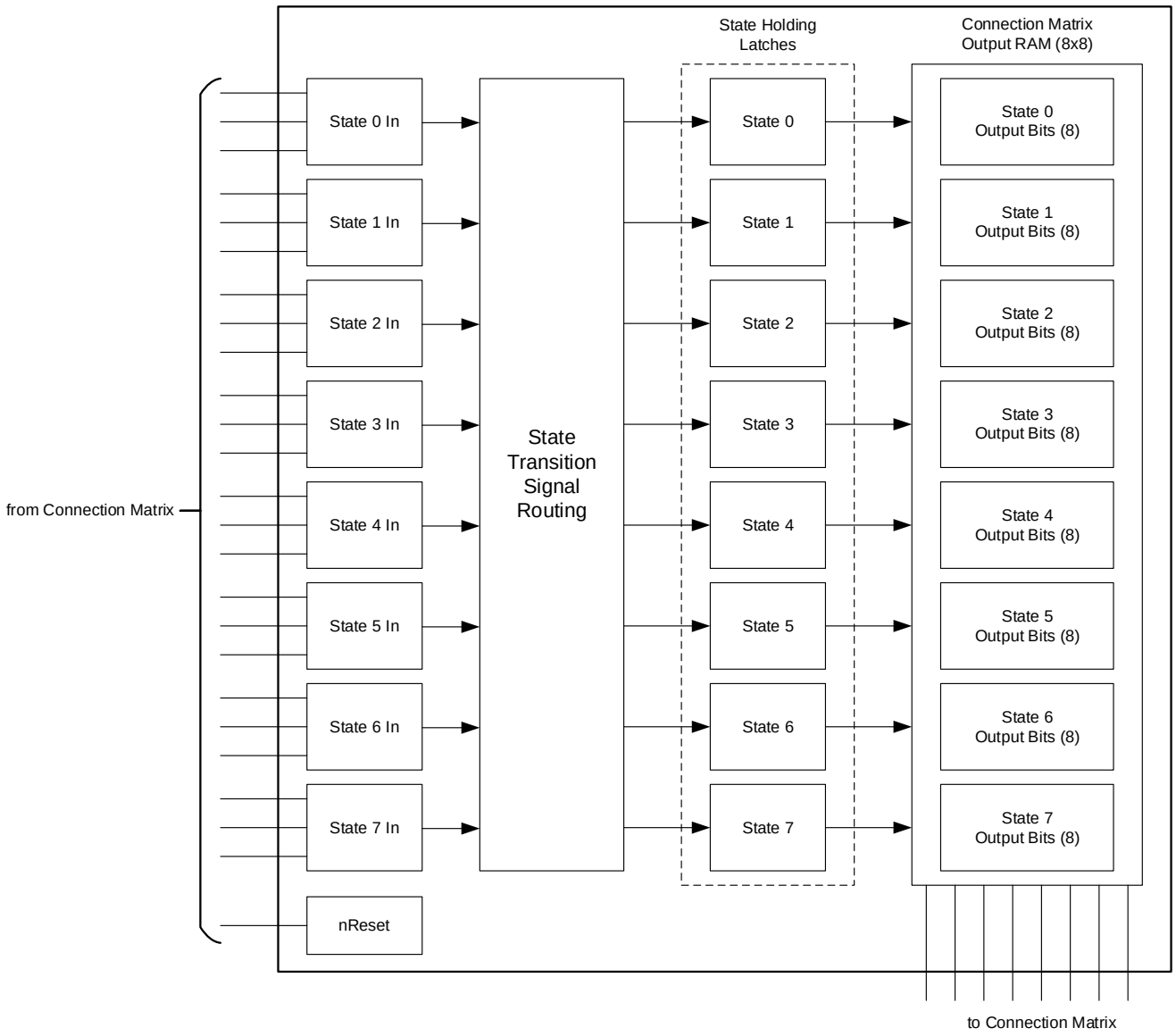


Figure 79. Asynchronous State Machine

15.2 ASM Inputs

The ASM macrocell has a total of 25 inputs which come from the Connection Matrix outputs. Of these 25 inputs, 24 are user selectable for driving general state transitions, and 1 is for driving a state transition to Initial/Reset state.

There are a total of 24 inputs to the ASM macrocell for general state transitions, highlighted in red in Figure 80. Each of these inputs is level sensitive and active HIGH. A high level input will trigger a state transition.

These inputs are grouped so that each set of 3 inputs can drive a state transition going into a particular state. As an example, there are three inputs that can drive a state transition to State 1. This sets an upper bound on the number of transitions that the user can select going into a particular state to be 3, shown in Figure 81.

There is no limitation on the number of transitions that can be supported coming out of a particular state. The user can select to have transitions going from a state to all other states, shown in Figure 82.

The ASM macrocell also has an nReset input highlighted in blue in Figure 80. This input is level sensitive and active LOW. An active signal on this input will drive an immediate state transition to the user-defined Initial/Reset state. The user can choose which state within the ASM Editor inside GPAK Designer is the initial state.

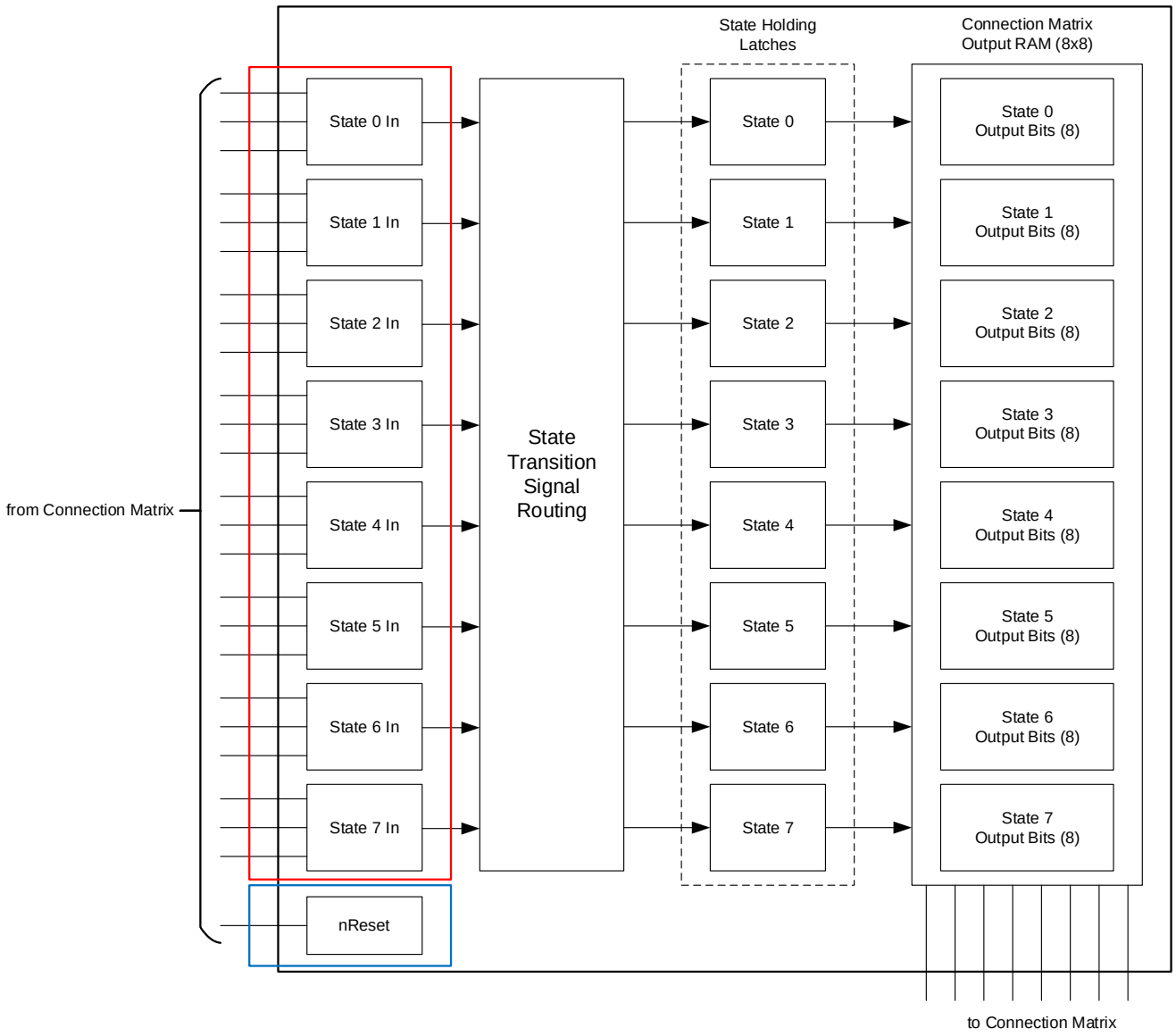


Figure 80. Asynchronous State Machine Inputs

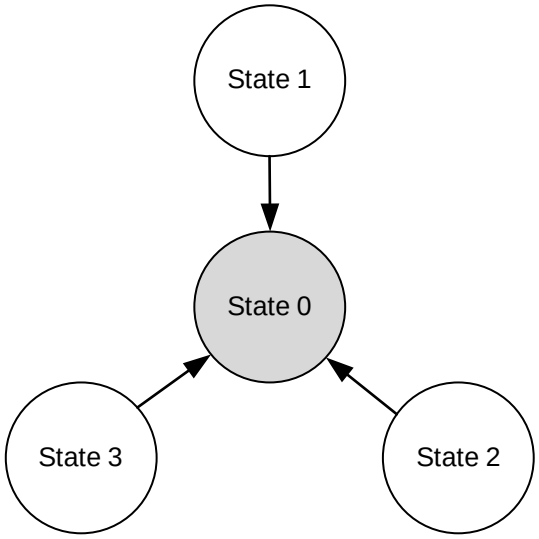


Figure 81. Maximum 3 State Transitions into Given State

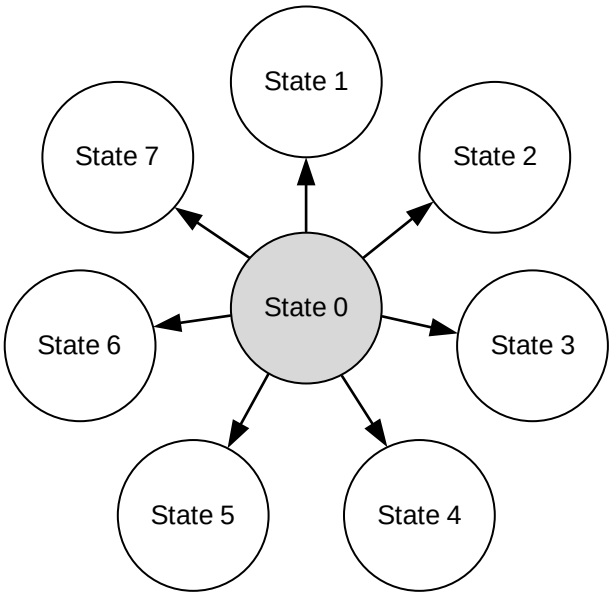


Figure 82. Maximum 7 State Transitions out of a Given State

15.3 ASM Outputs

There are a total of 8 outputs from the ASM macrocell, which go to the Connections Matrix inputs, and from there can be routed to other internal macrocells or pins. The 8 outputs are user-defined for each of the possible 8 states, this information is held in the Connection Matrix Output RAM, shown in Figure 83. The Connection Matrix Output RAM has a total of 64 bits, arranged as 8 bits per state. The values loaded in each of the 8 bits define the signal level on each of the 8 ASM macrocell outputs.

The ASM Editor inside the GPAK Designer software allows the user to make their selections for the value of each bit in the Connection Matrix Output RAM, which selects the level of the macrocell outputs based on the current state of the ASM macrocell, as shown in Figure 83.

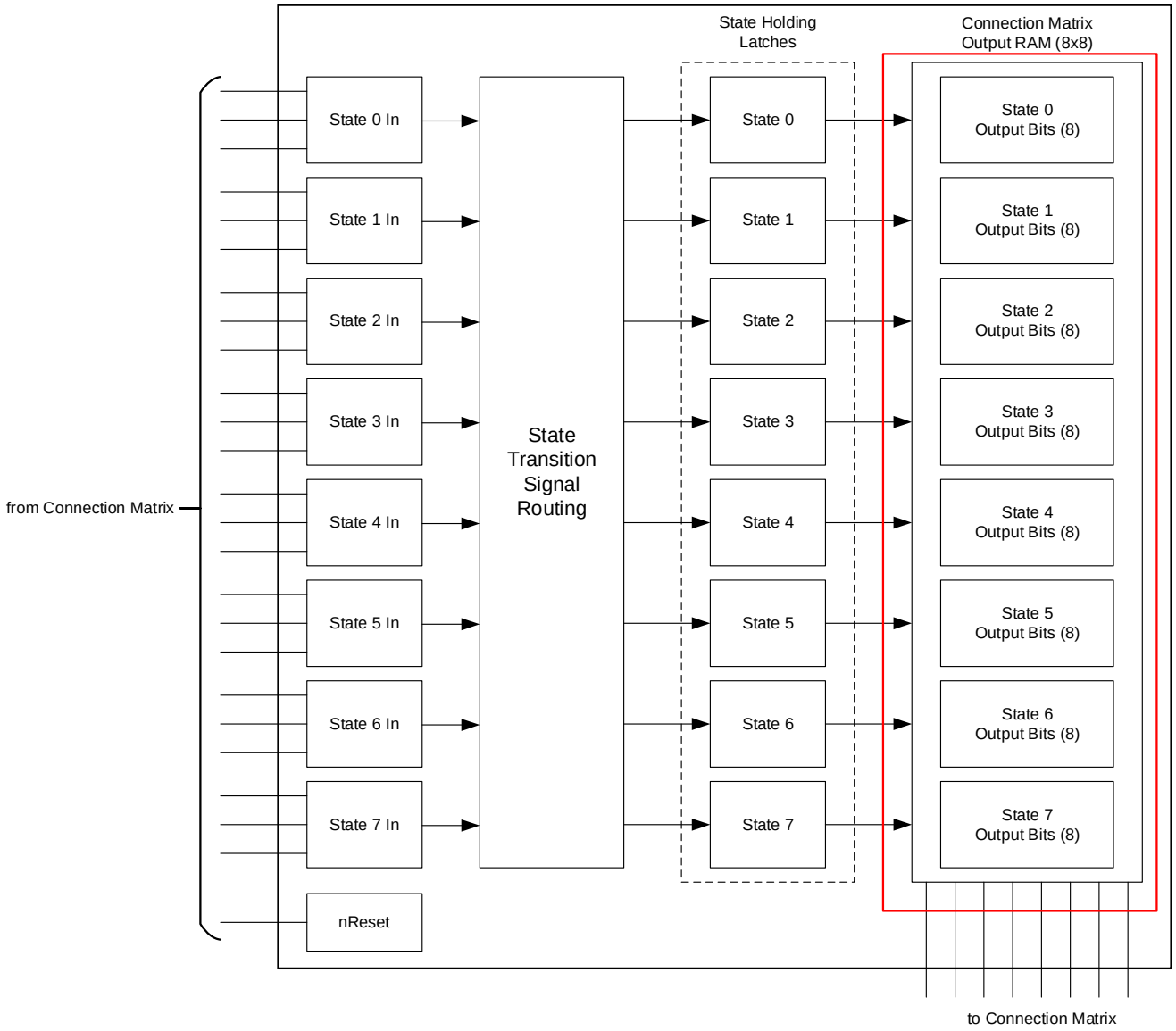


Figure 83. Connection Matrix Output RAM

Table 21. ASM Editor - Connection Matrix Output RAM

State Name	Connection Matrix Output RAM							
	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
State 0	0	0	0	0	0	0	0	1
State 1	0	0	0	0	0	0	1	0
State 2	0	0	0	0	0	1	0	0
State 3	0	0	0	0	1	0	0	0
State 4	0	0	0	1	0	0	0	0
State 5	0	0	1	0	0	0	0	0
State 6	0	1	0	0	0	0	0	0
State 7	1	0	0	0	0	0	0	0

There is a possibility to configure ASM (its settings and transitions) via I²C. Registers [197:0] correspond to ASM inputs, registers [1727:1664] correspond to ASM outputs configuration. Using I²C commands (see section 16.4 I2C Serial Communications Commands) it is possible to read ASM settings and connections, as well as change them. Additionally, the user can change Connection Matrix Output RAM bit configuration (bytes 0xD0 to 0xD7).

Note: After Connection Matrix Output RAM was updated via I²C, ASM outputs to Connection Matrix can be changed only after ASM changes its state or after reset event. To change ASM outputs to the Connection Matrix instantly after I²C write command, ASM must be in reset all the time.

15.4 Basic ASM Timing

The basic state transition timing from input on Matrix Connection output to output on Matrix Connection input is shown in Figure 84 and Figure 85. The time from a valid input signal to the time that there is a valid change of state and valid signals being available on the state outputs is State Machine Output Delay Time ($T_{st\_out\_delay}$). The minimum and maximum values of $T_{st\_out\_delay}$ define the differential timing between the shortest state transition (input on matrix output and output on matrix input) and the longest state transition (input on matrix output and output on matrix input).

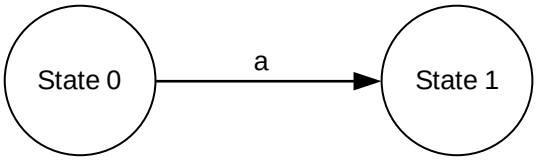


Figure 84. State Transition

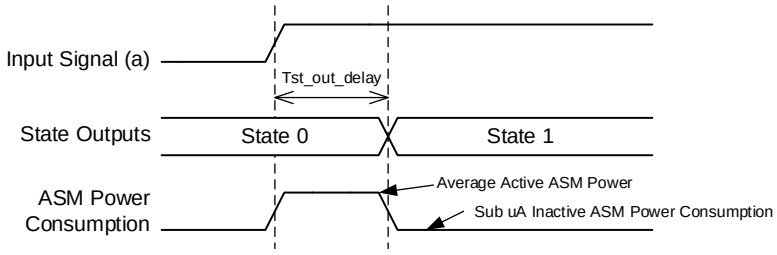


Figure 85. State Transition Timing

15.5 Asynchronous State Machines vs. Synchronous State Machines

It is important to note that this macrocell is designed for asynchronous operation, which means the following:

1. No clock source is needed, it reacts only to input signals.
2. The input signals do not have to be synchronized to each other, the macrocell will react to the earliest valid signal for state transition.
3. This macrocell does not have traditional set-up and hold time specifications, which are related to incoming clock, because this macrocell has no clock source.
4. The macrocell only consumes power while in state transition.

15.6 ASM Power Considerations

A benefit of the asynchronous nature of this macrocell is that it will consume power only during state transitions. Shown in Figure 84 and Figure 86, the current consumption of the macrocell will be a fraction of a µA between state transitions, and will rise only during state transitions. See section 3.4.6 Estimated Typical Current of Macrocell Configurations to find average current during state transitions.

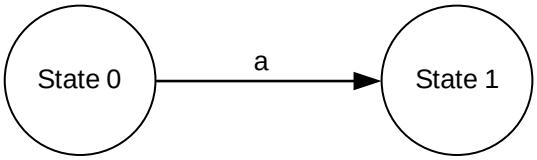


Figure 86. State Transition

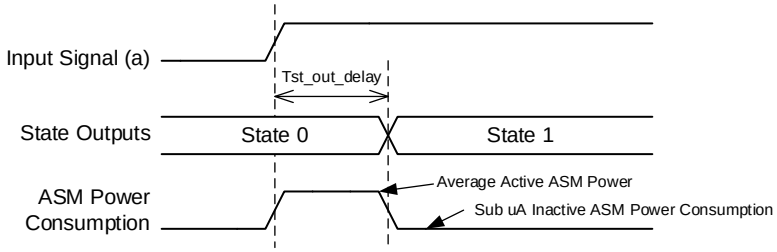


Figure 87. State Transition Timing and Power Consumption

15.7 ASM Logical vs. Physical Design

A successful design with the ASM macrocell must include both the logic level design and the physical level design. The GPAK Designer development software supports the user designs for the ASM macrocell at both the logic level and physical level. The logic level design of the user-defined state machine takes place inside the ASM Editor. In the ASM Editor, the user can select and name states, define and name allowed state transitions, define the Initial/Reset state, and define the output values for the 8 outputs in the Output RAM Matrix. The physical level design takes place in the general GPAK Designer window, and here the user makes connections for the sources for ASM input signals, as well as makes connections for destinations for ASM output signals.

15.8 ASM Special Case Timing Considerations

15.8.1. State Transition Pulse Input Timing

All inputs to the ASM macrocell are level sensitive. If the input to the state machine macrocell for a state transition is a pulse, there is a minimum pulse width on the input to the state machine macrocell (as measured at the matrix input to the macrocell), which is guaranteed to result in a state transition shown in Figure 88 and Figure 89. This pulse width is defined by the State Machine Input Pulse Acceptance Time (T_{st_pulse}). If a pulse width that is shorter than T_{st_pulse} is input to the state machine macrocell, it is indeterminate whether the state transition will happen or not. If a pulse that is rejected (invalid due to the pulse width being narrower than the guaranteed minimum of T_{st_pulse}), this will not stop a valid pulse on another state transition input that does meet minimum pulse width.

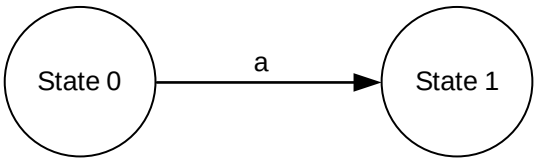


Figure 88. State Transition

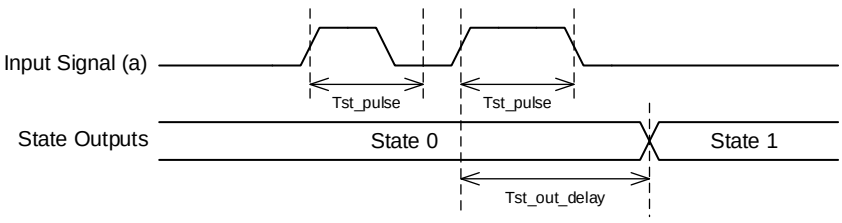


Figure 89. State Transition Pulse Input Timing

15.8.2. State Transition Competing Input Timing

There will be situations where two input signals can be valid inputs that will drive two different state transitions from a given state. In that sense, the two signals are “competing” (signals a and b in Figure 90), and the signal that arrives sooner should drive the state transition that will “win” or drive the state transition. If one signal arrives T_{st_comp} before the other one, it is guaranteed to win, and the state transition that it codes for will be taken, as shown in Figure 91. If the two signals arrive within T_{st_comp} of each other, it will be indeterminate which state transition will win, but one of the transitions will take place as long as the winning signal satisfies the pulse width criteria described in section 15.8.1 State Transition Pulse Input Timing, as shown in Figure 92.

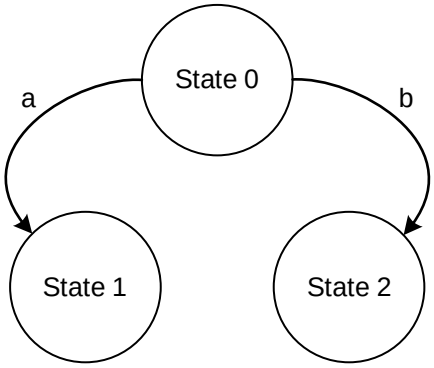


Figure 90. State Transition - Competing Inputs

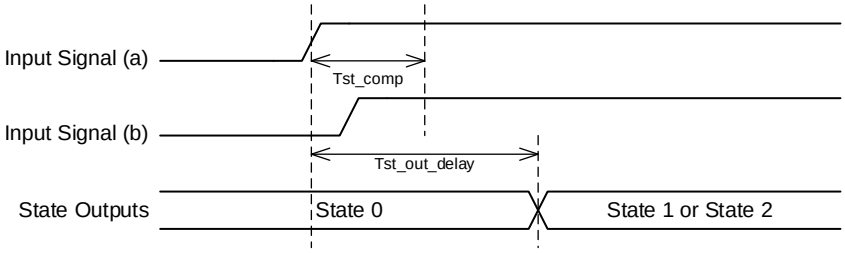


Figure 91. State Transition Timing - Competing Inputs Indeterminate

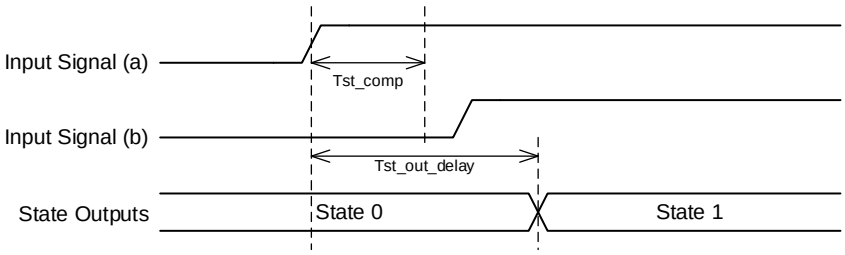


Figure 92. State Transition Timing - Competing Inputs Determinable

15.8.3. ASM State Transition Sequential Timing

It is possible to have a valid input signal for a transition out from a particular state be active before the state is active. If this is the case, the macrocell will only stay in that particular state for $T_{st\_out\_delay}$ time before making the transition to the next state. An example of this sequential behavior is shown in Figure 93 and the associated timing is shown in Figure 94.

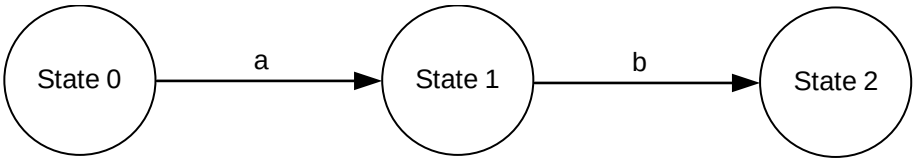


Figure 93. State Transition - Sequential

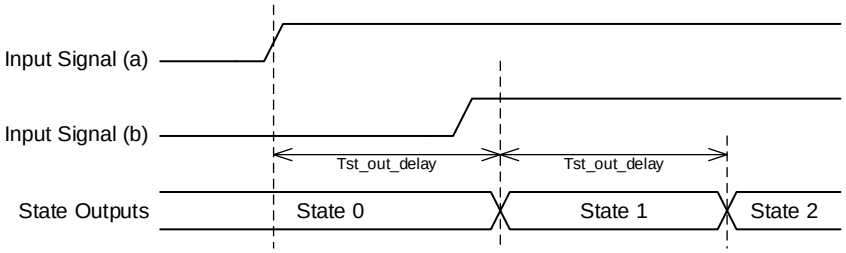


Figure 94. State Transition - Sequential Timing

15.8.4. State Transition Closed Cycling

It is possible to have a closed cycle of state transitions that will run continuously if there are valid inputs that are active at the same time. The rate at which the state transitions will take place is determined by $T_{st\_out\_delay}$. The example shown in Figure 95 involves cycling between two states, but any number of two – eight states can be included in state transition closed cycling of this nature. Figure 96 shows the associated timing for closed cycling.

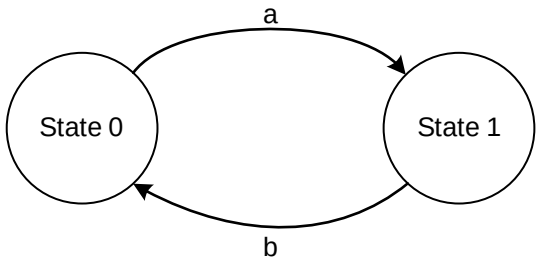


Figure 95. State Transition - Closed Cycling

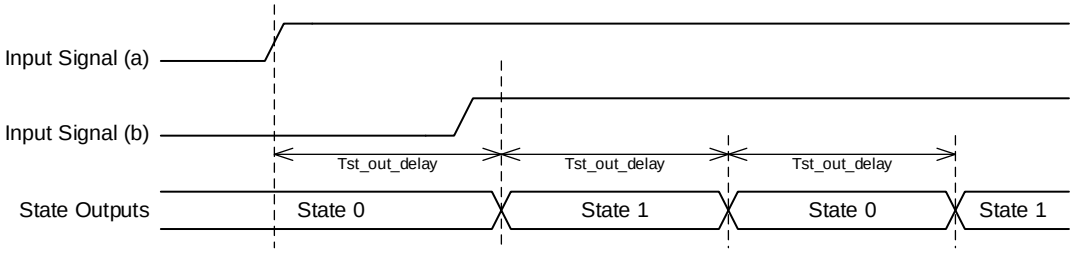


Figure 96.State Transition - Closed Cycling Timing

16. I²C Serial Communications Macrocell

16.1 I²C Serial Communications Macrocell Overview

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Master to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

An I²C bus Master is also able to read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving an I²C bus Master the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits register [1832], register [1870], and register [1871]. See section 16.5 I2C Serial Command Register Protection for more details on I²C read/write memory protection.

Note: GreenPAK I²C is fully compatible with standard I²C protocol.

I²C Serial Communications Macrocell can be connected to I²C pins from V_{DD1} domain and from V_{DD2} domain.

V_{DD1} I²C enable case: when register [1074] = register [1082] = 0.

V_{DD2} I²C enable case: when register [1130] = register [1138] = 1.

If V_{DD1} I²C is enabled and V_{DD2} I²C is enabled at the same time, I²C interface can go through V_{DD1} I²C buffers (IO6, IO7). In this case, V_{DD2} I²C buffers (IO13, IO14) cannot be used like GPIO.

16.2 I²C Serial Communications Device Addressing

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 97. After the Start bit, the first four bits are a control code, which can be set by the user in registers [1867:1864]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I²C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the Control Code to either "1111" or "0000" in a system with other slave device, please consult the I²C-bus specification and user manual to understand the addressing and implementation of these special functions, to ensure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG47525/28 are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9 and A8) will be "0" for all commands to the SLG47525/28.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. Figure 98 shows this basic command structure.

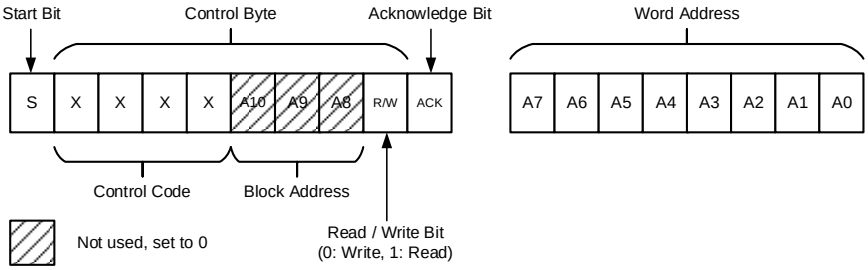


Figure 97. Basic Command Structure

16.3 I²C Serial General Timing

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 98. Timing specifications can be found in section 3.4.5 I2C Pins Timing Characteristics.

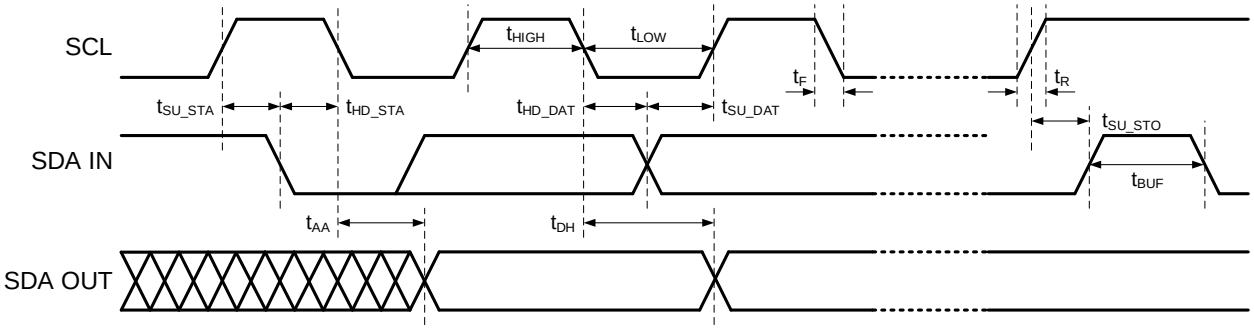


Figure 98. I²C General Timing Characteristics

16.4 I²C Serial Communications Commands

16.4.1. Byte Write Command

Following the Start condition from the Master, the Control Code [4 bits], the Block Address [3 bits], and the R/W bit (set to “0”), are placed onto the I²C bus by the Master. After the SLG47525/28 sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG47525/28, where the data byte is to be written. After the SLG47525/28 sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG47525/28 again provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG47525/28 generates the Acknowledge bit.

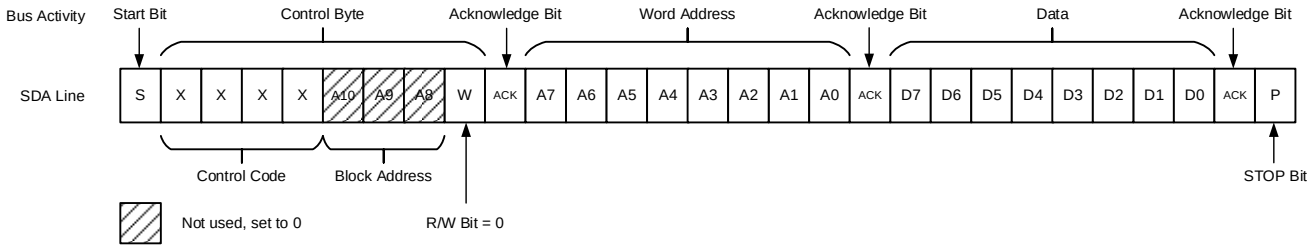


Figure 99. Byte Write Command, R/W = 0

16.4.2. Sequential Write Command

The write Control Byte, Word Address and the first data byte are transmitted to the SLG47525/28 in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Master continues to transmit data bytes to the SLG47525/28. Each subsequent data byte will increment the internal address counter

and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG47525/28 generates the Acknowledge bit.

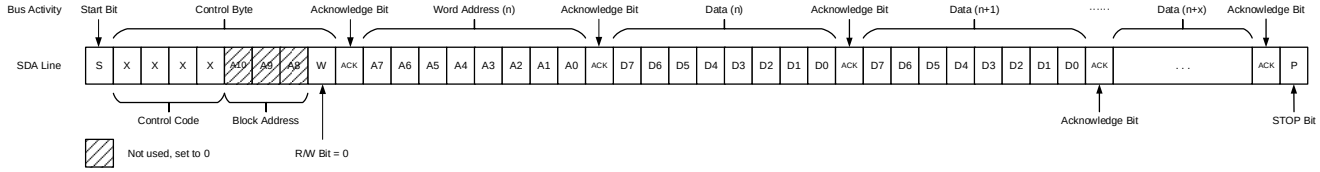


Figure 100. Sequential Write Command, R/W = 0

16.4.3. Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Write or Random Read command (which contains a write control byte) writes or reads data up to address n, the address pointer would get incremented to n+1 upon the STOP of that command. Subsequently, a Current Address Read command that follows would start reading data at n+1. The Current Address Read Command contains the Control Byte sent by the Master, with the R/W bit = “1”. The SLG47525/28 will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Master will not issue an Acknowledge bit and follow immediately with a Stop condition.

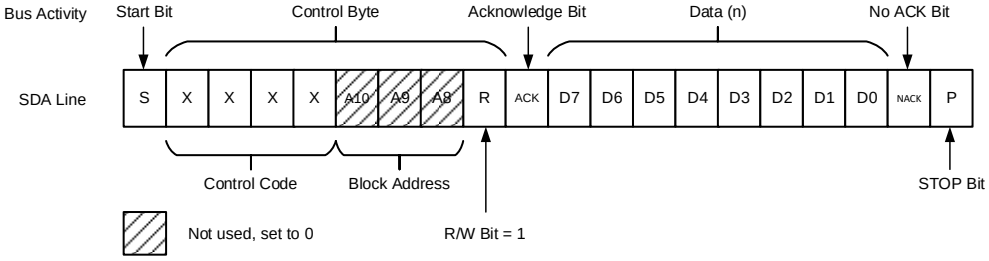


Figure 101. Current Address Read Command, R/W = 1

16.4.4. Random Read Command

The Random Read command starts with a Control Byte (with R/W bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Master issues a second control byte with the R/W bit set to “1”, after which the SLG47525/28 issues an Acknowledge bit, followed by the requested eight data bits.

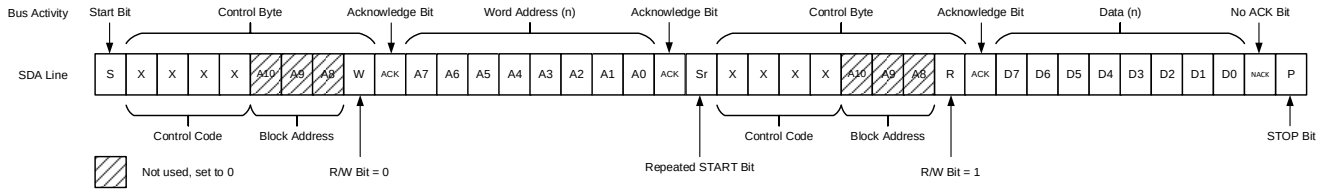


Figure 102. Random Read Command

16.4.5. Sequential Read Command

The Sequential Read command is initiated in the same way as a Current Address Read or Random Read command, except that once the SLG47525/28 transmits the first data byte, the Master issues an Acknowledge bit as opposed to a Stop condition in a random read. The Master can continue reading sequential bytes of data and will terminate the command with a Stop condition.

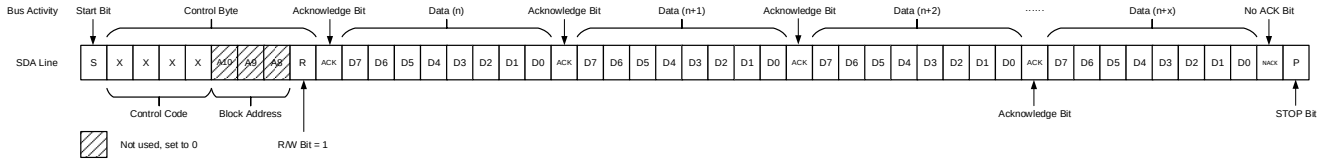


Figure 103. Sequential Read Command

16.4.6. I²C Serial Reset Command

If I²C serial communication is established with the device, it is possible to reset the device to initial power-up conditions, including configuration of all macrocells, and all connections provided by the Connection Matrix. This is implemented by setting register [1662] I²C reset bit to “1”, which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [1662] will be set to “0” automatically. Figure 104 illustrates the sequence of events for this reset function.

Note: I²C Serial Reset Command is not available during emulation.

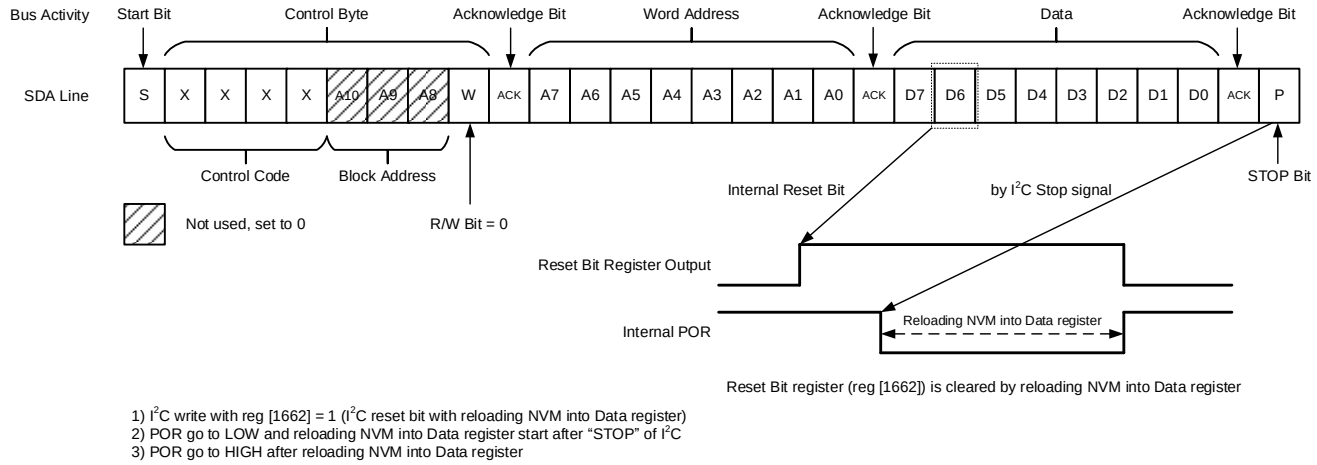


Figure 104. Reset Command Timing

16.4.7. Reading Counter Data via I²C

The current count value in four counters in the device can be read via I²C. The counters that have this additional functionality are 16-bit CNT0 and CNT1, and 8-bit counters CNT4 and CNT6.

16.4.8. I²C Serial Command Address Space

All register addresses are divided into four Banks to give the user greater control over access to reading and writing information in each bank. Each of the four banks is 512 bits (64 bytes) in length. Writing information to register bits in these Banks will change the configuration of the device, resulting in either a change in the interconnection options provided by the Connection Matrix, or a change in the configuration of individual macrocells. During the device use, all register bits can be read or written via I²C, unless protection bits are set to prevent this.

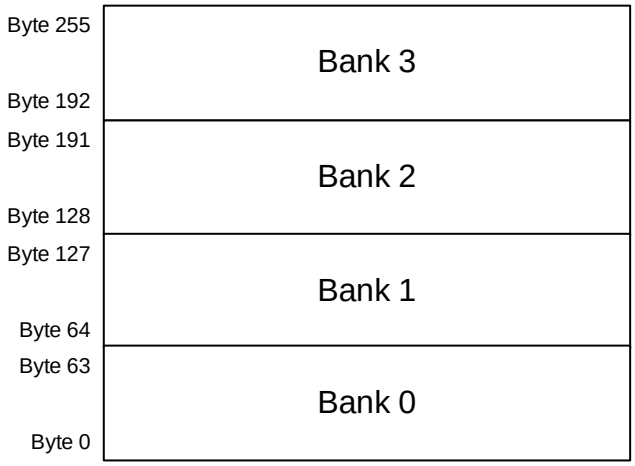


Figure 105. Register Bank Map

16.4.9. User RAM and OTP Memory Array

There are eight bytes of RAM memory that can be read and written remotely by I²C commands. The initial contents of this memory space can be selected by the user, and this information will be transferred from OTP memory to the RAM memory space during the power-up sequence. The lowest order byte in this array (User Configurable RAM/OTP Byte 0) is located at I²C address 0xD8, and the highest order byte in this array is located at I²C address 0xDF.

Table 22. RAM Array Table

I²C Address (hex)	Highest Bit Address	Lowest Bit Address	Memory Byte
D8	1735	1728	User Configurable RAM/OTP Byte 0
D9	1743	1736	User Configurable RAM/OTP Byte 1
DA	1751	1744	User Configurable RAM/OTP Byte 2
DB	1759	1752	User Configurable RAM/OTP Byte 3
DC	1767	1760	User Configurable RAM/OTP Byte 4
DD	1775	1768	User Configurable RAM/OTP Byte 5
DE	1783	1776	User Configurable RAM/OTP Byte 6
DF	1791	1784	User Configurable RAM/OTP Byte 7

16.5 I²C Serial Command Register Protection

The memory space is divided into four banks, each of which has 512 bits (64 bytes). There are three bits that allow the user to define rules for reading and writing bits in each of these banks via I²C:

- register [1832] I²C lock for read bits [1535:0] (Bank 0/1/2). If the system provides any read commands to the addresses in these three banks, the device will respond with ‘FFH’ in data field.
- register [1871] I²C lock for write bits [1535:0] (Bank 0/1/2). If the system provides any write commands to the addresses in these three banks, the device will acknowledge these commands, but will not do internal writes to the register space.
- register [1870] I²C lock for write all bits (Bank 0/1/2/3). If the system provides any write commands to the addresses in these four banks, the device will acknowledge these commands, but will not do internal writes to the register space.

Note 1: register [1870] has higher priority than register [1871], and if register [1870] is set, then register [1871] does not have any effect.

Note 2: If the user sets IOs 6 and 7 function to a selection other than SDA and SCL, all access via I^2C will be disabled.

If register [1870] is not set, register bits in Bank 3 are open to read and write commands via I^2C with the following exceptions:

- register [1871] Bank 0/1/2 I^2C-write protection bit is always protected from I^2C write.
- registers [1867:1864] I^2C Control Code Bit [3:0] is always protected from I^2C write.

Note 3: Any write commands that come to the device via I^2C that are not blocked, based on the protection bits, will change the contents of the RAM register bits that mirror the NVM bits. These write commands will not change the NVM bits themselves, and a POR event will restore the register bits to original programmed contents of the NVM.

16.5.1. Register Read/Write Protection

There are six read/write protect modes for the design sequence from being corrupted or copied. See Table 23 for details.

Table 23. Read/Write Protection Options

Bank	Byte	Bits	Description	Lock Status					
				Unlocked	Locked for read bits [1535:0]	Locked for write bits [1535:0]	Locked for write all bits	Locked for read and write bits [1535:0]	Locked for read bits [1535:0] and write all bits
				registers [1832]=0, [1871]=0, [1870]=0	registers [1832]=1, [1871]=0, [1870]=0	registers [1832]=0, [1871]=1, [1870]=0	registers [1832]=0, [1871]=x, [1870]=1	registers [1832]=1, [1871]=1, [1870]=0	registers [1832]=1, [1871]=x, [1870]=1
0	0-63	511-0	Connection Matrix Outputs Configuration	R/W	W	R	R	-	-
1	64-109	879-512		R/W	W	R	R	-	-
	110-127	880-1023	Reserved	-	-	-	-	-	-
2	128-186	1495-1024	Function Configuration for PINs, LUTs/DFFs, OSC, ASM, and some configuration for DLYs, ACMP	R/W	W	R	R	-	-
	187-191	1535-1496	Reserved	-	-	-	-	-	-
3	192-206	1655-1536	CNT/DLY counter data and some LUTs truth table, ACMP V_{REF}	R/W	R/W	R/W	R	R/W	R
	207	1663	Reserved	-	-	-	-	-	-
	207	1662	I^2C reset bit with reloading NVM into Data register	R/W	R/W	R/W	R	R/W	R
		1661-1659	Reserved	-	-	-	-	-	-
		1658-1656	OSC Power Control	R/W	R/W	R/W	R	R/W	R
	208-223	1791-1664	ASM output RAM and User configurable RAM/OTP	R/W	R/W	R/W	R	R/W	R
	224-228	1831-1792	Reserved	-	-	-	-	-	-
	229	1839-1836	Product Family ID	R	R	R	R	R	R
		1835-1833	Reserved	-	-	-	-	-	-
		1832	I^2C Lock for read bits [1535:0]	R	R	R	R	R	R

Bank	Byte	Bits	Description	Lock Status					
				Unlocked	Locked for read bits [1535:0]	Locked for write bits [1535:0]	Locked for write all bits	Locked for read and write bits [1535:0]	Locked for read bits [1535:0] and write all bits
				registers [1832]=0, [1871]=0, [1870]=0	registers [1832]=1, [1871]=0, [1870]=0	registers [1832]=0, [1871]=1, [1870]=0	registers [1832]=0, [1871]=x, [1870]=1	registers [1832]=1, [1871]=1, [1870]=0	registers [1832]=1, [1871]=x, [1870]=1
3	230	1847-1840	Pattern ID	R/W	R/W	R/W	R	R/W	R
	231-232	1863-1848	Reserved	-	-	-	-	-	-
	233	1871	I^2C Lock for write bits [1535:0]	R	R	R	R	R	R
		1870	I^2C Lock for write all bits	R	R	R	R	R	R
		1869-1868	Reserved	-	-	-	-	-	-
		1867-1864	I^2C Control Code	R	R	R	R	R	R
	234-239	1919-1872	Counter Current Value	R	R	R	R	R	R
	240-243	1951-1920	Macrocells Output Values (Connection Matrix Inputs)	R	R	R	R	R	R
	244	1959-1952	Connection Matrix Virtual Inputs	R/W	R/W	R/W	R	R/W	R
	245-247	1983-1960	Macrocells Output Values (Connection Matrix Inputs)	R	R	R	R	R	R
	248-255	2047-1984	Reserved	-	-	-	-	-	-

R/W	Allow Read and Write Data
W	Allow Write Data Only
R	Allow Read Data Only
-	The Data is protected for Read and Write

17. Analog Temperature Sensor

The SLG47525/28 has an Analog Temperature sensor (TS) with an output voltage linearly-proportional to the Centigrade temperature. The TS is rated to operate over a -40 °C to 180 °C temperature range. The error in the whole temperature range does not exceed ±10.3 % (±5.7 % in a range from -40 °C to 100 °C). TS output voltage variation over V_{DD} at constant temperature is less than ±10.3 %. For more details refer to section 3.7 Analog Temperature Sensor Characteristics.

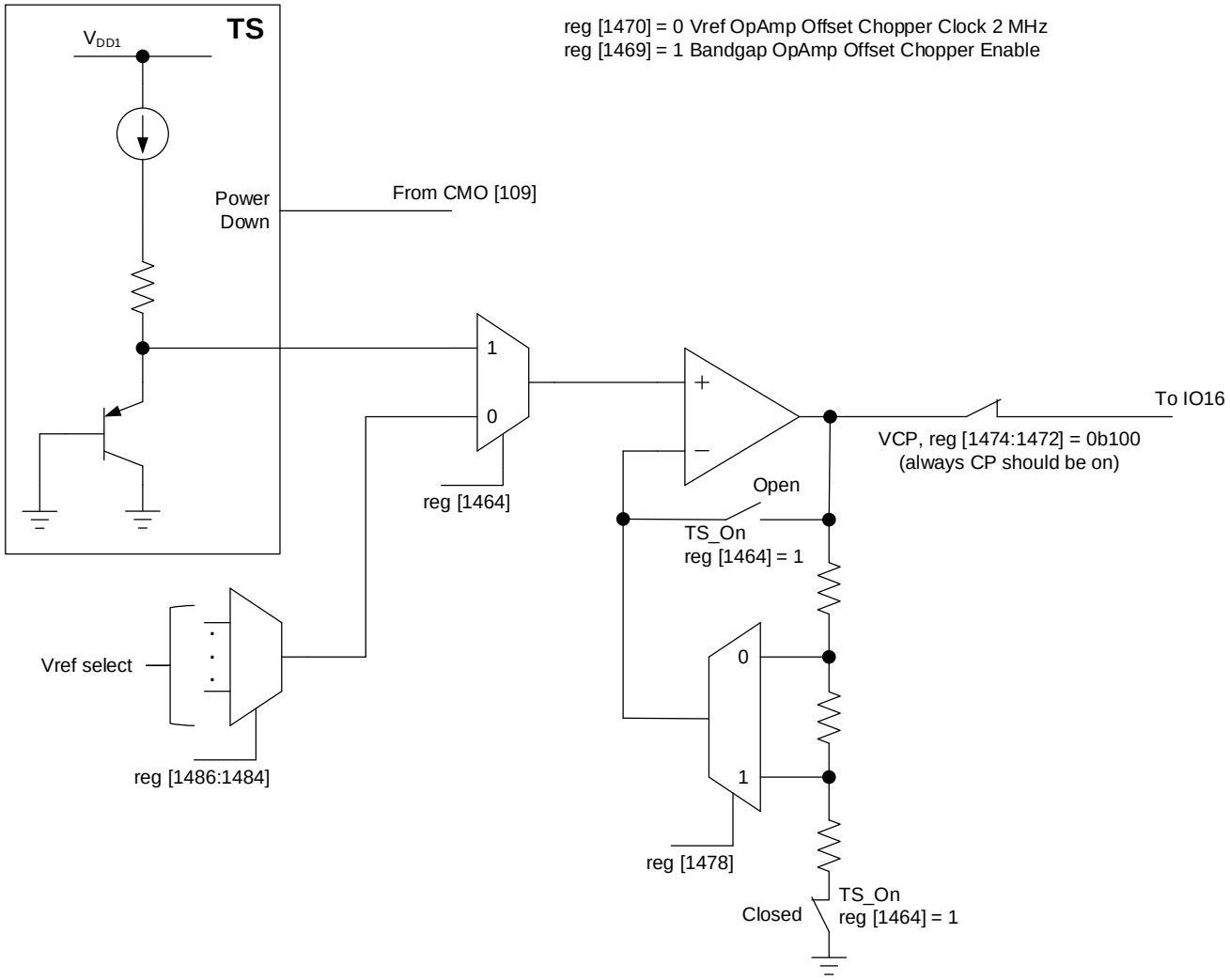


Figure 106. Analog Temperature Sensor Structure Diagram

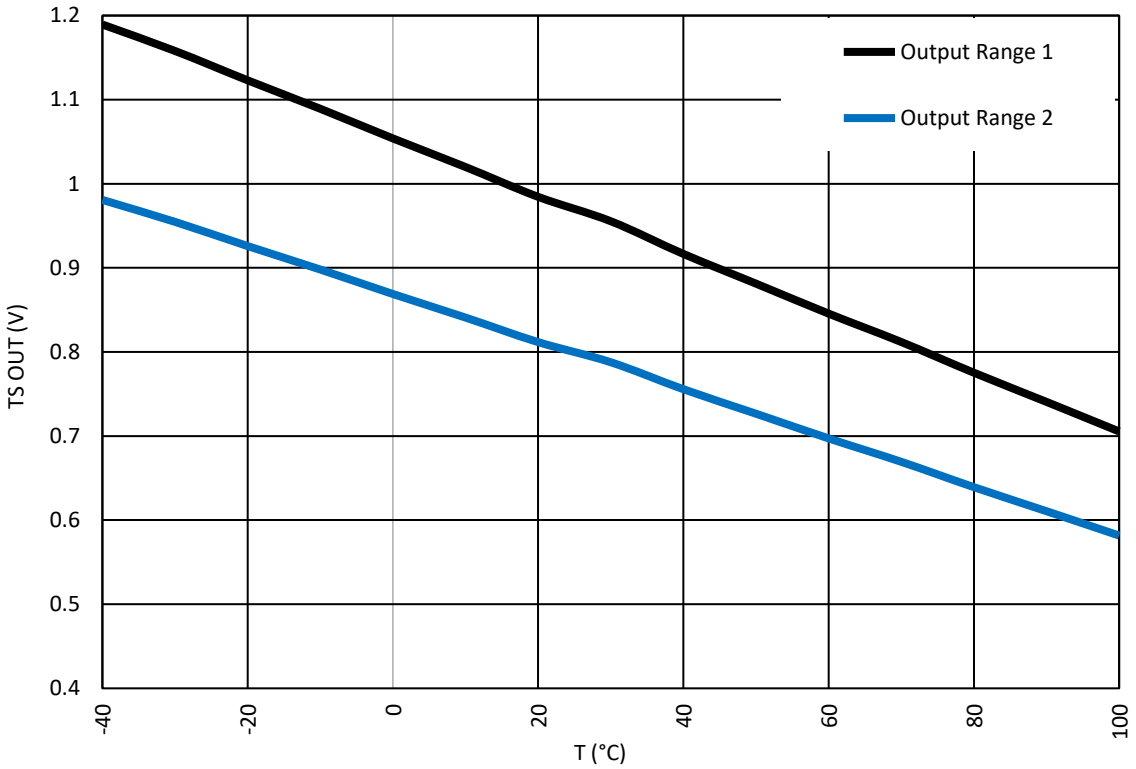
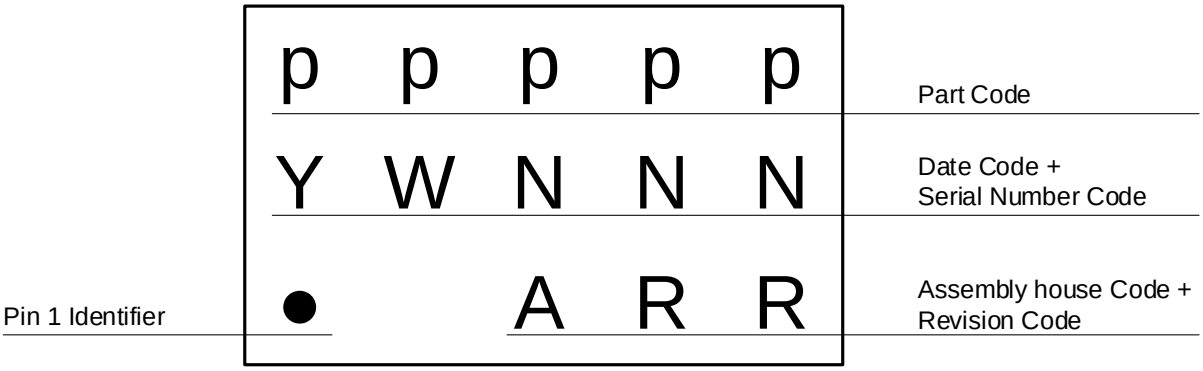


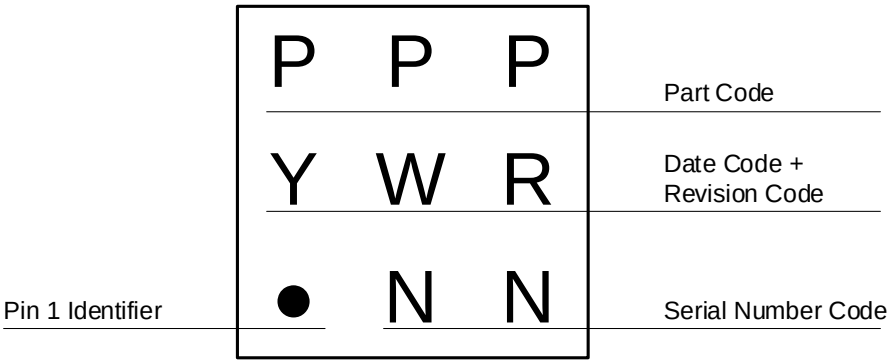
Figure 107. TS Output vs. Temperature, V_{DD} = 1.71 to 5.5 V

18. Package Top Marking Definitions

18.1 STQFN 20L 2 mm x 3 mm 0.4P COL Package

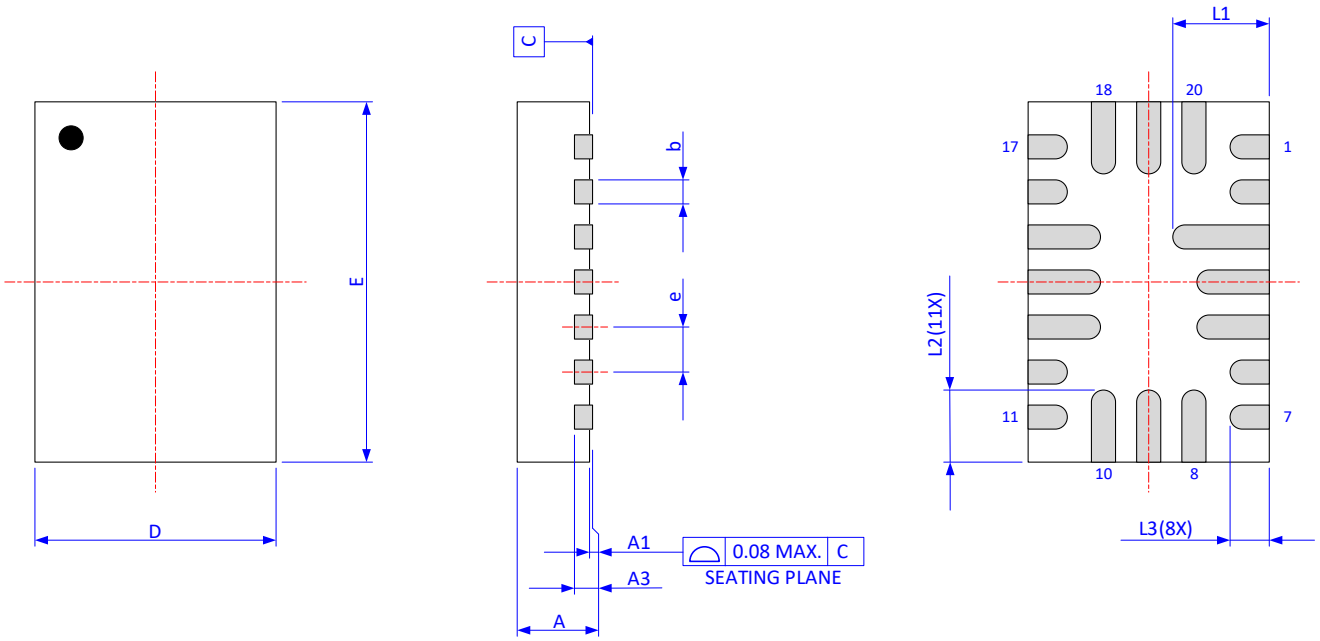


18.2 STQFN 14L 2 mm x 2.2 mm 0.4P COL Package



19. Package Information

19.1 Package Outlines for STQFN 20L 2 mm x 3 mm 0.4P COL Package



Top View Side View Bottom View

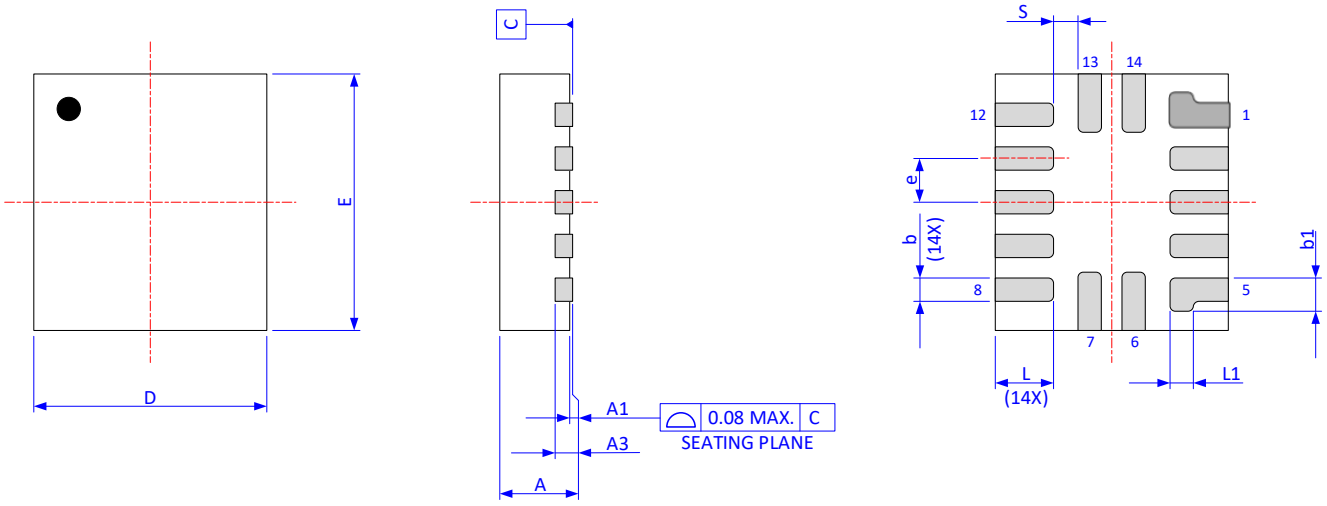
Notes:

1. All dimensions are in millimeters.
2. Dimension “b” applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension “b” should not be measured in that radius area.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

Symbol	Millimeter		
	Min.	Nom.	Max.
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.150 REF.		
b	0.13	0.18	0.23
D	2.00 BSC		
E	3.00 BSC		
e	0.40 BSC		
L1	0.75	0.80	0.85
L2	0.55	0.60	0.65
L3	0.275	0.325	0.375

Figure 108. Package Outline Drawing for STQFN 20L 2 mm x 3 mm 0.4P COL

19.2 Package Outlines for STQFN 14L 2 mm x 2.2 mm 0.4P COL Package



Top View Side View Bottom View

Notes:

1. All dimensions are in millimeters.
2. Dimension “b” applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension “b” should not be measured in that radius area.
3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

Symbol	Min.	Nom.	Max.
A	0.50	0.55	0.60
A1	0.005	--	0.05
A3	0.10	0.15	0.20
b	0.13	0.18	0.23
b1	0.28 TYP		
D	1.95	2.00	2.05
E	2.15	2.20	2.25
e	0.40 BSC		
L	0.45	0.50	0.55
L1	0.18 TYP		
S	0.21 TYP		

Figure 109: Package Outline Drawing for STQFN 14L 2 mm x 2.2 mm 0.4P COL

19.3 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 24.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The STQFN-20 and STQFN-14 packages are qualified for MSL 1.

Table 24. MSL Classification

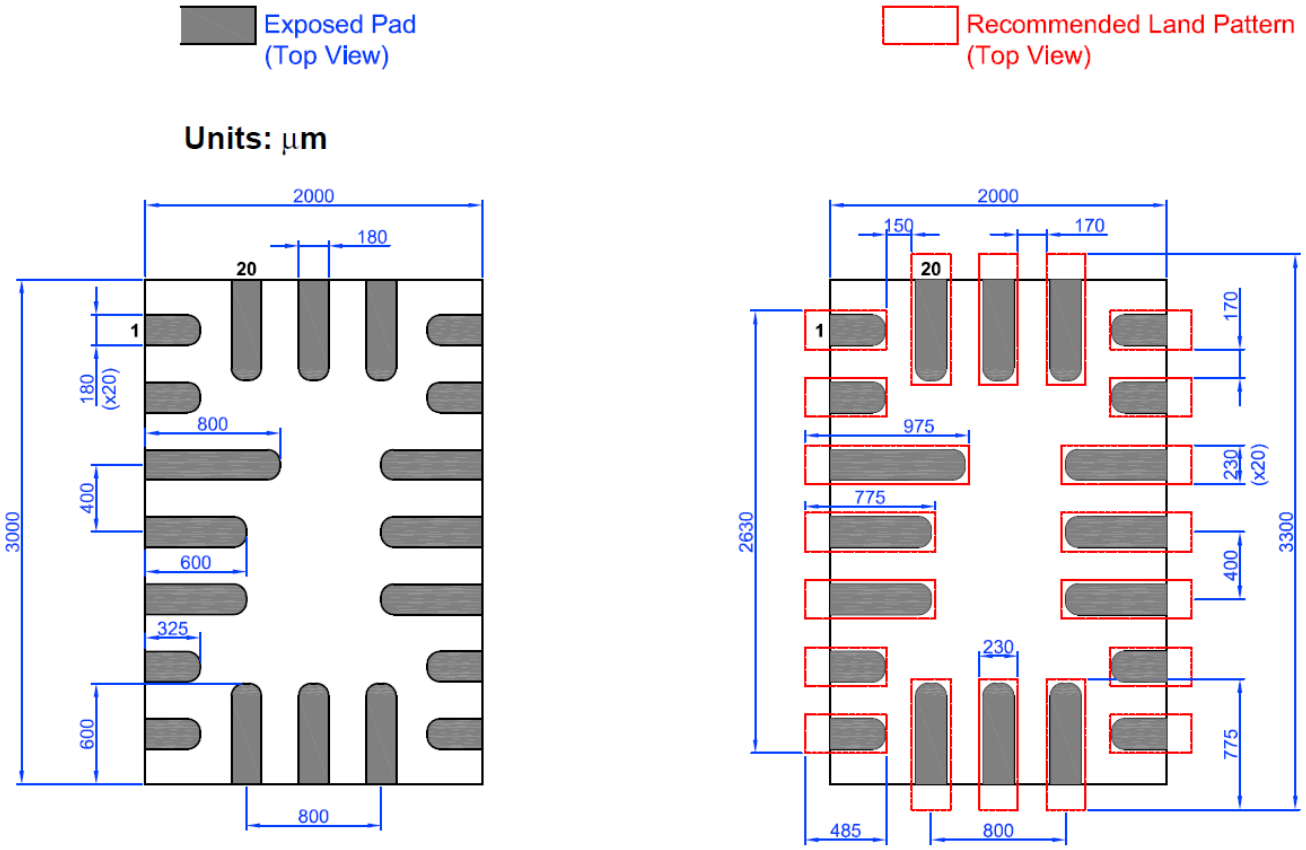
MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

19.4 Soldering Information

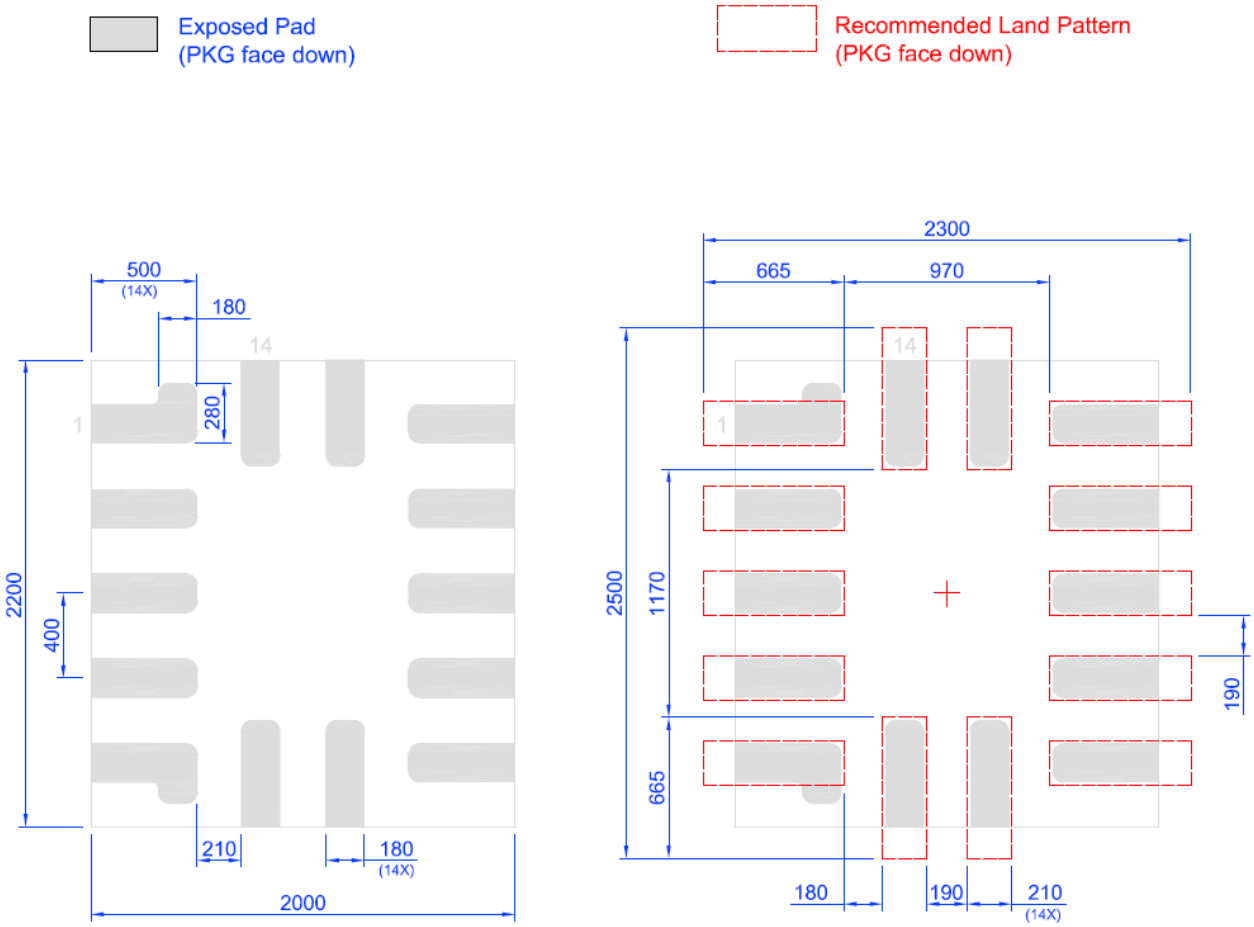
Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

20. PCB Layout Guidelines

20.1 Recommended Landing Pattern for STQFN 20L 2 mm x 3 mm 0.4P COL Package



20.2 Recommended Landing Pattern for STQFN 14L 2 mm x 2.2 mm 0.4P COL Package



Unit:um

21. Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Renesas Electronics Corporation's or your local sales representative.

Table 25. Ordering Information

Part Number	Package	Size (mm)	Shipment Form
SLG47528V	20-pin STQFN	2 mm x 3 mm x 0.55 mm, 0.4 mm pitch	Tape and Reel
SLG47525V	14-pin STQFN	2 mm x 2.2 mm x 0.55 mm, 0.4 mm pitch	Tape and Reel

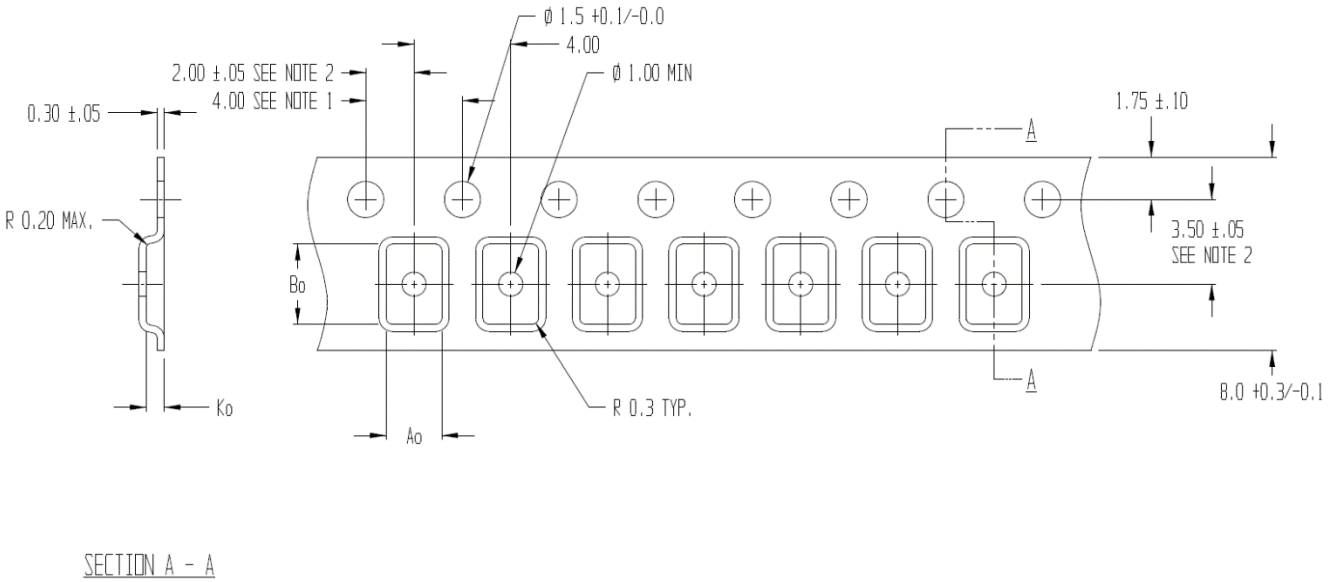
21.1 Tape and Reel Specifications

Package type	# of pins	Nominal Package size (mm)	Max units	Reel Dia. (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			Per Reel		Pockets	Length (mm)	Pockets	Length (mm)		
STQFN 20L 2mm x 3mm 0.4P COL Green	20	2 x 3 x 0.55	3000	178	100	400	100	400	8	4
STQFN 14L 2mm x 2.2mm 0.4P COL Green	14	2 x 2.2 x 0.55	3000	178	100	400	100	400	8	4

21.2 Carrier Tape Drawing and Dimensions

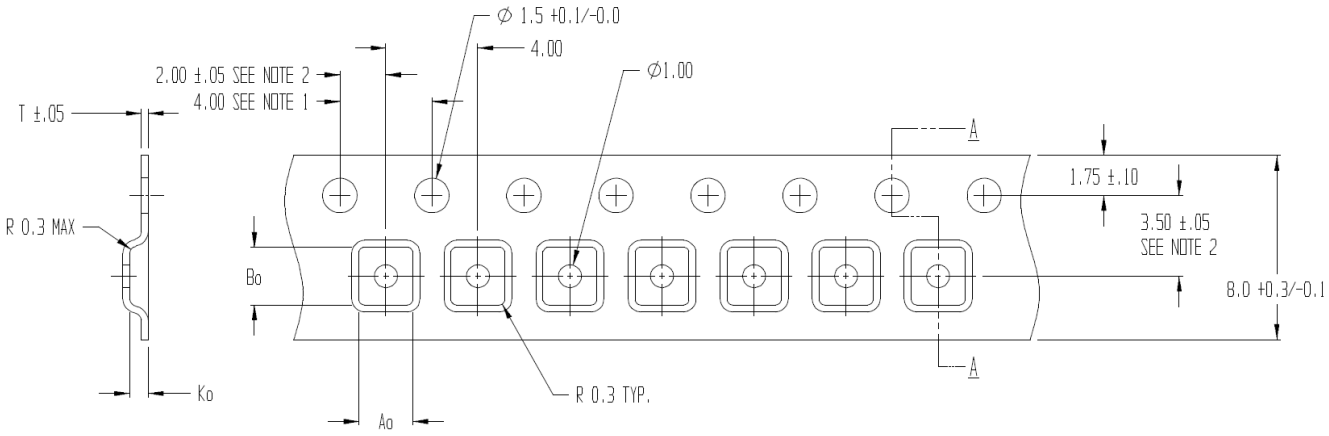
Package type	Pocket BTM length (mm)	Pocket BTM width (mm)	Pocket depth (mm)	Index hole pitch (mm)	Pocket pitch (mm)	Index hole diameter (mm)	Index hole to tape edge (mm)	Index hole to pocket center (mm)	Tape width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2mm x 3mm 0.4P COL Green	2.30	3.30	0.75	4	4	1.5	1.75	3.5	8
STQFN 14L 2mm x 2.2mm 0.4P COL Green	2.30 ± 0.05	2.45 ± 0.05	0.80	4	4	1.5	1.75	3.5	8

21.2.1. STQFN 20L 2 mm x 3 mm 0.4P COL Carrier Tape Drawing



SECTION A - A

21.2.2. STQFN 14L 2 mm x 2.2 mm 0.4P COL Carrier Tape Drawing



SECTION A - A

Glossary

A

ACK	Acknowledge Bit

B

BG	Bandgap

C

CLK	Clock
CMI	Connection Matrix Input
CMO	Connection Matrix Output
CNT	Counter

D

DFF	D Flip-Flop
DI	Digital Input
DILV	Low Voltage Digital Input
DLY	Delay

E

ESD	Electrostatic Discharge
EV	End Value

F

FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

I

IN	Input
IO	Input/Output

L

LSB	Least Significant Bit

LUT	Look Up Table
LV	Low Voltage

M

MSB	Most Significant Bit
MUX	Multiplexer

N

NPR	Non-Volatile Memory Read/Write/Erase Protection
nRST	Reset
NVM	Non-Volatile Memory

O

OD	Open-Drain
OE	Output Enable
OSC	Oscillator
OTP	One Time Programmable
OUT	Output

P

PD	Power-Down
POR	Power-On Reset
PP	Push-Pull
PWR	Power
P DLY	Programmable Delay

R

R/W	Read/Write

S

SCL	I^2C Clock Input
SDA	I^2C Data Input/Output
SLA	Slave Address
SMT	With Schmitt Trigger
SV	nSET Value

T

TS	Temperature Sensor

V

Vref	Voltage Reference

W

WOSMT	Without Schmitt Trigger

Revision History

Revision	Date	Description
1.01	Jul 02, 2024	Updated Figure 50. ACMP1 Block Diagram. Updated Figure 52. ACMP3 Block Diagram.
1.00	Jun 07, 2024	Initial release